# N-Channel 20 V (D-S) 175 °C MOSFET

DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC
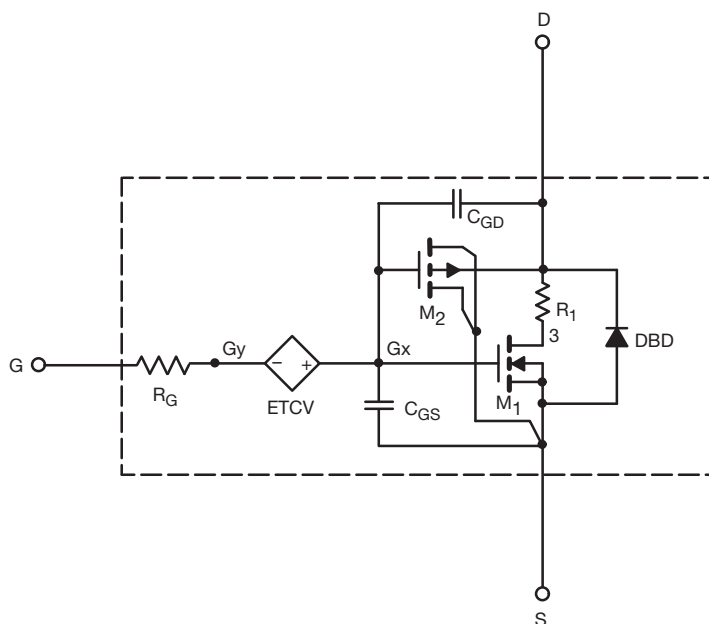
Note
- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ µA	0.40	-	V
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 5$ A	0.024	0.024	Ω
		$V_{GS} = 2.5$ V, $I_D = 4$ A	0.030	0.027	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 15$ V, $I_D = 5$ A	21	27	S
Body Diode Voltage	V_{SD}	$I_S = 5$ A	0.72	0.75	V
Dynamic[b]					
Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1 MHz	392	387	pF
Output Capacitance	C_{oss}		90	80	
Reverse Transfer Capacitance	C_{rss}		36	37	
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 5$ A	4	4.5	nC
Gate-Source Charge	Q_{gs}		0.4	0.4	
Gate-Drain Charge	Q_{gd}		0.7	0.7	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)
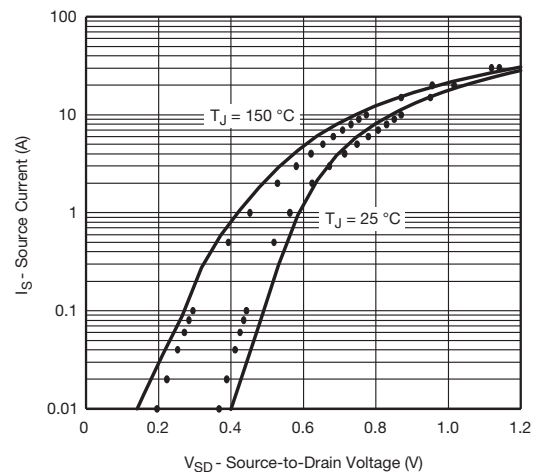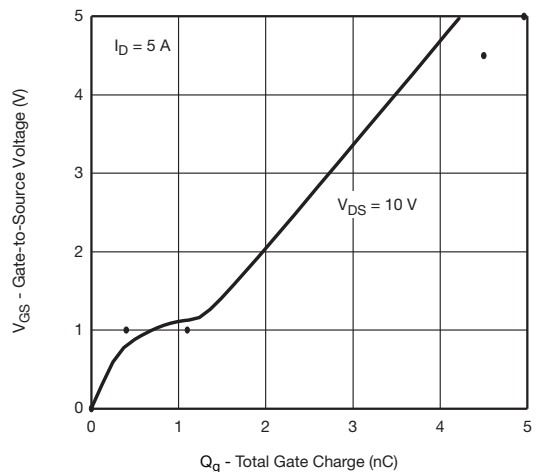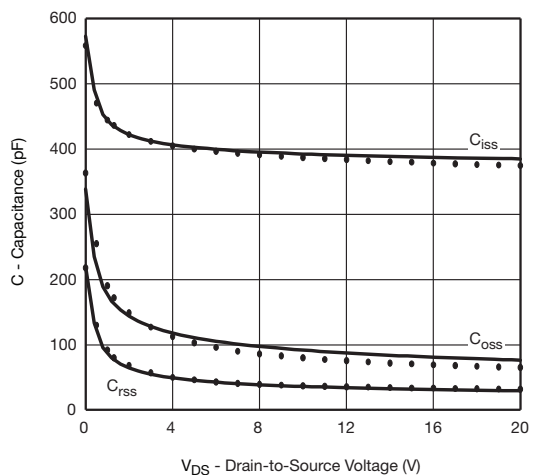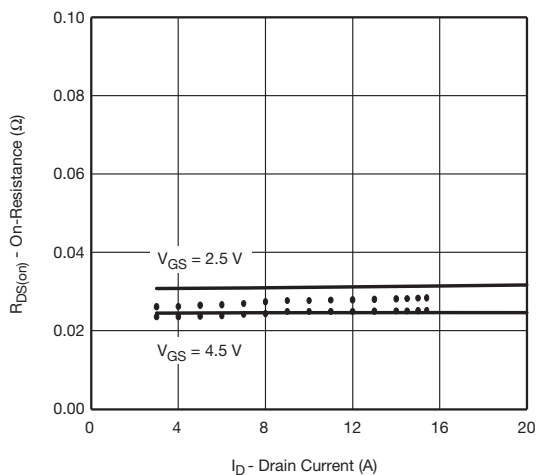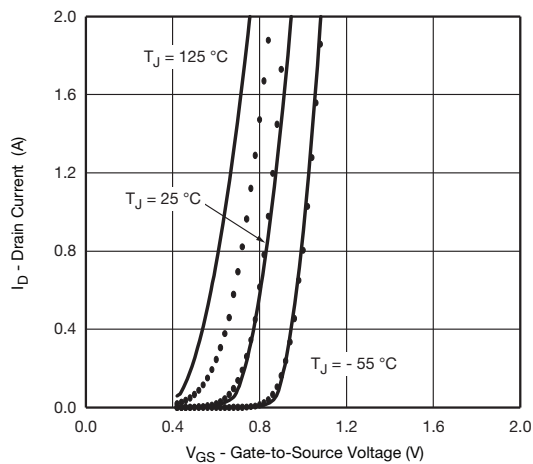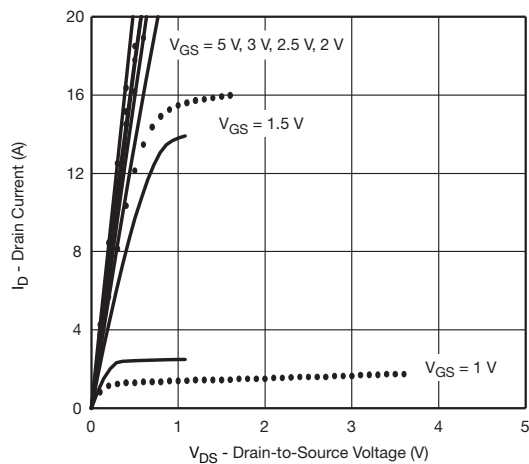
Note

- Dots and squares represent measured data.