Ho Chi Minh City University of Technology
Faculty of Computer Science and Engineering

LOGIC DESGIN WITH HDL

Practical session - Semester 212

ASSIGNMENT

Updated on 21/04/2022

1 Introduction

1.1 Aims

- Practice, improve the ability of using Verilog HDL to design digital circuits.
- Practice the analysis, design skills following hierarchy approach.
- Knowledge about popular circuits that are used in digital systems.
- Practice research, self-study, documentation, presentation skills.

1.2 Requirements

- Work in a group of 2-4 members.
- Each group chooses 1 topic, study about theories, applications, then designs and implements the circuit in the topic using Verilog HDL. Write test benches to simulate the design.
- Make demo scenarios. May design more modules to demo on FPGA if possible.
- Report structure:
  - Introduction: introduce the topic, scope and summary the report content.
  - Backgrounds and applications: theory of any concept in the topic and applications of the circuit.
  - Design: present the ideal, block diagram, flowchart of the design.
  - Implementation: technical document implemented blocks, modules.
  - Results: present the experiment setups, waveform, explanations and report timing, resources.
  - Conclusion: summary working achievements, advantages, disadvantages and future works.
- Groups can propose more features, contents for the chosen topic.
- Compress the report (.pdf), source code (.v) in only 1 .zip file. Name the .zip file the group ID. Submit on BK-elearning by deadline.

1.3 Evaluation criteria

- The content of presented theories, applications.
- The basic functions of implemented circuit.
- The content and presentation of the report.
- Source code: hardware design rule, coding rule, coding style.
- Bonus: extra functions, contents of design, studies and works.

2 Topics

2.1 FIFO - First In First Out

FIFO - First In First Out is one of the most popular logic circuits in digital systems. It works as a buffer memory, where the data which is written to first will be the data read out first as Figure 1. The implement logic is often based on **ring buffer** principle.

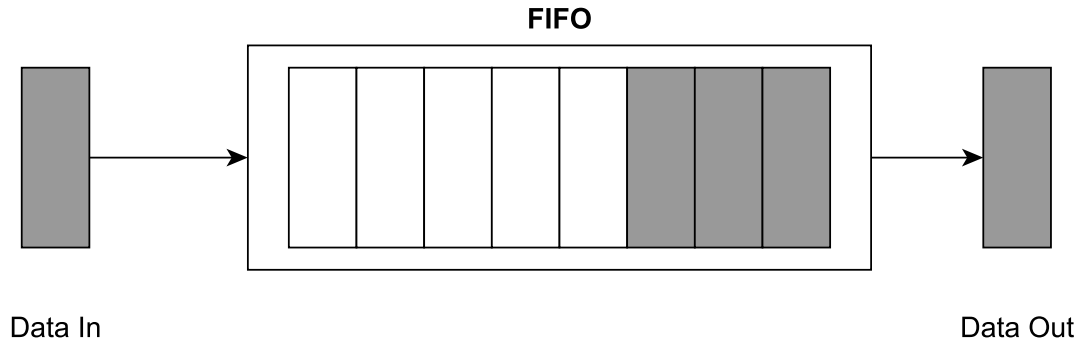

Figure 1: FIFO

Let's study ring buffer, FIFO theory and it's applications. Then design and implement a FIFO circuit using Verilog HDL. Write test benches to verify the implemented circuit.

Bonus: Write more modules and plan scenarios to demo on board.

2.2 Other topics

Groups can choose any other topics which are classified in 2 kinds below:

*** Technical topics:**

These topics are small and popular circuits in digital systems. If groups choose this kind of topic, you must do the same as topic 1 - FIFO: study the theory, applications, design and implement using Verilog HDL, write test benches. Groups will get bonuses if demo on board.

Some proposed topics:

- PWM - Pulse Width Modulation generator.
- CRC - Cyclic Redundant Check generator/checker.
- SPI - Serial Peripheral Interface master and slave controller.
- ...

*** Application topics:**

Groups can choose any application to implement and MUST demo on the FPGA board, no need to study and report the theory and applications. In this kind of topic, groups may need to use some extra circuits, modules or elements (groups can buy available modules). The chosen topic must have at least 2 functions. More functions will get bonuses.

Some proposed topics:

- Digital clock.
- Sport clock.
- Crossroad traffic light.
- ...

3 References

Websites:

- https://www.fpga4student.com/
- https://www.fpga4fun.com/
- https://www.element14.com/
- https://www.hackster.io/
- https://www.instructables.com/circuits/howto/fpga/
- ...

If you have any questions or need help, don't hesitate to ask your instructor in class or via email.