Week 7: Assignment

1. Which of the following statement declares a memory of size 64 KByte with word size 4 byte?
    a. reg [16383:0] Mem[7:0];
    b. reg [65535:0] Mem[31:0];
    c. reg [31:0] Mem[16383:0];
    d. reg [3:0] Mem[65535:0];

    Answer: (c)

    Memory size= $64\ KByte$

    Word size = $4\ byte = 32\ bits$

    Total number of words= $\frac{64}{4} = 16K = 16 \times 1024 = 16384$

    Thus option (c) correctly realizes the memory requirement of 64Kbytes as an array of 16K words with individual word of size 32 bits.

2. Which of the following statement declares a 2-dimensional array of 2K rows and 1K columns where every array element can store an octal digit?
    a. reg [1023:0] Data[2:0][2047:0];
    b. reg [2:0] Data[2047:0][1023:0];
    c. reg [2047:0] Data[2:0][1023:0];
    d. reg [2:0] Data[1023:0][2047:0];

    Answer: (b)

    Row size = $2K = 2048$

    Column size = $1K = 1024$

    Word or element size = $3\ bit\ (for\ storing\ octal\ number)$

    Thus option (b) correctly implements the 2-D storage requirement of $2K \times 1K$ with individual cell of size 3 bits.

3. Which of the following statements are true for bidirectional bus?
    a. Variable of **inout** type is not a good choice for implementing bidirectional data bus.
    b. Values of bidirectional variables are updated in procedural block.
    c. Variable of type **tri** is preferred over variable of type **inout** in implementing bidirectional data bus.
    d. None of these.

    Answer: (a) & (c)

    Synthesis as well as simulation tool gives inconsistent behavior for inout data type. Thus options (a) and (c) are true. Since, inout port is wire type and tri is a specific type of wire, variables of these types must be updated using continuous assignment statement. Thus option (b) is false.

4. Which of the following are true for register banks?
    a. Both register read and write operation must be synchronous with clock.

b. Register read operation can be carried out using blocking as well as continuous assignment.
c. Register write operation can be carried out using both blocking and non-blocking assignment in synchronism with the clock.
d. Reset signal may be used to synchronously clear all registers to 0.

Answer: (b) and (d)

Only register write operation must be synchronous with clock. Thus option (a) is false. Register read operation can be realized using either blocking assignment or continuous assignment. Thus option (b) is true. Register write operation can only be carried out using non-blocking assignment statement. Thus option (c) is false. The reset facility is used to initialize all the registers to 0 in synchronism with the clock. Thus option (d) is true.

5. For a 10-stage pipeline implementation of some computation, the maximum speedup cannot exceed .....

Answer: Range of 9.9 to 10.0

To process m data, the speedup of an n stage pipelined implementation overall over an equivalent non-pipelined implementation will be:

$$= \frac{m \times n}{n + (m - 1)} \approx n$$

when input data m is large.

6. Consider inter-stage pipeline registers are assumed to be of zero latency and the stage delays are specified in nanoseconds. Which of the following pipelines will have the highest clock frequency?
   a. 4-stage pipeline with stage delays 4, 3, 6 and 5
   b. 4-stage pipeline with stage delays 9, 7, 2, and 3
   c. 5-stage pipeline with stage delays 6, 2, 7, 3 and 1
   d. 5-stage pipeline with stage delays 3, 8, 2, 1 and 2

Answer: (a)

Since maximum clock frequency is upper-bounded by the largest pipeline stage delay, option (a) with largest stage delay of 6 is correct.

7. The stage delays in a 5-stage pipeline are 12, 50, 14, 8 and 18 nanoseconds. The 2nd stage is replaced with a functionally equivalent design involving three stages with respective delays 15, 18 and 17 nanoseconds. The throughput of the pipeline increases by ..... percent.

Answer: Between 177.0 to 178.0

Initially, the throughput of 5-stage implementation is $= \frac{1}{50}$

After extending to two additional stages, throughput become $= \frac{1}{18}$

% improvement $= \frac{\left(\frac{1}{18} - \frac{1}{50}\right)}{\frac{1}{50}} \times 100 \approx 177.78$

8. Which of the following statements are true regarding forwarding the same value from one pipeline register stage to the next?
    a. Forwarding is necessary to make the data available to the specific stage that requires the data.
    b. To retain the data unaltered during intermediate stages of computation until it reaches the desired stage for processing.
    c. The forwarding increases inter-stage buffer requirements as well as overall delays in pipeline implementation.
    d. None of the above.

    Answer: (a) and (b)

    Since input data is also required at some later computational stage, it must be forwarded through all the previous stages. Thus option (a) is true. Preserving the data in all the previous stage is necessary to ensure individual stage is performing on separate data. Thus option (b) is also true. Forwarding reduces the overall delay by making all previous stage free for processing new data. Thus option (c) is false.

9. What function does the following switch-level model realize?

```
module surprise (in1, in2, out);
input in1, in2;   output out;
supply1vplus;  supply0 vgnd;
wire t;
pmos (out, vplus, in1);
pmos (out, vplus, in2);
nmos (out, t, in1);
nmos (t, vgnd, in2);
endmodule
```

    a. Exclusive NOR
    b. NAND
    c. NOR
    d. Exclusive OR

    Answer: (b)

    Since the two pmos switches are connected in parallel to output, the output will be 0 when both the in1 and in2 are 1. Further two nmos are connected in series, thus out will be discharged to 0 when both in1 and in2 are 1. For all other values of in1 and in2 output remains 1. This is the behavior of NAND function.

10. Number of bidirectional switches of type **tranif0** required to implement a 16-to-1 multiplexer with 4 selection input line is ……

    Answer: 32

    Since a 16-to-1 multiplexer implementation must have 16 rows each one containing 4 tran switches for four select lines, there will be 64 switches half of which will be of type tranif0 and other half will be tranif1.