Week 8: Assignment

1. Suppose that in a MIPS32 based computer, memory locations 250, 261, 272 and 283 (in decimal) contains the data 23, 74, 33 and 45 (in decimal) respectively.

   For the following MIPS32 code segment, the final value of R7 will be …….

```
LW      R2, 272(R0)
LW      R3, 228(R2)
SLT     R4, R3, R2
ADDI    R5,R0, 2
MUL     R6,R4,R5
SUB     R7,R6,R2
HLT
```

   Answer: -33

   The values of registers get updated in the following sequence:

   $R2 = Mem[R0 + 272] = Mem[0 + 272] = 33$

   $R3 = Mem[R2 + 228] = Mem[33 + 228] = 74$

   $R4 = 0, Since\ R3 > R2$

   $R5 = 0 + 2 = 2$

   $R6 = 0 * 2 = 0$

   $R7 = 0 - 33 = -33$

2. Suppose that in a MIPS32 based computer, memory locations 50, 75, 105 and 140 (in decimal) contains the data 15, 63, 72 and 59 (in decimal) respectively.

   After execution of the following MIPS32 code segment, memory location 75 will contain ……..

```
ADDI    R1,R0,100
LW      R2,40(R1)
LW      R3,-9(R2)
SUBI    R2,R2,49
ADD     R3, R2, R3
SW      R2,50(R3)
HLT
```

   Answer: 10

   The values of registers get updated in the following sequence:

   $R1 = 0 + 100 = 100$

   $R2 = Mem[100 + 40] = 59$

   $R3 = Mem[59 - 9] = 15$

$R2 = 59 - 49 = 10$

$R3 = 10 + 15 = 25$

$Mem[25 + 50] = 10$

3. For the register value **R4=75**, after execution of the instruction "**SLTI R1,R4, 30**", the contents of R1 will be ……..

   Answer: 0

   Here R4=75 and SLTI instruction set R1 to 1 only when value of R4 is less than 30; otherwise R1 is set to 0.

4. For the instruction encoding as discussed in the lectures, what will be the hexadecimal machine code for the instruction "**ADDI R25,R19,201**"?

   a. 32'h2a7100c9
   b. 32'h2e1701b9
   c. 32'h2a79000c9
   d. None of the above

   Answer: (c)

   For I-type instruction "**ADDI R25,R19,201**" the machine code will be:

   001010 10011 11001 0000 0000 1100 1001

   which is 2a7900c9.

5. For the following code segment, what will be the hexadecimal machine code for the BNEQZ instruction, assuming the instruction encoding as discussed in the lectures?

```
Loop:   ADD     R12,R15,R10
        SUBI    R11,R12,215
        MUL     R13,R12,R11
        SUB     R13,R13,R10
        ADDI    R27,R13,117
        BNEQZ   R27,Loop
```

   a. 32'h3b60fffa
   b. 32'h3a7000c
   c. 32'h3b90f0fb
   d. None of the above

   Answer: (a)

   When executing instruction "BNEQZ **R27,Loop**", PC points to the next instruction to be executed. So branch target will be -6 which in 16-bit 2's complement form is 1111 1111 1111 1010. Thus the instruction will be

   001110 11011 00000 1111 1111 1111 1010

   which is 3b60fffa.

6. Assume the value stored in memory location 100 is 9. The value of R11 after execution of the following code will be ….

```
                LW      R2,100(R0)
                ADDI    R11, R0, 0
LOOP:           ADD     R11,R2,R11
                SUBI    R2, R2, 1
                BNEQZ   R2, LOOP
                HLT
```

Answer: 45

The values of registers get updated in the following sequence:

1. $R2 = Mem[0 + 100] = 9$
2. $R11 = 0 + 0 = 0$
3. $R11 = R2 + R11 = 9 + 0 = 9$
4. $R2 = 9 - 1 = 8$

5. *Continue execution of instruction* 3 *and* 4 *until* $R2$ *not become* 0.

Thus the result will be sum of $9 + 8 + \cdots + 1 = 45$

7. The decimal number -17 is represented in 6-bit binary 2's complement notation. It is sign extended to 16 bits. The sign extended value in hexadecimal will be
   a. FFF5
   b. FFD7
   c. FFEF
   d. None of the above

Answer: (c)

In 6-bit -17 is represented as 101111 which after sign extended to 16 bits become: 1111 1111 11 10 1111.

8. Which of the following statements are true regarding execution of HALT instruction in a pipelined processor as discussed in the lecture?
   a. The processor will be stopped in instruction decoding stage.
   b. The execution must be continued till the end of pipeline stages.
   c. Subsequent instruction following this may be allowed to enter the pipeline.
   d. None of the above.

Answer: (b) and (c)

After encountering HALT instruction in decoding phase, the processor will continue till the end of all the pipeline stages to ensure execution of all previous instruction is completed. Thus option (a) is false and option (b) is true. Instructions appearing after HALT may be allowed but their write pipeline stages will be disabled. Thus option (c) is also true.

9. Why is the **`TAKEN_BRANCH`** signal required in the Verilog implementation of the pipelined processor as discussed in the lecture?
    a. It is used for locating the branch target in a pipelined architecture.
    b. Instruction entered in the pipeline after branch instruction will check this signal before performing write operation.
    c. It is used to prevent instruction appearing after branch instruction to enter into pipeline.
    d. None of the above.

    Answer: (b)

    In a pipelined processor the **execute** micro operation set the TAKEN_BRANCH signal in case the branch is actually taken and instruction following this branch instruction currently inside the pipeline verify the state of this signal before doing any write operation. Thus option (b) is true and options (a) and (c) are false.

10. Which of the following are true for test bench simulating execution of program in a pipelined processor as discussed in the lecture?
    a. The PC, HALTED and TAKEN_BRANCH all registers/flags may not require initialization.
    b. The test bench will load the program and initialize necessary registers before the program automatically starts executing.
    c. The result of execution can be verified from the output of the program.
    d. All of these.

    Answer: (b)

    After loading the program into the memory it is necessary to set PC to the starting address of the program and initialize the flags HALTED and TAKEN_BRANCH to start the execution of the program automatically. Thus option (a) is false whereas option (b) is true. To verify the output the values stored in memories and registers must be printed explicitly. Thus option (c) is also false.