Week 6: Assignment

1. Which of the following statements is/are false?
    a. Control path realizes the underlying FSM and for state transition it depends on control signal.
    b. All physical building blocks (both combinational and sequential) of a design are termed as data path.
    c. Control path is typically derived from the flow chart of the algorithm for physical implementation.
    d. Control path is usually designed later in the synthesis process after implementing data path and control module operates on top of data path modules.

    Answer: (a) and (b)

    Control path implements the underlying FSM by providing necessary control signals. Thus option (a) is false. For generating necessary control signals control path may contains combinational as well as sequential elements. Thus option (b) is also false. All states and state transitions are derived from the flow chart of the algorithm to be implemented. Thus option (c) is true. All the identified functional blocks required in the data path are implemented with necessary control signals before designing control path. Thus option (d) is also true.

2. Multiplying 2 n-bit numbers which of the following is true for Booth's multiplication?
    a. The algorithm performs exactly n shift operations and for storing multiplication result it requires storage of size 2n+1 bit.
    b. The multiplier iterates n-times and either addition or subtraction of multiplier is performed at each iteration.
    c. Addition or subtraction is avoided if both the bits of encountered bit pair "M_0M_{-1}" of the multiplier ($M_{n-1}...M_0M_{-1}$) are in same logical state.
    d. Addition is only performed in a particular stage of multiplication if the encountered bit pair "M_0M_{-1}" of the multiplier ($M_{n-1}...M_0M_{-1}$) shows the pattern "10".

    Answer:(c)

    A 2n bit storage is required to store the result of multiplication of two n-bit number. Thus option (a) is false. Addition or subtraction is only performed in a particular step if the two bits "M_0M_{-1}" of the multiplier ($M_{n-1}...M_0M_{-1}$) are not same. Thus option (b) is false and option (c) is true. Addition is performed, if the bit pair "M_0M_{-1}" of the multiplier ($M_{n-1}...M_0M_{-1}$) is "01". Thus option (d) is also false.

3. What do you mean by synthesizable Verilog?
    a. A software tool that can synthesize a given Verilog description.
    b. A software tool that the simulation tool can verify for synthesis.
    c. A subset of the language Verilog features that are well supported by synthesis tool.

d. None of the above.

Answer: (c)

Not all Verilog language features are supported by the synthesis tool. A subset of Verilog language constructs that are accepted by the synthesis tool is termed as synthesizable Verilog. Thus option (a) and (b) are not correct whereas option (c) is correct.

4. For combinational circuit synthesis, which of the following are recommended?
   a. Feedback connections from output to input may be allowed.
   b. If "if…else" construct is used, value must be assigned to the output variable for all possible combinations of the inputs.
   c. Procedural assignment must not be used.
   d. All of the above.

   Answer: (b)

   Feedback connection from output to input results in sequential behavior and must not be present in a combinational circuit. Thus option (a) is correct. If values of output variables are not specified for all input permutation, the circuit may be realized sequential. Thus option (b) is also correct. Continuous as well as procedural assignment both can be used in realizing combinational circuit. Thus option (c) is not correct.

5. What does the following Verilog code realize?

```
input A, B, C, D;
input [2:0] S;
output reg f;
always @(A or B or C or D or S[0] or S[1] or S[2])
begin
      if (S == 1)      f  =  A & B;
      if (S == 2)      f  = B;
      if (S == 3)      f = C | D;
end
```

   a. A combinational circuit will be realized
   b. A sequential circuit with 3 latches will be realized
   c. A 3-input multiplexer will be realized
   d. A sequential circuit with 1 latch will be realized

   Answer: (b)

   Here the variable f is not updated for all possible values of 3-bit vector S, thus a sequential circuit will be realized. Here 1 latch will be inferred to retain the state of variable f. Thus options (a), (b) and (c) are not correct whereas option (d) is correct.

6. Which of the following statements are true?
   a. Both the input and output arguments of function and task appear in the same order.
   b. A task can be called from an assignment statement.

c. Function can return more than one output value.
d. Functions and tasks without event or delay control can be used for modeling combinational logic.

Answer: (d)

A function does not take as arguments only outputs; it only takes inputs as arguments. Thus option (a) is false. Tasks can return more than one output value and cannot be used in assignment statement. Thus option (b) is false. Function only returns a single output value. Thus option (c) is also false. For modeling combinational logic both functions and tasks without event or delay control can be used. Thus option (d) is false.

7. Which of the following Verilog constructs are synthesizable?
   a. User defined primitives
   b. All operators
   c. All assignment statements
   d. Built-in gate primitives

   Answer: (c) and (d)

   Only combinational user defined primitives are synthesizable. Thus option (a) is not correct. Operators === and !== are not synthesizable. Thus option (b) is also not correct. Continuous as well as procedural assignments are synthesizable. Thus option (c) is correct. All built-in gate primitives are synthesizable. Thus option (d) is also correct.

8. Which of the following statements are true?
   a. Tasks may execute in 0 simulation time.
   b. Functions can call other functions or tasks.
   c. Data dependent loops must be avoided for combinational synthesis.
   d. Combinational feedback loop may be considered for combinational synthesis.

   Answer: (c)

   As tasks may contain delay, the simulation of such tasks will be delayed. Thus option (a) is false. Function can only call other function. Thus option (b) is also false. Data dependent loops are not synthesizable. Thus option (c) is true. Combinational feedback loop may lead to sequential element and must be avoided for combinational synthesis. Thus option (d) is false.

9. Which of the following statements are false?
   a. Non-blocking assignment statement should be used inside procedural blocks for modeling combinational logic.
   b. The “default” case assignment must be used for realizing sequential circuits.
   c. Incomplete specification of conditional expression may be used to realize combinational logic.
   d. User defined primitive must not be used for synthesis.

Answer: (a), (b) and (c)

Inside procedural block blocking assignments should be used for modeling combinational logic. Thus option (a) is false. The "default" case assignment must be used for realizing combinational circuits. Thus option (b) is false. Incomplete specification of conditional expression may infer latches. Thus option (c) is also false. Only combinational user defined primitives are synthesizable. Thus option (d) is true.

10. Which of the following statements are true about the verilog code:

```
input x, y, z;
output reg w;
always @ (z)
  if(z)       w = x;
  else        w = y;
```

a. Behavioral model of a 2 to 1 multiplexer.

b. A latch will be inferred for output w.

c. Description of a synthesizable combinational logic.

d. Description of a synthesizable sequential logic.

Answer: (b) and (d)

Since the sensitivity list does not contain all input variables, a latch will be inferred at the output w. Thus options (a) and (c) are false whereas options (b) and (d) are true.