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Unit 11: Analog Switches

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Digital Circuit and BJT Inverter

1
Unit

1.1 INTRODUCTION

Today, All most digital systems are based on integrated circuit (IC) technology wherein various design options and trade-offs exist. The choices must be made for digital circuit family based on level of integration and programmable versus fixed-function circuits.

The various integrated circuit technologies have widely differing characteristics. Integrated circuit process and Device Engineers continue to make improvements in these technologies. Some understanding of integrated circuit fabrication techniques is required to understand the relative characteristics of different logic families, such as TTL, ECL, NMOS and CMOS. An appreciation for the direction and rate of change in fabrication technology becomes important, if product designs are to provide good possibilities for evolutionary improvement.

Excellent system designs needs that design decisions result in a good balance among system characteristics, logic design, circuit design, layout and design fabrication technology.

Digital Circuit

- Combinational circuit
- Sequential circuit

Logic gates

- i) AND, OR, NOT
- ii) NAND, NOR

iii) EX-OR, EX-NOR

Digital I.C. are manufactured utilizing 2-basic Technologies: Bipolar and Mos.

Bipolar families:

RTL, DTL, IIL, HTL, TTL, ECL etc.

MOS families:

PMOS, NMOS, CMOS etc.

When any logic family Require to be selected to perform some specific Task, the most important characteristics in selecting a logic family are:

- Propagation Delay
- Fan-out
- Power Dissipation
- Noise Margin
- Power Delay Product

These parameters has own importance and play important role in study of Digital Integrated Electronics.

1.2 PROPAGATION DELAY

Rise Time, Fall Time & Propagation Delay determines the speed of the logic family. These parameters describes that the time delay that results when a logic gates make transition from one state to another.

Time delay occurred due to the fact that capacitance associated with the digital circuit can not get charged & discharged instantly.

Rise Time ' t_R ' is the time required for output to change form 10% to 90% of difference between $V(0)$ to $V(1)$.

Similarly, Fall time ' t_F ' is the Time required for an output to change form 90% to 10% of difference between $V(1)$ to $V(0)$.

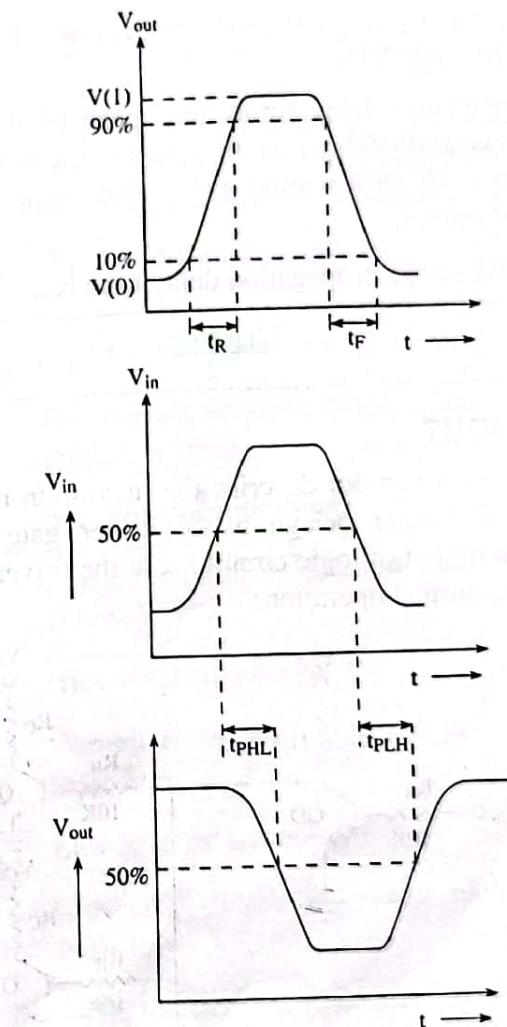


Fig. 1.1 : Diagram illustrating propagation delay

The Rise Time ' t_R ' and Fall Time ' t_F ' need not always be equal. Propagation delay of switching circuit, [defines how fast circuit output responds due to the change in its input.]

The propagation delay describes the Time lag between an input signal transition and corresponding output transition. The propagation delay is measured between points on the input

and output wave forms where the voltage lies half way (50%) between $V(0)$ and $V(1)$.

Propagation delay limits the speed of the circuit. The turn on propagation delay time t_{PLH} , low to the high transition of output, Turn off propagation delay time t_{PHL} , high to low transition of output.

The Average propagation delay time is

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

1.3 FANOUT

The term Fan-out describes the maximum number of the load gate of similar design as of driver gate that can be connected at output of logic circuit i.e. at the driver gate without degrading its normal operation.

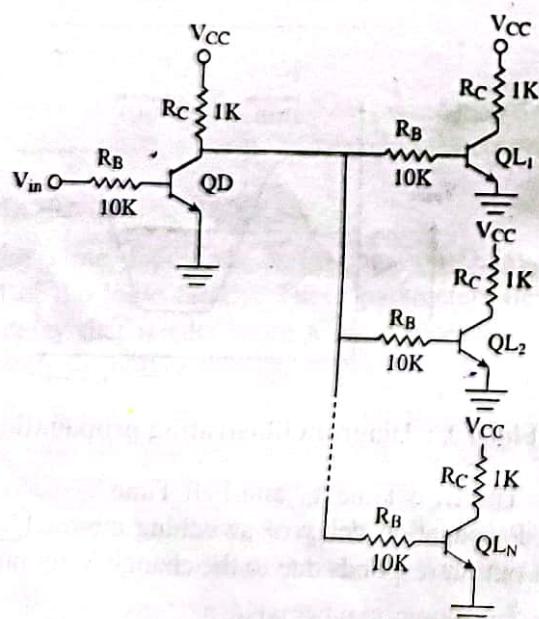


Fig. 1.2 : BJT Inverter having N load gates

The larger the "fan-out" betters the driving capability of the gate.

It is represented by 'N' and it is expresses as

The fan-out

$$N = \left\lceil \frac{|I_{OH}|}{|I_{IH}|}, \frac{|I_{OL}|}{|I_{IL}|} \right\rceil \text{ Minimum of Two.}$$

I_{IH} : High level input current

The current at input when a high level voltage is applied at input.

I_{IL} : Low level Input current

Current at input when a low level voltage is applied at input.

I_{OH} : High level output current

Current at output with input such that output is at logic high.

I_{OL} : Low level output current

Current at output with input such that output is at logic low.

Similarly, the term 'Fan-in' refers to the number of input that a signal gate can accommodate.

e.g. A 3 - Input AND gate has Fan-in of 3.

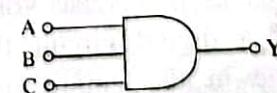


Fig. 1.3 : Input AND gate

1.4 POWER DISSIPATION

It represents the amount of power delivered from power supply to the gate. The power dissipation is a parameter expressed in 'mW' and represents the amount of power needed by a gate.

There are two components of power dissipated in a logic circuit.

- Static power Dissipation
- Dynamic power Dissipation

The amount of power consumed by circuit when it is not changing its states is termed as static power dissipation. The dynamic power dissipation is the power consumed by circuit when it is in switching states.

The amount of power dissipated in a gate is calculated as $V_{CC} \times I_C$. The current drain from the power supply depends on the logic states of gate.

Average power dissipation

$$P_{D(\text{avg})} = V_{CC} \times I_{C(\text{avg})}$$

$$I_{C(\text{avg})} = \frac{I_{CH} + I_{CL}}{2}$$

I_{CH} : Current corresponding to the high level output.

I_{CL} : Current corresponding to low level output.

1.5 NOISE MARGIN

It is defined as the Noise voltage added to an Input voltage signal of a digital circuit that does not cause an undesirable change in the circuit output. Noise margin is expressed in volts and represents the maximum noise signal that can be tolerated by the gate.

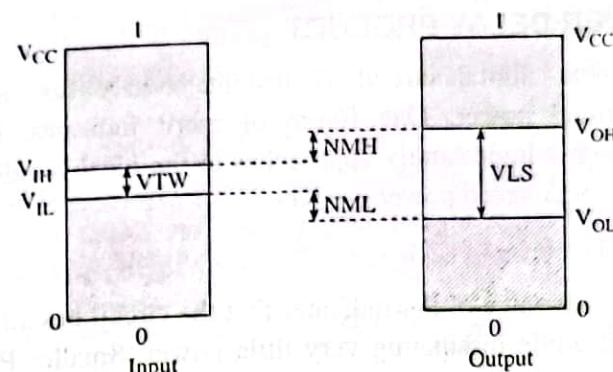


Fig. 1.4 : Illustration for noise margin

From diagram,

$$NMH = V_{OH} - V_{IH}$$

$$NML = V_{IL} - V_{OL}$$

$$VTW = V_{IH} - V_{IL}$$

$$VLS = V_{OH} - V_{OL}$$

V_{IH} – High level Input voltage

It is the minimum voltage at input that is recognized as logic 1 by the given gate.

V_{IL} – Low level Input voltage

It is the maximum voltage at input that is recognized as logic 0 by the given gate.

In order to compensate for any noise signals, the circuit must be designed such that $V_{IL} > V_{OL}$ and $V_{IH} < V_{OH}$.

A smaller transition width and larger logic swing will improve the noise margin. Large value of NMH & NML results in gate that can process noise fluctuations without losing digital character of logic levels.

The absolute noise margin NM for a gate is smaller of two noise margins.

$$NM = \min [NML, NMH]$$

1.6 POWER DELAY PRODUCT

An ideal digital circuit is instantaneously fast and requires minimal power. One figure of merit indicates, the degree to which a logic family approaches to the ideal is called the power delay or speed power product.

$$P_{DP} = t_p \times P_D$$

A smaller value of P_{DP} indicates that the circuit has a fast response time while dissipating very little power. Smaller P_{DP} , closer towards the ideal.

1.7 BJT INVERTER

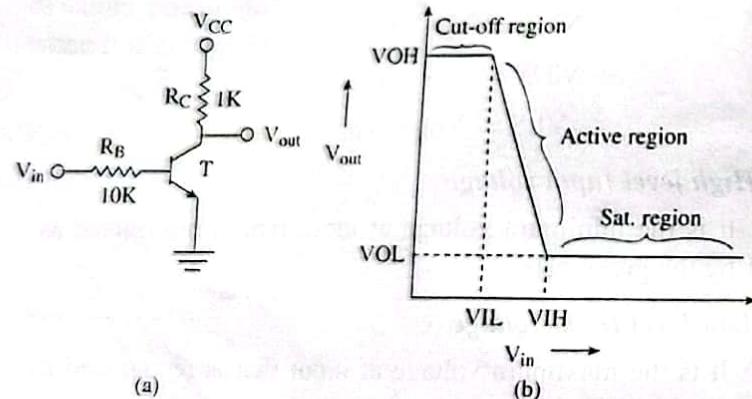


Fig. 1.5 : BJT inverter and its VTC

The CKT diagram of BJT Inverter is shown above.

For Input voltage ' V_{in} ' below the turn on voltage $V_{BE(on)}$ of the transistor, the transistor is in cut-off mode, since the base voltage becomes negligible, the collector current is essentially zero and the output voltage ' V_{out} ' is equal to V_{CC} .

When the Input is increased above $V_{BE(on)}$, the transistor turns on and enters into the forward active mode. Further

increase in the input voltage causes the output voltage to drop due to increasing collector current.

$$V_{out} = V_{CC} - I_c R_C \quad \dots \dots \dots (i)$$

With the sufficient Input voltage, when the output voltage has fallen sufficiently, the transistor will enter into saturation. The output voltage V_{out} becomes low i.e. $V_{CE(sat)}$.

Thus, as summary, one write it as

Case I: when Input is at low

The Transistor becomes at cut-off and output become at high.

Case II: When Input is at high.

The Transistor T turns into saturation mode and output become at low.

That's why above BJT circuit acts as Inverter.

1.8 ✓ VOLTAGE TRANSFER CHARACTERISTICS (VTC)

When output is plotted w.r. to input, the nature of graph obtained is term as VTC for that circuit.

The Input output voltage characteristics (VTC) shows a constant output voltage V_0 of V_{CC} for V_i going from zero to $V_{BE(on)}$. As V_i is increased above first break point at $V_i = V_{BE(cut-in)} = 0.6$ V and $V_0 \approx V_{CC}$, the transistor enters forward Active mode.

The collector current ($I_C = \beta I_B$) causes a voltage drop in the collector resistor and the collector voltage $V_C = V_0 = (V_{CC} - I_c R_C)$ falls.

The active mode operation continues for increasing V_i until, the collector voltage drops to about $V_{CE(sat)} = 0.1$ V.

Now, The Collector Base Junction (CBJ) is forward biased and mode changes to saturation. Input voltage higher than that required to forward bias the CBJ drive transistor heavily into saturation.

The Input voltage at the second break point is calculated using condition that transistor is on the verge of going from active to saturation mode.

1.9 NOISE MARGIN

To calculate noise margin of circuit, one must require to compute four parameters V_{OH} , V_{IH} , V_{OL} & V_{IL} . Thus, let's apply four conditions on BJT Inverter circuit.

Case I: When transistor is at cut-off mode

$$V_O = V_{OH} = V_{CC}$$

$$\therefore V_{OH} = V_{CC} \quad \dots \dots \text{(i)}$$

Case II: when transistor is at edge of conduction

$$V_{in} = V_{IL} = V_{BE(on)} = 0.7V$$

$$\therefore V_{IL} = V_{BE(on)} = 0.7 V \quad \dots \dots \text{(ii)}$$

Case III: When Transistor is at edge of saturation.

$$V_{in} = V_{IH} \quad \dots \dots \text{(i)}$$

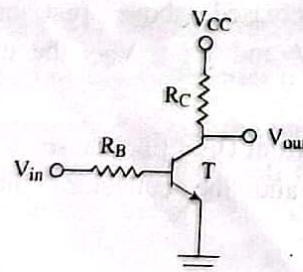


Fig. 1.6 : BJT inverter

Applying kvl at input of ckt

$$V_{in} - I_B [EOS] R_B - V_{BE(sat)} = 0$$

$$\therefore V_{in} = V_{BE(sat)} + I_B(EOS)R_B$$

$$\therefore V_{IH} = V_{BE(sat)} + I_B(EOS)R_B \quad \dots \dots \text{(ii)}$$

Applying kvl at O/P side

$$V_{CC} - I_C(sat) R_C - V_{CE(sat)} = 0$$

$$V_{CC} - V_{CE(sat)} = I_C(sat) \times R_C$$

$$\therefore I_C(sat) = \frac{V_{CC} - V_{CE(sat)}}{R_C} \quad \dots \dots \text{(iii)}$$

But we Know relation between base & collector current

$$I_B(EOS) = \frac{I_C(sat)}{\beta} \quad \dots \dots \text{(iv)}$$

$$= \frac{V_{CC} - V_{CE(sat)}}{\beta R_C} \quad \dots \dots \text{(v)}$$

From equation (ii) & (v)

$$V_{IH} = V_{BE(sat)} + \frac{R_B}{\beta R_C} [V_{CC} - V_{CE(sat)}] \quad \dots \dots \text{(vi)}$$

Case IV:

When Transistor is at saturated mode

$$V_O = V_{OL} = V_{CE(sat)}$$

$$\therefore V_{OL} = V_{CE(sat)} = 0.2 V \quad \dots \dots \text{(vii)}$$

Thus, by knowing these four parameters, one could compute

$$NMH = V_{OH} - V_{IH}$$

$$NML = V_{IL} - V_{OL}$$

$$VTW = V_{IH} - V_{IL}$$

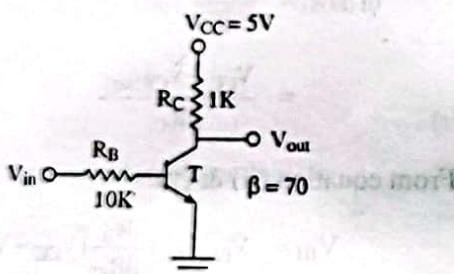
$$V_{LS} = V_{OH} - V_{OL}$$

Note: Above voltage are applicable for NO load condition at O/P of Inverter.

Example

For the BJT inverter circuit shown below, the transistor used is an npn type with specifications as follows: $V_{BE(on)} = 0.7 \text{ V}$, $V_{BE(sat)} = 0.8 \text{ V}$, $V_{CE(sat)} = 0.1 \text{ V}$, $\beta = 70$, $R_B = 10 \text{ k}$, $R_C = 1 \text{ K}$, $V_{CC} = 5 \text{ V}$. Compute

- i) Noise Margin [NMH and NML]
- ii) Voltage Logic Swing [VLS].
- iii) Voltage Transition Width (VTW).



Solution:

Case I: When transistor is a cut-off mode,

$$\boxed{V_O = V_{OH} = V_{CC}}$$

$$\therefore V_{OH} = 5 \text{ V} \quad \dots \dots \dots \text{(i)}$$

Case II: When transistor is at edge of conduction.

$$\boxed{V_{in} = V_{IL} = V_{BE(on)}}$$

$$\therefore V_{IL} = 0.7 \text{ V} \quad \dots \dots \dots \text{(ii)}$$

Case III: When transistor is at edge saturation.

$$\boxed{V_{in} = V_{IH}}$$

$$V_{IH} = V_{BE(sat)} + \frac{R_B}{\beta R_C} [V_{CC} - V_{CE(sat)}]$$

$$= 0.8 + \frac{10 \text{ k}}{70 \times 1 \text{ k}} [5 - 0.1]$$

$$= 0.8 + \frac{1}{7} [4.9]$$

$$= 0.8 + 0.7$$

$$V_{IH} = 1.5 \text{ V} \quad \dots \dots \dots \text{(iii)}$$

Case IV: When transistor is at saturated mode.

$$V_O = V_{OL} = V_{CE(sat)}$$

$$\therefore V_{OL} = 0.1 \text{ V} \quad \dots \dots \dots \text{(iv)}$$

$$\therefore \text{Thus, i) } \boxed{NMH = V_{OH} - V_{IH}}$$

$$= 5 - 1.5 = 3.5 \text{ V}$$

$$NMH = 3.5 \text{ V}$$

$$\boxed{NML = V_{IL} - V_{OL}}$$

$$= 0.7 - 0.1 = 0.6 \text{ V}$$

$$NML = 0.6 \text{ V}$$

$$\therefore \text{ii) } \boxed{V_{LS} = V_{OH} - V_{OL}}$$

$$= 5 - 0.1 = 4.9 \text{ V}$$

$$V_{LS} = 4.9 \text{ V}$$

$$\therefore \text{iii) } \boxed{VTW = V_{IH} - V_{IL} = 1.5 - 0.7}$$

$$= 0.8 \text{ V}$$

$$VTW = 0.8 \text{ V}$$

1.10 FANOUT

As we know, fan-out of the Inverter is the No. of identical circuit that the Inverter can drive before output V_0 enters the transition region. The O/P of inverter must have either at low or high.

Case I: When output is at low

When the output of BJT Inverter (Driver) is at logic low, it can drive practically any no. of identical inverters load gates, since each load transistor is operating in the cut-off mode. No current is drawn via the collector resistor of the driver and output voltage remains at logic low.

Case II: When output is at high

For logical high output of the driver, since saturation Base current of each load inverter is supplied by the driver, the output voltage decreases from V_{CC} . Thus, no. of load gates at O/P get restricted.

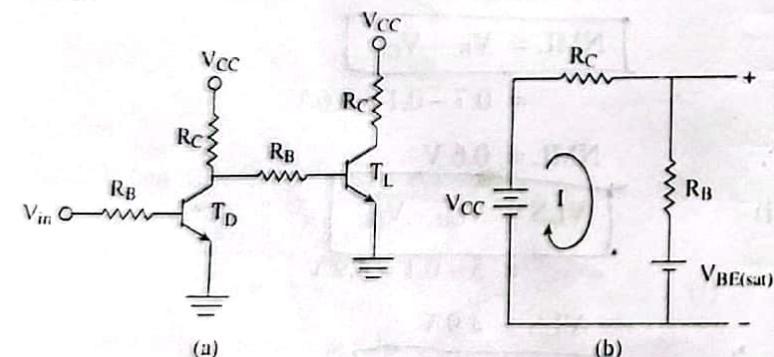


Fig. 1.7 : BJT inverter illustrating fan-out

From above diagram

$$V_{OH} - IR_B - V_{BE(\text{sat})} = 0$$

$$\therefore V_{OH} = IR_B + V_{BE(\text{sat})} \quad \dots \dots \text{(i)}$$

Applying kvl on diagrams 1.7 b loop

$$V_{CC} - IR_C - IR_B - V_{BE(\text{sat})} = 0$$

or,

$$I(R_B + R_C) = V_{CC} - V_{BE(\text{sat})}$$

$$I = \frac{V_{CC} - V_{BE(\text{sat})}}{R_B + R_C} \quad \dots \dots \text{(ii)}$$

From equation (i) & (ii)

$$V_{OH} = V_{BE(\text{sat})} + \frac{R_B}{R_B + R_C} [V_{CC} - V_{BE(\text{sat})}] \quad \dots \dots \text{(iii)}$$

Due to the application of one load gate, V_{OH} gets reduced, as a consequence NMH also reduced.

With N load gates, the V_{OH} becomes

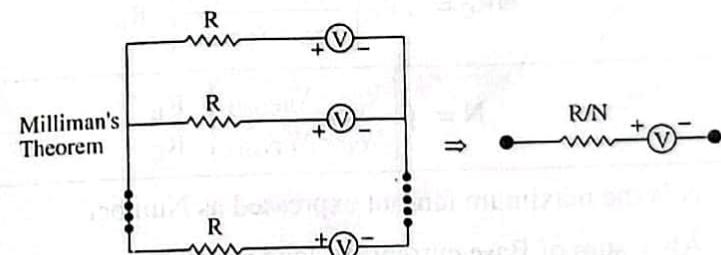


Fig. 1.8 : Circuit indicating Milliman's theorem

Based on Milliman's Theorem equation (iii) could be written as

$$V_{OH} = V_{BE(\text{sat})} + \frac{R_B / N}{\frac{R_B}{N} + R_C} [V_{CC} - V_{BE(\text{sat})}] \quad \dots \dots \text{(iv)}$$

The maximum Fan-out is the maximum no. of gates that can be connected at output.

This implies

$$NMH = 0$$

$$\text{i.e. } V_{OH} - V_{IH} = 0$$

$$\text{i.e. } V_{OH} = V_{IH}$$

Substituting these two values

$$V_{BE(sat)} + \frac{R_B/N}{R_B + R_C} [V_{CC} - V_{BE(sat)}] = V_{BE(sat)} + \frac{R_B}{\beta R_C} [V_{CC} - V_{CE(sat)}]$$

$$\frac{R_B/N}{R_B + NR_C} [V_{CC} - V_{BE(sat)}] = \frac{R_B}{\beta R_C} [V_{CC} - V_{CE(sat)}]$$

$$\beta R_C [V_{CC} - V_{BE(sat)}] = (R_B + NR_C) [V_{CC} - V_{CE(sat)}]$$

or,

$$R_B + NR_C = \beta R_C \left[\frac{V_{CC} - V_{BE(sat)}}{V_{CC} - V_{CE(sat)}} \right]$$

or,

$$NR_C = \beta R_C \left[\frac{V_{CC} - V_{BE(sat)}}{V_{CC} - V_{CE(sat)}} \right] - R_B$$

$$\therefore N = \beta \left[\frac{V_{CC} - V_{BE(sat)}}{V_{CC} - V_{CE(sat)}} \right] - \frac{R_B}{R_C}$$

N is the maximum fan-out expressed as Number.

Also, sum of Base currents of load resistors

$$IL = NI_{B(sat)} = NKI_{B(EOS)}$$

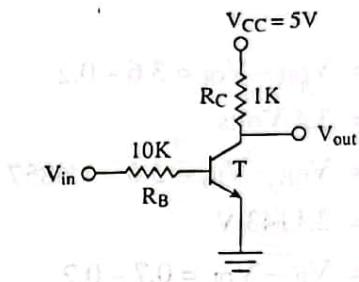
When K is over driven factor,

$$K = \frac{I_{B(sat)}}{I_{B(EOS)}}$$

EOS - Edge of saturation.

Example:

- For the BJT inverter circuit shown below. Assume $\beta = 70$, $V_{BE(on)} = 0.7$ V, $V_{BE(sat)} = 0.8$ V, $V_{CE(sat)} = 0.2$ V,
- Calculate logic swings and Noise Margin for fan-out = 5.
 - Compute fan-out for $NMH = NML$.



Solution:

- (i) For fan-out = 5.

$$V_{OH} = V_{BE(sat)} + \frac{R_B/N}{R_B + R_C} [V_{CC} - V_{BE(sat)}]$$

$$= 0.8 \text{ V} + \frac{10/5}{10+1} [5 - 0.8]$$

$$= 0.8 + \frac{2}{2+1} [4.2]$$

$$= 0.8 + \frac{2}{3} \times 4.2 = 0.8 + 2.8$$

$$V_{OH} = 3.6 \text{ V} \quad \dots\dots\dots (i)$$

$$V_{IH} = V_{BE(sat)} + \frac{R_B}{\beta R_C} [V_{CC} - V_{CE(sat)}]$$

$$= 0.8 + \frac{10}{70 \times 1} [5 - 0.2]$$

$$V_{IH} = 0.8 + \frac{1}{7} \times 4.8$$

$$V_{IH} = 1.4857 \text{ V} \quad \dots\dots\dots (ii)$$

$$V_{IL} = V_{BE(on)} = 0.7 \text{ V} \quad \dots\dots\dots (iii)$$

$$V_{OL} = V_{CE(sat)} = 0.2 \text{ V} \quad \dots\dots\dots (iv)$$

Thus,

$$\text{i) } V_{LS} = V_{OH} - V_{OL} = 3.6 - 0.2 \\ = 3.4 \text{ Volts}$$

$$NMH = V_{OH} - V_{IH} = 3.6 - 1.4857 \\ = 2.1143 \text{ V}$$

$$NML = V_{IL} - V_{OL} = 0.7 - 0.2 \\ = 0.5 \text{ V}$$

ii) Fan-out for $NMH = NML$.

$$\text{Thus, } V_{OH} - V_{IH} = V_{IL} - V_{OL}$$

$$V_{BE(sat)} + \frac{R_B|N|}{R_B + R_C} [V_{CC} - V_{BE(sat)}]$$

$$- V_{BE(sat)} - \frac{R_B}{\beta R_C} [V_{CC} - V_{CE(sat)}] = 0.7 - 0.2$$

$$\frac{R_B|N|}{R_B + NR_C} [V_{CC} - V_{BE(sat)}] - \frac{R_B}{\beta R_C} [V_{CC} - V_{CE(sat)}] = 0.5$$

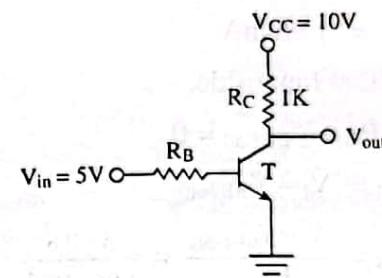
$$\frac{R_B}{R_B + NR_C} [5 - 0.8] - \frac{10k}{70 \times 1k} [5 - 0.2] = 0.5$$

$$\text{or, } \frac{R_B}{R_B + NR_C} [4.2] - \frac{1}{7} \times 4.8 = 0.5$$

After calculation, the value N Becomes 25.42.

Thus $N = 25$

- 7-2. For the transistor shown in figure below is specified to have ' β ' in the range 50 to 150. Find the value of R_B that results in saturation with an overdrive factor of at least '10'. Use $V_{BE(on)} = 0.7 \text{ V}$, $V_{BE(sat)} = 0.8 \text{ V}$, $V_{CE(sat)} = 0.2 \text{ V}$.



Solution:

For $V_i = 5 \text{ V}$,

The transistor T turns into saturation mode, applying kvl at output side,

$$V_{CC} - I_{C(sat)} R_C - V_{CE(sat)} = 0$$

$$\text{or, } I_{C(sat)} R_C = V_{CC} - V_{CE(sat)}$$

$$\therefore I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \\ = \frac{10 - 0.2}{1k} = \frac{9.8}{1000} \\ = 9.8 \text{ mA}$$

$$\text{But } I_{C(sat)} = \beta I_{B(EOS)}$$

$$\therefore I_{B(EOS)} = \frac{I_{C(sat)}}{\beta} = \frac{9.8 \times 10^{-3}}{50} \\ = 1.96 \times 10^{-3} = 1.96 \text{ mA}$$

Now, we know over drive factor

$$K = \frac{I_{B(sat)}}{I_{B(EOS)}}$$

$$I_{B(sat)} = K I_{B(EOS)} \\ = 10 \times 1.96 \times 10^{-4} \text{ A} \\ = 1.96 \times 10^{-3} \text{ A}$$

$$= 1.96 \text{ mA}$$

Now, Applying KVL at Input side,

$$V_i - I_{B(\text{sat})} \times R_B - V_{BE(\text{sat})} = 0$$

$$I_{B(\text{sat})} R_B = V_i - V_{BE(\text{sat})}$$

$$\therefore R_B = \frac{V_i - V_{BE(\text{sat})}}{I_{B(\text{sat})}} = \frac{5 - 0.8}{1.96 \times 10^{-3}}$$

$$= \frac{4.2}{1.96 \times 10^{-3}} = 2142.857 \Omega$$

$$= 2.142 \text{ k}\Omega$$

Once, Again Computing the things for $\beta = 150$.

$$I_{B(EOS)} = \frac{I_{C(\text{sat})}}{\beta} = \frac{9.8 \times 10^{-3}}{150}$$

$$= 6.533 \times 10^{-5} \text{ A}$$

Again, Overdrive factor

$$K = \frac{I_{B(\text{sat})}}{I_{B(EOS)}}$$

$$\therefore I_{B(\text{sat})} = K I_{B(EOS)}$$

$$= 10 \times 6.533 \times 10^{-5} \text{ A}$$

$$= 6.533 \times 10^{-4} \text{ A}$$

and,

$$R_B = \frac{V_i - V_{BE(\text{sat})}}{I_{B(\text{sat})}} = \frac{5 - 0.8}{6.533 \times 10^{-4}}$$

$$= \frac{4.2 \times 10^4}{6.533} = 6428.899 \Omega$$

$$= 6.428 \text{ k}\Omega$$

Thus, the value of R_B ranges from $2.142 \text{ k}\Omega$ to $6.428 \text{ k}\Omega$.

SUMMARY

This chapter provides the Analysis Techniques for the static and dynamic characteristics in selecting logic family and BJT inverter circuit with following ideas.

- Important characteristics in selecting logic family are
 - Propagation Delay
 - Fan-out
 - Power dissipation
 - Noise Margin
 - Power Delay Product
- BJT Inverter functions are discussed with some typical parameters mentioned below.
 - BJT as NOT gate
 - Voltage Transfer Characteristics (VTC)
 - Noise margin, NMH, NML
 - Fan-out N
- Typically important Numerical based on BJT inverter are analytically solved.

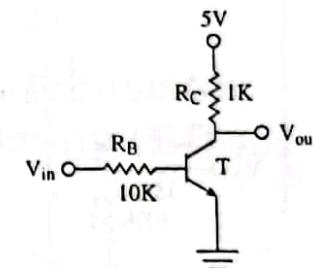
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PROBLEMS

1. Define propagation delay. Discuss the role played by rise time, fall time on digital circuit speed. Also discuss the terms mentioned below.
 - i) Rise time versus fall time
 - ii) t_{PLH} versus t_{PHL}
 - iii) Input versus output signal transition.
2. Define fan-out. Discuss the importance of terms fan-in and fan-out in digital circuit.
3. Define power dissipation. Discuss the terms mentioned below.
 - i) Static versus dynamic power dissipation
 - ii) Average power dissipation.
4. Draw logic level diagram to represent noise margins. Discuss the terms mentioned below.
 - i) High level versus low level Noise Margins
 - ii) Voltage transition width versus voltage logic swing.
5. Draw BJT inverter circuit and for "BJT inverter", discuss the terms mentioned below.
 - i) BJT as NOT gate
 - ii) Voltage transfer characteristics
 - iii) Noise Margin.
6. Draw BJT inverter circuit. Discuss its operation and derive an expression of fan-out for N number of load gates.
7. For the BJT Inverter shown in diagram 7 below,



Assume $\beta = 30$

$V_{BE(on)} = 0.7 \text{ V}$

$V_{BE(sat)} = 0.8 \text{ V}$

$V_{CE(sat)} = 0.1 \text{ V}$

Calculate the noise margins, logic swings and transition width.

8. For the BJT inverter shown in diagram 7 above,

Assume $\beta = 50$

$V_{BE(on)} = 0.7 \text{ V}$

$V_{BE(sat)} = 0.8 \text{ V}$

$V_{CE(sat)} = 0.2 \text{ V}$

- a) Calculate noise margin for fan-out = 10

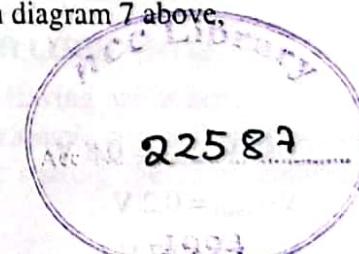
- b) Compute fan-out for $NMH = NML$

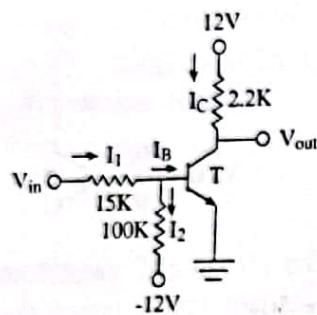
9. The transistor shown in diagram 9 below is specified to have ' β ' in the Range 50 – 150. Find the value of R_B that results in saturation with an overdrive factor of at least 20

Use $V_{BE(on)} = 0.7 \text{ V}$

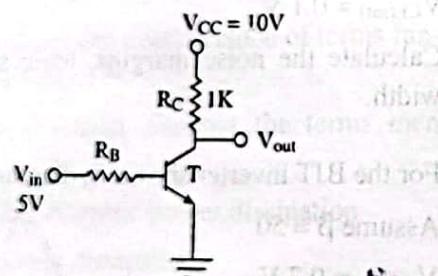
$V_{BE(sat)} = 0.8 \text{ V}$

$V_{CE(sat)} = 0.2 \text{ V}$





10. For silicon transistor shown in diagram 10 below with $hFE = 30$, find the output levels for input levels '0' V and '12' V.



Use $V_{BE(sat)} = 0.8$ V

$V_{CE(sat)} = 0.2$ V

$V_{BE(on)} = 0.7$ V

Also calculate I_1 , I_2 , I_B & I_C .

Resistor Transistor Logic (RTL)

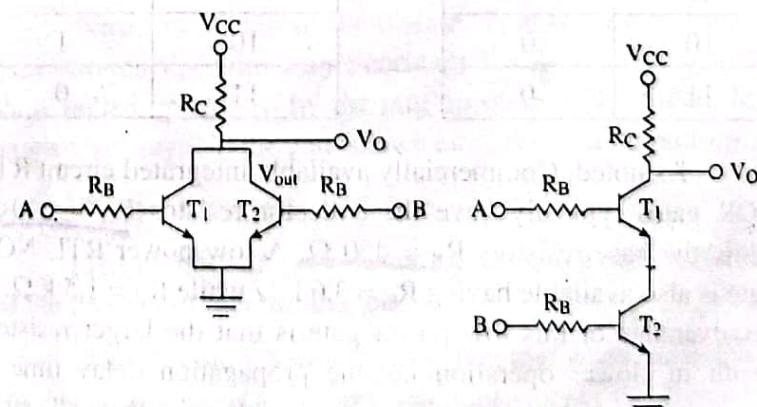
2
Unit

2.1 INTRODUCTION

Historically, The RTL gate is the first gate to have been used extensively and many installations employing this type of gate are still in operation. Thus, discussion begins for logic gates by considering the Resistor Transistor (RTL). This type of gate is no longer used in new design, but for a number of reasons the RTL becomes useful starting point. On the other hand, this gate is elegantly simple and hence may be used conveniently to develop concepts useful in connection with all types of gate.

2.2 RESISTOR TRANSISTOR LOGIC (RTL)

RTL is a first digital IC Having wide acceptance in commercial market. The circuit is a simple connection of two or more saturating transistor inverter sharing the same collector resistor.



(a) RTL NOR gate

(b) RTL NAND gate

Fig 2.1: (a) RTL as NAND and (b) NOR gate

A 2-Input digital gate is illustrated in diagram 2.1 above.

When the Input voltage is less than $V_{BE(on)}$, the transistor is in cut-off mode. Hence, output becomes high. When input voltage exceeds $V_{BE(on)}$, the transistor starts conducting & saturates. Thus output becomes at low.

Here, the output of two inverters are wired AND providing NOR output.

Similarly, A 2-Input NAND gate of RTL is illustrated in fig 2.1b.

When both the transistors are conducting. The path between V_{CC} and ground is complete i.e. V_{CC} is connected to ground. Hence, output becomes at low.

If any one input is at low, the path is broken. Hence, output remains at high.

Truth table for NOR gate

AB	VO
00	1
01	0
10	0
11	0

Truth table for NAND gate

AB	VO
00	1
01	1
10	1
11	0

As noted, Commercially available integrated circuit RTL NOR gates typically have the collector resistor $R_C = 640 \Omega$ while the base resistors $R_B = 450 \Omega$. A low power RTL NOR gate is also available having $R_C = 3.6 \text{ k}\Omega$ while $R_B = 1.5 \text{ k}\Omega$. A disadvantage of this low power gate is that the larger resistors result in slower operation i.e. the propagation delay time is longer. The reason for this longer delay is that all stray capacitors and capacitors inherent in the active devices must charge and discharge via these larger resistors.

full - up \rightarrow Active - Transistor is used
Passive - Resistor is used (not Transistor).
Resistor Transistor Logic (RTL) | 27

2.3 PULL UP RESISTOR

The collector resistor R_C in the RTL gate is often called a passive pull-up Resistor. As shown in diagram a load capacitance C_L is connected at output of RTL NOR gate. This capacitance is due to in part of stray capacitance and in part to the capacitance associated with the base-emitter junctions of gates driven by the gate shown.

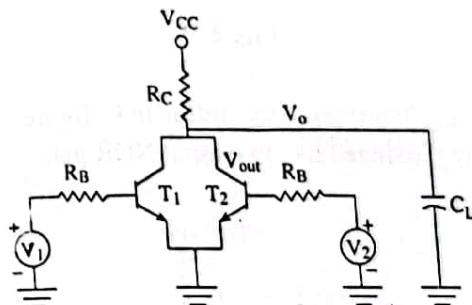


Fig 2.2: RTL NOR gate with a capacitive load

Assume initially that V_1 is high and V_2 low, so that T_1 saturated, T_2 cut-off, and V_O in the 0-state.

Now, let V_1 fall to the 0-state. T_1 now – cut off and V_O rises towards V_{CC} with a time constant $T = R_C \times C_L$. We say that V_O is pulled up to V_{CC} by the pull-up resistor R_C . Since, R_C is passive, we say that the gate shown employs passive pull-up.

2.4 FAN-OUT

The number of gates driven by a single gate is referred to as the Fan-out of that driving gate.

The Fan-out is limited by the fact that when the output of the driving gate is at logic high, the transistors of the driven gate must all be furnished with enough current to saturate them. The

current required is supplied by V_{CC} via RC of driving gate and hence get limited by ohm's law.

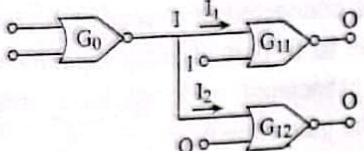
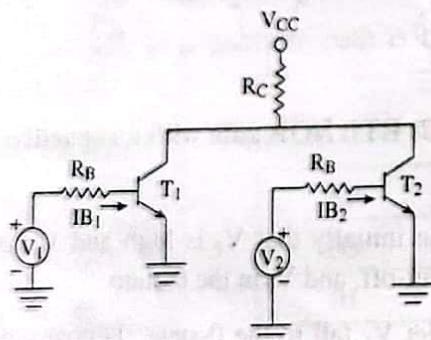


Fig. 2.3:

Let us consider the following figure where two transistors are paralleled like two input NOR gate.

Fig. 2.4: The V-I characteristics of T_1 depends on operating condition of T_2 .

Let T_2 is in cut-off mode, then there is no effect of T_2 on the operation of T_1 . But when T_2 is in saturation, when V_2 rises to bring T_1 out of cut-off, the collector Junction of T_1 is also at forward biased. Hence, T_1 is either cut-off or in saturation, but never in the active region.

In diagram, A gate Go drives one Input of "N" different gates.

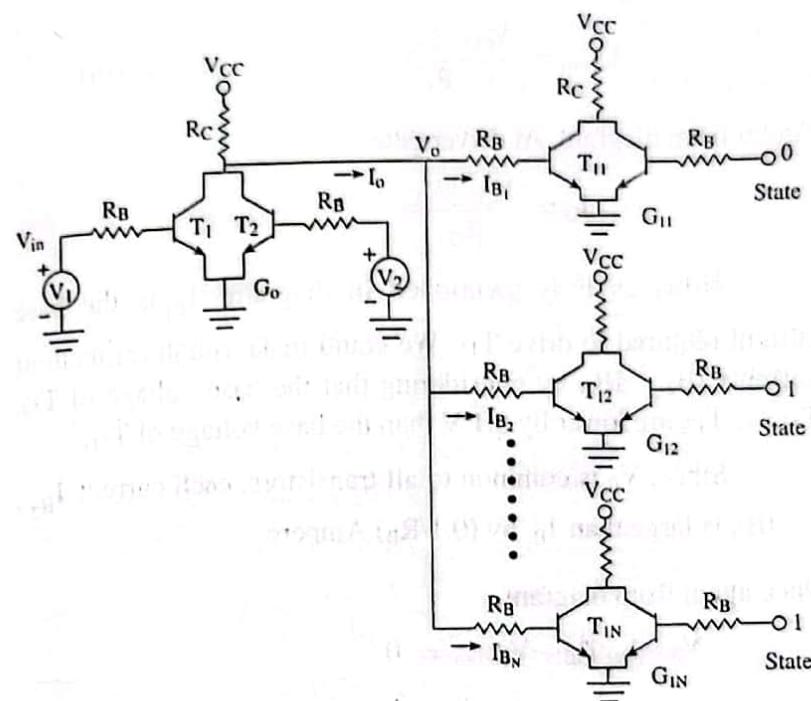


Fig. 2.5: Gate Go drives N two input gates

In every case except one, the transistor paralleling the driven transistor is in saturation. The transistors $T_{12}, T_{13}, \dots, T_{1N}$ are in saturation, if they are not cut-off. The transistor T_{11} may operate in active region. Allowing for this worst case condition, we now estimate the allowable Fan-out.

From above diagram

$$V_0 = I_{B(EOS)} R_B + V_{BE(sat)} \quad \dots\dots (i)$$

$$\text{But } I_{B(EOS)} = \frac{I_{C(sat)}}{\beta} \quad \dots\dots (ii)$$

Applying kvl at T_{11}

$$V_{CC} - I_{C(sat)} R_C - V_{CE(sat)} = 0$$

$$\text{or, } I_{C(sat)} R_C = V_{CC} - V_{CE(sat)}$$

$$\therefore I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \quad \dots\dots \text{(iii)}$$

Again from diagram, At driver gate

$$I_O = \frac{V_{CC} - V_0}{R_C}$$

Now, as it is mentioned in diagram, I_{B_1} is the base current required to drive T_{11} . We could make rough estimate of currents I_{B_2}, \dots, I_{B_N} by considering that the base voltage of $T_{12}, T_{13}, \dots, T_{1N}$ are lower by 0.1 V than the base voltage of T_{11} .

Since, V_0 is common to all transistors, each current I_{B_2}, \dots, I_{B_N} is large than I_{B_1} by $(0.1/R_B)$ Ampere.

Once again from diagram,

$$V_0 - I_{B_1} R_B - V_{BE(sat)} = 0$$

$$I_{B_1} R_B = V_0 - V_{BE(sat)}$$

$$I_{B_1} = \frac{V_0 - V_{BE(sat)}}{R_B}$$

$$\text{Again, } V_0 - I_{B_2} R_B - V_{BE(sat)} + 0.1 = 0$$

$$I_{B_2} R_B = V_0 - V_{BE(sat)} + 0.1$$

$$\therefore I_{B_2} = \frac{V_0 - V_{BE(sat)}}{R_B} + \frac{0.1}{R_B}$$

$$\therefore I_{B_2} = I_{B_1} + \frac{0.1}{R_B}$$

If N be the fan-out, then

$$I_O = I_{B_1} + I_{B_2} + I_{B_3} + \dots + I_{B_N}$$

$$I_O = I_{B_1} + (N-1) I_{B_2}$$

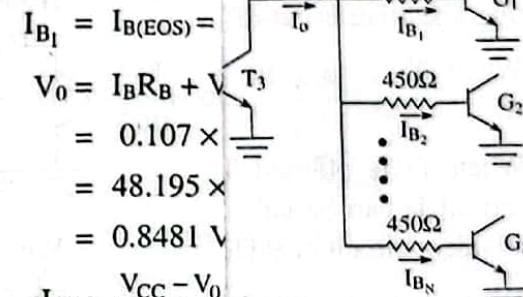
$$I_{C(sat)} = \frac{V_{CC} - V_C}{R_C} \quad \begin{cases} V_{in} = 0, T_1 = OFF, T_2 = ON, T_3 = OFF \\ V_{in} = 1, T_1 = ON, T_2 = OFF, T_3 = ON \end{cases}$$

$$= 7.5 \times 10^{-3} \text{ A}$$

$$\text{But, } I_{B(EOS)} = \frac{I_{C(sat)}}{\beta} = \frac{7.5 \times 10^{-3}}{50} = 150 \mu\text{A}$$

$$I_{B(EOS)} = 0.107 \text{ mA}$$

Also,



$$I_O = \frac{V_{CC} - V_0}{R_C}$$

$$= 6.487 \times 10^{-3} \text{ A}$$

$$= 6.487 \text{ mA}$$

Also,

$$I_{B_2} = I_{B_1} + \frac{0.1}{R_B} \quad \begin{matrix} 100\Omega \\ \beta = 50 \end{matrix}$$

$$= 0.3293 \times I_{B_1}$$

Now,

$$I_O = I_{B_1} + (N-1) I_{B_2}$$

or,

$$(N-1) I_{B_2} = I_O - I_{B_1} = \frac{V_{CC} - V_{BE(sat)}}{R_C}$$

or,

$$N-1 = \frac{I_O - I_{B_1}}{I_{B_2}}$$

\therefore

$$N = \frac{I_O - I_{B_1}}{I_{B_2}} + \text{a value less than } V_{CC}/R_C$$

$$= 19.374 + \text{a value less than } V_{CC}/R_C$$

$$N = 20 \quad \text{than that of ordinary gate, fan out.}$$

buffer driving N gates

Equivalent of
'N' driven gates

it circuit of RTL buffer

'RC' limit the output current

a value less than V_{CC}/R_C . The

active pull up to achieve a very

input current capability of the

than that of ordinary gate, fan out.

$$\therefore I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \quad \dots\dots \text{(iii)}$$

Again from diagram, At driver gate

$$I_O = \frac{V_{CC} - V_0}{R_C}$$

Now, as it is mentioned in diagram, I_{B_1} is the base current required to drive T_{11} . We could make rough estimate of currents I_{B_2}, \dots, I_{B_N} by considering that the base voltage of $T_{12}, T_{13}, \dots, T_{1N}$ are lower by 0.1 V than the base voltage of T_{11} .

Since, V_0 is common to all transistors, each current I_{B_2}, \dots, I_{B_N} is large than I_{B_1} by $(0.1/R_B)$ Ampere.

Once again from diagram,

$$V_0 - I_{B_1} R_B - V_{BE(sat)} = 0$$

$$I_{B_1} R_B = V_0 - V_{BE(sat)}$$

$$I_{B_1} = \frac{V_0 - V_{BE(sat)}}{R_B}$$

$$\text{Again, } V_0 - I_{B_2} R_B - V_{BE(sat)} + 0.1 = 0$$

$$I_{B_2} R_B = V_0 - V_{BE(sat)} + 0.1$$

$$\therefore I_{B_2} = \frac{V_0 - V_{BE(sat)} + 0.1}{R_B}$$

$$\therefore I_{B_2} = I_{B_1} + \frac{0.1}{R_B}$$

If N be the fan-out, then

$$I_O = I_{B_1} + I_{B_2} + I_{B_3} + \dots + I_{B_N}$$

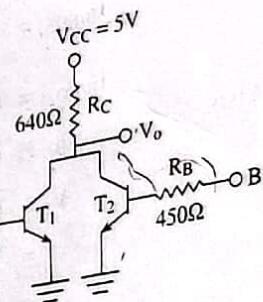
$$I_O = I_{B_1} + (N-1) I_{B_2}$$

$$N = \frac{I_0 - I_{B_1}}{I_{B_2}} + 1$$

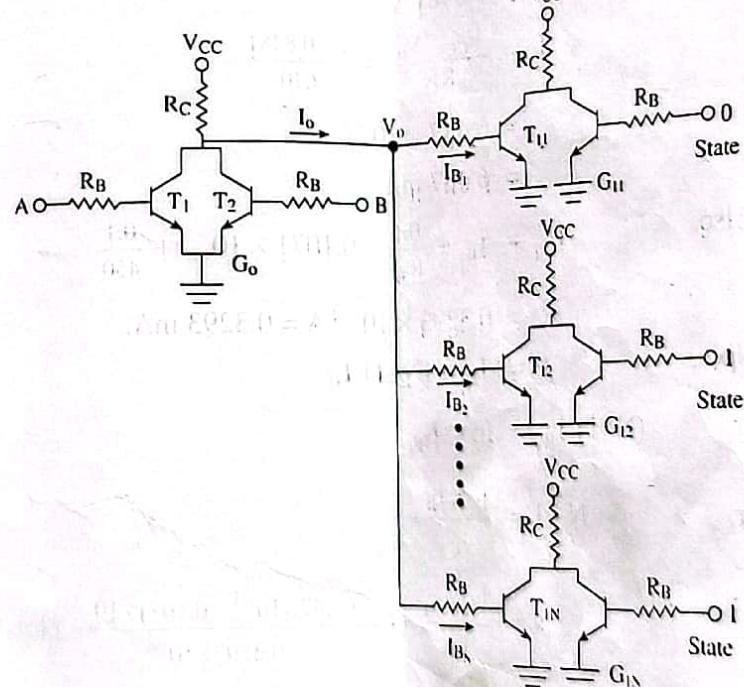
N – Fan-out represented in numbers.

Example:

For the RTL circuit shown in diagram below, Compute Fan-out value N . Assume $V_{BE(on)} = 0.7$ V, $V_{BE(sat)} = 0.8$ V, $V_{CE(sat)} = 0.2$ v and $\beta = 70$.



Solution:



Applying KVL at T_{11}

$$V_{CC} - I_{C(sat)} R_C - V_{CE(sat)} = 0$$

$$\therefore I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \quad \dots\dots \text{(iii)}$$

Again from diagram, At driver gate

$$I_0 = \frac{V_{CC} - V_0}{R_C}$$

Now, as it is mentioned in diagram, I_{B_1} is the base current required to drive T_{11} . We could make rough estimate of currents I_{B_2}, \dots, I_{B_N} by considering that the base voltage of $T_{11}, T_{12}, \dots, T_{IN}$ are lower by 0.1 V than the base voltage of T_{11} .

Since, V_0 is common to all transistors, each current I_{B_2}, \dots, I_{B_N} is large than I_{B_1} by $(0.1/R_B)$ Ampere.

Once again from diagram,

$$V_0 - I_{B_1} R_B - V_{BE(sat)} = 0$$

$$I_{B_1} R_B = V_0 - V_{BE(sat)}$$

$$I_{B_1} = \frac{V_0 - V_{BE(sat)}}{R_B}$$

$$\text{Again, } V_0 - I_{B_2} R_B - V_{BE(sat)} + 0.1 = 0$$

$$I_{B_2} R_B = V_0 - V_{BE(sat)} + 0.1$$

$$\therefore I_{B_2} = \frac{V_0 - V_{BE(sat)}}{R_B} + \frac{0.1}{R_B}$$

$$\therefore I_{B_2} = I_{B_1} + \frac{0.1}{R_B}$$

If N be the fan-out, then

$$I_0 = I_{B_1} + I_{B_2} + I_{B_3} + \dots + I_{B_N}$$

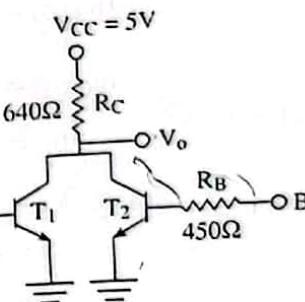
$$I_0 = I_{B_1} + (N-1) I_{B_2}$$

$$N = \frac{I_0 - I_{B_1}}{I_{B_2}} + 1$$

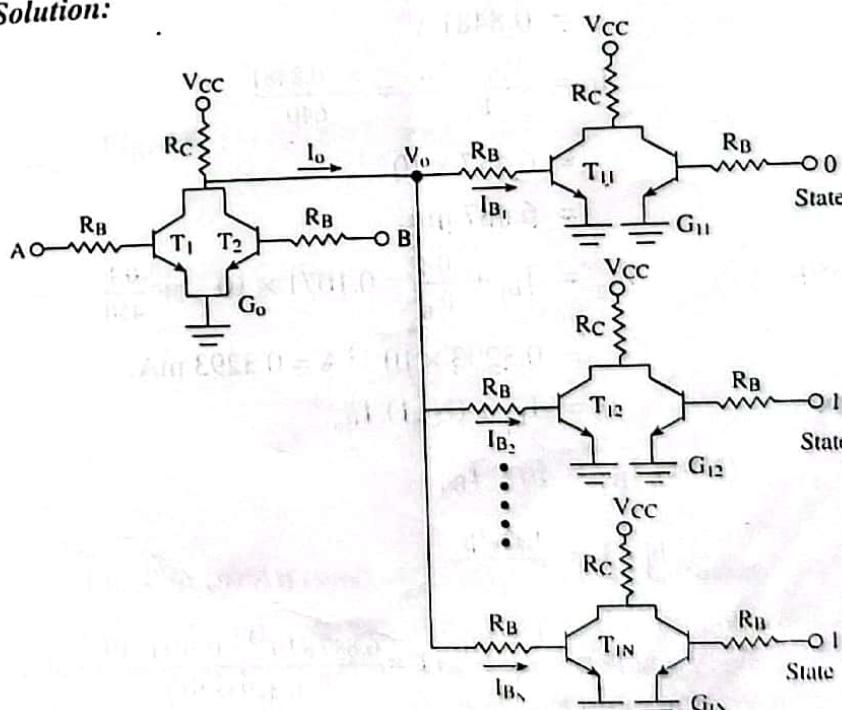
N - Fan-out represented in numbers.

Example:

For the RTL circuit shown in diagram below. Compute Fan-out value N . Assume $V_{BE(on)} = 0.7$ V, $V_{BE(sat)} = 0.8$ V, $V_{CE(sat)} = 0.2$ V and $\beta = 70$.



Solution:



Applying KVL at T_{11}

$$V_{CC} - I_{C(sat)} R_C - V_{CE(sat)} = 0$$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{5 - 0.2}{640\Omega}$$

$$= 7.5 \times 10^{-3} \text{ A} = 7.5 \text{ mA}$$

$$I_{B(EOS)} = \frac{I_{C(sat)}}{\beta} = \frac{7.5 \times 10^{-3}}{70} = 0.107 \times 10^{-3}$$

But,

$$I_{B(EOS)} = 0.107 \text{ mA}$$

Also,

$$I_{B_1} = I_{B(EOS)} = 0.107 \text{ mA.}$$

$$V_0 = I_B R_B + V_{BE(sat)}$$

$$= 0.107 \times 10^{-3} \times 450 + 0.8$$

$$= 48.195 \times 10^{-3} + 0.8$$

$$= 0.8481 \text{ V}$$

$$I_O = \frac{V_{CC} - V_0}{R_C} = \frac{5 - 0.8481}{640}$$

$$= 6.487 \times 10^{-3}$$

$$= 6.487 \text{ mA.}$$

Also,

$$I_{B_2} = I_{B_1} + \frac{0.1}{R_B} = 0.1071 \times 10^{-3} + \frac{0.1}{450}$$

$$= 0.3293 \times 10^{-3} \text{ A} = 0.3293 \text{ mA.}$$

Now,

$$I_O = I_{B_1} + (N-1) I_{B_2}$$

or,

$$(N-1) I_{B_2} = I_O - I_{B_1}$$

or,

$$N-1 = \frac{I_O - I_{B_1}}{I_{B_2}}$$

∴

$$N = \frac{I_O - I_{B_1}}{I_{B_2}} + 1 = \frac{6.847 \times 10^{-3} - 0.1071 \times 10^{-3}}{0.3293 \times 10^{-3}} + 1$$

$$= 19.374 + 1 = 20.374$$

$$N = 20$$

2.5 AN RTL BUFFER

$$V_{in} = 0, T_1 = OFF, T_2 = ON, \bar{T}_3 = OFF$$

$$V_{in} = 1, T_1 = ON, \bar{T}_2 = OFF, T_3 = ON$$

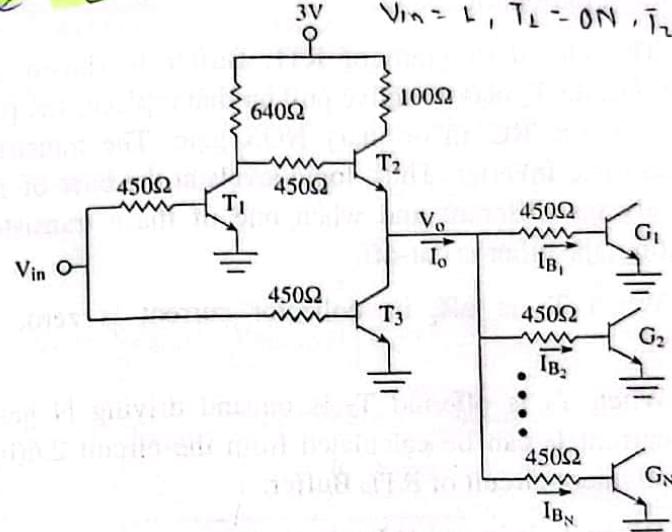


Fig. 2.6: (a) An RTL buffer driving N gates

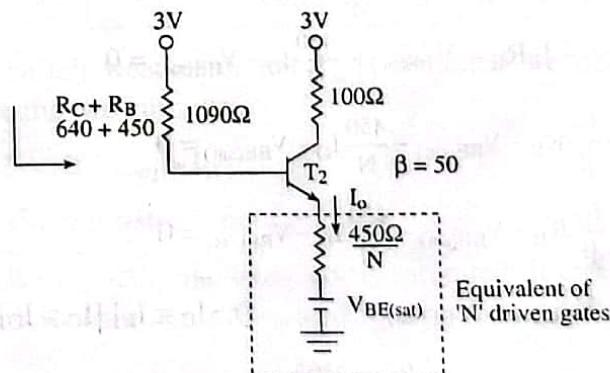


Fig. 2.6: (b) An equivalent circuit of RTL buffer

The pull up resistance 'RC' limit the output current available to drive other gates, to a value less than V_{CC}/R_C . The Buffer is an RTL gate using an active pull up to achieve a very low output impedance. Thus output current capability of the buffer is significantly greater than that of ordinary gate, resulting a significant increase in fan out.

e.g. If ordinary RTL gate has a fan out of 5, then the buffer has a fan-out of 25.

The circuit diagram of RTL Buffer is shown above. Here, transistor T_2 acts as active pull up that replaces the passive pull up resistor 'RC' in ordinary NOR gate. The transistor T_1 serves as logic Inverter. Thus, logic levels at the base of T_2 and T_3 are always different and when one of these transistors is conducting, the other is cut-off.

When T_2 is off, its collector current is zero, T_3 is saturated.

When T_3 is off and T_2 is on and driving N gate. Its output current I_o can be calculated from the circuit 2.6(b). i.e. from Equivalent circuit of RTL Buffer.

Case I: When T_2 is in active Region:

Applying kvl at input side of circuit,

$$V_{CC} - I_B R_B - V_{BE(on)} - \frac{450}{N} I_O - V_{BE(sat)} = 0$$

$$\text{or, } 3 - \frac{I_C}{\beta} R_B - V_{BE(on)} - \frac{450}{N} I_O - V_{BE(sat)} = 0$$

$$\text{or, } 3 - \frac{I_C}{\beta} R_B - V_{BE(on)} - \frac{450}{N} I_O - V_{BE(sat)} = 0$$

$$\text{or, } 3 - V_{BE(on)} - V_{BE(sat)} \quad [\because I_C \equiv I_E] \quad [I_C \equiv I_O]$$

$$= \left[\frac{R_B}{\beta} + \frac{450}{N} \right] I_O$$

$$\therefore I_O = \frac{3 - V_{BE(on)} - V_{BE(sat)}}{\frac{1090}{\beta} + \frac{450}{N}}$$

$$\boxed{I_O = \frac{3 - V_{BE(on)} - V_{BE(sat)}}{\frac{1090}{\beta} + \frac{450}{N}}} \quad \dots\dots (i)$$

Case II: When T_2 is saturated.

Applying kvl at output of ckt,

$$V_{CC} - I_{C(sat)} R_C - V_{CE(sat)} - \frac{450}{N} I_O(sat) - V_{BE(sat)} = 0$$

$$V_{CC} - I_{O(sat)} R_C - V_{CE(sat)} - \frac{450}{N} I_O(sat) - V_{BE(sat)} = 0$$

$$[\because I_C \equiv I_E], \quad [\because I_C \equiv I_O]$$

$$\text{or, } V_{CC} - V_{CE(sat)} - V_{BE(sat)} = \left[R_C + \frac{450}{N} \right] I_O(sat)$$

$$\therefore I_O(sat) = \frac{V_{CC} - V_{CE(sat)} - V_{BE(sat)}}{R_C + \frac{450}{N}}$$

$$\therefore I_O(sat) = \boxed{\frac{3 - V_{CE(sat)} - V_{BE(sat)}}{100 + \frac{450}{N}}} \quad \dots\dots (ii)$$

To tell weather or not T_2 is saturated we need only to compare the two currents.

For, If $I_O(sat) > I_O$

The transistor is not saturated.

If $I_O(sat) < I_O$, the transistor is saturated. It can be verified that the transistor is not saturated for $N = 1$ and is saturated for $N \geq 2$.

The buffer is ordinarily employed to drive a large number of gates. We therefore assume that $N \geq 2$ and that the transistor T_2 is saturated.

Also, since $I_O(sat)$ is responsible to drive all N load gates, the current supplied to each gate is

$$I_{B_1} = I_{B_2} = I_{B_N} = I_B,$$

Thus,

$$I_B = \frac{I_{O(\text{sat})}}{N}$$

..... (iii)

2.6 AN RTL EX-OR GATE

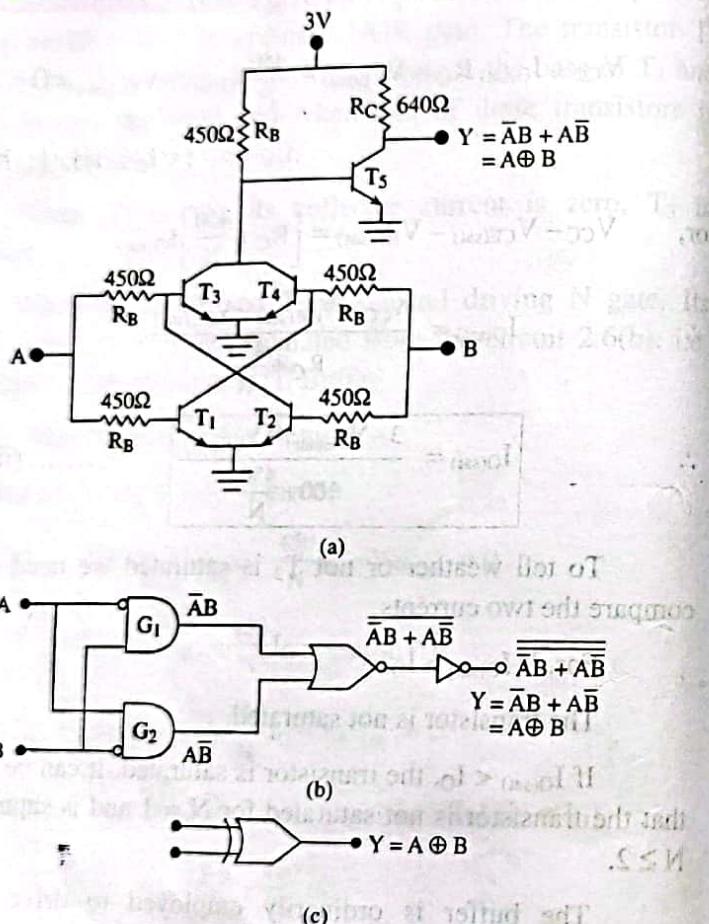


Fig. 2.7: RTL as exclusive OR gate

An RTL circuit capable to perform EX-OR operation is shown in diagram 2.7(a).

In above diagram, transistors T_1 & T_2 acts as inverter, Transistors T_3 and T_4 acts as RTL NOR gate and Transistor T_5 acts as NOT gate.

Hence, Input to T_3 is $A\bar{B}$. Similarly the input to T_4 is $\bar{A}B$. These two operations are represented by G_1 & G_2 respectively in diagram 2.7(b).

Referring to the diagram 2.7(a), Transistor T_3 , T_4 perform NOR operation. Transistor T_5 inverts the NOR output, producing an OR gate.

Thus, output of T_5 is $Y = \bar{A}\bar{B} + A\bar{B}$ as required.

$$\text{i.e. } Y = A \oplus B$$

2.7 ADVANTAGE & DISADVANTAGE OF THE RTL CIRCUIT

Advantages:

In summary, The RTL circuit has advantages of

- Being simple
- Using low power

Disadvantages:

- A small logic swing
- A low Noise Margin

2.8 MANUFACTURER'S SPECIFICATION

There are four basic types of RTL gates.

1. Medium power gate (MRTL), where $R_C = 640 \Omega$, $R_B = 450 \Omega$.
2. The low power gate (LRTL), Where $R_C = 3.6 \text{ K} \Omega$, $R_B = 1.5 \text{ K} \Omega$.
3. The buffer, Available in either the medium or low power class.
4. The EX- OR gate.

$$V_{OH}/V_{OL} = 1.2 \text{ V}/0.2 \text{ V}$$

$$V_{IH}/V_{IL} = 0.8 \text{ V}/0.7 \text{ V}$$

$$NMH/NML = 0.4 \text{ V}/0.5 \text{ V}$$

$$V_{LS} = 1 \text{ V}$$

$$\text{Fan-out} = 5$$

$$\text{Power dissipation} = 16 \text{ mW}$$

$$\text{Propagation delay} = 12 \text{ ns}$$

2.9 CHARGE COMPENSATION TO REDUCE PROPAGATION DELAY TIME

As we know, propagation delays result from the necessity to establish and remove base charges as transistors are turned ON and OFF. One way by which it is obtained is to provide for the flow of impulsive current into and out of the base. In RTL, such impulsive current may be provided by bridging capacitors across the base resistors R_B as shown in diagram 2.8(a).

The use of capacitors to draw charge abruptly out of semiconductor is called charge compensation.

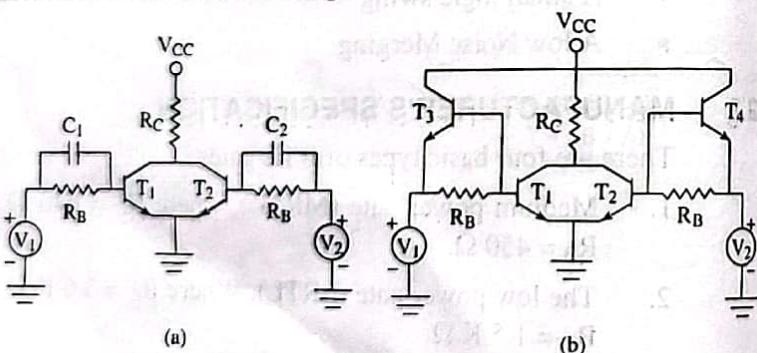


Fig. 2.8: (a) Capacitors C_1 and C_2 shunted across base resistor R_B , (b) Transistors T_3 and T_4 shunted across R_B

In IC's the conventional capacitors occupy a large amount of area on the IC chip. The Junction capacitance of a transistor is sometimes employed when capacitors are required.

In diagram 2.8(b), Such Junction capacitors have been bridged across the base resistors R_B via addition of transistor T_3 & T_4 .

SUMMARY

This chapter provides the study of various RTL gates and corresponding development for RTL gate and some important characteristics with following ideas.

- RTL NAND and NOR gates are discussed with basic configuration and operation.
- RTL NOR gate Fan-out are discussed and expression for N is derived.
- RTL as a buffer are discussed with its importance and significances.
- RTL as a Ex-OR gate are discussed
- Advantages and Disadvantages for RTL are discussed
- Charge compensation to Reduce propagation delay time are discussed with various configuration.

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PROBLEMS

1. For "Resistor Transistor Logic". Discuss the terms mentioned below:
 - i) RTL as NAND and NOR gate
 - ii) Passive pull up
 - iii) Fan-out
2. Draw RTL Buffer circuit. Discuss its operation with Buffer significance and derive an expression of current for T_2 both states active and saturated.
3. For "Resistor Transistor Logic". Discuss the terms mentioned below:
 - i) RTL as Ex-OR gate
 - ii) Advantages and disadvantages of RTL
 - iii) Charge compensation to reduce propagation delay.
4. For the RTL circuit shown in diagram 4 below

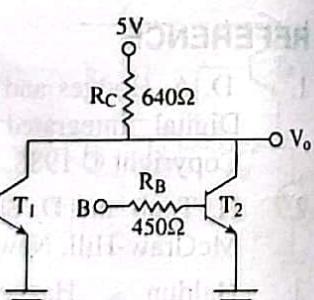
Assume $\beta = 30$,

$V_{BE(on)} = 0.7 \text{ V}$,

$V_{BE(sat)} = 0.8 \text{ V}$,

$V_{CE(sat)} = 0.1 \text{ V}$

Calculate the logic swing and noise margin for fan-out = 5.



• • •

Diode Transistor Logic (DTL)

3
Unit

3.1 INTRODUCTION

An I.C. development a short at time later consisted of a diode AND circuit followed by a bipolar transistor inverter. This was called Diode Transistor Logic (DTL) and it is IC versions of logic circuits made with discrete diodes, transistors, and resistors that had long been popular with digital circuit designers. The advantages of the integrated form was that the batch processing of the integrated circuits resulted in a product of very small size and high reliability, eventually at a very low price. The IC-DTL yields grater fan-out and improved noise margins.

3.2 DIODE TRANSISTOR LOGIC (DTL)

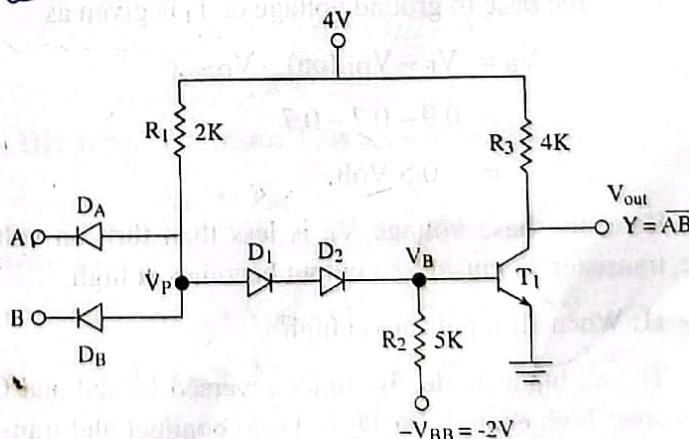


Fig. 3.1: A 2-input DTL NAND gate

A schematic of the type of Diode Transistor Logic (DTL) that appeared on the commercial market in 1962 is shown in diagram 3.1(a). The circuit is basically a 2-Input diode AND circuit followed by a transistor Inverter. Hence, this is a 2-Input NAND-gate. Where $Y = \overline{AB}$

For two or more than 2-Inputs, the circuit performs NAND operation only.

Operation:

Case – I: When at least one Input is at low.

The input diode becomes forward biased and corresponding diode conducts such that

From diagram,

$$\mathbf{V}_P - \mathbf{V}_{D(\text{eff})} - \mathbf{V}_{in} = 0$$

$$\begin{aligned}V_P &= V_{D(on)} + V_{in} \\&= 0.7 + 0.2 \\&= 0.9 \text{ V}\end{aligned}$$

Now, the base to ground voltage of T_1 is given as

$$V_B = V_P - V_{D1}(\text{on}) - V_{D2(\text{on})}$$

$$= 0.9 - 0.7 - 0.7$$

$$\equiv -0.5 \text{ Volt.}$$

Here, the base voltage V_B is less than turn on voltage. Hence, transistor T_1 cut-off, so output becomes at high.

Case – II: When all inputs are at high

The all input diodes becomes reversed biased and OFF. VP becomes high enough for D_1 & D_2 to conduct and transistor T_1 to go into saturation. Hence, output becomes at low.

When VP decreases (Due to return of inputs to logic low), Diode D₁ & D₂ becomes OFF. The resistance R₂ provides a discharge path for the charge stored in the transistor. V_{BB} supply is used to Inverse the rate of discharge.

3.3 NOISE MARGIN

To compute Noise margin of DTL gate, one have to apply four conditions at transistor T_1 .

Case I: When T_1 is at cut-off mode.

$$V_0 = V_{OH} = V_{CC} \quad \dots \dots \text{(i)}$$

i.e. $V_{OH} = V_{CC} = 4 \text{ V}$ (ii)

Case II: When transistor T_1 is at edge of conduction,

$$V_{in} = V_{IL}$$

Applying kvl,

$$-V_{in} = V_{D(on)} + V_{D(on)} + V_{D(on)} + V_{BE(on)} = 0$$

$$V_{in} = V_{D(on)} + V_{D(on)} + V_{BE(on)} - V_{D(on)}$$

$$\begin{aligned} V_{IL} &= V_{D(on)} + V_{D(on)} + V_{BE(on)} - V_{D(on)} \\ &= 0.7 + 0.7 + 0.7 - 0.7 \\ &= 1.4 \text{ V} \end{aligned}$$

Case III: When Transistor T_1 is at edge of saturation,

$$V_{in} = V_{IH}$$

Applying kvl

$$-V_{in} = V_{D(on)} + V_{D(on)} + V_{D(on)} + V_{BE(sat)} = 0$$

$$V_{\text{t}} = V_{D(\text{on})} + V_{D(\text{on})} + V_{BE(\text{sat})} - V_{D(\text{on})}$$

$$\therefore V_{\text{III}} = 0.7 + 0.7 + 0.8 - 0.7 \\ = 1.5 \text{ V} \quad \dots\dots \text{ (iv)}$$

Case IV:

When Transistor is at saturated mode.

$$V_0 = V_{OL} = V_{CE(sat)}$$

$$\therefore V_{OL} = V_{CE(sat)} = 0.2V \quad \dots \dots \dots (v)$$

Now, Noise margin of DTL gate can be computed as accordingly

$$\begin{aligned} NMH &= V_{OH} - V_{IH} \\ &= 4 - 1.5 = 2.5V \end{aligned}$$

$$\begin{aligned} NML &= V_{IL} - V_{OL} = 1.4 - 0.2 \\ &= 1.2V \end{aligned}$$

$$\begin{aligned} VTW &= V_{IH} - V_{IL} = 1.5 - 1.4 \\ &= 0.1V \end{aligned}$$

$$\begin{aligned} VLS &= V_{OH} - V_{OL} = 4 - 0.2 \\ &= 3.8V \end{aligned}$$

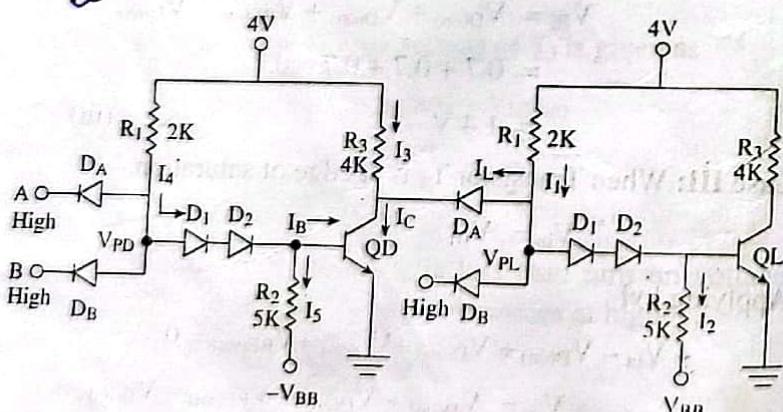
3.4 FAN-OUT

Fig. 3.2: A DTL gate with fan-out

Diagram 3.2 shows, the DTL driving N load gates.

Here, All inputs of driver circuit is at high. Thus, transistor QD turns into saturated mode.

From diagram,

$$I_{C(sat)} = I_3 + I_L \quad \dots \dots \dots (i)$$

For N-load gates

$$I_{C(sat)} = I_3 + NI_L \quad \dots \dots \dots (ii)$$

$$\text{But } I_L = I_1 - I_2 \quad \dots \dots \dots (iii)$$

$$I_{C(sat)} = I_3 + N(I_1 - I_2) \quad \dots \dots \dots (iv)$$

$$\therefore N = \frac{I_{C(sat)} - I_3}{I_1 - I_2} \quad \dots \dots \dots (v)$$

To compute fan-out value N, one should have to calculate each value of equation (v) step by step.

To compute I_3 :

Applying kvl at QD

$$V_{CC} - I_3 R_3 - V_{CE(sat)} = 0$$

$$I_3 R_3 = V_{CC} - V_{CE(sat)}$$

$$\therefore I_3 = \frac{V_{CC} - V_{CE(sat)}}{R_3} \quad \dots \dots \dots (vi)$$

To compute I_1 applying kvl

$$V_{CC} - I_1 R_1 - V_{PL} = 0$$

$$\therefore I_1 = \frac{V_{CC} - V_{PL}}{R_1} \quad \dots \dots \dots (vii)$$

$$\text{But } V_{PL} = V_{D(on)} + V_{CE(sat)} \quad \dots \dots \dots (viii)$$

Similarly, to compute I_2 :

Applying kvl,

$$V_{PL} - V_{D(on)} - V_{D(on)} - I_2 R_2 - (-V_{BB}) = 0$$

$$\therefore I_2 R_2 = V_{PL} - 2V_{D(on)} + V_{BB}$$

$$\therefore I_2 = \frac{V_{PL} - 2V_{D(on)} + V_{BB}}{R_2} \quad \dots \dots \text{(ix)}$$

To compute $I_{C(sat)}$:

$$\text{We know } I_{C(sat)} = \beta I_B$$

But here,

$$I_B = I_4 - I_5$$

$$I_4 = \frac{V_{CC} - V_{PD}}{R_1}$$

$$\text{But } V_{PD} = V_{D(on)} + V_{D(on)} + V_{BE(sat)} \\ = 2V_{D(on)} + V_{BE(sat)} \quad \dots \dots \text{(x)}$$

Similarly, to compute I_5 :

Applying kvl,

$$V_{BE(sat)} - R_2 I_5 - (-V_{BB}) = 0$$

$$\therefore I_5 = \frac{V_{BE(sat)} + V_{BB}}{R_2} \quad \dots \dots \text{(xi)}$$

Thus by knowing all these value, the fan-out of DTL gate is computed as

$$N = \frac{I_{C(sat)} - I_3}{I_1 - I_2}$$

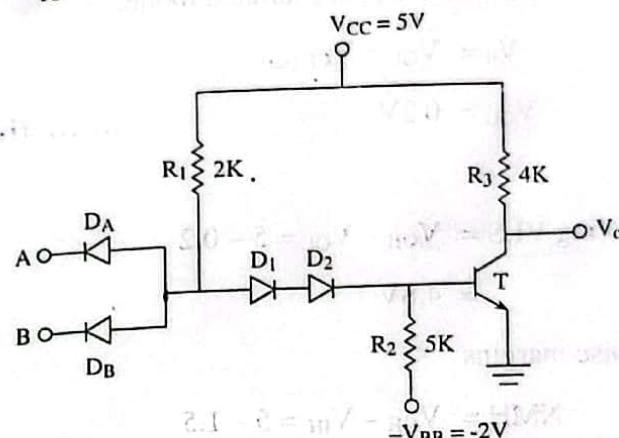
$\beta I_B \geq I_C$ for QD in saturation.

Example:

For the DTL circuit shown in diagram below, Assume that $V_{D(on)} = V_{BE(on)} = 0.7 \text{ V}$, $V_{BE(sat)} = 0.8 \text{ V}$, $V_{CE(sat)} = 0.2 \text{ V}$ and $\beta = 30$ compute:

- The logic swing and Noise Margins

- Fan-out value, when driver circuit output becomes at low.



Solution:

- To compute logic swing and Noise Margins. Let us apply four conditions at transistor T.

Case I: When transistor T is at cut-mode.

$$\boxed{\begin{aligned} V_0 &= V_{OH} = V_{CC} \\ V_{OH} &= 5 \text{ V} \end{aligned}} \quad \dots \dots \text{(i)}$$

Case II: When transistor T is at edge of conduction.

$$\boxed{\begin{aligned} V_{in} &= V_{IL} \\ V_{IL} &= V_{D(on)} + V_{D(on)} + V_{BE(on)} - V_{D(on)} \\ &= 0.7 \text{ V} + 0.7 \text{ V} + 0.7 \text{ V} - 0.7 \text{ V} \\ &= 1.4 \text{ V} \end{aligned}} \quad \dots \dots \text{(ii)}$$

Case III: When transistor T is at edge of saturation.

$$\boxed{\begin{aligned} V_{in} &= V_{IH} \\ V_{IH} &= V_{D(on)} + V_{D(on)} + V_{BE(sat)} - V_{D(on)} \\ &= 0.7 \text{ V} + 0.7 \text{ V} + 0.8 \text{ V} - 0.7 \text{ V} \end{aligned}}$$

$$= 1.5V \quad \dots \dots \text{ (iii)}$$

Case IV: When transistor T is at saturated mode.

$$V_0 = V_{OL} = V_{CE(sat)}$$

$$V_{OL} = 0.2V \quad \dots \dots \text{ (iv)}$$

Thus,

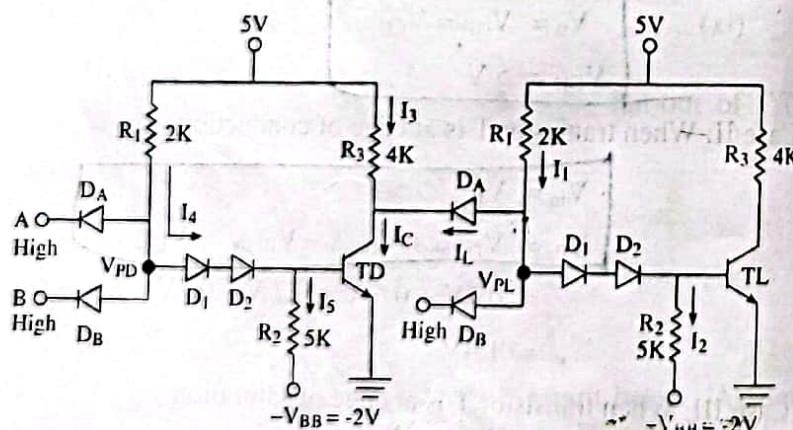
$$\begin{aligned}\text{Logic Swing } VLS &= V_{OH} - V_{OL} = 5 - 0.2 \\ &= 4.8V\end{aligned}$$

Noise margins

$$\begin{aligned}NMH &= V_{OH} - V_{IH} = 5 - 1.5 \\ &= 3.5V\end{aligned}$$

$$\begin{aligned}NML &= V_{IL} - V_{OL} = 1.4V - 0.2 \\ &= 1.2V\end{aligned}$$

ii) To compute fan-out, Let us connect load gate to driver gate



Here, from diagram,

$$I_{C(sat)} = I_3 + N I_L$$

$$I_{C(sat)} - I_3 = N (I_1 - I_2)$$

$$N = \frac{I_{C(sat)} - I_3}{I_1 - I_2} \quad \dots \dots \text{ (i)}$$

$$I_3 = \frac{V_{CC} - V_{CE(sat)}}{R_3}$$

$$= \frac{5 - 0.2}{4k}$$

$$= 1.2 \times 10^{-3} A$$

$$I_3 = 1.2 \text{ mA.}$$

$$V_{PL} = V_{D(on)} + V_{CE(sat)}$$

$$= 0.7 + 0.2$$

$$= 0.9 \text{ V.}$$

$$I_1 = \frac{V_{CC} - V_{PL}}{R_1}$$

$$= \frac{5 - 0.9}{2k}$$

$$= 2.05 \times 10^{-3} A$$

$$= 2.05 \text{ mA}$$

$$I_2 = \frac{V_{PL} - 2V_{D(on)} + V_{BB}}{R_2}$$

$$= \frac{0.9 - 2 \times 0.7 + 2}{5k}$$

$$= \frac{2.9 - 1.4}{5k}$$

$$= 0.3 \times 10^{-3} A$$

$$= 0.3 \text{ mA}$$

Again, from diagram

$$I_B = I_4 - I_5$$

$$\begin{aligned} V_{PD} &= 2V_{D(on)} + V_{BE(sat)} \\ &= 2 \times 0.7 + 0.8 \\ &= 1.4 + 0.8 \\ &= 2.2V \end{aligned}$$

$$I_4 = \frac{V_{CC} - V_{PD}}{R_1}$$

$$= \frac{5 - 2.2}{2k}$$

$$= 1.4 \times 10^{-3} A$$

$$= 1.4 mA$$

$$I_5 = \frac{V_{BE(sat)} + V_{BB}}{R_2}$$

$$= \frac{0.8 + 2}{5k}$$

$$= 0.56 \times 10^{-3} A$$

$$= 0.56 mA$$

Now,

$$I_B = I_4 - I_5$$

$$= 1.4 mA - 0.56 mA$$

$$= 0.84 mA$$

$$I_{C(sat)} = \beta I_B$$

$$= 30 \times 0.84 mA$$

$$= 25.2 mA$$

Thus,

$$N = \frac{I_{C(sat)} - I_3}{I_1 - I_2}$$

$$= \frac{25.2 mA - 1.2 mA}{2.05 mA - 0.3 mA}$$

$$= \frac{24 mA}{1.75 mA}$$

$$= 13.7142$$

$$N = 14$$

3.5 MODIFIED DTL GATES

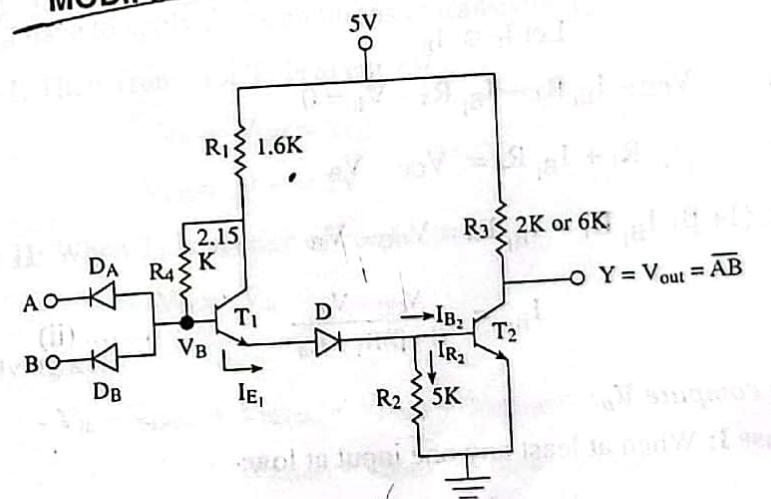


Fig. 3.3: Modified DTL gate

The schematic diagram of modified DTL gate is shown above. In comparing to DTL gate, it is very much similar, but one of the series diode has been replaced by a transistor T_1 that when 'ON' is self biased to operate in the forward active mode. Also R_4 is connected between base and collector of T_1 . When T_1 operates in its active region and provides current gain between its base and emitter.

With T_2 conducting, T_1 acts as an emitter follower, supplying the current to base of T_2 . Hence, there is a current gain $(1 + \beta)$ from base of T_1 to the base of T_2 .

From diagram

$$I_{E_1} = (1 + \beta) I_{B_1} \quad \dots \dots \dots \text{(i)}$$

To compute I_B :

Applying kvl at T_1

$$V_{CC} - I_C R_1 - I_{B_1} R_4 - V_B = 0$$

$$\text{Let } I_C \equiv I_E$$

$$\text{or, } V_{CC} - I_{E_1} R_1 - I_{B_1} R_4 - V_B = 0$$

$$\text{or, } I_{E_1} R_1 + I_{B_1} R_4 = V_{CC} - V_B$$

$$\text{or, } (1 + \beta) I_{B_1} R_1 + I_{B_1} R_4 = V_{CC} - V_B$$

$$\therefore I_{B_1} = \frac{V_{CC} - V_B}{(1 + \beta) R_1 + R_4} \quad \dots \dots \text{(ii)}$$

To compute V_B :

Case I: When at least any one input at low:

$$\begin{aligned} V_B &= V_{D(\text{on})} + V_{in} = 0.7 + 0.2 \\ &= 0.9 \text{ V} \end{aligned} \quad \dots \dots \text{(iii)}$$

Case II: When all inputs at high:

$$\text{Then, } V_B - V_{BE(\text{on})} - V_{D(\text{on})} - V_{BE(\text{sat})} = 0$$

$$\begin{aligned} \therefore V_B &= V_{BE(\text{on})} + V_{D(\text{on})} + V_{BE(\text{sat})} \\ &= 0.7 + 0.7 + 0.8 \\ &= 2.2 \text{ V} \end{aligned} \quad \dots \dots \text{(iv)}$$

Again from diagram,

$$I_{B_2} = I_{E_1} - I_{R_2}$$

$$\text{Here, } I_{R_2} = \frac{V_{BE_2(\text{sat})}}{R_2} \quad \dots \dots \text{(v)}$$

Thus, this circuit could able to increase the base current of T_2 by a factor $(1 + \beta)$ and hence corresponding increase in fan out is obvious.

3.6 NOISE MARGIN

To compute noise margin of modified DTL gate, one should have to apply four conditions at transistor T_2

Case I: Then Transistor T_2 is at cut-off

$$V_0 = V_{OH} = V_{CC}$$

$$\therefore V_{OH} = V_{CC} = 5V \quad \dots \dots \text{(i)}$$

Case II: When T_2 is at edge of conduction

$$V_{in} = V_{IL}$$

Applying kvl

$$-V_{in} - V_{D(\text{on})} + V_{BE(\text{on})} + V_{D(\text{on})} + V_{BE(\text{on})} = 0$$

$$\therefore V_{in} = V_{BE(\text{on})} + V_{D(\text{on})} + V_{BE(\text{on})} - V_{D(\text{on})}$$

$$V_{IL} = 0.7 + 0.7 + 0.7 - 0.7$$

$$= 1.4 \text{ V} \quad \dots \dots \text{(ii)}$$

Case III: When T_2 is at edge of saturation

$$V_{in} = V_{IH}$$

Again, Applying kvl,

$$-V_{in} - V_{D(\text{on})} + V_{BE(\text{on})} + V_{D(\text{on})} + V_{BE(\text{sat})} = 0$$

$$\therefore V_{in} = V_{BE(\text{on})} + V_{D(\text{on})} + V_{BE(\text{sat})} - V_{D(\text{on})}$$

$$V_{IH} = 0.7 + 0.7 + 0.8 - 0.7$$

$$= 1.5 \text{ V} \quad \dots \dots \text{ (iii)}$$

Case IV: When T_2 is at saturated mode.

$$V_0 = V_{OL} = V_{CE(\text{sat})}$$

$$\therefore V_{OL} = V_{EC(\text{sat})} = 0.2 \text{ V} \quad \dots \dots \text{ (iv)}$$

The value of Noise margin of modified DTL gate is computed as accordingly

$$NMH = V_{OH} - V_{IH}$$

$$= 5 - 1.5$$

$$= 3.5 \text{ V}$$

$$NML = V_{IL} - V_{OL}$$

$$= 1.4 - 0.2$$

$$= 1.2 \text{ V}$$

$$VTW = V_{IH} - V_{IL}$$

$$= 1.5 - 1.4$$

$$= 0.1 \text{ V}$$

$$VLS = V_{OH} - V_{OL}$$

$$= 5 - 0.2$$

$$= 4.8 \text{ V}$$

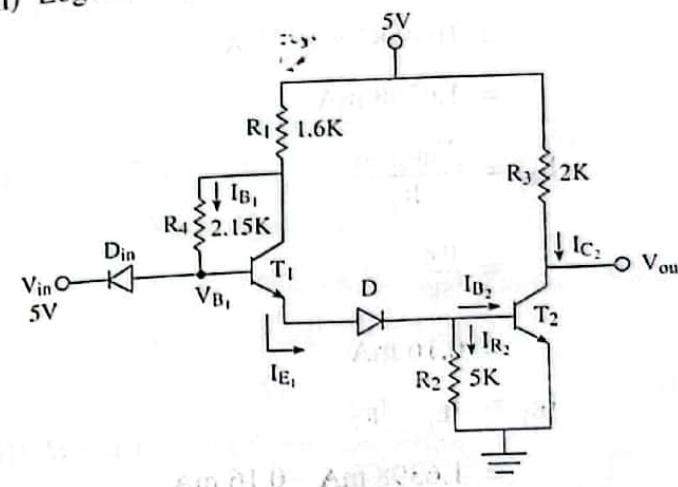
Example:

For the Modified DTL inverter circuit shown in diagram below, assume $V_{D(\text{on})} = V_{BE(\text{on})} = 0.7\text{V}$, $V_{BE(\text{sat})} = 0.8\text{V}$, $V_{CE(\text{sat})} = 0.2\text{V}$ and $\beta = 19$. For input connected to 5 volts, T_1 always operates in forward active mode wherein T_2 remains in saturation. Compute

- Voltage V_{B1} and currents I_{B1} , I_{E1} , I_{B2} , I_{R2} and I_{C2} .

ii) The Resistance value R_3 .

iii) Logic swing and Noise Margins.



Solution:

- Here, For $V_{in} = 5\text{V}$, the transistor T_1 operates in forward active mode and T_2 turns into saturated mode.

$$\text{Thus, } V_{B1} = V_{BE1(\text{on})} + V_{D(\text{on})} + V_{BE2(\text{sat})}$$

$$= 0.7 + 0.7 + 0.8$$

$$= 2.2 \text{ V}$$

$$I_{B1} = \frac{V_{CC} - V_{B1}}{(1+\beta) R_1 + R_4}$$

$$= \frac{5 - 2.2}{(1+19)1.6k + 2.15k}$$

$$= \frac{2.8}{32k + 2.15k}$$

$$= 8.1991 \times 10^{-5} \text{ A}$$

$$= 81.991 \mu\text{A}$$



$$\begin{aligned} I_{E_1} &= (1 + \beta) I_{B_1} \\ &= (1 + 19) 81.991 \times 10^{-6} \text{ A} \\ &= 1639.82 \times 10^{-6} \text{ A} \\ &= 1.6398 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_{R_2} &= \frac{V_{BE_2(\text{sat})}}{R_2} \\ &= \frac{0.8}{5k} \\ &= 0.16 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_{B_2} &= I_{E_1} - I_{R_2} \\ &= 1.6398 \text{ mA} - 0.16 \text{ mA} \\ &= 1.4798 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_{C_2} &= \beta I_{B_2} \\ &= 19 \times 1.4798 \text{ mA} \\ &= 28.1162 \text{ mA} \end{aligned}$$

(ii) Now, Applying KVL at o/p side of T_2 .

$$V_{CC} - I_{C_2(\text{sat})} R_3 - V_{CE(\text{sat})} = 0.$$

$$\begin{aligned} \therefore R_3 &= \frac{V_{CC} - V_{CE(\text{sat})}}{I_{C_2(\text{sat})}} \\ &= \frac{5 - 0.2}{28.1162 \times 10^{-3}} \\ &= 170.720 \Omega \\ &= 0.1707 \text{ k}\Omega. \end{aligned}$$

(iii) To compute logic swing and noise margin. One should have to apply four conditions at T_2 .

Case I: When T_2 is at cut-off mode.

$$\begin{aligned} V_0 &= V_{OH} = V_{CC} \\ V_{OH} &= 5 \text{ V} \end{aligned} \quad \dots \dots \dots \text{(i)}$$

Case II: When T_2 is at edge of conduction,

$$\begin{aligned} V_{in} &= V_{IL} \\ V_{in} &= V_{BE(on)} + V_{D(on)} + V_{BE(on)} - V_{D(on)} \\ V_{IL} &= 0.7 + 0.7 + 0.7 - 0.7 \\ &= 1.4 \text{ V} \end{aligned} \quad \dots \dots \dots \text{(ii)}$$

Case III: When T_2 is at edge of saturation

$$\begin{aligned} V_{in} &= V_{IH} \\ V_{IH} &= V_{BE(on)} + V_{D(on)} + V_{BE(sat)} - V_{D(on)} \\ &= 0.7 + 0.7 + 0.8 - 0.7 \\ &= 1.5 \text{ V} \end{aligned} \quad \dots \dots \dots \text{(iii)}$$

Case IV: When T_2 is at saturated mode,

$$\begin{aligned} V_0 &= V_{OL} = V_{CE(sat)} \\ V_{OL} &= 0.2 \text{ V} \end{aligned} \quad \dots \dots \dots \text{(iv)}$$

$$\begin{aligned} \text{Thus, logic swing, } V_{LS} &= V_{OH} - V_{OL} = 5 - 0.2 \\ &= 4.8 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{Noise margin NMH} &= V_{OH} - V_{IH} = 5 - 1.5 \\ &= 3.5 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{NML} &= V_{IL} - V_{OL} = 1.4 - 0.2 \\ &= 1.2 \text{ V} \end{aligned}$$

3.7 INPUT-OUTPUT CHARACTERISTICS

The input-output characteristics of the DTL gate at different temp. 125°C , 25°C & -55°C obtain the form of shape as shown in diagram.

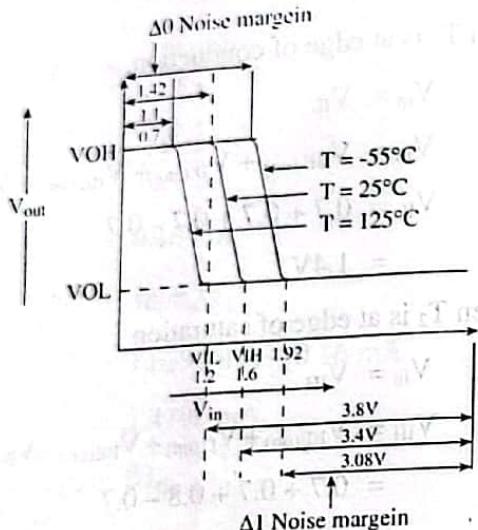


Fig. 3.4: I/O characteristics

The value of noise margins Δ_0 and Δ_1 also indicate in diagram.

It is interesting to compare the I/O characteristics of DTL gate with I/O of RTL gate, with regard to the Δ_0 and Δ_1 noise margins.

Here, one could observe that at 25°C the Δ_0 noise margin for DTL is approximately 1.2 while for RTL, it is 0.45 V, similarly the Δ_1 noise margin for DTL is 3.4V while for RTL it is 0.24V. This significant increase in noise margin is one of major advantage of DTL over RTL.

3.8 MANUFACTURES SPECIFICATIONS

Typical manufactures specifications of DTL gate are shown in table and are based on discussed in this section.

$$V_{\text{OH}}/V_{\text{OL}} = 4.8 \text{ V}/0.2 \text{ V}$$

$$V_{\text{IH}}/V_{\text{IL}} = 1.5 \text{ V}/1.2 \text{ V}$$

$$\text{NMH/NML} = 3.3 \text{ V}/1.0 \text{ V}$$

$$V_{\text{LS}} = 4.6 \text{ V}$$

$$\text{Fan-out} = 8$$

$$\text{Power dissipation per gate} = 10 \text{ mw}$$

$$\text{Propagation Delay} = 30 \text{ n sec.}$$

SUMMARY

This chapter provides brief discussion for about DTL and IC-DTL. DTL study also includes corresponding Modification and development with some typical parameters.

- DTL NAND gate circuit are discussed
- Noise Margins, logic swings for DTL NAND gates are computed analytically.
- DTL NAND gate Fan-out are discussed and expression for N is derived.
- Modified DTL (IC-DTL) gate circuit are discussed and corresponding derivations are derived.
- For IC-DTL, some important parameters discussed are
 - Noise margin
 - I/O characteristics
 - Manufacturer's specification.

- Typical important numerical are solved for both DTL and IC-DTL.

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PROBLEMS

- Draw DTL circuit and for DTL gate, discuss the terms mentioned below:
 - DTL NAND gate
 - Noise margins
- Draw DTL circuit and obtain an expression of fan-out for N load gates.
- Draw IC-DTL (modified DTL) circuit and for IC-DTL circuit discuss the terms mentioned below.
 - IC-DTL as NAND gate.

- Noise margin
- I/O characteristics

4. For DTL circuit shown in diagram 4 below:

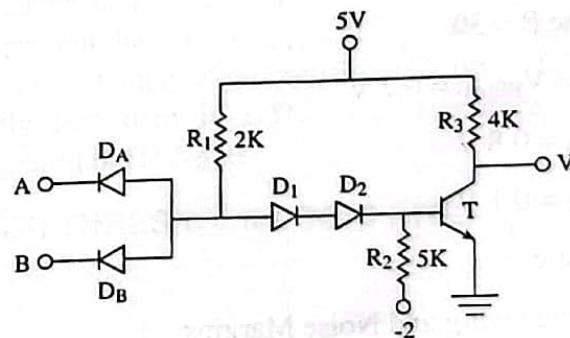
Assume $V_{D(on)} = V_{BE(on)} = 0.7 \text{ V}$

$V_{BE(sat)} = 0.8 \text{ V}$

$V_{CE(sat)} = 0.2 \text{ V}$ and $\beta = 30$.

Calculate:

- The logic swing & Noise margins
- Fan-out for diver circuit low o/p.

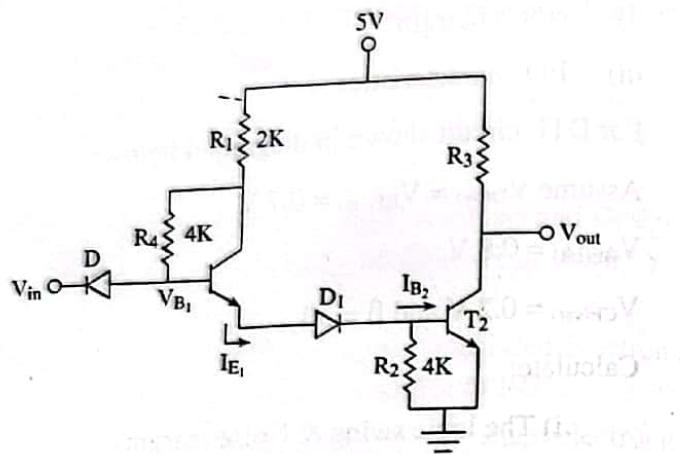


5. For the DTL inverter shown in diagram, 5 below

Assume $\beta = 19$

$V_{CE(sat)} = 0.2 \text{ V}$, $V_{BE(sat)} = 0.8 \text{ V}$

$V_{D(on)} = V_{BE(on)} = 0.7 \text{ V}$ Calculate minimum value of R_3 , so that T_2 remains in saturation, where input is connected to 10V. Suppose T_1 always operates in forward active mode.



6. For DTL circuit shown in diagram 5 above

Assume $\beta = 30$

$$V_{D(on)} = V_{BE(on)} = 0.7 \text{ V}$$

$$V_{BE(sat)} = 0.8 \text{ V}$$

$$V_{CE(sat)} = 0.1 \text{ V}$$

Calculate:

- logic swing and Noise Margins
- Voltage at V_{B1} and current I_B1, I_E1, I_C2 , if $V_{in} = 5 \text{ V}$ and $R_3 = 3\text{K}$.

High Threshold Logic (HTL)

4
Unit

INTRODUCTION

The another IC version of logic circuit made with Diodes (zener), Transistor and Resistors are High Threshold Logic that had been suitable to operate in environments which are very Noisy electrically. The HTL gate have propagation time as high as hundreds of nano seconds, while conventional DTL gates have propagation delay times, typically about some tens of nano seconds. The temperature sensitivity for HTL gate is significantly less than IC-DTL gate. Therefore, temperature effect is ignored in HTL gate.

HIGH THRESHOLD LOGIC (HTL)

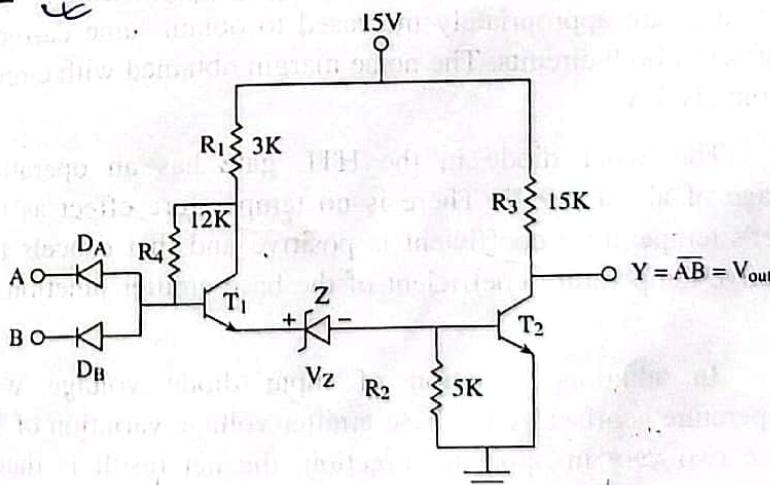


Fig. 4.1: HTL gate

There are circumstances where logic circuits must operate in environment which is very noisy electrically. Especially in industrial environment, the noise level becomes quite high due to presence of Motors, high voltage Switches, Relays etc. By using higher supply voltage 15 V and 6.9 volts zener diode in the DTL circuit, one may obtain high noise immunity gate as shown in diagram 4.1, also termed as HTL gate.

For two or more than two inputs the HTL circuit performs NAND operations only.

We note that in the HTL gate the supply voltage has been raised from 5 to 15V. To sustain a higher voltage the diode, hence been replaced by a zener diode. The corresponding resistance value in circuit also increased with supply voltage, otherwise the increased supply voltage would result in a large increase in current and therefore in power dissipation in the HTL gate.

Noise margin depends on the supply voltage, the resistances are appropriately increased to obtain same currents (approx) in both circuits. The noise margin obtained with circuit is typically 7 V.

The zener diode in the HTL gate has an operating voltage of about 6.9 V. There is no temperature effect as the zener's temperature coefficient is positive and that cancels the negative temperature coefficient of the base-emitter junction of T_2 .

In addition, variation of input diode voltage with temperature is offset by the base-emitter voltage variation of T_1 . Since two vary in opposite direction, the net result is that a negligible variation of VTC w.r. to temperature.

4.3 NOISE MARGIN

To compute noise margins of HTL gate, one should have to apply four conditions at T_2 of HTL gate.

Case I: When T_2 is at cut-off mode.

$$\begin{aligned} V_O &= V_{OH} = V_{CC} \\ \therefore V_{OH} &= 15 \quad \dots\dots\dots (i) \\ \therefore V_{in} &= V_{IL} \end{aligned}$$

Case II: When T_2 is at edge of conduction

$$V_{in} = V_{IL}$$

Applying kvl

$$\begin{aligned} -V_{in} - V_{D(on)} + V_{BE(on)} + VZ + V_{BE(on)} &= 0 \\ \therefore V_{in} &= V_{BE(on)} + VZ + V_{BE(on)} - V_{D(on)} \\ \therefore V_{IL} &= V_{BE(on)} + VZ + V_{BE(on)} - V_{D(on)} \\ &= 0.7 + 6.9 + 0.7 - 0.7 \\ &= 7.6 \text{ V} \quad \dots\dots\dots (ii) \end{aligned}$$

Case III: When T_2 is at edge of saturation

$$V_{in} = V_{IH}$$

Again applying kvl

$$\begin{aligned} -V_{in} - V_{D(on)} + V_{BE(on)} + VZ + V_{BE(sat)} &= 0 \\ \therefore V_{in} &= V_{BE(on)} + VZ + V_{BE(sat)} - V_{D(on)} \\ \therefore V_{IH} &= 0.7 + 6.9 + 0.8 - 0.7 \\ &= 7.7 \text{ V} \quad \dots\dots\dots (iii) \end{aligned}$$

Case IV: When T_2 is at saturated mode

$$\begin{aligned} V_O &= V_{OL} = V_{CE(sat)} \\ \therefore V_{OL} &= V_{CE(sat)} = 0.2 \text{ V} \quad \dots\dots\dots (iv) \end{aligned}$$

Thus, Noise margin are computed as accordingly.

$$NMH = V_{OH} - V_{IH} = 15 - 7.7 = 7.3 \text{ V}$$

$$NML = V_{IL} - V_{OL} = 7.6 - 0.2 = 7.4 \text{ V}$$

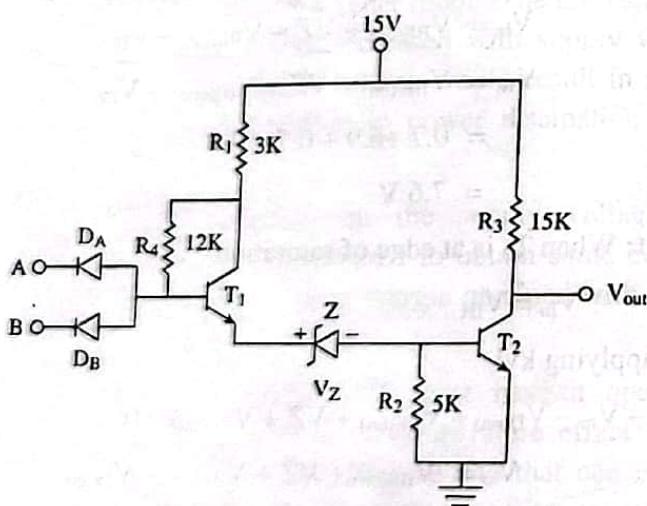
$$VTW = V_{IH} - V_{IL} = 7.7 - 7.6 = 0.1 \text{ V}$$

$$VLS = V_{OH} - V_{OL} = 15 - 0.2 = 14.8 \text{ V}$$

Example:

For the HTL circuit shown in diagram below, Assume $V_{D(on)} = V_{BE(on)} = 0.7 \text{ V}$, $V_{BE(sat)} = 0.8 \text{ V}$, $V_{CE(sat)} = 0.1 \text{ V}$ and zener diode voltage $VZ = 6.9 \text{ V}$. Compute

- i) Noise margins NMH and NML
- ii) Transition width and logic swing.



Solution:

To compute noise margin one should have to apply four conditions at T_2 .

Case I: When T_2 is at cut-off mode.

$$V_0 = V_{OH} = V_{CC}$$

Case II: When T_2 is at edge of conduction,

$$V_{in} = V_{IL}$$

$$\begin{aligned} V_{IL} &= V_{BE(on)} + VZ + V_{BE(on)} - V_{D(on)} \\ &= 0.7 + 6.9 + 0.7 - 0.7 \\ &= 7.6 \text{ V} \dots\dots\dots \text{(ii)} \end{aligned}$$

Case III: When T_2 is at edge of saturation

$$V_{in} = V_{IH}$$

$$\begin{aligned} V_{IH} &= V_{BE(on)} + VZ + V_{BE(sat)} - V_{D(on)} \\ &= 0.7 + 6.9 + 0.8 - 0.7 \\ &= 7.7 \text{ V} \dots\dots\dots \text{(iii)} \end{aligned}$$

Case IV: When T_2 is at saturated mode.

$$V_0 = V_{OL} = V_{CE(sat)}$$

$$V_{OL} = 0.1 \text{ V} \dots\dots\dots \text{(iv)}$$

Thus, noise margins

$$(i) \quad NMH = V_{OH} - V_{IH} = 15 - 7.7 = 7.3 \text{ V}$$

$$\begin{aligned} NML &= V_{IL} - V_{OL} \\ &= 7.6 - 0.1 = 7.5 \text{ V} \end{aligned}$$

$$(ii) \quad \text{Transition width } VTW = V_{IH} - V_{IL} = 7.7 - 7.6 = 0.1 \text{ V}$$

$$\text{Logic swing } VLS = V_{OH} - V_{OL} = 15 - 0.1 = 14.9 \text{ V}$$

4.4 INPUT-OUTPUT CHARACTERISTICS

The input voltage at which T_2 begins to come out of cut off is

$$\begin{aligned} V_i &= V_{BE2} + VZ + V_{BE1} - VDA \\ &= 0.65 + 6.9 + 0.7 - 0.75 \\ &= 7.5 \text{ V} \dots\dots\dots \text{(i)} \end{aligned}$$

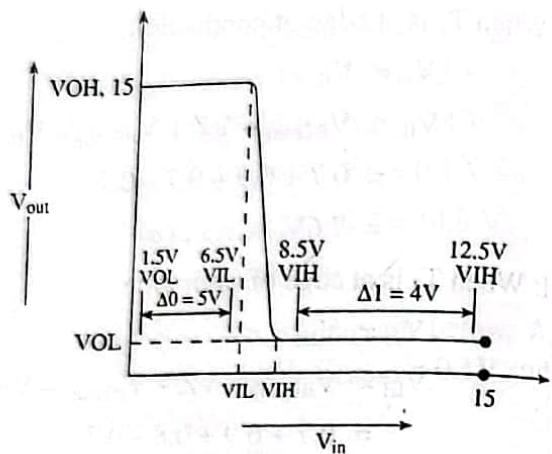


Fig. 4.2: I/O characteristics of HTL

The input voltage at which transistor T_2 is at edge of saturation is

$$V_i = V_{BE2} + VZ = V_{BE1} - VDA$$

$$\begin{aligned} V_i &= 0.75 + 6.9 + 0.70 - 0.75 \\ &= 7.6 \text{ V} \end{aligned} \quad \dots \dots \dots \text{(ii)}$$

Using the results in equation (i) & (ii) input-output characteristics is plotted and the nature of graph obtained is as shown in diagram 4.2 above.

The value of Noise Margins Δ_0 and Δ_1 are also indicated in I/O characteristics diagrams.

4.5 MANUFACTURER'S SPECIFICATIONS

Typical manufacturer's specifications for HTL gate are shown in table below.

$$V_{OH}/V_{OL} = 12.5 \text{ V}/1.5 \text{ V}$$

$$V_{IH}/V_{IL} = 8.5 \text{ V}/6.5 \text{ V}$$

$$NMH/NML = 4 \text{ V}/5 \text{ V}$$

$$V_{LS} = 11 \text{ V}$$

$$\text{Fan-out} = 10$$

Propagation Delay = 100 ns
tpd (HL)

Propagation Delay = 200 ns
tpd (LH)

SUMMARY

High Threshold Logic (HTL) that specially designed to becomes suitable for noisy environment are discussed with following ideas.

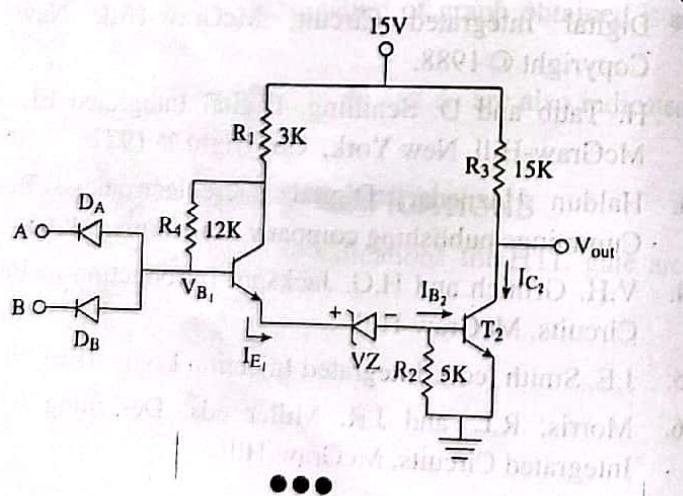
- Typical HTL gate circuits are discussed with its significance and about suitable environment.
- HTL gate noise margins are analytically computed.
- HTL I/O characteristics are discussed with graph.
- Typical manufactures specifications for HTL gate are discussed
- Important numerical based on HTL gate are solved.

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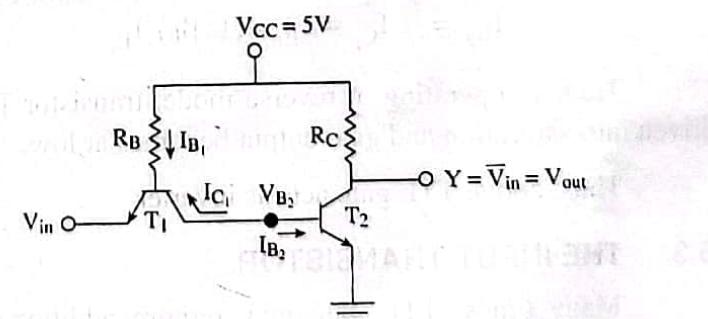
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PROBLEMS

1. Draw HTL circuit and discuss where HTL gate becomes more suitable? Also discuss the terms mentioned below.
 - i) Noise margins
 - ii) I/O characteristics
 - iii) Manufacturer's specifications
2. List out basic differences between the terms mentioned below.
 - i) DTL versus modified DTL
 - ii) IC-DTL versus HTL
3. For HTL circuit shown in diagram 3 below
 Assume $V_{D(on)} = V_{BE(on)} = 0.7 \text{ V}$
 $V_{BE(sat)} = 0.8 \text{ V}$, $V_{CE(sat)} = 0.1 \text{ V}$
 and Zener diode voltage $V_Z = 6.9 \text{ V}$
 Calculate:
 - i) Logic swing & Noise Margins.
 - ii) Current I_{B_1} , I_{E_1} , I_{R_2} , I_{B_2} and I_{C_2} and voltage V_{B_1} ,

**Transistor Transistor Logic (TTL)****5 Unit****5.1 INTRODUCTION**

The first "New" digital design become possible by the IC fabrication process was transistor-transistor Logic (TTL). In these circuits diode AND function of DTL was performed by a multi-emitter transistor. The use of a multi-emitter transistor in place of diode not only makes more efficient use of silicon surface area in the input stage but it also serves to decrease the propagation delay time of the TTL gate. The DTL speed limitation is overcome in the transistor-transistor logic (TTL) gate. This chapter also include Schottky TTL and that employed to clamp the transistor out of saturation and hence decreases the propagation delay time.

5.2 TTL AS INVERTER**Fig. 5.1: A TTL inverter gate**

The schematic diagram of TTL Inverter gate is shown above. The circuit have input V_{in} and output as V_{out} .

Case I: When input V_{in} is at low.

The base emitter junction of transistor T_1 becomes forward biased.

From diagram,

$$V_{B_2} - V_{CE_1(sat)} - V_{in} = 0$$

$$\therefore V_{B_2} = V_{CE_1(sat)} + V_{in}$$

$$= 0.2 + 0.2 = 0.4 \text{ volt}$$

As V_{B_2} becomes 0.4 V which is not sufficient for conduction of the transistor T_2 .

Hence, T_2 remains at cut-off and output becomes at high.

Case II: When Input V_{in} is at high.

The transistor T_1 operates in reverse active mode i.e. Active mode in which role of emitter and collector are interchanged. In this mode of operation the collector of transistor T_1 operates as an emitter and emitter as a collector.

From diagram

$$I_{B_2} = -I_{C_1} \equiv I_{E_1} = (1+\beta_R) I_{B_1}$$

Thus T_1 operating in reverse mode, transistor T_2 will be driven into saturation and gate output becomes at low.

Thus, above TTL gate acts as inverter

5.3 THE INPUT TRANSISTOR

Many times, TTL gate may require additional inputs. These additional inputs may be made available by paralleling T_1 with additional input transistors.

The paralleling of transistors with a common base and a common collector results as far as terminal behavior is

connected in single multi-emitter transistor. In IC, these multi-emitter transistor is fabricated with emitter region and a collector region, all within the same base region i.e. If 3-emitters are required, then 3-n-type materials fabricated within base region.

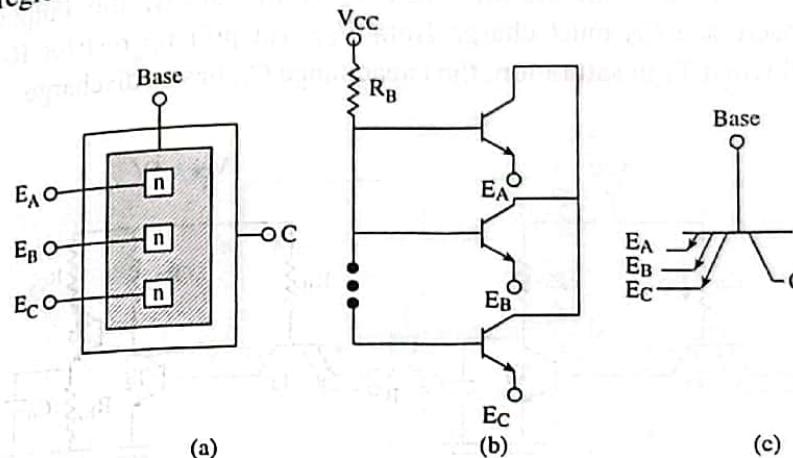


Fig. 5.2: (a) Pictorial representation, (b) Circuit diagram, (c) Symbol

In practice, we do not parallel input transistor but construct a transistor with a single common collector, a single common base and multiple emitters.

The physical structure of such a multi emitter transistor is shown in diagram 5.2(a), corresponding circuit in diagram 5.2(b) and its symbol in diagram 5.2(c),

Advantages:

- It reduces silicon chip area
- It eliminates the parasitic capacitance that arises via individual separate transistors-devices.

5.4 THE ACTIVE PULL-UP

The speed limitation in TTL gate is primarily due to the capacitive effects at output of gate, from collector of T_2 to ground.

In diagram 5.3(a), when T_2 is in cut-off, the output capacitance C_O must charge from V_{CC} via pull up resistor R_C and when T_2 is in saturation, the capacitance C_O has to discharge.

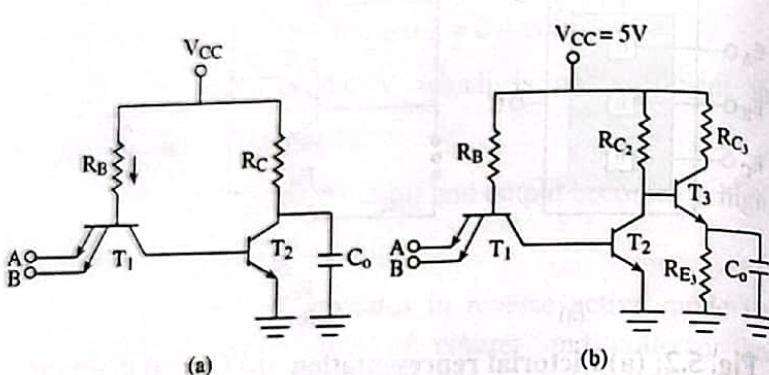


Fig. 5.3: (a) R_C as passive pull-up (b) T_3 as active pull-up

As output capacitance is C_O , the capacitance charges as well as output rises from logic '0' to logic '1' with time constant $T = R_C C_O$.

In diagram 5.3(b), the pull up resistor R_C can be replaced with an emitter follower T_3 , which aids in fast charging of load capacitance C_O . The common transistor provides fast discharging.

The scheme in which the pull up resistor is replaced by an emitter follower is known as "Active pull up". The output configuration is known as totem-pole because one transistor is stacked on top of others.

5.5 THE STANDARD TTL NAND GATE

The schematic diagram for standard TTL gate is shown in diagram 5.4. For two or more than two inputs the circuit performs NAND operation only.

Here, T_1 acts as input transistor, T_2 acts as phase splitter, T_4 & D acts as active pull up.

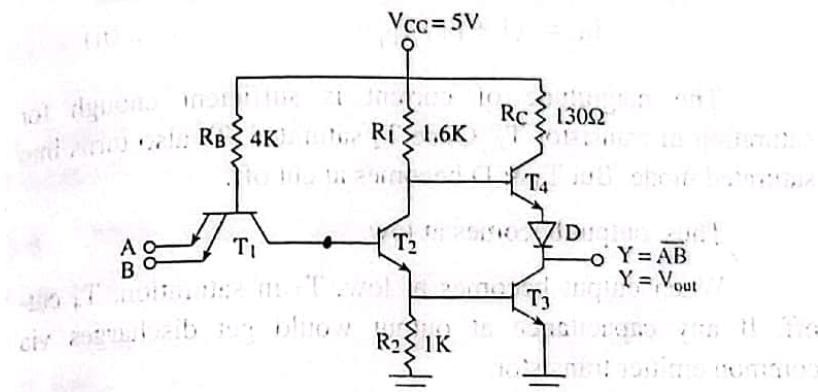


Fig. 5.4: A TTL NAND gate

Case - I:

When at least one input is at low.

The base-emitter junction of input transistor T_1 becomes forward biased and majority of current follows via it. From diagram

$$\begin{aligned} V_{B2} &= I_{CE1(sat)} + V_{BE} \\ &= 0.2V + 0.2V \\ &= 0.4V \end{aligned} \quad \dots\dots (i)$$

Hence, the transistor T_2 is cut-off. Once T_2 is cut-off, T_3 becomes cut-off. But T_4 & diode D are conducting and act as an emitter follower. Thus, output becomes at high.

When output is at high, T_3 cut-off and T_4 in saturation, the output capacitance is charged via series combination of emitter follower T_4 & diode D.

Case - II: When all inputs are at high.

The input transistor T_1 operates in reverse mode i.e. the role of collector & emitter of T_1 are interchanged.

From diagram

$$I_{B_2} = (1 + \beta_R) I_{B_1} \quad \dots \dots \text{(ii)}$$

The magnitude of current is sufficient enough for saturation of transistor T_2 . Once T_2 saturated, T_3 also turns into saturated mode. But T_4 & D becomes at cut off.

Thus, output becomes at low.

When output becomes at low, T_3 in saturation, T_4 cut-off. If any capacitance at output would get discharged via common emitter transistor.

Also the output of T_2 is provided to base of T_3 & T_4 with voltage swing in opposite directions so that when one is 'ON' other being 'OFF' and vice-versa.

Why Diode 'D'?

For case II, when all inputs are high, we noted that output becomes at low. The transistor T_2 & T_3 are in saturation.

From diagram

$$V_{C_2} - V_{CE_2(\text{sat})} - V_{BE_3(\text{sat})} = 0$$

$$\therefore V_{C_2} = V_{CE_2(\text{sat})} + V_{BE_3(\text{sat})} = 0.1 + 0.8 \\ = 0.9 \text{ V} \quad \dots \dots \text{(i)}$$

Also

$$V_{C_3} = V_{CE_3(\text{sat})}$$

$$= 0.1 \text{ V} \quad \dots \dots \text{(ii)}$$

In the absence of diode D between the T_3 & T_4 .

$$\begin{aligned} V_{BE_4} &= V_{B_4} - V_{C_3} = V_{C_2} - V_{C_3} \\ &= 0.9 - 0.1 \\ &= 0.8 \text{ V} \end{aligned}$$

This voltage is sufficient to turn 'ON' the transistor T_4 .

But we need low output so that T_4 cut-off.

Thus, a wide diode 'D' in series with T_4 , such that 0.8 V is divided between diode & transistor V_{BE} , none of them becomes forward biassed. Hence, output becomes at low.

5.6 ANALYSIS OF TTL NAND GATE

Case I: When at least any one input is at low.

Base-emitter of T_1 becomes forward biassed, T_2 & T_3 cut-off, while T_4 & D conducting.

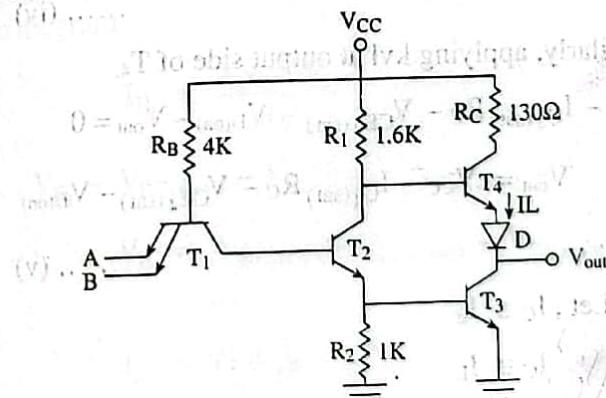


Fig. 5.5: Standard TTL NAND gate

From diagram

$$I_{B_1} = \frac{V_{CC} - V_{B_1}}{R_B} \quad \dots \dots \text{(i)}$$

$$\text{Also, } V_{B_1} - V_{BE_1(\text{sat})} - V_{in} = 0$$

$$\therefore V_{B_1} = V_{BE(\text{sat})} + V_{in} \quad \dots \dots \text{(ii)}$$

Since only T_4 conducting, applying KVL at input side of T_4 .

$$V_{CC} - I_{B_4} R_I - V_{BE_4(\text{sat})} - V_{D(\text{on})} - V_{out} = 0$$

$$\therefore V_{out} = V_{CC} - I_{B_4} R_I - V_{BE_4(\text{sat})} - V_{D(\text{on})}$$

..... (iii)

$$\text{Let } I_C \equiv I_E$$

$$\text{But } I_E = I_L = (1 + \beta) I_B.$$

$$\therefore I_B = \frac{I_L}{1 + \beta}$$

$$\therefore V_{out} = V_{CC} - \frac{I_L}{1 + \beta} R_I - V_{BE_4(\text{sat})} - V_{D(\text{on})} \quad \dots \dots \text{(iv)}$$

Similarly, applying kvl at output side of T_4 .

$$V_{CC} - I_{C_4(\text{sat})} R_C - V_{CE_4(\text{sat})} - V_{D(\text{on})} - V_{out} = 0$$

$$\therefore V_{out} = V_{CC} - I_{C_4(\text{sat})} R_C - V_{CE_4(\text{sat})} - V_{D(\text{on})} \quad \dots \dots \text{(v)}$$

$$\text{Let, } I_C \equiv I_E$$

$$I_C \equiv I_L$$

$$\therefore V_{out} = V_{CC} - I_L R_C - V_{CE_4(\text{sat})} - V_{D(\text{on})} \quad \dots \dots \text{(vi)}$$

From equation (iv) & (vi)

$$V_{CC} - \frac{I_L}{1 + \beta} R_I - V_{BE_4(\text{sat})} - V_{D(\text{on})}$$

$$= V_{CC} - I_L R_C - V_{CE_4(\text{sat})} - V_{D(\text{on})}$$

$$\therefore I_L R_C - \frac{R_I}{1 + \beta} I_L = V_{BE_4(\text{sat})} - V_{CE_4(\text{sat})}$$

$$\text{or, } I_L \left[R_C - \frac{R_I}{1 + \beta} \right] = V_{BE_4(\text{sat})} - V_{CE_4(\text{sat})}$$

$$\therefore I_L = \frac{V_{BE_4(\text{sat})} - V_{CE_4(\text{sat})}}{\left[R_C - \frac{R_I}{1 + \beta} \right]} \quad [\because 1 + \beta \gg R_I]$$

$$I_L = \frac{V_{BE_4(\text{sat})} - V_{CE_4(\text{sat})}}{R_C} \quad \dots \dots \text{(vii)}$$

Case - II

When all inputs are at high.

Input transistor T_1 operates in reverse mode, the transistor T_2 & T_3 turns into saturated mode, but T_4 cut-off.

From diagram

$$I_{B_1} = \frac{V_{CC} - V_{B_1}}{R_B} \quad \dots \dots \text{(i)}$$

$$\text{Here, } V_{B_1} - V_{BE_1(\text{on})} - V_{BE_3(\text{sat})} - V_{BE_3(\text{sat})} = 0$$

$$\therefore V_{B_1} = V_{BE_1(\text{on})} + V_{BE_2(\text{sat})} + V_{BE_3(\text{sat})} \quad \dots \dots \text{(ii)}$$

$$I_{B_2} = (1 + \beta_R) I_{B_1} \quad \dots \dots \text{(iii)}$$

$$I_{C_2} = \frac{V_{CC} - V_{C_2}}{R_1} \quad \dots \dots \text{(iv)}$$

Here, also,

$$V_{C_2} - V_{CE_2(\text{sat})} - V_{BE_3(\text{sat})} = 0$$

$$\therefore V_{C_2} = V_{CE_2(\text{sat})} + V_{BE_3(\text{sat})}.$$

From diagram

$$I_{E_2} = I_{B_2} + I_{C_2} \quad \dots \dots \dots \text{(v)}$$

$$I_{B_3} = I_{E_2} - I_{R_2} \quad \dots \dots \dots \text{(vi)}$$

$$\text{But, } I_{R_2} = \frac{V_{BE_3(\text{sat})}}{R_2} \quad \dots \dots \dots \text{(vii)}$$

$$I_{C_3} = \beta I_{B_3} \quad \dots \dots \dots \text{(viii)}$$

$$\text{i.e. } I_L = \beta I_{B_3}$$

In this way, voltage at each nodes and current in each branches computed analytically.

5.7 VOLTAGE TRANSFER CHARACTERISTICS

For standard TTL NAND gate, when output is plotted against input, the nature of graph obtained is shown in diagram 5.6

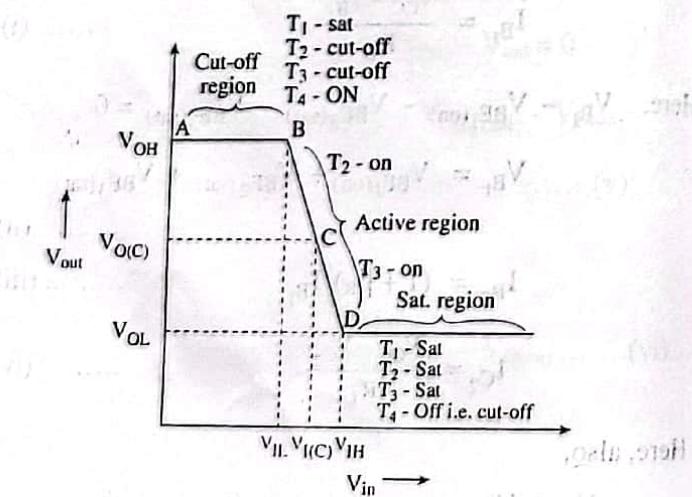


Fig. 5.6: VTC of TTL NAND gate

For cut-off region of graph, the mode of operation of transistors becomes, T_1 sat, T_2 & T_3 cut-off and T_4 ON.

For active region of graph, when T_2 -ON then T_3 essentially becomes, 'ON' and out-put gradually goes on decreasing.

For saturated region of graph, the mode of operation of transistor of TTL gate becomes T_1 -sat, T_2 -sat, T_3 -sat but T_4 -cut-off.

Analytically we obtain segment AB with

$$V_{OH} = V_{CC} - V_{BE_4} - V_D$$

$$= 5 - 0.7 - 0.7$$

$$= 3.6 \text{ V}$$

The first break point occurs when T_2 becomes ON i.e.

$$V_{C_1} = V_{B_2} = V_{BE(\text{on})} = 0.7 \text{ V}$$

$$\text{But } V_{B_2} = V_{CE_1(\text{sat})} + V_{in}$$

$$V_{in} = V_{IL} = V_{B_2} - V_{CE_1(\text{sat})}$$

$$= 0.7 - 0.2 = 0.5 \text{ V}$$

Second break point occurs when T_3 turns ON.

$$V_{I(c)} = V_{BE_3(\text{on})} + V_{BE_2(\text{on})} - V_{CE_1(\text{sat})}$$

$$= 0.7 + 0.7 - 0.2$$

$$= 1.4 - 0.2$$

$$= 1.2 \text{ V}$$

$$V_{O(c)} = V_{C_2} - V_{BE_4(\text{on})} - V_{D(\text{on})}$$

Similarly, the third& final break point occurs when T_4 saturated.

$$V_{out} = V_{ol} = V_{CE(sat)} = 0.2 \text{ V}$$

With T_2 saturated, T_1 is still saturated.

$$V_{in} = V_{IH} = V_{BE_3(sat)} + V_{BE_2(sat)} + V_{CE_1(sat)}$$

With $V_{in} \geq V_{IH}$, T_1 operates in reverse active mode with base-emitter Junction reverse biased and base-collector Junction forward biased.

Also, Base of T_1 is clamped at

$$\begin{aligned} V_{B_1} &= V_{BC_1(on)} + V_{BE_2(sat)} + V_{BE_3(sat)} \\ &= 0.7 + 0.8 + 0.8 \\ &= 2.3 \text{ Volts.} \end{aligned}$$

5.8 FAN-OUT

Case - I: When all inputs are at high.

In standard TTL circuits, when all inputs are at high, the transistor T_1 operates in reverse mode, the high level input current is given as

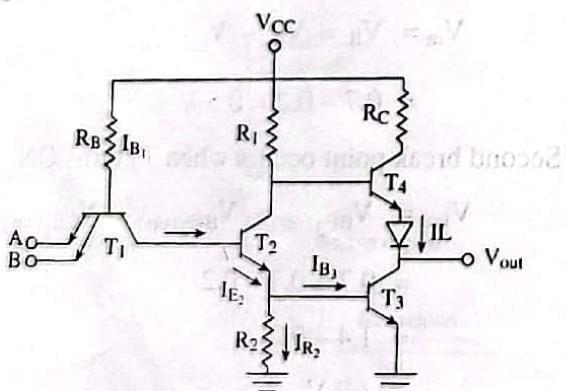


Fig. 5.7: Standard TTL NAND gate

$$I_{IH} = \frac{\beta R I_{B_1}}{M} \quad \dots \dots \text{(i)}$$

Where, M is the number of emitters to input transistor.

βR -reverse current gain.

$$\text{Here, } I_{B_1} = \frac{V_{CC} - V_{B_1}}{R_B} \quad \dots \dots \text{(ii)}$$

To compute V_{B_1} applying KVL,

$$V_{B_1} - V_{BE_1(on)} - V_{BE_2(sat)} - V_{BE_3(sat)} = 0$$

$$V_{B_1} = V_{BE(on)} + V_{BE_2(sat)} + V_{BE_3(sat)}$$

$$\therefore \quad \dots \dots \text{(iii)}$$

Case II: When at least any one input is at low.

The input transistor of TTL circuit operates in saturated mode. The low level input current is given as

$$I_{IL} = I_{B_1} \quad \dots \dots \text{(iv)}$$

To compute I_{B_1} , applying KVL, we get

$$V_{CC} - I_{B_1} R_B - V_{BE_1(sat)} - V_{in} = 0$$

$$I_{B_1} R_B = V_{CC} - V_{BE_1(sat)} - V_{in}$$

$$\therefore I_{B_1} = \frac{V_{CC} - V_{BE_1(sat)} - V_{in}}{R_B} \quad \dots \dots \text{(v)}$$

Now, To compute fan-out:

We compute Fan-out for both output states low and high.

Case I: When output of standard TTL is at low.

Fan-out is define as

$$(i) \quad NL = \frac{I_{C_3(EOS)}}{I_{IL}} \quad \dots \dots \text{(i)}$$

From diagram

$$I_{C_3} = \beta I_{B_3} \quad \dots \dots \text{(ii)}$$

$$\text{But } I_{B_3} = I_{E_2} - I_{R_2} \quad \dots \dots \text{(iii)}$$

$$I_{R_2} = \frac{V_{BE_3(\text{sat})}}{R_2} \quad \dots \dots \text{(iv)}$$

$$I_{E_2} = I_{B_2} + I_{C_2} \quad \dots \dots \text{(v)}$$

$$I_{C_2} = \frac{V_{CC} - V_{C_2}}{R_1} \quad \dots \dots \text{(vi)}$$

$$\text{But } V_{C_2} - V_{CE_2(\text{sat})} - V_{BE_3(\text{sat})} = 0$$

$$\therefore V_{C_2} = V_{CE_2(\text{sat})} + V_{BE_3(\text{sat})} \quad \dots \dots \text{(vii)}$$

$$\text{Now, } I_{B_2} = (1 + \beta R) I_{B_1} \quad \dots \dots \text{(viii)}$$

To compute I_{B_1} , applying KVL,

$$V_{CC} - I_{B_1} R_B - V_{BE_1(\text{on})} - V_{BE_2(\text{sat})} - V_{BE_3(\text{sat})} = 0$$

$$\text{or, } I_{B_1} R_B = V_{CC} - V_{BE_1(\text{on})} - V_{BE_2(\text{sat})} - V_{BE_3(\text{sat})}$$

$$\therefore I_{B_1} = \frac{V_{CC} - V_{BE_1(\text{on})} - V_{BE_2(\text{sat})} - V_{BE_3(\text{sat})}}{R_B}$$

Case - II: When output of standard TTL gate is at high:

Fan-Out is expressed as

$$NH = \frac{I_L}{I_{IH}} \quad \text{(i)}$$

$$I_L = \frac{V_{BE_4(\text{sat})} - V_{CE_4(\text{sat})}}{R_C} \quad \dots \dots \text{(ii)}$$

Expression I_L already derived in analysis of TTL and expressed as equation (vii) there.

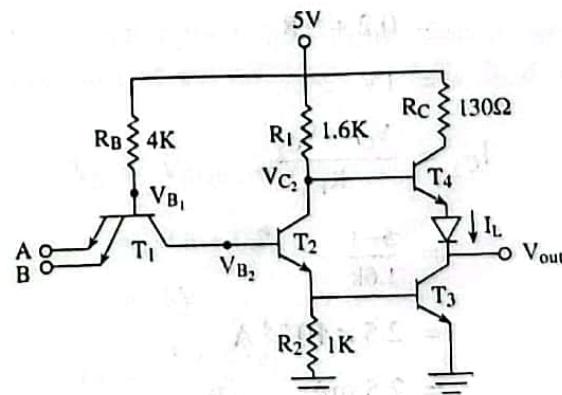
$$I_{IH} = \frac{\beta R \times I_{B_1}}{M}$$

It is already derived in starting of fan-out section.

Example:

For the standard TTL circuit shown below assume that $V_{D(\text{on})} = V_{BE(\text{on})} = 0.7\text{V}$, $V_{BE(\text{sat})} = 0.8\text{V}$, $V_{CE(\text{sat})} = 0.2\text{V}$, $\beta F = 30$, and $\beta R = 0.2$. Compute voltages at each Nodes and current in each branches.

- i) For $V_A = V_B = 5\text{V}$.
- ii) For $V_A = V_B = 0.2\text{V}$.
- iii) Fan-out for both output states.



Solution:

- (i) For $V_A = V_B = 5\text{V}$,

T_1 operates in reverse mode, T_2 and T_3 turns into saturated mode and T_4 turns into cut-off mode.

$$\begin{aligned} V_{B_1} &= V_{BE_1(\text{on})} + V_{BE_2(\text{sat})} + V_{BE_3(\text{sat})} \\ &= 0.7 + 0.8 + 0.8 \\ &= 2.3\text{V} \end{aligned}$$

$$I_{B_1} = \frac{V_{CC} - V_{B_1}}{R_B}$$

$$= \frac{5 - 2.3}{4k}$$

$$= 0.675 \times 10^{-3} A$$

$$= 0.675 \text{ mA}$$

$$I_{B_2} = (1 + \beta_R) I_{B_1}$$

$$= (1 + 0.2) \times 0.675 \text{ mA}$$

$$= 0.81 \text{ mA}$$

$$V_{C_2} = V_{CE_2(\text{sat})} + V_{BE_3(\text{sat})}$$

$$= 0.2 + 0.8$$

$$= 1V$$

$$I_{C_2} = \frac{V_{CC} - V_{C_2}}{R_J}$$

$$= \frac{5 - 1}{1.6k}$$

$$= 2.5 \times 10^{-3} A$$

$$= 2.5 \text{ mA}$$

$$I_{E_2} = I_{B_2} + I_{C_2}$$

$$= 0.81 \text{ mA} + 2.5 \text{ mA}$$

$$= 3.31 \text{ mA}$$

$$I_{R_2} = \frac{V_{BE_3(\text{sat})}}{R_2}$$

$$= \frac{0.8}{1k}$$

$$= 0.8 \text{ mA}$$

$$I_{B_3} = I_{E_2} - I_{R_2}$$

$$= 3.31 \text{ mA} - 0.8 \text{ mA}$$

$$= 2.51 \text{ mA}$$

$$I_{C_3} = \beta I_{B_3}$$

$$= 30 \times 2.51 \text{ mA}$$

$$= 75.3 \text{ mA}$$

$$I_{C_3} = I_L = 75.3 \text{ mA}$$

Thus,

(ii) For $V_A = V_B = 0.2V$,

The base-emitter junction of T_1 becomes forward biased, T_2 and T_3 becomes at cut-off mode and T_4 & diode D are conducting.

Here,

$$V_{B_1} = V_{BE(\text{sat})} + V_{in}$$

$$= 0.8 + 0.2$$

$$= 1V$$

$$I_{B_1} = \frac{V_{CC} - V_{B_1}}{R_B}$$

$$= \frac{5 - 1}{4k}$$

$$= 1 \text{ mA}$$

$$I_L = \frac{V_{BE_4(\text{sat})} - V_{CE_4(\text{sat})}}{R_C}$$

$$= \frac{0.8 - 0.2}{130\Omega}$$

$$= 4.6153 \times 10^{-3}$$

$$I_L = 4.6143 \text{ mA}$$

(iii) Fan-out for both output states.

$$I_{IH} = \frac{\beta_R \times I_{B1}}{M} \quad \dots \dots \dots \text{(i)}$$

$$\begin{aligned} V_{B1} &= V_{BE(on)} + V_{BE2(sat)} + V_{BE3(sat)} \\ &= 0.7 + 0.8 + 0.8 \\ &= 2.3 \text{ V} \end{aligned}$$

$$\begin{aligned} I_{B1} &= \frac{V_{CC} - V_{B1}}{R_B} \\ &= \frac{5 - 2.3}{4k} \\ &= 0.675 \text{ mA} \end{aligned}$$

From equation (i),

$$\begin{aligned} I_{IH} &= \frac{0.2 \times 0.675 \text{ mA}}{2} \\ &= 0.0675 \times 10^{-3} \text{ mA} \\ &= 67.5 \times 10^{-6} \text{ A} \\ &= 67.5 \mu\text{A} \end{aligned}$$

Similarly,

$$\begin{aligned} I_{IL} &= \frac{V_{CC} - V_{BE1(sat)} - V_{in}}{R_B} \quad \dots \dots \dots \text{(ii)} \\ &= \frac{5 - 0.8 - 0.2}{4k} \end{aligned}$$

$$I_{IL} = 1 \text{ mA}$$

Case I: Fan-out for low output state is expressed as

$$N_L = \frac{I_{C1(EOS)}}{I_{IL}} \quad \dots \dots \dots \text{(iii)}$$

$$\begin{aligned} I_{B1} &= \frac{V_{CC} - V_{B1}}{R_B} \\ &= \frac{5 - 2.3}{4k} \\ &= 0.675 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_{B2} &= (1 + \beta_R) I_{B1} \\ &= (1 + 0.2) \times 0.675 \text{ mA} \\ &= 0.81 \text{ mA} \end{aligned}$$

$$\begin{aligned} V_{C2} &= V_{CE2(sat)} + V_{BE3(sat)} \\ &= 0.2 + 0.8 \\ &= 1 \text{ V} \end{aligned}$$

$$\begin{aligned} I_{C2} &= \frac{V_{CC} - V_{C2}}{R_1} = \frac{5 - 1}{1.6k} \\ &= 2.5 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_{E2} &= I_{B2} + I_{C2} \\ &= 0.81 \text{ mA} + 2.5 \text{ mA} \end{aligned}$$

$$\begin{aligned} I_{R2} &= \frac{V_{BE3(sat)}}{R_2} \\ &= \frac{0.8}{1k} \\ &= 0.8 \text{ mA} \end{aligned}$$

$$\begin{aligned}I_{B_3} &= I_{E_2} - I_{R_2} \\&= 3.31 \text{ mA} - 0.8 \text{ mA} \\&= 2.51 \text{ mA}\end{aligned}$$

$$\begin{aligned}I_{C_3(\text{EOS})} &= \beta I_{B_3} \\&= 30 \times 2.51 \text{ mA} \\&= 75.3 \text{ mA.}\end{aligned}$$

From equation (iii)

$$NL = \frac{I_{C_3(\text{EOS})}}{I_{IL}} = \frac{75.3 \text{ mA}}{1 \text{ mA}}$$

$$NL = 75$$

Case II: Fan-out for High output states

$$NH = \frac{I_L}{I_{IH}}$$

$$\begin{aligned}I_L &= \frac{V_{BE_4(\text{sat})} - V_{CE_4(\text{sat})}}{R_C} = \frac{0.8 - 0.2}{130\Omega} \\&= 4.6153 \text{ mA.}\end{aligned}$$

$$I_{IH} = 0.06753 \text{ mA.}$$

$$\begin{aligned}NH &= \frac{4.6153 \text{ mA}}{0.0675 \text{ mA}} \\&= 68.37\end{aligned}$$

$$NH = 68$$

5.9 TYPES OF TTL GATE

Basically TTL gates are classified under four categories differing principally on speed, power dissipation, output states etc.

- (a) High speed TTL
- (b) Schottky TTL
- (c) Open collector TTL
- (d) Tri-state logic TTL

(a) High Speed TTL:

High speed TTL gate is shown in diagram 5.8. The speed of the standard TTL gate is limited by finite storage time of transistor as it gets saturated. The long time constant as capacitive load charge and discharge via relatively large valued resistors in the circuit also contribute to the transient delays.

[One technique to speed up the operation of the TTL gate is to reduce the value of all resistances.] The trade-off is the corresponding increase in the power consumption.

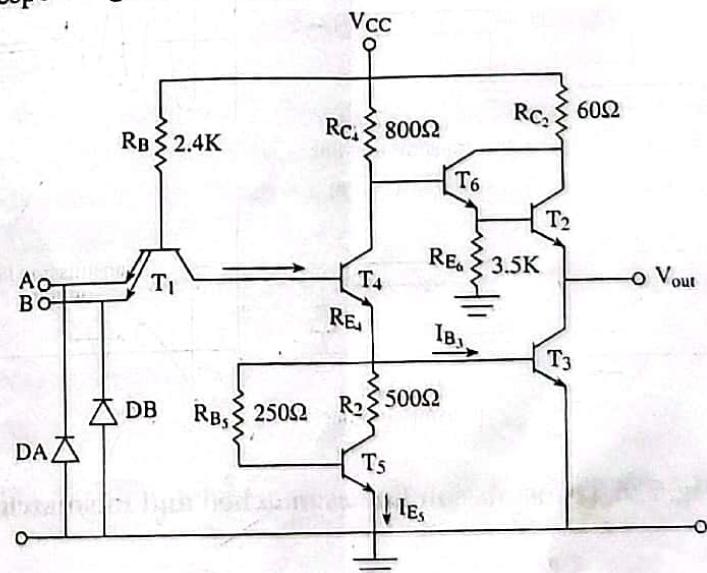


Fig. 5.8: High-speed TTL gate

In addition to the reduction in resistor values, the other changes are:

The Input Diode:

The diode acts as input "clamp" to suppress the ringing that result from the fast voltage transitions found in TTL system.

Eg. suppose out-put voltage of TTL gate suddenly changes from logic high to logic low. Let this signal allowed to pass via wire, if the wire which acts as transmission line, is not terminated properly, then ringing results as illustrated in diagram 5.9(a), but get eliminated up to some extent in diag. 5.9(b) when terminated properly. The input diode clamp the negative under shoot at approximately $-0.75V$ and absorbs enough of applied energy to prevent a large positive overshoot which might turn the gate 'ON' again. This suppression of the ringing is illustrated in diagram 5.9(b).

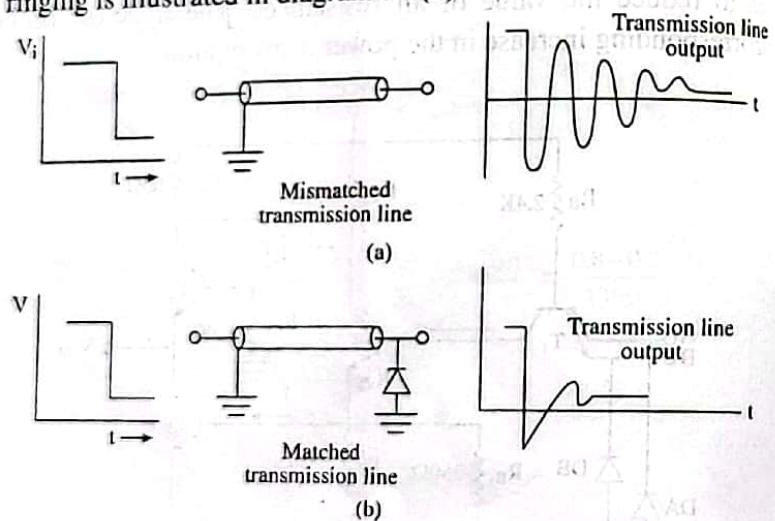


Fig. 5.9: Transmission line as matched and mismatched

The Darlington Circuit:

In high speed TTL gate, the transistors T_6 and T_2 are in a Darlington configuration. [The Darlington pair produces increased current gain, leading to increase in the current

sourcing capability. The output impedance is low, results in reduction in the time required to charge capacitive load, allowing higher speed of operation.

In a Darlington circuit only the input transistor T_6 and not the O/P transistor T_2 can be driven to saturation. No matter whether t_6 is saturated or in active region, voltage across T_{CE6} is positive.

Also, since $V_{BC2} = V_{CE6}$, the collector base Junction of T_2 can never be forward-biased. Hence, T_2 can never saturate.

Active Pull-down:

In high speed TTL circuit, the transistors T_5 followed by its two resistors $250\ \Omega$ and $500\ \Omega$ acts as active pull down. The emitter resistance of T_4 pulls the base of T_3 down to ground when T_4 cut-off. The emitter resistance of T_4 is replaced by T_5 & two resistors.

T_3 to be turned ON, T_5 appears as a resistance, turning T_3 faster. T_3 to be turned OFF, The turn-off base current of T_3 is due to the collector current of T_5 (Discharging base charges of T_3 via T_5 is faster).

Thus, propagation delay time decreased with active pull down.]

Some other advantages are:

- Operation over a wide range of temperature.
- I/O characteristics exhibits the much more abrupt change between levels i.e. the transition between logic level is achieved with much smaller change in input voltage

[A final advantage of the active pull down is to be seen in its effects on I/O characteristics of TTL gate.] Characteristics with active pull down and resistor pull down are compared in diagram 5.10.

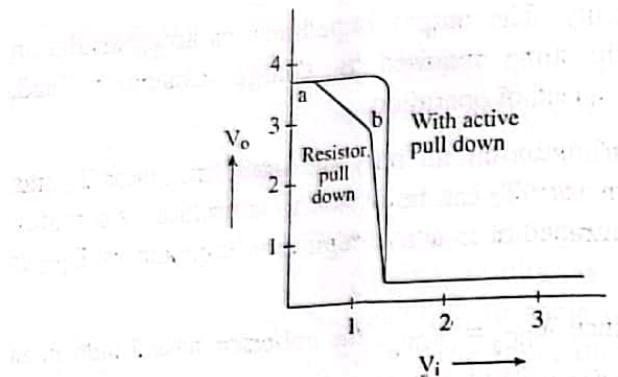


Fig. 5.10: Resistor pull down versus active pull down

Until T_3 turns ON, the active pull-down provide no path for emitter current of T_4 . Thus T_4 and T_3 go on simultaneously and the region B-C in the VTC is absent, with active pull-down.

(b) Schottky TTL

A transistor with schottky diode clamp is indicated in diagram 5.11(a), such a diode transistor combination is referred to as a schottky transistor is shown in diagram 5.11(b).

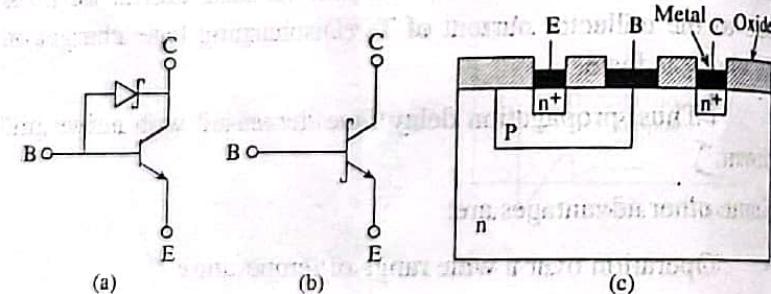


Fig. 5.11: (a) Schottky diode between base and collector (b) Schottky transistor (c) Cross-section of Schottky transistor

A reduction in storage time results in reduction of propagation delay. This is because of time required for transistor to come out of saturation delays switching of transistor ON condition to OFF condition.

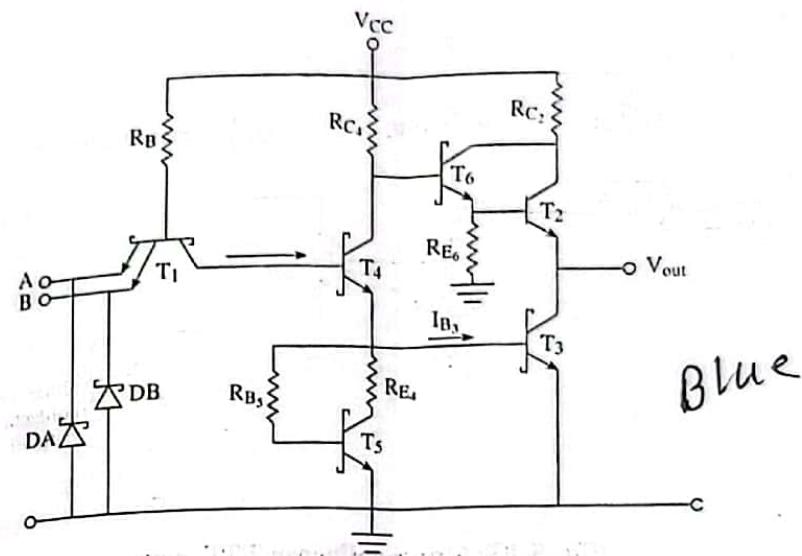


Fig. 5.12: Schottky-clamped TTL NAND gate

Transistor saturation can be eliminated by placing schottky diode between base & collector of each saturated transistor in the circuit. The schottky diode is formed by a junction of metal & semi-conductor in contrast to conventional diode. The voltage across conducting diode is only 0.4 V. Hence, presence of schottky diode between base & collector prevents transistor entering into saturation mode.

In diagram 5.12, except T_2 , all the transistors are replaced by schottky transistors. The main significance of schottky TTL gate is that it decreases propagation delay without sacrifice of power dissipation.

(c) Open Collector TTL

Open collector TTL is illustrated in diagram 5.13. At collector of transistor T_2 , no any transistor connected, rather it is kept open while emitter of T_2 is connected to base of T_3 , and load resistor R_L is connected externally to output.

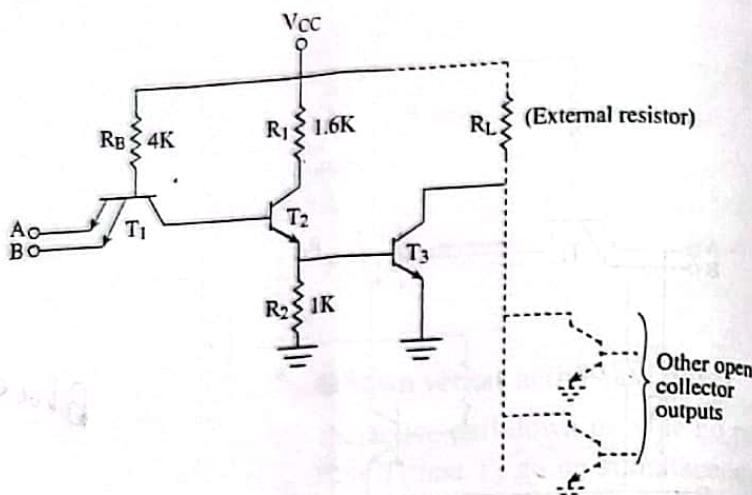


Fig. 5.13: Open collector TTL gate

Basic operation:**Case I:** When at least any one input is at low.

The base-emitter junction of input transistor T_1 becomes forward biased.

$$\begin{aligned}V_{B_2} &= V_{CE_1(\text{sat})} + V_{in} = 0.2 + 0.2 \\&= 0.4 \text{ V}\end{aligned}$$

Thus, T_2 becomes cut-off and T_3 cut-off. The output level will be high, if an external resistor R_L is connected between V_{CC} & output.

Case II: When all inputs are at high.

For all input high, input transistor T_1 operates in reverse mode i.e. Role of collector and emitter interchanged.

$$I_{B_2} = (1 + \beta_R) I_{B_1}$$

Hence, T_2 , T_3 conducts and saturate. The output value goes to low to 0.2 V.

As noted in diagram of open collector TTL gate, they use only lower transistor of totem pole pair, the collector is open and an external pull up resistor is connected for proper operation of the circuit.

Applications:

In many applications such as Bus organized digital system, where various outputs must be ANDed using TTL gates with totem pole output would require AND gates.

The output of open collector can be wired AND and connected to a common pull up load. It is useful for driving LED, Relay, switches etc.

Disadvantage:

Slow switching speed.

(d) Tri-state Logic TTL

The circuit of Tri-state logic TTL gate is shown in diagram 5.14. It is a special type of totem pole gate that allows the wired connection of output for purpose of forming common bus system, known as Tri-state gate.

As from its name, it is obvious, A tri-state exhibits 3-output states.

1. A low level output when lower transistor in totem pole is ON and the upper transistor is OFF.
2. A high level output when upper transistor in Totem pole is ON and the lower transistor is OFF.
3. A third state when both transistors in the Totem pole are OFF. The third state provide an open circuit or high Impedance state that allows a direct wire connection of many output to a common line. Three state gate eliminates the need of open collector gates in bus configuration.

Transistor T_1 to T_5 form the totem pole TTL-circuit.

Transistors T_6 , T_7 & T_8 associated with control input form a circuit similar to open collector TTL gate. Two circuits are connected together via a diode D:

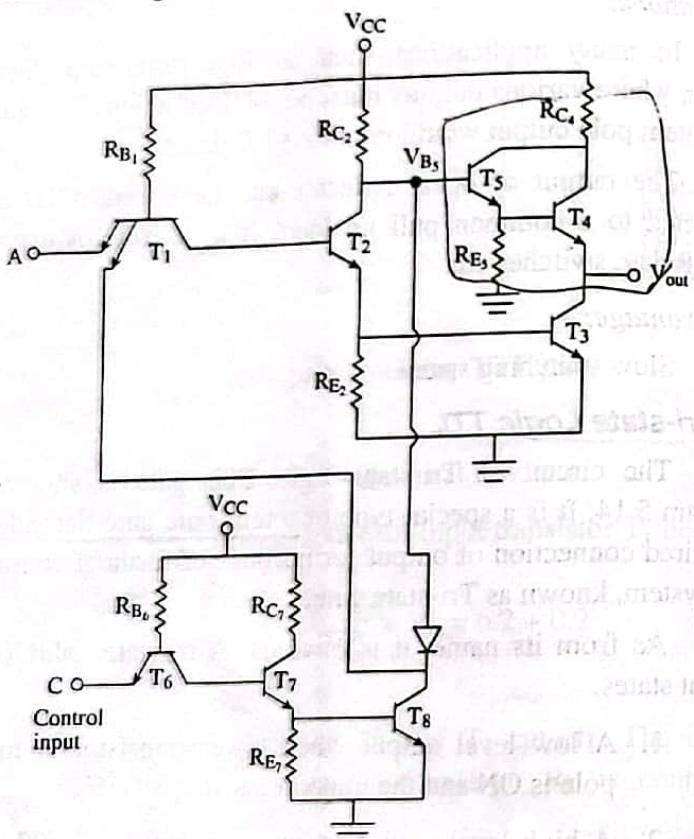


Fig. 5.14: Tri-state logic TTL gate

Basic operation

Case I: When control input c is at low.

The base emitter junction of T_6 becomes forward biased. Hence, transistor T_7 & T_8 cut-off, that prevents diode D from conducting and also the emitter of T_1 connected to T_8 has no

conduction path. Thus, T_8 has no effect. Hence output V_{out} depends on 'A' only.

Sub-case Ia:

When input A is at low.

Input transistor T_1 base-emitter junction becomes forward biased that causes lower transistor T_2 , T_3 in totem pole 'OFF' and upper transistor T_4 , T_5 'ON'. Hence output becomes at high.

Sub-case Ib:

When input A is at high.

Input transistor T_1 operates reverse in reverse mode that causes lower transistors T_2 , T_3 to saturate i.e. 'ON' and upper transistors T_4 , T_5 'OFF' in the Totem pole. Hence, output becomes at low.

Case II: When control input C at high.

Transistor T_6 operates in reverse mode, which turn transistors T_7 & T_8 to saturate. Now the voltage at base of T_5 is calculated as

$$V_{B5} - V_{D(on)} - V_{CE8(sat)} = 0$$

$$\begin{aligned} \therefore V_{B5} &= V_{D(on)} + V_{CE8(sat)} \\ &= 0.7 + 0.2 \\ &= 0.9 \text{ V} \end{aligned}$$

Hence T_4 & T_5 cut-off. At the same time, one of emitter of T_1 is connected to logic low. Hence T_2 , T_3 becomes at cut-off.

Thus, both T_3 & T_4 in the totem pole are turned 'OFF' and output of the circuit behaves like an open circuit with very high output impedance.

5.10 MANUFACTURES SPECIFICATIONS

Typical manufacturer's specification for TTL gate is shown in table below:

$$V_{OH}/V_{OL} = 3.5V/0.2V$$

$$V_{IH}/V_{IL} = 1.5V/0.5V$$

$$NMH/NML = 2V/0.3V$$

$$\text{Voltage logic swing} = 3.3V$$

$$\text{Fan-out} = 10$$

$$\text{Power dissipation per gate} = 10 \text{ mW}$$

$$\text{Propagation Delay Time} = 10 \text{ ns}$$

The characteristics of TTL gates are temperature dependent. The source of this dependence is the temperature dependence of the base-emitter and base collector junction voltages. Instead we shall take note of this temperature dependence as it is evidenced in typical average characteristics published by manufacturers.

TTL: Performance characteristics at 25°c

	Series 74	Series 74S	Series 74LS
Min $V_{OH}/\text{Max } V_{OL}$	2.4V/0.4V	2.7/0.5V	2.7/0.5V
Min $V_{IH}/\text{Max } V_{IL}$	2.0V/0.8V	2.0/0.8V	2.0/0.8V
Min $I_{OH}/\text{Min } I_{OL}$	-0.4 mA/16mA	-1 mA/20mA	-0.4 mA/8mA
Max $I_{IH}/\text{Max } I_{IL}$	40μA/-1.6mA	50μA/-2mA	20μA/-0.4mA
Propagation Delay	10ns	3ns	10ns
Power Dissipation/ gate	10mW	20mW	2mW

Advanced Schottky TTL: characteristics at 25°c

	Series 74F	Series 74AS	Series 74ALS
Min $V_{OH}/\text{Max } V_{OL}$	2.7/0.5V	Same as 74s	Same as 74LS
Min $V_{IH}/\text{Max } V_{IL}$	2.0/0.8V	"	"
Min $I_{OH}/\text{Min } I_{OL}$	-1mA/20mA	-2mA/20mA	-0.4mA/4mA
Max $I_{IH}/\text{Max } I_{IL}$	20 μA/ -0.6 mA	0.2 mA/ -2mA	20 μA/ -0.2mA
Propagation Delay	2.5 ns	1.5 ns	4 ns
Power Dissipation/gate	4 mW	20 mW	1mW

5.11 A COMPARISON BETWEEN DTL & TTL

A simple comparison between the DTL and TTL gate will illustrate the greater advantage of the latter in the speed of removal of stored base charge from base of T_3 . The rate at which the stored base charge of T_3 is being removed, is $h_{FE} I_{B1}$, where h_{FE} is current gain.

The discharge rate for TTL is computed as 22 mA approx., and as 0.38 mA in the DTL case.

This faster removal of charge stored in T_3 result in TTL gate which operates at propagation delay times that are one tenth those of DTL gates. ✓

SUMMARY

This chapter is devoted to brief discussion of transistor-transistor logic and their corresponding developments, standards, Analysis and Design. In addition to these some typical TTL characteristics, TTL types are discussed with following ideas:

- TTL Inverter circuits, a concept of multi-emitter transistor, Active pull up are discussed.
- The standard TTL NAND gate circuit are discussed with Analysis for various inputs.
- Standard TTL typical important characteristics are discussed with Voltage Transfer Characteristics (VTC), Fan-out (N).
- Types of TTL gates discussed are
 - High Speed TTL
 - Schottky TTL
 - Open collector TTL
 - Tri – State Logic TTL
- The important Numerical based on standard TTL are solved analytically.

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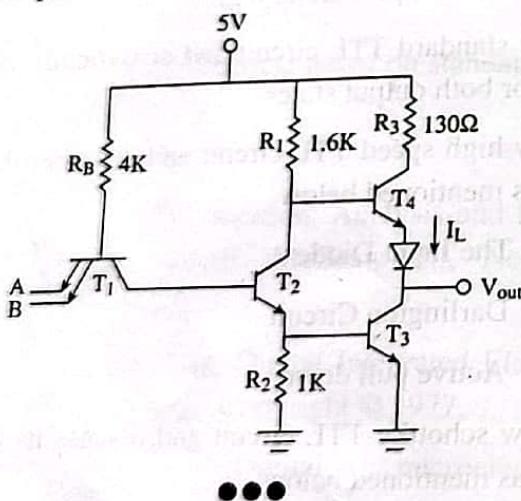
PROBLEMS

1. Draw TTL inverter circuit and explain its operation. Also discuss the terms mentioned below.
 - i) Multi emitter input transistor
 - ii) The active pull up.
2. Draw standard TTL circuit and derive an expression for voltages at each nodes and current in each branches for conditions mentioned below.
 - i) For at least any one input at low
 - ii) For all inputs are at high.
3. Draw standard TTL circuit and analytically compute Fan-out for both output states.
4. Draw high speed TTL circuit and discuss role play by the terms mentioned below.
 - i) The Input Diode
 - ii) Darlington Circuit
 - iii) Active pull down.
5. Draw schottky TTL circuit and discuss its operation with terms mentioned below.
 - i) Schottky diode
 - ii) Schottky Transistor
 - iii) Significances of schoty TTL

6. Draw open collector TTL circuit and discuss its operations with necessary application
7. Draw Tri-state logic TTL circuit and discuss its operation with necessary explanation.
8. For the TTL gate shown below in diagram 8, Assume $V_{BE(on)} = 0.7 \text{ V}$, $V_{BE(sat)} = 0.8 \text{ V}$, $V_{CE(sat)} = 0.1 \text{ V}$ and $\beta_F = 70$, $\beta_R = 0.1$.

Calculate:

- i) Fan-out both output stages
- ii) Value of voltage at each nodes and current in each branches for $V_A = V_B = 5 \text{ V}$.
- iii) Repeat case (ii) for $V_A = V_B = 0.1 \text{ V}$.



Emitter Coupled Logic (ECL)

6
Unit

6.1 INTRODUCTION

All the other logic forms considered (RTL, DTL, TTL) suffers from a common and fundamental limitation on their speed of operation. This limitation occurs because in all these logic types transistors are driven into saturation, resulting in an increased propagation Delay time. This consideration prompts us to inquire whether a logic form becomes possible in which transistors are switched from cut-off to an operating point in the Active region.

One way of avoiding saturation in a digital circuit is found in the emitter coupled logic (ECL) circuit. These circuits exhibit the shortest propagation delay time of any of commercially available digital ICs. They also require the most power to operate.

6.2 Emitter Coupled Logic (ECL)

ECL is the fastest commercially available form of digital IC, with typical propagation delay time of less than 1ns and clock rates approaching 1GHz. The basis of all ECL circuit is the non-saturating current switch, shown in diagram 6.1.

High speed of operation results from the fact that the transistors operate between active and cut-off region instead of between saturation & cut-off region. The operation of an ECL

gate is dependent on a differential Amplifier. This configuration also termed as emitter coupled pair.

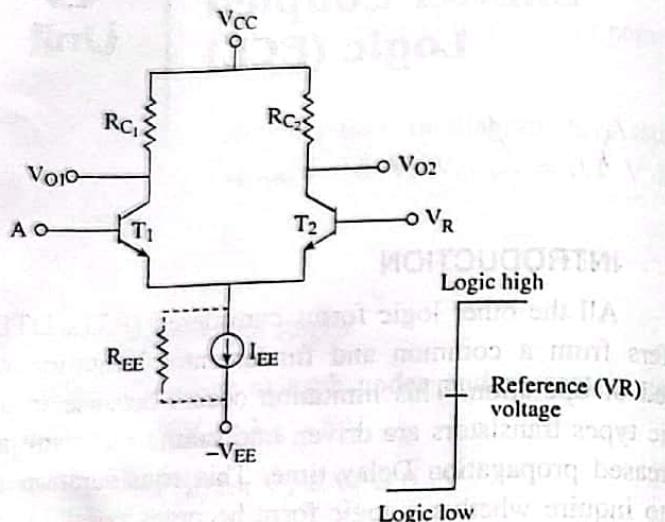


Fig. 6.1: Schematic of basic current switch (emitter coupled pair)

By a judicious choice of values for R_C and I_{EE} , the circuit designed so that the transistor in current switch do not saturate. This is one reason for the short propagation delay time typical to ECL gate.

If $V_A > V_R$, the transistor T₁ conducts, T₂ cut-off.

Output V_{O2} becomes high and V_{O1} becomes low.

If $V_A < V_R$, Then conduction Current changes from T₁ to T₂. Output, V_{O1} becomes high and V_{O2} becomes low.

The transistor that conducts is always in forward active mode so that transistor switch back and forth between cut-off and active states.

The ECL circuit operation basically exhibits

- A positive logic swing
 - Logic high as $-0.75V$ and logic low as $-1.55V$
 - Swing value as $0.8V$
 - Reference voltage is midway voltage between logic high & low i.e. $V_R = -1.175V$
-
- A graph showing a square wave voltage waveform. The top level is labeled "Logic high" at $-0.75V$. The bottom level is labeled "Logic low" at $-1.55V$. The midpoint between them is labeled "VR Reference voltage" at $-1.175V$.

Fig. 6.2:

6.3 AN ECL GATE

An ECL gate incorporating the basic structure is sown in diagram 6.3. The input transistor T₁ here parallel by a number of transistors to provide for multiple gate inputs.

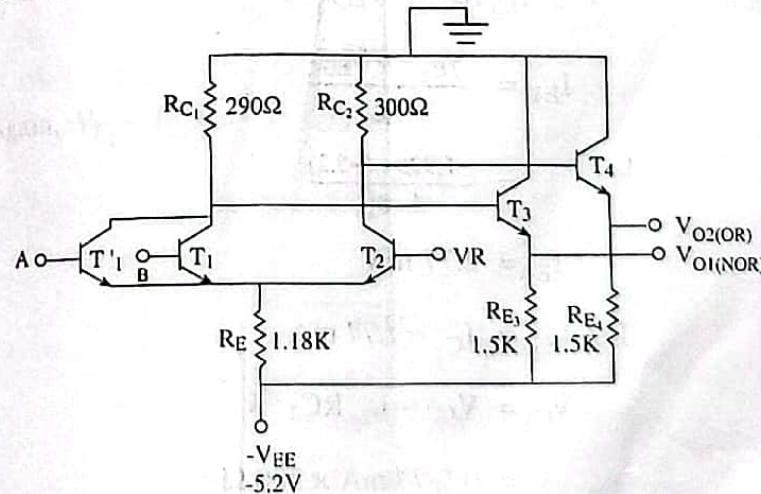


Fig. 6.3: An ECL gate

Outputs are taken at the collectors via emitters followers. The emitter followers provide buffering and low impedance at the output terminals. The collector resistors of the transistors are

grounded and emitter of transistors are connected to a negative supply voltage.

The circuit yields two complementary outputs which can be verified as accordingly.

Case I: When all inputs are at low.

All inputs transistors becomes at cut-off mode, but T_2 conducts. Calculating voltage at common emitter point.

From diagram applying KVL,

$$V_R - V_{BE(on)} - V_{E_2} = 0$$

$$\therefore V_{E_2} = V_R - V_{BE(on)}$$

$$= -1.175 - 0.75$$

$$= -1.925 \text{ Volt}$$

Again, $V_{E_2} - I_{E_2} R_E - (-V_{EE}) = 0$

$$I_{E_2} = \frac{V_{E_2} - (-V_{EE})}{R_E}$$

$$= \frac{-1.925 - (-5.2)}{1.18K}$$

$$I_{E_2} = 2.77 \text{ mA}$$

Let $I_{E_2} \approx I_{C_2} = 2.77 \text{ mA}$

$$V_{C_2} = V_{CC} - I_{C_2} R_{C_2}$$

$$= 0.277 \text{ mA} \times 300 \Omega$$

$$= -0.825 \text{ Volt}$$

Thus, computing both output

$$V_{O2(OR)} = V_{C_2} - V_{BE_4}$$

$$= -0.825 - 0.75$$

$$= -1.575 \text{ Volt (low)}$$

Similarly, $V_{O1(NOR)} = V_{C_1} - V_{BE_3}$

$$V_{O1(NOR)} = 0 - 0.075$$

$$= -0.75 \text{ (high)}$$

Case II: When at least any one input is at high.

The input transistor conducts but T_2 cut-off. Voltage at common emitter point can be computed as

From diagram applying KVL,

$$V_i - V_{BE(on)} - V_{E_1} = 0$$

$$V_i - V_{BE(on)} - V_{E_1} = V_i - V_{BE(on)}$$

$$\therefore V_{E_1} = -0.75 - 0.75$$

$$= -1.50 \text{ V}$$

Again, $V_{E_1} - I_{E_1} R_E - (-V_{EE}) = 0$

$$I_{E_1} = \frac{V_{E_1} - (-V_{EE})}{R_E}$$

$$= \frac{-1.50 - (-5.2)}{1.18K}$$

$$= \frac{-1.5 + 5.2}{1.18K}$$

$$= 3.13 \text{ mA (Approx)}$$

Let $I_{E_1} \approx I_{C_1} = 3.13 \text{ mA}$

$$V_{C_1} = V_{CC} - I_{C_1} R_{C_1}$$

$$= 0 - 3.13 \text{ mA} \times 290 \Omega$$

gate is dependent on a differential Amplifier. This configuration also termed as emitter coupled pair.

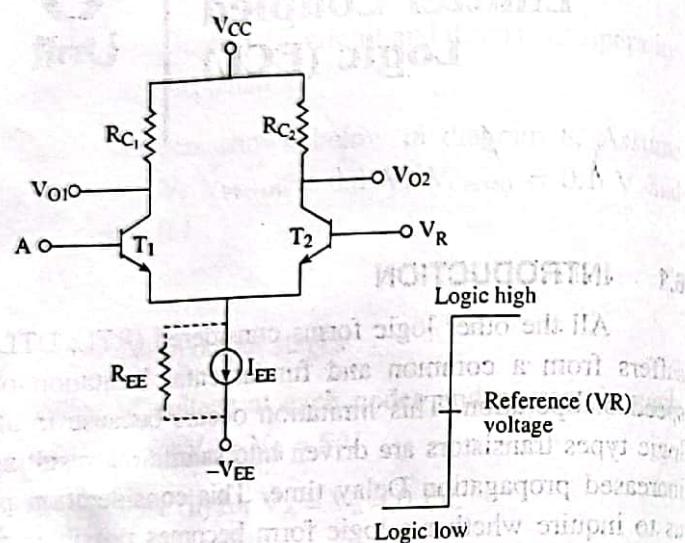


Fig. 6.1: Schematic of basic current switch (emitter coupled pair)

By a judicious choice of values for R_C and I_{EE} , the circuit is designed so that the transistor in current switch do not saturate. This is one reason for the short propagation delay time typical to ECL gate.

If $V_A > V_R$, the transistor T₁ conducts, T₂ cut-off.

Output V_{O2} becomes high and V_{O1} becomes low.

If $V_A < V_R$, Then conduction Current changes from T₁ to T₂. Output, V_{O1} becomes high and V_{O2} becomes low.

The transistor that conducts is always in forward active mode so that transistor switch back and forth between cut-off and active states.

The ECL circuit operation basically exhibits

- A positive logic swing
 - Logic high as $-0.75V$ and logic low as $-1.55V$
 - Swing value as $0.8V$
 - Reference voltage is midway voltage between logic high & low i.e. $V_R = -1.175V$
-
- A diagram showing the reference voltage VR. It consists of a vertical line with three points labeled: Logic high at $-0.75V$, VR Reference voltage at $-1.175V$, and Logic low at $-1.55V$.

Fig. 6.2:

6.3 AN ECL GATE

An ECL gate incorporating the basic structure is shown in diagram 6.3. The input transistor T₁ here parallel by a number of transistors to provide for multiple gate inputs.

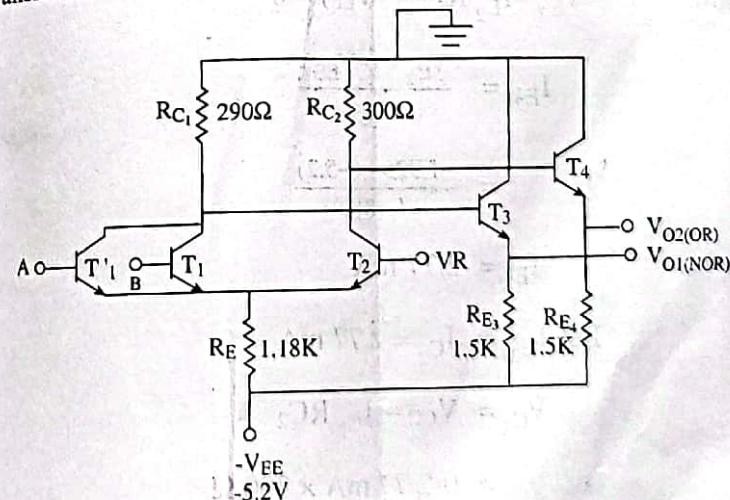


Fig. 6.3: An ECL gate

Outputs are taken at the collectors via emitters followers. The emitter followers provide buffering and low impedance at the output terminals. The collector resistors of the transistors are

grounded and emitter of transistors are connected to a negative supply voltage.

The circuit yields two complementary outputs which can be verified as accordingly.

Case I: When all inputs are at low.

All inputs transistors becomes at cut-off mode, but T_2 conducts. Calculating voltage at common emitter point.

From diagram applying KVL,

$$V_R - V_{BE(on)} - V_{E_2} = 0$$

$$\begin{aligned}\therefore V_{E_2} &= V_R - V_{BE(on)} \\ &= -1.175 - 0.75 \\ &= -1.925 \text{ Volt}\end{aligned}$$

$$\text{Again, } V_{E_2} - I_{E_2} R_E - (-V_{EE}) = 0$$

$$\begin{aligned}\therefore I_{E_2} &= \frac{V_{E_2} - (-V_{EE})}{R_E} \\ &= \frac{-1.925 - (-5.2)}{1.18K} \\ I_{E_2} &= 2.77 \text{ mA}\end{aligned}$$

$$\text{Let } I_{E_2} \approx I_{C_2} = 2.77 \text{ mA}$$

$$\begin{aligned}V_{C_2} &= V_{CC} - I_{C_2} R_{C_2} \\ &= 0 - 2.77 \text{ mA} \times 300 \Omega \\ &= -0.825 \text{ Volt}\end{aligned}$$

Thus, computing both output

$$V_{O2(OR)} = V_{C_2} - V_{BE_4}$$

$$= -0.825 - 0.75$$

$$= -1.575 \text{ Volt (low)}$$

$$\text{Similarly, } V_{O1(NOR)} = V_{C_1} - V_{BE_3}$$

$$V_{O1(NOR)} = 0 - 0.075$$

$$= -0.75 \text{ (high)}$$

Case II: When at least any one input is at high.

The input transistor conducts but T_2 cut-off. Voltage at common emitter point can be computed as

From diagram applying KVL,

$$\begin{aligned}V_i - V_{BE(on)} - V_{E_1} &= 0 \\ \therefore V_{E_1} &= V_i - V_{BE(on)} \\ &= -0.75 - 0.75 \\ &= -1.50 \text{ V}\end{aligned}$$

$$\text{Again, } V_{E_1} - I_{E_1} R_E - (-V_{EE}) = 0$$

$$\begin{aligned}\therefore I_{E_1} &= \frac{V_{E_1} - (-V_{EE})}{R_E} \\ &= \frac{-1.50 - (-5.2)}{1.18K} \\ &= \frac{-1.5 + 5.2}{1.18K} \\ &= 3.13 \text{ mA (Approx)}\end{aligned}$$

$$\text{Let } I_{E_1} \approx I_{C_1} = 3.13 \text{ mA}$$

$$\begin{aligned}\text{Now, } V_{C_1} &= V_{CC} - I_{C_1} R_{C_1} \\ &= 0 - 3.13 \text{ mA} \times 290 \Omega\end{aligned}$$

$$= -0.907 \text{ V (Approx.)}$$

Thus, computing both outputs

$$\begin{aligned} V_{O1(\text{NOR})} &= V_{C_1} - V_{BE_3} \\ &= -0.907 - 0.75 \\ &= -1.65 \text{ (low)} \end{aligned}$$

$$\begin{aligned} V_{O2(\text{OR})} &= V_{C_2} - V_{BE_4} \\ &= 0 - 0.75 \\ &= -0.75 \text{ V (High)} \end{aligned}$$

6.4 VOLTAGE TRANSFER CHARACTERISTICS

An ECL gate Yields two complementary outputs OR and NOR. Thus, its VTC is symmetric, except for low state at NOR output.

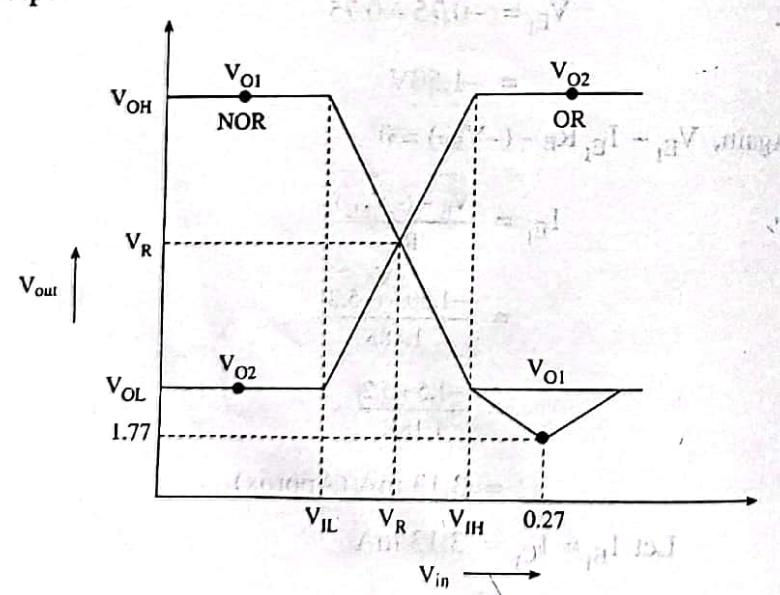


Fig. 6.4: Transfer characteristic of an ECL gate

Let us consider the condition in which input voltage gets increased above reference voltage. The collector current of T_1 increases and V_{CE_1} starts decreasing. With sufficient input voltage, T_1 will saturate.

Assuming $V_{CE(\text{sat})} = 0 \text{ V}$, T_1 enters into saturation.

Applying voltage divider rule at ECL gate

$$\begin{aligned} V_{E_1} &= V_{C_1} = V_{CC} - \frac{R_{C_1}}{R_{C_1} + R_E} [V_{CC} - V_{CE(\text{sat})} - (-V_{EE})] \\ &= -\frac{R_{C_1}}{R_{C_1} + R_E} V_{EE} \\ &= -\frac{290\Omega \times 5.2}{290 + 1.18K} \\ &= -1.02 \text{ Volt} \end{aligned}$$

Therefore, computing value at edge of saturation.

Form diagram of ECL gate

$$\begin{aligned} V_{in} &= V_{BE(\text{on})} + V_{E_1} \\ &= -1.02 + 0.75 \\ &= -0.27 \text{ V} \\ V_{O1} &= V_{C_1} - V_{BE(\text{on})} \\ &= -1.02 - 0.75 \\ &= -1.77 \text{ V} \end{aligned}$$

This point is indicated & shown in VTC. However, in the normal mode of operation, none of the transistor in the ECL circuit saturates, because the input do not rise higher than -0.7 Volt .

6.5 NOISE MARGIN

It is now of special interest to observe that the reference voltage and resistors in ECL gate have been selected such that the gate output voltage symmetrically straddle the input voltage transition region. We note that mean of output voltage is $\frac{1}{2}(-0.76 - 1.58) = -1.170V$.

This is very nearly equal to the reference voltage $V_R = -1.175 V$. As a result Noise margins are very nearly equal.

The output of a driving gate is $-0.76 V$ at logic 1. In order for driven gate to recognize an input as being at logic 1. This input must not be less than $-1.1V$.

Hence, Δ_1 noise margin is

$$\Delta_1 = -0.76 - (-1.1) = 0.34 V$$

Δ_0 Noise Margin is

Similarly,

$$\Delta_0 = -1.25 - (-1.58) = 0.33 V$$

It is to be noted that these Noise Margin are typical and not worst-case margins.

6.6 SPEED OF OPERATION

It is fact that of all gates ECL is the fastest. The speed of an ECL gate is adversely affected by capacitive loading. It is mainly due to the emitter follower used at gate outputs.

When base voltage of an emitter follower changes sharply in the direction to increase emitter current, the emitter follows. The capacitance at output charges very rapidly via low output impedance ($\approx 6 \Omega$ in MECL-II).

When input changes in reverse direction, the emitter voltage remains fixed momentarily due to the coupled capacitor. Since the base voltage has dropped, the emitter follower cuts off

and capacitance must discharge via relatively large emitter resistance ($1.5 K\Omega$).

If the capacitive loading is moderate, the discharge time won't be large. As the logic levels are separated by a voltage difference which is small in comparison with the separation between the logic levels and supply voltage.

e.g. Consider the OR output of ECL gate, let output is at high initially.

$$i.e. V_{O2(1)} = -0.76 V.$$

Now, transition occurred and output changes from logic high to logic low.

$$i.e. V_{O2(0)} = -1.58 V.$$

The time T required to make the transition between logic level can be shown to be

$$T = R C \ln \left[\frac{V_{O2(1)} - (-V_{EE})}{V_{O2(0)} - (-V_{EE})} \right]$$

Using the values given above, we find that

$$T \approx 0.2RC$$

If $C = 5 \text{ pF}$, then

$$T = 1.5 \text{ nsec}$$

However, It had seen that one can decrease the time $t_{pd(HL)}$ and t_f by shunting R_E with an external resistor but in expense of power dissipation.

6.7 ADVANTAGES & DISADVANTAGES OF ECL

Advantages:

- Operation in cut-off & active region without going into saturation makes ECL faster logic

- Due to differential Amplifier circuit input impedance is high and due to emitter follower O/P impedances is very low.
- Complementary outputs 'OR' & 'NOR' are available simultaneously.
- V_{CC} used as ground, which practically eliminates current spikes.
- Gate parameter do not degrade over a long periods due to temperature.

Disadvantages:

- Logic swing is small (0.8 V)
- Noise margin low.
- Power dissipation per gate is high.
- Level shifters require to interface with other logic family.
- Propagation delay gets increased by capacitive loading.

6.8 TEMPERATURE COMPENSATED BIAS SUPPLY

The transfer and other characteristic of ECL gates are temperature dependent, as with other gates. As we know, the value of noise margin, logic swing etc. depends on the reference voltage. Thus, any change in reference voltage ' V_R ' due to temperature, effect overall circuit behavior of gate. It is very essential that temperature must require to be used effectively to achieve compensated overall circuit behaviour properly.

The reference supply circuit below ensures also symmetry in logic level and stable transfer characteristics over a wide range of temperature.

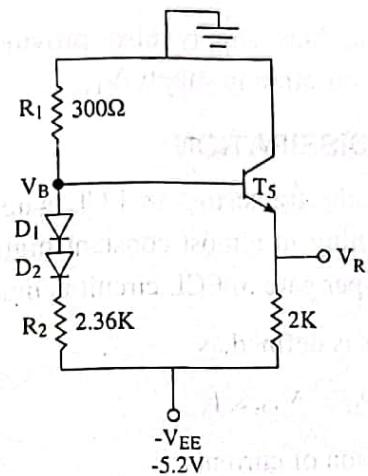


Fig. 6.5: Reference supply circuit ECL gate

Assuming that diodes D_1 and D_2 operates at a forward bias of 0.75 V at temp. $T = 25^\circ\text{C}$.

Computing base voltage of T_5 using voltage divider rule.

$$\begin{aligned} V_B &= \frac{R_1}{R_1 + R_2} [V_{EE} - VD_1 - VD_2] \\ &= -0.425 \text{ V} \end{aligned}$$

Again from diagram

$$\therefore V_B - V_{BE5} - V_R = 0$$

$$\begin{aligned} \therefore V_R &= V_B - V_{BE5} \\ &= -0.425 - 0.75 \\ &= -1.175 \text{ V} \end{aligned}$$

As temperature changes, the mid point of the range from logic 0 to logic 1, also changes by the same amount as ' V_R '. Since the V_R lies mid-way between the two output logic levels, independent of temperature variations, the noise margin Δ_0 and

Δ_1 are same. The bias supply also provides a measure of compensation for variation in supply V_{EE} .

6.9 POWER DISSIPATION

Since, All the transistors in ECL gate are operating in active mode, resulting in almost constant high supply currents. Power dissipation per gate in ECL circuit is much higher.

Power dissipations is defined as

$$P_D = V_{EE} \times I_S \quad \dots \dots \text{(i)}$$

where I_S – summation of currents

The power current in either of state is given by

$$I_S = I_E + I_{E_3} + I_{E_4} \quad \dots \dots \text{(ii)}$$

Since, outputs are at complementary state, $I_{E_3} + I_{E_4}$ is constant.

From diagram of ECL gate,

$$I_{E_3} = \frac{V_E - (-V_{EE})}{R_E} = \frac{V_E + V_{EE}}{R_E}$$

$$I_{E_3} = \frac{V_{E_3} - (-V_{EE})}{R_{E_3}} = \frac{V_{E_3} + V_{EE}}{R_{E_3}}$$

$$I_{E_4} = \frac{V_{E_4} - (-V_{EE})}{R_{E_4}} = \frac{V_{E_4} + V_{EE}}{R_{E_4}}$$

6.10 FAN-OUT

Since, the output current of the gate is from emitter followers and the input current to load gate is the base current of the non-saturating current switch transistors. Thus, there becomes parental of high Fan-out.

At low clock rate, the Fan-out is of order of I_E/I_B , that is the current gain βF , which is order of 100.

Also each load gate have a finite load capacitance which get charged & discharged as driving gate changes state i.e. when transition occurred. Hence, changing voltage at input of load gate takes time. In most applications, this limits the number of load gates or Fan-out to about 10.

6.11 MANUFACTURE'S SPECIFICATIONS

Typical manufacturer's specifications at $TA = 25^\circ\text{C}$ is illustrations in table below.

$$V_{OH}/V_{OL} = -0.9 \text{ V}/-1.7 \text{ V}$$

$$V_{IH}/V_{IL} = -1.2 \text{ V}/-1.4 \text{ V}$$

$$NMH/NML = 0.3 \text{ V}/0.3 \text{ V}$$

$$\text{Logic swing} = 0.8 \text{ V}$$

$$\text{Fan-out} = 10$$

$$\text{Power dissipation} = 24 \text{ mw}$$

Per gate

$$\text{Propagation delay} = 2 \text{ ns}$$

$$\text{Supply voltage} = -5.2 \text{ V}$$

6.12 LEVEL TRANSLATION

It is often necessary to interconnect two different logic systems such as ECL and TTL (DTL). One approach is to use time division multiplexing of M digital signal to form a single digital signal. Although the bit rate of each M signal may be handled using TTL, the bit rate of composite signal is M times faster and may require ECL to process it.

Basically, we deals with two types mentioned below:

- Saturated logic to ECL translation
- ECL to saturated logic translation

(a) Saturated logic to ECL Translation

The circuit of commercial unit used to translate term saturated logic to ECL is shown in diagram above.

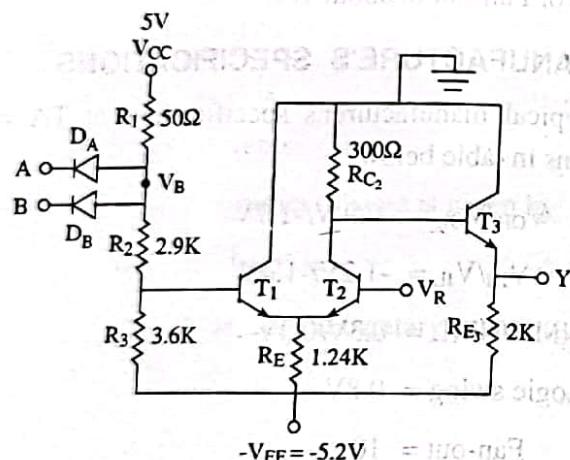


Fig. 6.6: Saturated logic to ECL translator

Basic Operation:

Case – I: When at least any one input is at low.

The input diode becomes forward biased and majority of current follows via it. This causes transistor T_1 to be at cut-off. Hence T_2 conducting.

Since, T_2 conducting path between V_{CC} (ground) and $-V_{EE}$ get established. Here, $V_{C_2} \approx V_{B_3}$ almost becomes negligible which makes T_3 to become at cut-off mode. Thus, output becomes at low.

Case II: When all Input are at high.

All input Diode becomes reversed biased and magnitude of current becomes sufficient enough to make T_1 'ON'. Thus T_2 becomes cut-off. Here, $V_{C_2} \approx V_{B_4}$ becomes sufficient enough to make T_3 'ON'. Thus, output becomes at high.

Thus, above circuit perform AND operation for Two or more than two inputs. $Y = AB$ verified from basic operation of circuit.

AB	Y
00	0
01	0
10	0
11	1

To make reference voltage ' V_R ' constant, the base of T_2 connected to temperature compensated biased supply circuit, so the overall circuit behavior maintained properly due to if any temperature change.

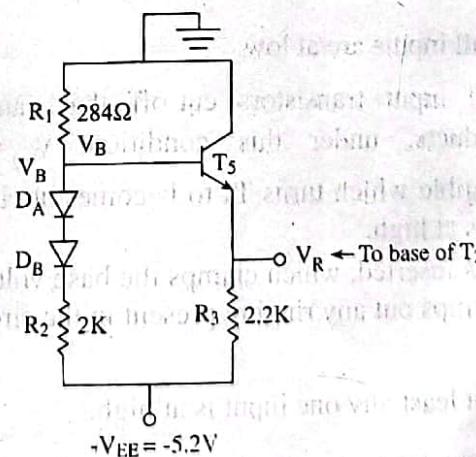


Fig. 6.7: Reference supply circuit

(b) ECL to Saturated Logic Translation

Level shifting from an ECL output to drive TTL inputs can be performed using the circuit illustrated in diagram 6.8. For two or more than two inputs, the circuit perform NOR function of ECL compatible signal while shifting output to TTL levels.

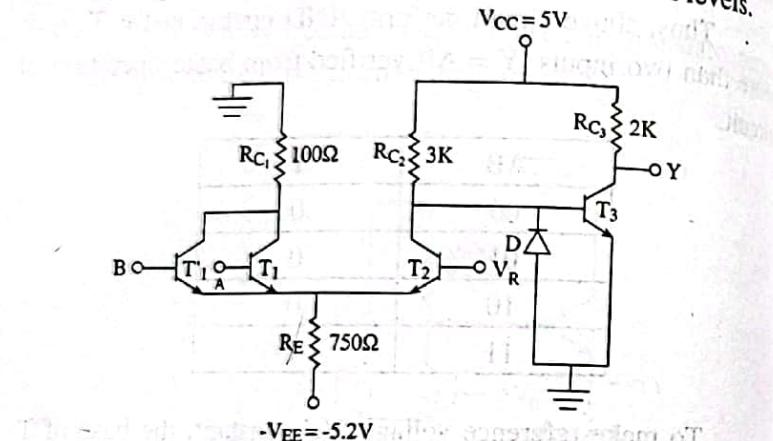


Fig. 6.8: ECL to saturated logic translator

Operation:

Case - I:

When all inputs are at low.

The all input transistors cut-off that causing T_2 to becomes conducts, under this condition $V_{C2} \approx V_{B3}$ almost becomes negligible which turns T_3 to becomes at cut-off. Thus, output becomes at high.

Diode is inserted, which clamps the base voltage of T_3 to -0.7 V and clamps out any ringing present in the circuit.

Case II:

When at least any one input is at high.

The input transistor conducts and T_2 becomes cut-off. Which result in saturation of transistor T_3 . Thus output becomes at low.

Truth Table

AB	Y
0 0	1
0 1	0
1 0	0
1 1	0

Thus, above circuit perform NOR operation i.e.

$$Y = \overline{A+B}$$

6.13 ECL-GATE INTERCONNECTIONS

Most often ECL gate interconnection required in various applications of digital circuit. A pair of wires a length of co-axial cable etc. used to make interconnection between terminal pairs must to be viewed as a length of transmission line.

The transmission line character of the interconnection makes itself especially apparent when the wave from encountered make transitions between levels in times which are comparable to time of propagation along the line. If transition time is longer than the time of propagation along the line, the line can be approximated by lumped circuit elements.

e.g. A transmission-line interconnection between gates is illustrated in diagram 6.9(a).

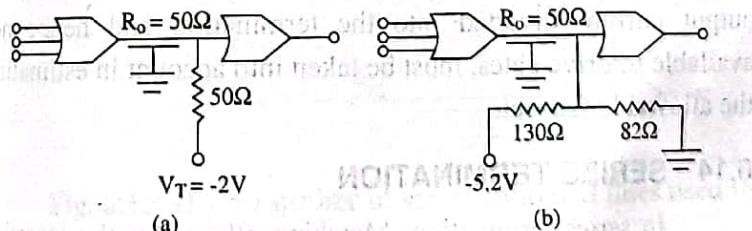


Fig. 6.9: (a) A matched transmission line inter connection between gates using an auxiliary supply voltage VT for termination (b) An arrangement which avoids the auxiliary voltage

Here a $50\ \Omega$ line and matching termination have been used. So far DC operation is concerned, one end of the terminating resistor is connected to the emitter of the output emitter follower of the driving gate. If this terminating resistor were larger, it would be allowable to return the other end to the -5.2 V supply. In such case, Terminating resistor connected in parallel with emitter resistor of the output emitter follower of the driving gate. Here small resistances of termination result in excessive current via output of emitter follower with consequent excessive dissipation in both transistor & termination.

To circumvent this difficulty, the terminating resistor is returned instead to an auxiliary terminating voltage $V_T(-2\text{ V})$ as illustrated in diagram 6.9(a). If return is not sufficient to justify a separate supply, the arrangement in diagram 6.9(b) may be used. This arrangement limits the current in the output emitter follower but at expense of considerable dissipation in the added resistors.

Finally, we may note that in fast ECL gates, where it is virtually certain that a terminating arrangement as in above diagram 6.9(a) & (b) will be used, the manufacturer will often omit using an emitter resistor in driving gate. At any event, the output current diverted into the termination and hence not available to drive gates, must be taken into account in estimating the allowable fan-out.

6.14 SERIES TERMINATION

In series termination, Matching allows for the insertion of an additional resistor R_s in series with output of driving gate as illustrated in diagram 6.10(a).

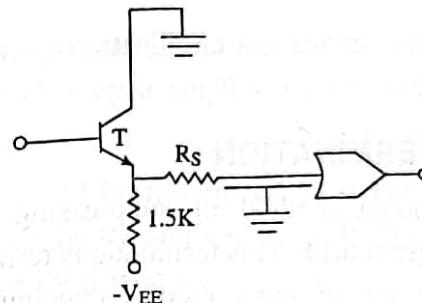


Fig. 6.10: (a) A line matched at its input end

Series matching has the advantage that no auxiliary supply voltage is required. On the other hand, series resistor limits the available output current and thereby restricts the fan-out to about 10.

When the series terminated line does not occur in the parallel terminated gate, difficulty arises.

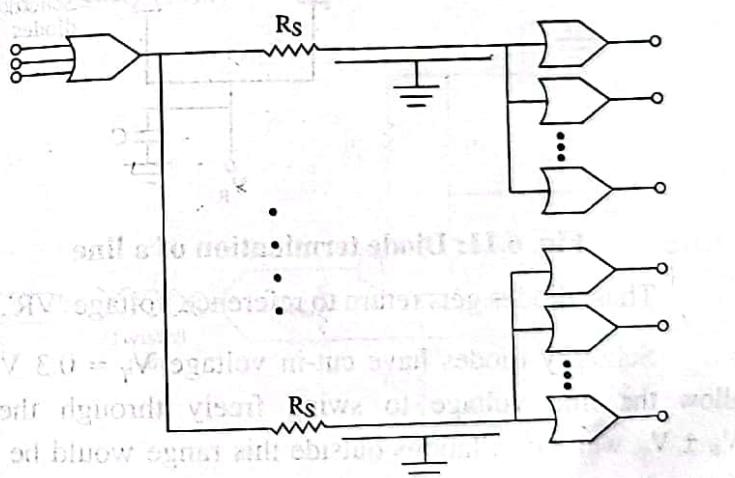


Fig. 6.10: (b) A number of series-matched lines used to accommodate a large fan-out

The difficulty can be relieved by arranging the spacing between driven gates to be small in comparison with spacing of gates from input side the line. When many driven gates must be

accommodated, the configuration illustrated in diagram 6.10 becomes effective.

6.15 DIODE TERMINATION

An additional method of suppressing oscillations is illustrated in diagram 6.11. This technique is termed as a natural extension of the use of input diodes, encountered earlier in connection with TTL gates. In above configuration such Schottky diodes are used and one have noted that the ECL levels symmetrically straddle the reference voltage.

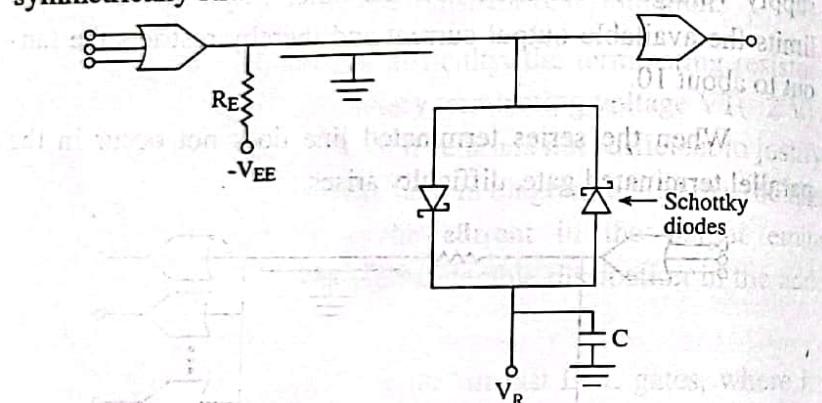


Fig. 6.11: Diode termination of a line

Thus, diodes gets return to reference voltage 'VR'.

Schottky diodes have cut-in voltage $V_y \approx 0.3$ V would allow the line voltage to swing freely through the range $V_R \pm V_y$, while oscillations outside this range would be sharply damped.

6.16 TWISTED PAIR LINES

The transmission line of ECL wave form used to face second difficulty like cross-talk, or unintended coupling of signals between circuits. When signals are transmitted with high

speed, A large magnitude signal might get coupled from one signal path to another by a small stray capacitance or mutual inductance.

Crosstalk could be minimized by using co-axial cables but such cables are bulky and certainly do not readily allow a distribution of taps for driven gates.

A feature of ECL gates which is of great use in suppressing crosstalk is the fact that gates have two outputs (OR and NOR) which are of opposite polarity. Whatever the change in voltage at one output, the change at the other output is equal and opposite as illustrated in diagram 6.12. The difference in output between OR and NOR output is transmitted over a twisted pair of wires to a difference amplifier. The difference amplifier acts as receiver.

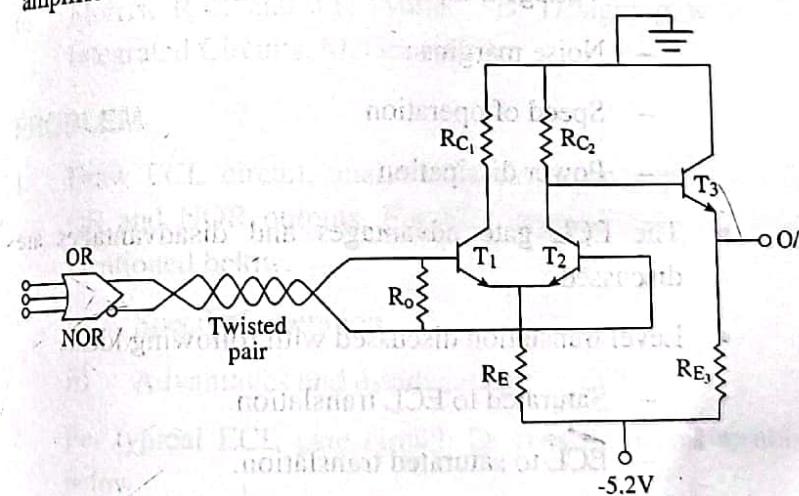


Fig. 6.12: Twisted pair transmission in ECL

The twisting of transmission wires keeps the wires together and also regularly reverses their relative positions. Thus, any signal path which might have induced in it, A signal from one of the wires in the pair may well be expected to have

an equal and opposite signal induced by other wire. Hence, crosstalk from the twisted pair to other signal paths may be expected to be minimal.

SUMMARY

This chapter provides discussion for emitter/coupled logic as largest logic family and some typical static and dynamic characteristics are presented analytically. For ECL gate specifically described parameters in details are:

- Typical ECL gate are discussed and related expressions are derived and values are computed analytically.
- For ECL gate important characteristics discussed are
 - Voltage transfer characteristics
 - Noise margins
 - Speed of operation
 - Power dissipation
- The ECL gate advantages and disadvantages are discussed.
- Level translation discussed with following ideas.
 - Saturated to ECL translation.
 - ECL to saturated translation.
- The ECL gate interconnections are discussed with following ideas.
 - Series termination
 - Diode termination
 - Twisted pair lines.

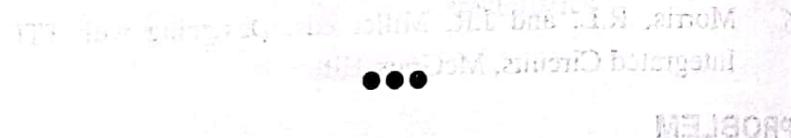
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PROBLEM

1. Draw ECL circuit, analytically derive an expression for OR and NOR outputs. For ECL gate, discuss the terms mentioned below.
 - i) Speed of operation
 - ii) Advantages and disadvantages of ECL
2. For typical ECL gate circuit. Discuss the terms mention below:
 - i) Voltage transfer characteristics
 - ii) Noise margin
 - iii) Fan-out
 - iv) Power dissipation

3. For an ECL gate, draw temperature compensated bias supply circuit and discuss its stable transfer characteristics over wide range of temperature.
4. For level translation, discuss the terms mentioned below.
 - i) Saturated logic to ECL translation.
 - ii) ECL to saturated logic translation.
5. Discuss ECL Gate interconnection and for ECL gate interconnection, discuss the terms mentioned below.
 - i) Series termination
 - ii) Diode termination
 - iii) Twisted pair lines



Integrated Injection Logic (IIL)

7
Unit

7.1 INTRODUCTION

Integrated Injection Logic (IIL) is the most recent logic system to be introduced to commercial application. IIL has the elegant simplicity of DCTL. A typical gate uses very little real estate and consumes very little power. For this reasons IIL is eminently suited for medium and large scale integration applications.

A family of bipolar logic circuit that challenges the MOSFET circuits in large scale integration (LSI) is IIL. This digital IC is designed around a multi-collector inverting transistor that operates in the Reverse or upside down mode.

7.2 INTEGRATED INJECTION LOGIC (IIL)

The circuits that have so far been described in this chapter are generally applicable for use in small scale (SSI) and medium scale (MSI) integrated circuits, but their use in large scale (LSI) integrated circuit is generally prohibited because of their relatively large area and power dissipation.

e.g. Even a modest 500 – gate array, designed with TTL (LS), would dissipate 1W of power and cover a surface area of 25mm^2 . This surface area is about maximum for a high yield IC, but the power dissipation is excessive.

The bipolar transistor answer to the challenge of MOSFETS in LSI is Integrated Injection Logic (IIL).

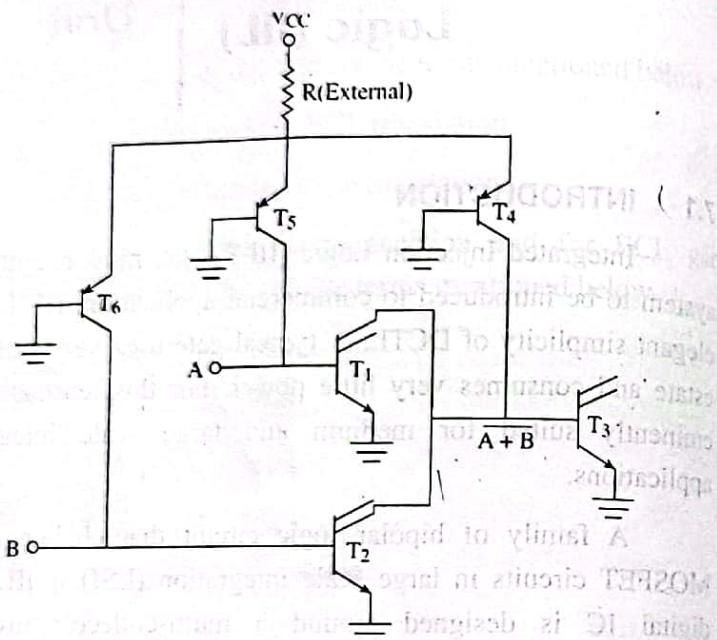


Fig. 7.1: Basic configuration of IIL

The basic structure of the IIL gate is a transistor with multiple collectors and a single emitter together with a mechanism for supplying base current is illustrated in diagram 7.1.

The operation performed is the NOR operation. Thus, if a collector of gate whose input A, is connected to a collector of a gate whose input is B and the joined collectors are in turn connected to the base of another gate i.e. T₃. The logic that appears at the base is $\overline{A+B}$.

Here, transistors T₁, T₂, T₃ are npn type having single base, single emitter and multiple collectors. Similarly, T₄, T₅ & T₆ are pnp type transistors. A single injector used to serve many transistors.

Input A applied at base of T₁ becomes \overline{A} at collectors output. Similarly, input B becomes \overline{B} at collector output of T₂. These \overline{A} , \overline{B} is provided as base of T₃.

Hence, based on Demorgan's Theorem,

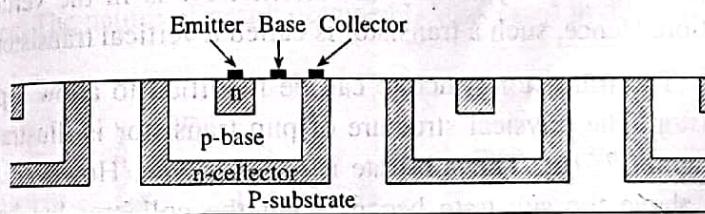
$$\overline{A} \cdot \overline{B} = \overline{A+B}$$

Thus, IIL circuit illustrated above perform NOR operation.

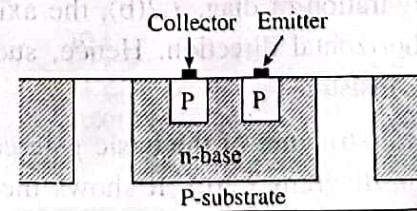
7.3 PHYSICAL LAYOUT OF IIL

To appreciate the features of IIL for its comparative merits, it becomes essential to study in details about the physical construction of an IIL integrated circuit. Thus, let us consider the matter in a simplified manner.

The physical structure of an integrate circuit npn transistor is illustrates in diagram 7.2(a). The substrate is a p-type silicon provide isolation from one transistor to another. The collector, base, emitters are n-type, p-type & n-type respectively.



(a)



(b)

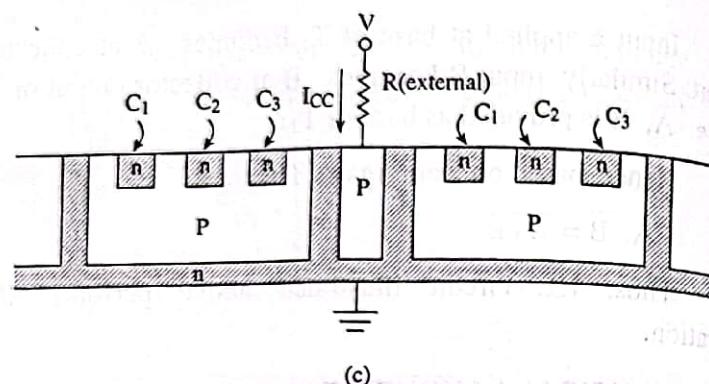


Fig. 7.2: (a) Physical structure of npn vertical transistor (b) physical layout structure of pnp lateral transistor (c) the physical structure of the basic gate configuration in IIL

Since, the base is very thin, very few of electrons injected into the base will be lost in base as a result of recombination. Finally, we note that the emitter is almost surrounded by the collector. Thus, an electron leaving the emitter, from no matter what point and in which direction, can hardly fail to reach the collector. In configuration of diagram 7.2(a), the axis of symmetry of current flow is in the vertical direction. Hence, such a transistor is called a vertical transistor.

The transistor structure can be modified to allow a pnp transistor. The physical structure of pnp transistor is illustrated in diagram 7.2(b). The substrate is again p-type. However, the layer above the substrate becomes not the collector but base. The emitter and collector are formed by p-type diffusions into the base. In configuration of diag. 7.2(b), the axis of symmetry of current is in horizontal direction. Hence, such transistor is termed as lateral transistor.

The physical structure of the basic gate configuration in IIL is illustrated in diagram 7.2(c). It shows the pnp transistor which supplies base current to the npn transistor. The p region marked "Injector" is the emitter of Transistor, its collector is the

p-type base of the npn transistor and its base is the n-type emitter of the npn transistor. Altogether the two transistors, one npn and one pnp, are formed with only four separated regions, the two transistors using two regions in common. For this reason IIL is also termed as merged - transistor logic (MTL).

It is noted that the pnp transistor via which base current is injected into the npn transistor as illustrated in diagram 7.2(c), serving two transistors on each side. Current I_{CC} is supplied for the injector from supply source V via an external resistor-R. A single injector used to serve many transistors, so that all injector current required by a single chip can be supplied via a single external resistor-R as indicated in diagram 7.2 (c).

7.4 ADJUSTABILITY OF SPEED

With different integrated circuit chip, different speeds are get associated. In IIL, it turns out that the trade off between speed and power can be effected on a single chip by a simple expedient of changing the current I_{CC} injected into the chip.

A normalized propagation delay time is plotted against I_{CC} . The nature of graph obtained is illustrated in diagram 7.3.

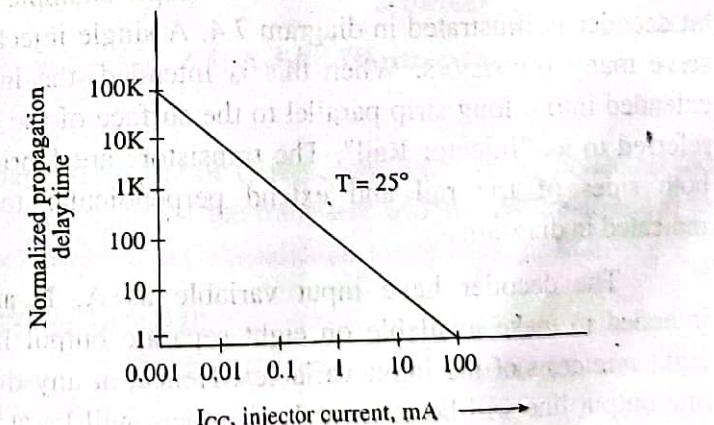


Fig. 7.3: Normalized propagation delay time versus injector current

Since, voltage at injector is constant, the input power is proportional to average input current I_{cc} .

At medium current levels the principal source of propagation delay is the need to establish and remove excess minority carrier base charge in the transistor. Here, propagation delay is independent of the current. In this current range, An increase in I_{cc} will increase the power dissipation without reducing delay.

At low current level the propagation delay time is principally the time required to charge junction and parasitic capacitors. Here propagation delay gets decrease at expense of a proportionate increase in dissipation.

At high current levels, the transistor turns into saturated mode. In saturation, the base charge increases more than in proportion to transistor current. Here, in this current range, an increase in I_{cc} will not only increase the dissipation but will also increase the delay.

7.5 AN IIL DECODER

IIL can be used as a decoder. A simple example of 3 to 8 bit decoder is illustrated in diagram 7.4. A single injector could serve many transistors. When this is intended, the injector is extended into a long strip parallel to the surface of the chip and referred to as "Injector Rail". The transistors are fabricated on both sides of the rail and extend perpendicular to rail as indicated in diagram.

The decoder have input variable as A, B and C is intended to make available on eight separate output lines, the eight minterms of the input variables. Hence, at any time, only one output line will be at logic 1, all others will be at logic 0. The line selected to be at logic 1 is determined by the logic levels of the inputs.

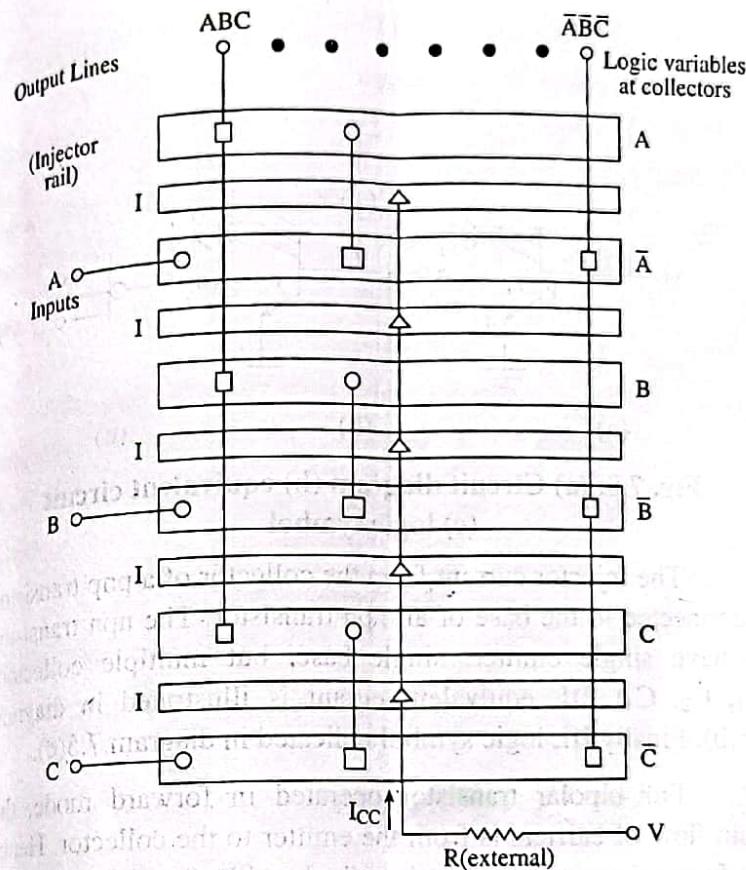


Fig. 7.4: A 3-bit IIL decoder

Here, the symbol ○-represent base, □-as collector and Δ-as injector current of the transistor which have be arranged to be parallel rather than perpendicular to the Injector Rail.

7.6 STANDARD IIL

There are three ways of drawing a basic IIL circuit as illustrated in diagram 7.5(a), (b), (c).

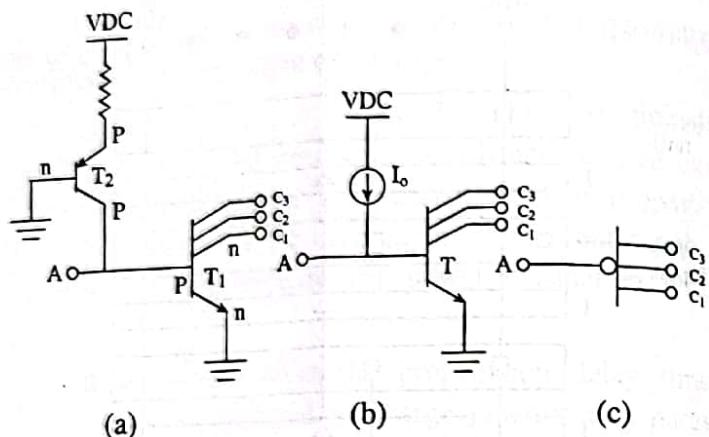


Fig. 7.5: (a) Circuit diagram (b) equivalent circuit
(c) logic symbol

The injector current from the collector of a pnp transistor is connected to the base of an npn transistor. The npn transistor T₁ have single emitter, single base, but multiple collectors (C₁, C₂, C₃). IIL equivalent circuit is illustrated in diagram 7.5(b). Finally IIL logic symbol indicated in diagram 7.5(c).

For bipolar transistor operated in forward mode, the main flow of carriers is from the emitter to the collector. Hence the forward current gain is described as β_D (beta down). Since the flow of carriers is down into the silicon.

But for the npn transistor in the IIL circuit, the forward current is β_U (beta up). Since the flow of carriers is now up to the surface of the silicon. Compared to normal connection β_D corresponds to beta forward (β_F), which is generally very large, while β_U is the same as beta reverse (β_R), which is usually rather small.

i.e.

$$\beta_D \equiv \beta_F \approx 100$$

$$\beta_U \equiv \beta_R \approx 5$$

7.7 VOLTAGE TRANSFER CHARACTERISTICS

The voltage transfer characteristics of a single inverter is determined only in a cascade of similar inverters. Then, since the output is directly connected to the input of load transistor, with the driving transistor 'OFF', $V_{out} = V_{BE(sat)}$. With the inverter transistor 'ON', $V_{out} = V_{EC(sat)}$

$$V_{OH} = V_{BE(sat)} = 0.8 \text{ V}$$

$$V_{OL} = V_{EC(sat)} = 0.1 \text{ V}$$

The transition width is from the transistor at the edge of conduction $V_{BE(EOC)}$ to the transistor at the edge of saturation $V_{BE(EOS)}$.

$$V_{IH} = V_{BE(EOS)} = 0.7 \text{ V}$$

$$V_{IL} = V_{BE(EOC)} = 0.6 \text{ V}$$

Using typical values,

$$NMH = V_{OH} - V_{IH} = 0.8 - 0.7$$

$$= 0.1 \text{ V}$$

$$NML = V_{IL} - V_{OL} = 0.6 - 0.1$$

$$= 0.5 \text{ V}$$

$$VLS = V_{OH} - V_{OL} = 0.8 - 0.1$$

$$= 0.7 \text{ V}$$

Operation with these low values is possible only because a complete digital system can be designed for a single chip.

7.8 FAN-OUT

To determine the Fan-Out of circuit, with an input in the high state, each collector of the inverting transistor must be capable of sinking the injector current I_o . Therefore the total collector current I_{CT} is expressed as

$$I_{CT} = NI_o \quad \dots \dots \text{(i)}$$

Where N-Number N of collectors

I_0 -Injector current

But the base current for the transistor is the injector current I_0 .

Thus, current gain of transistor is

$$\beta_U \geq \frac{I_{CT}}{I_B} = \frac{NI_0}{I_0} =$$

Hence, for circuit configuration, the current gain β_U restricts the number of collector N_{max} . of the multi collector transistor to be ≤ 5 . However the low Fan-out is not a serious limitation. Most IIL circuits are designed with from two to five collectors.

7.9 POWER DELAY PRODUCT

For IIL, Power dissipation is expressed as

$$P_D = V_{DC} \times I_0 \quad \dots \dots \text{(ii)}$$

Where V_{DC} -supply voltage (0.7 to 1V)

I_0 -Injector Current

Injector current can be changed by varying supply voltage or series resistance.

Increased I_0 causes faster switching of inverter transistor, but there is an increase in the power dissipation. However, the power delay product in IIL does remain constant over a very large range of injector currents, which is illustrated in graph 7.6.

Average propagation delay time is plotted against the average power dissipation. The dashed lines are for a constant power delay products of 0.1 PJ and 1.0 PJ. The solid lines represent the power delay products of production of micro processor unit using 8- μm design rule and a development using 5- μm design rule.

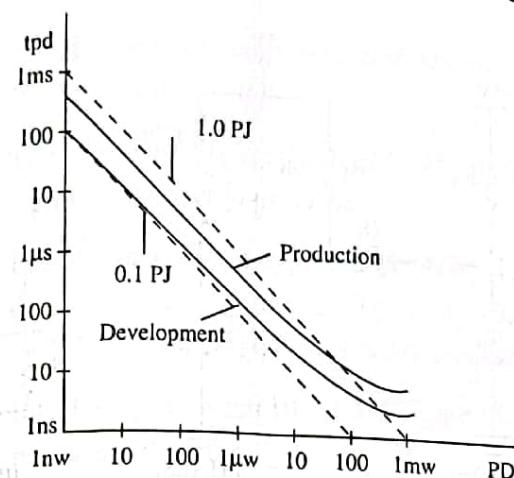


Fig. 7.6: Power delay product curves for production IIL and development IIL

At high I_0 (Injector current), The charge storage and bulk series resistance effects in the neutral base region of switching transistor limit the minimum value of propagation delay time

7.10 INTERFACING IIL AND TTL

The interfacing of IIL and TTL (LS) is very simple which is illustrated in diagram 7.7. Here, resistor RA can be 'ON' or 'OFF' the chip. The value of RA is made as large as possible, provided that the static and dynamic characteristic of the interface are met.

The static requirement is that in high state, V_{in} to LS circuit must be 2.7 V with $I_{IH} \leq 20 \mu A$.

The dynamic requirement is that in low state, the output transistor TA must be able to sink the receiver input current, but this is generally no problem, since for TTL (LS), $I_{IL} \leq 0.4 \text{ mA}$ with $V_{in} = 0.4 \text{ V}$.

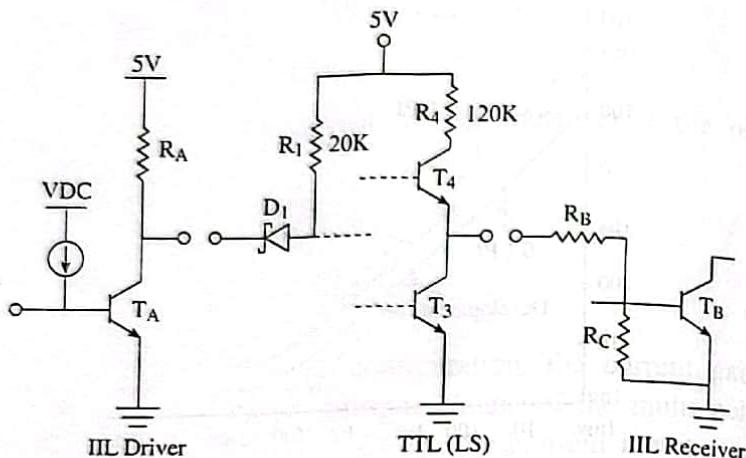


Fig. 7.7: Interfacing IIL and TTL

Driving an IIL gate from TTL (LS) also provide no problem. With the LS output in high state (≥ 2.7 V), the Thevenin's equivalent resistance of R_B and R_C must provide adequate drive to the IIL receiver input transistor T_B . With LS output in low state, the voltage divider ensures that T_B is 'OFF'. The values of R_B and R_C are as large as possible considering the speed of operation of the circuit.

SUMMARY

This chapter basically involve in discussion for IIL gate and corresponding physical structure and standard IIL gate. In addition to these, some typical characteristics and various other parameters specifically described in details are:

- Typical IIL gate circuits are discussed with current injector.
- For IIL gate, the physical layout are discussed

- An IIL decoder configurations are discussed with "Injector Rail".
- The standard IIL gate circuits are discussed with significance and importance.
- For IIL gate, some typical important characteristics discussed are: Voltage Transfer Characteristics (VTC), Fan-out (N), Power delay product.
- Interfacing between IIL and TTL are discussed with necessary diagram.

In the chapter the development of bipolar gate circuit are described and their principal static and dynamic characteristic are presented.

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PROBLEMS

1. Draw basic configuration of IIL circuit and discuss its operation with necessary explanation.
2. Discuss physical lay-out of IIL and explain the terms mentioned below.
 - i) Physical structure of npn vertical transistor.
 - ii) Physical structure of pnp lateral transistor
 - iii) Physical structure of IIL
3. Draw typical IIL NOR gate circuit with current injector and discuss IIL Physical lay-out and Explain why IIL is also termed as merged transistor logic?
4. Discuss IIL as decoder and draw 3-inputs to 8 outputs decoder configuration with injector Rail. Also construct decoder for
 - i) 2 inputs to 4 outputs.
 - ii) 4 inputs to 16 outputs.
5. Discuss standard IIL gate circuit, and for IIL discuss the terms mentioned below.
 - i) Voltage Transfer Characteristics
 - ii) Fan-out
 - iii) Power Delay Product
 - iv) Interfacing between IIL and TTL.

● ● ●

MOS Gates

**8
Unit**

Summary of MOSFET Equations:

Cut-off Region:

$$V_{GS} < V_T$$

$$I_D = 0$$

Ohmic/Linear Region:

$$V_{DS} \leq (V_{GS} - V_T) \text{ or, } V_{GD} \geq V_T$$

$$I_D = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

Saturation/Pinch off mode:

$$V_{DS} \geq (V_{GS} - V_T)$$

$$I_D = K (V_{GS} - V_T)^2$$

The constant K is given by

$$K = \frac{\mu \epsilon W}{2tL}$$

Where,

μ = Mobility of carriers in channel [Electrons in n – channel device]

ϵ = Dielectric constant of oxide insulating layer.

W = Channel Width.

L = Channel Length.

8.1 INTRODUCTION

The inverter is the basic circuit from which MOS logic circuits are developed. The MOS inverter exhibits all of the essential features of MOS logic gates except for logic function. DC and transient analysis and design techniques can be developed using the inverter as a vehicle.

In this chapter, the Analysis Techniques for DC voltage transfer characteristics, Noise Margins and propagation delay etc are discussed for NMOS circuits. Alternative load elements are compared, considering power consumption, circuit density, transfer characteristics and transient performance.

8.2 THE NMOS INVERTER

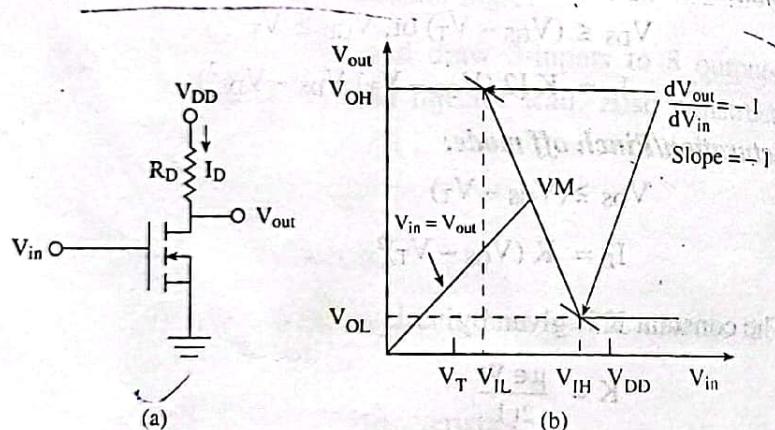


Fig. 8.1: Voltage transfer characteristics

NMOS Inverter circuit is illustrated in diagram 8.1(a) and its voltage transfer characteristics in diagram 8.1(b).

For input voltage ' V_i ' less than the threshold voltage ' V_T ' of the MOSFET, The device is at cut-off and output voltage ' V_o '

remains at V_{DD} . The nominal voltage repeating a logic high level is

$$V_{OH} = V_{DD} \quad \dots\dots (i)$$

As input voltage increases above the threshold voltage, The MOSFET starts conducting.

$$V_O = V_{DD} - I_D R_D \quad \dots\dots (ii)$$

At $V_{in} = V_{IL}$, the output voltage is near V_{DD} and the MOSFET is operating in the saturation region. i.e. As $V_{DS} > V_{GS} - V_T$, device becomes in pinch-off mode.

$$I_D = K (V_{GS} - V_T)^2 \quad \dots\dots (iii)$$

Substituting I_D in equation (ii)

$$V_O = V_{DD} - KR_D (V_{GS} - V_T)^2$$

$$\therefore V_O = V_{DD} - KR_D (V_i - V_T)^2 \quad \dots\dots (iv)$$

Differentiate equation (iv) with respect to (vi)

$$\frac{dV_O}{dV_i} = 0 - 2 KR_D (V_i - V_T) \left(\frac{dV_i}{dV_i} - 0 \right)$$

$$= 0 - 2 KR_D (V_i - V_T) (1 - 0)$$

$$= - 2 KR_D (V_i - V_T)$$

$$\therefore \frac{dV_O}{dV_i} = - 2 KR_D (V_i - V_T) \quad \dots\dots (v)$$

Equating slope $\frac{dV_O}{dV_i} = - 1$ at $V_i = V_{IL}$, equation (v) can be written as

$$- 1 = - 2 KR_D (V_{IL} - V_T)$$

$$\text{or, } V_{IL} - V_T = \frac{1}{2} KR_D$$

$$\therefore V_{IL} = V_T + \frac{1}{2 KR_D} \quad \dots \dots (\text{vi})$$

At $V_i = V_{IH}$, the output voltage is now near V_{DD} and MOSFET is operating in the linear region. i.e. As $V_{DS} < V_{GS} - V_T$, the device operating in ohmic/linear mode.

$$I_D = K [2(V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \dots \dots (\text{vii})$$

Substituting I_D in equation (ii)

$$V_O = V_{DD} - KR_D [2(V_{GS} - V_T) V_{DS} - V_{DS}^2]$$

$$\text{i.e. } V_O = V_{DD} - KR_D [2(V_i - V_T) V_O - V_O^2] \quad \dots \dots (\text{viii})$$

Differentiating equation (viii) with respect to V_O ,

$$\frac{dV_O}{dV_O} = 0 - KR_D \left[2 \frac{d(V_i, V_O)}{dV_O} - 2 V_T \frac{dV_O}{dV_O} - 2 V_O \frac{dV_O}{dV_O} \right]$$

$$\text{or, } 1 = -2 KR_D \left[V_i \frac{dV_O}{dV_O} + V_O \frac{dV_i}{dV_O} - V_T - V_O \right]$$

$$1 = -2 KR_D \left[V_i + V_O \frac{dV_i}{dV_O} - V_T - V_O \right]$$

$$\text{or, } V_O \frac{dV_i}{dV_O} + V_i - V_T - V_O = -\frac{1}{2 KR_D}$$

$$\text{or, } V_O \frac{dV_i}{dV_O} = V_T + V_O - V_i - \frac{1}{2 KR_D}$$

$$\text{or, } \frac{dV_i}{dV_O} = \frac{V_T + V_O - V_i - \frac{1}{2 KR_D}}{V_O}$$

$$\therefore \frac{dV_O}{dV_i} = \frac{V_O}{V_T + V_O - V_i - \frac{1}{2 KR_D}} \quad \dots \dots (\text{ix})$$

Equating slope $\frac{dV_O}{dV_i} = -1$ at $V_i = V_{IH}$, equation (ix) becomes

$$-1 = \frac{V_O}{V_T + V_O - V_{IH} - \frac{1}{2 KR_D}}$$

$$\text{or, } V_{IH} + \frac{1}{2 KR_D} - V_T - V_O = V_O$$

$$\therefore V_{IH} = V_T + 2V_O - \frac{1}{2 KR_D} \quad \dots \dots (\text{x})$$

The output low level, V_{OL} is the output voltage of an identical inverter load. The MOSFET assumed to be in the linear range of its V-I characteristics under this conditions.

To compute V_{OL} , from equation (viii)

$$V_O = V_{DD} - KR_D [2(V_i - V_T) V_O - V_O^2]$$

For low output above, equation can be written as

$$V_{OL} = V_{DD} - KR_D [2(V_{DD} - V_T) V_{OL} - V_{OL}^2] \quad \dots \dots (\text{xi})$$

V_{OL} is small, so V_{OL}^2 can be neglected.

$$V_{OL} = V_{DD} - KR_D [2(V_{DD} - V_T) V_{OL} - V_{OL}^2]$$

$$\therefore V_{OL} + 2KR_D [(V_{DD} - V_T)] V_{OL} = V_{DD}$$

$$\therefore V_{OL} [1 + 2KR_D (V_{DD} - V_T)] = V_{DD}$$

$$\therefore V_{OL} = \frac{V_{DD}}{[1 + 2KR_D (V_{DD} - V_T)]} \quad \dots \dots (\text{xii})$$

An additional point on VTC that is often useful is the mid point voltage V_M at which $V_{in} = V_{out} = V_{GS} = V_{DS}$ for which the MOSFET is in saturation.

$$V_M = V_{DD} - K_R D (V_M - V_T)^2$$

Knowing different values, different parameters can be computed as accordingly.

$$\begin{aligned} NMH &= V_{OH} - V_{IH} = 5 - 2.6 \\ &= 2.4 \text{ V} \end{aligned}$$

$$\begin{aligned} NML &= V_{IL} - V_{OL} = 1.25 - 0.3 \\ &= 0.95 \text{ V} \end{aligned}$$

$$\begin{aligned} VLS &= V_{OH} - V_{OL} = 5 - 0.3 \\ &= 4.7 \text{ V} \end{aligned}$$

$$\begin{aligned} VTW &= V_{IH} - V_{IL} = 2.6 - 1.25 \\ &= 1.35 \text{ V} \end{aligned}$$

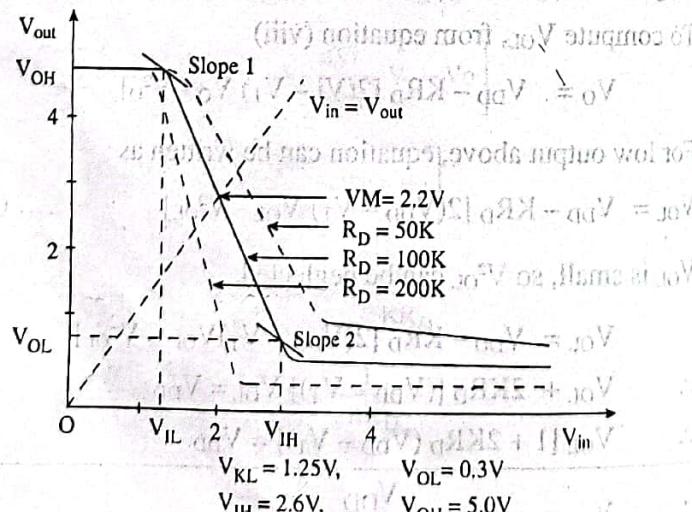


Fig. 8.2: MNOS inverter, Resistor load

The graphical approach to determine critical points on VTC is illustrated in above diagram 8.2. This much information is all that is required to define voltage levels and Noise margins for NMOS gate.

PROPAGATION DELAY

8.3

When input changes from V_{OH} to V_{OL} , the inverter transistor turn-off while load current is flowing. The time required for V_{out} to change from V_{OL} to the 50% point can be calculated by assuming the lumped load capacitance is charged by a constant current equal to the average current via load device.

The appropriate average capacitor charging current I_{LH} (avg) is obtain by averaging load current at $V_{out} = V_{OL}$ and at $V_{out} = \frac{(V_{OH} + V_{OL})}{2}$.

The propagation delay time is computed as

$$\Delta t = \frac{C \Delta V}{I(\text{avg})} \quad \dots \dots \text{(i)}$$

In this specific case,

$$t_{PLH} = \frac{CL(V_{OH} - V_{OL})/2}{I_{LH}(\text{avg})} \quad \dots \dots \text{(ii)}$$

Now, when input changes from V_{OL} to V_{OH} , both the inverter and load devices are conducting. Thus, current available to discharge the load capacitance from V_{OH} to the 50% point is the difference between two currents. These currents computed separately for each device at V_{OH} and at 50% point. The two net currents at end points are used to obtain I_{HL} (avg).

$$t_{PHL} = \frac{CL(V_{OH} - V_{OL})/2}{I_{HL}(\text{avg})} \dots \dots \text{(iii)}$$

The average Propagation Delay

$$t_p = \frac{t_{PLH} + t_{PHL}}{2} \dots \dots \text{(iv)}$$

8.4 POWER DISSIPATION

Power dissipation:

- Static Power Dissipation
- Dynamic power Dissipation

The static power dissipation at logic low output is

$$P_{D(s)} = V_{DD} \times I_D \dots \dots \text{(i)}$$

$$I_D = K [2(V_i - V_T) V_{OL} - V_{OL}^2] \dots \dots \text{(ii)}$$

The static power dissipation at logic high output is negligible, because inverter MOSFET becomes cut-off thus negligible current thereby negligible power.

The dynamic power dissipation is the power dissipation during output transitions. This arises in charging & discharging the load capacitance C_L in each cycle of input clock pulse. It is significant in high clock rates i.e. when the input clock period 'T' is comparable to $(T_{PHL} + T_{PLH})$. The energy transferred to C_L during the charging interval is given by $\frac{1}{2} C_L V_{LS}^2$, which is also energy discharged by C_L .

Average dynamic power dissipation in each period is

$$P_D(d) = \frac{C_L V_{LS}^2}{T}$$

With frequency of operation $f = \frac{1}{T}$, and $V_{LS} \approx V_{DD}$.

$$P_{D(d)} = f C_L V_{DD}^2 \dots \dots \text{(ii)}$$

8.5 DELAY POWER PRODUCT

Since, the propagation delay is proportional to the logic swing and load capacitance, $V_{LS} \approx V_{DD}$. The static delay power product of an NMOS inverter is expressed as

$$D_{P(s)} = kdp C_L V_{DD}^2 \dots \dots \text{(i)}$$

Where kdp is constant which depends on the inverter circuit configuration. For resistive load

$$kdp \approx \ln(2)$$

The dynamic delay power product is

$$D_{P(d)} = tpf C_L V_{DD}^2$$

$$\text{If, } f\text{-max} = \frac{1}{t_{PLH} + t_{PHL}} = \frac{1}{2tp}$$

$$D_{P(d)} = \frac{1}{2} \frac{f}{f\text{-max}} C_L V_{DD}^2 \dots \dots \text{(ii)}$$

The dynamic delay power product increases with frequency of switching.

From equation (i) & (ii)

$$D_P = kdp C_L V_{DD}^2 + \frac{1}{2} \frac{f}{f\text{-max}} C_L V_{DD}^2$$

$$D_P = C_L V_{CC}^2 \left[kpd + \frac{1}{2} \frac{f}{f\text{-max}} \right]$$

8.6 FAN-OUT

With virtually no Input (gates) currents drawn by load, An NMOS inverter can drive any numbers of identical circuit without degradation in logic levels under static condition. Each load inverter presents a significant gate capacitance at output of driving gate. Hence switching response of driver deteriorates with large number of gates.

8.7 NMOS AS NAND GATE

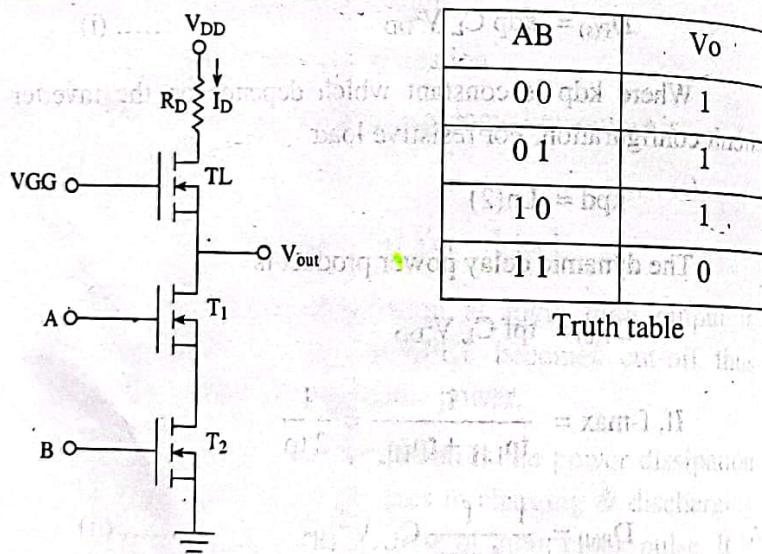


Fig. 8.3: NMOS NAND gate

NMOS as NAND gate is illustrated in diagram 8.3. Here V_{DD} , V_{GG} , V_T are all positive. Logic '0' is represented by the voltage less than the threshold voltage and logic '1' by a voltage above the threshold voltage.

Operation

Case I: When at least any one input is at low i.e. below threshold - voltage.

Under this conditions, The path between V_{DD} and ground not get established. Hence output becomes at high.

Case II: When all inputs are at high i.e. above Threshold voltage.

Under this condition MOSFET TL, T_1 , T_2 all are conducting. The path between V_{DD} and ground gets established. Hence output become at low.

Additional input can be provided by including additional MOSFET in series, that increases drop across series MOSFET so that it is necessary to decrease the drop, to make the total drop well below V_T to ensure the output a logic '0'. This is achieved by increasing W/L ratio to reduce the resistance of the channel.

8.7 NMOS AS NOR GATE

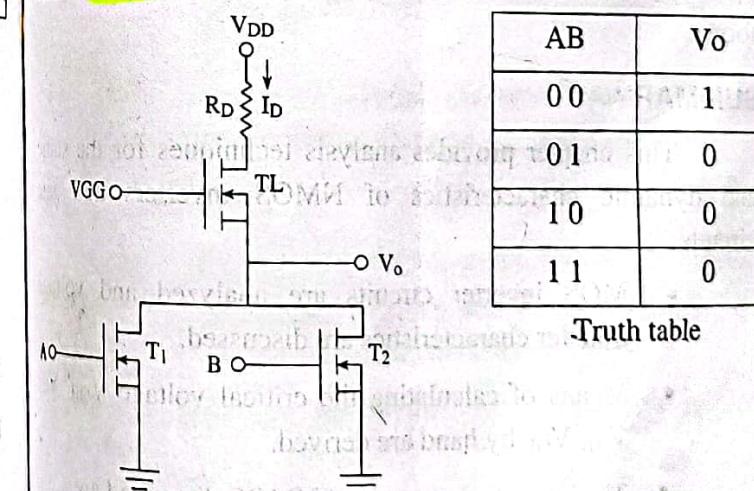


Fig. 8.4: NMOS NOR gate

The circuit of NMOS as NOR gate is illustrated in diagram 8.4. Here also V_{GG} , V_{DD} , V_T are all positive.

Operation:**Case I:**

When all inputs are at logic low i.e. below Threshold voltage.

Under this condition MOSFET T_1 , T_2 , cut-off and only MOSFET T_L conducting. Hence, output becomes at high.

Case II:

When at least any input at logic high i.e. above Threshold.

The MOSFET conducts having high input and path between V_{DD} and ground gets established. Hence output becomes at low.

Here also an additional MOSFET T_L connected with T_1 and T_2 . Truth table of NOR gate is represented in diagram above.

SUMMARY

This chapter provides analysis techniques for the static and dynamic characteristics of NMOS inverters and gate circuits.

- MOS inverter circuits are analyzed and voltage transfer characteristics are discussed.
- Means of calculating the critical voltage V_{OH} , V_{OL} , V_{IH} , V_{OL} by hand are derived.
- The important concept of NMOS discussed are
 - Propagation delay
 - Power dissipation
 - Delay power product

- Fan out
- NMOS NAND & NOR gate

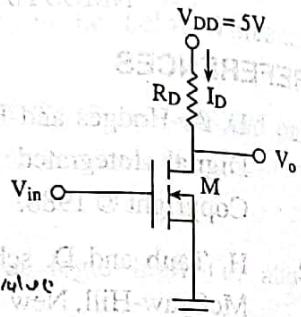
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PROBLEMS

1. Draw NMOS inverter circuit with resistive load. Derive an expression for V_{OH} , V_{OL} , V_{IL} and V_{IH} and indicates critical points on voltage transfer characteristics.
2. For NMOS inverter circuit, discuss the terms mentioned below.
 - a) Propagation delay
 - b) Power dissipation
 - c) Delay power product
 - d) Fan-out

3. Draw NMOS NAND and NOR gate circuit and explain its operation with truth table.
4. For a resistive load NMOS inverter shown in diagram 4 below with $R_D = 10 \text{ k}$, $V_{DD} = 5 \text{ V}$, $K = 20 \mu\text{A}/\text{V}^2$, $V_T = 1.0\text{V}$.
- a) Calculate V_{OH} , V_{IL} , V_{IH} , and V_{OL}
- b) Calculate NMH , NML , V_{TW} and V_{LS} .
- c) Find average power dissipated, if $f = 1000 \text{ Hz}$, and $C_L = 0.5 \text{ F}$.



Complementary Metal Oxide (CMOS)

**9
Unit**

9.1 INTRODUCTION

CMOS is rapidly becoming the most favored because of its lower power dissipation, shorter propagation delay and shorter rise and fall time.

In this chapter, the analysis techniques for DC voltage transfer characteristics, Noise Margins and propagation delay etc are discussed for CMOS circuits.

9.2 CMOS INVERTER

A CMOS inverter is illustrated in diagram 9.1(a) and its VTC in diagram 9.1 (b). The gate of PMOS upper device is connected to the gate of NMOS lower device.

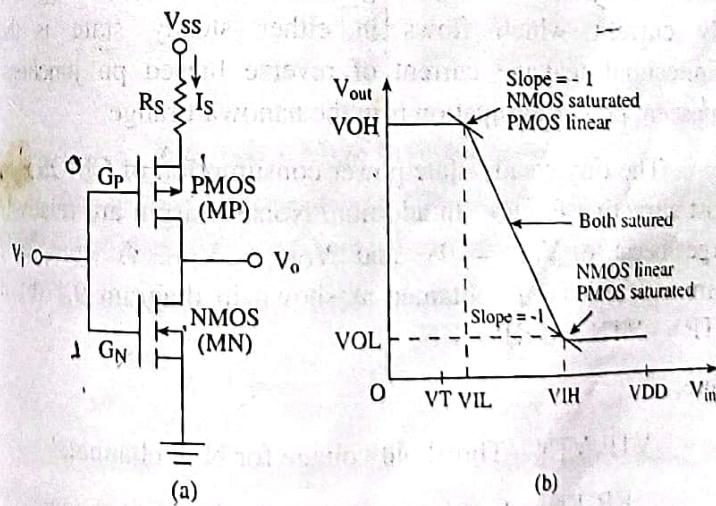


Fig. 9.1: (a) CMOS inverter (b) VTC

The wide popularity of CMOS technology is due to its virtually zero static power dissipation and large Noise margins in either logic states. CMOS can operate over a range of power supply voltage and at relatively high speed.

Here, input voltage V_i controls the gate bias for both MN & MP. Hence neither one drives the other; instead each device operates in a mode complementary to other. For perfectly matched MN & MP i.e. both having the same conduction parameter, the CMOS inverter operation is as follows.

Case I: When V_i is at low.

The NMOS is cut-off while the PMOS device is conducting, so V_{out} is very close to V_{DD} i.e. output becomes at high.

Case II: When V_i is at high.

The NMOS device is conducting while PMOS device is cut-off. Thus, out-out becomes at low.

We see from the above that in either state, one transistor in the series path from V_{DD} to ground is non-conducting. The only current which flows in either steady state is the infinitesimal leakage current of reverse biased pn junctions. Quiescent power dissipation is in the nanowatt range.

The tiny steady-state power consumption of CMOS is its most attractive feature. In addition, Noise Margin are relatively large because $V_{OL} = 0V$ and $V_{OH} = V_{DD}$. A completely symmetrical VTC is obtained as shown in diagram 9.1 (b). If $V_{TP} = -V_{TN}$ and $K_P = K_N$.

Here,

V_{TP} , V_{TN} – Threshold voltage for N, P channel.

K_P , K_N – Conduction parameter for N, P channel

TRANSIENT ANALYSIS OF CMOS INVERTER

9.3 The transient Analysis of CMOS inverter is illustrated in diagram 9.2. It shows the NMOS in a P type well, with the PMOS formed in the n-type substrate. The well always be more heavily doped than substrate, because it must be formed by overcompensating the initial substrate doping concentration. Thus, capacitances per unit area are higher for device formed in wells.

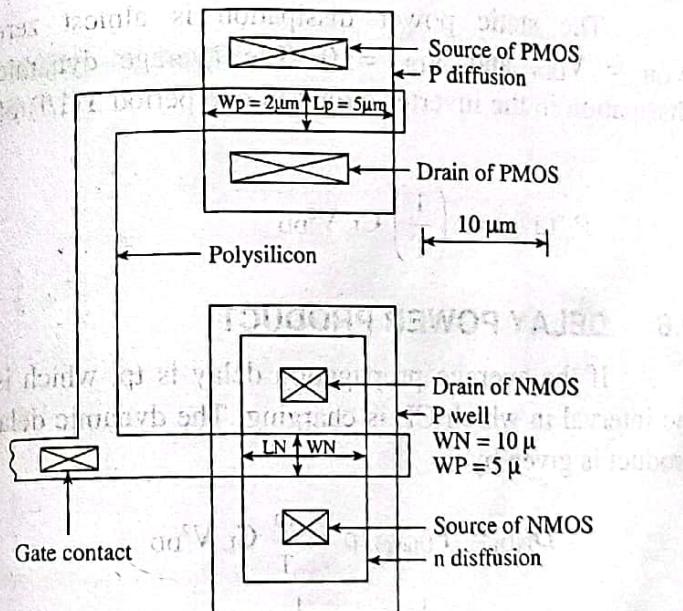


Fig. 9.2: CMOS inverter layout

For a near-minimum size CMOS inverter, the channel length L and width W are typical as indicated in diagram 9.2.

To obtain approximately equal values of K_P & K_N

$$\frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N} \quad \dots\dots (i)$$

This equality is often desired in order to obtain equal rise and fall times when driving capacitive loads.

9.4 FAN-OUT

Under static condition, A CMOS inverter has practically no limit in driving CMOS inputs. The dynamic fan-out is limited by the allowable propagation delay in an application. CMOS inverter fan out is usually limited to 10 to prevent excessive delay at output.

9.5 POWER DISSIPATION

The static power dissipation is almost zero, since $V_{OH} = V_{DD}$, and $V_{OL} = 0$. The average dynamic power dissipation in the inverter circuit in one period $T(1/f)$ of a clock is

$$P_D(\text{avg}) = \left(\frac{1}{T} \right) C_L V_{DD}^2$$

9.6 DELAY POWER PRODUCT

If the average propagation delay is tp , which is approx the interval in which C_L is charging. The dynamic delay power product is given by

$$D_{P(D)} = P_{D(\text{avg})} tp = \frac{tp}{T} C_L V_{DD}^2$$

$$\text{Using, } f\text{-max} = \frac{1}{2tp} \quad \& \quad f = \frac{1}{T}$$

The above equation becomes

$$D_{P(D)} = \frac{1}{2} \left[\frac{f}{f \text{ max}} \right] C_L V_{DD}^2$$

9.7 PROPAGATION DELAY

The charging of C_L via the PMOSFET device & discharging via NMOSFET device contribute to via to delays tp_{LH} to tp_{HL} .

$$tp_{LH} = \frac{C_L}{2 k_p [V_{DD} - |VTP|]} \left[\frac{2|VTP|}{V_{DD} - |VTP|} + \ln \frac{3V_{DD} - 4|VTP|}{V_{DD}} \right]$$

$$tp_{HL} = \frac{C_L}{2 k_n [V_{DD} - |VTN|]} \left[\frac{2|VTN|}{V_{DD} - |VTN|} + \ln \frac{3V_{DD} - 4|VTN|}{V_{DD}} \right]$$

The propagation delay

$$tp = \frac{tp_{LH} + tp_{HL}}{2}$$

9.8 CMOS AS NAND GATE

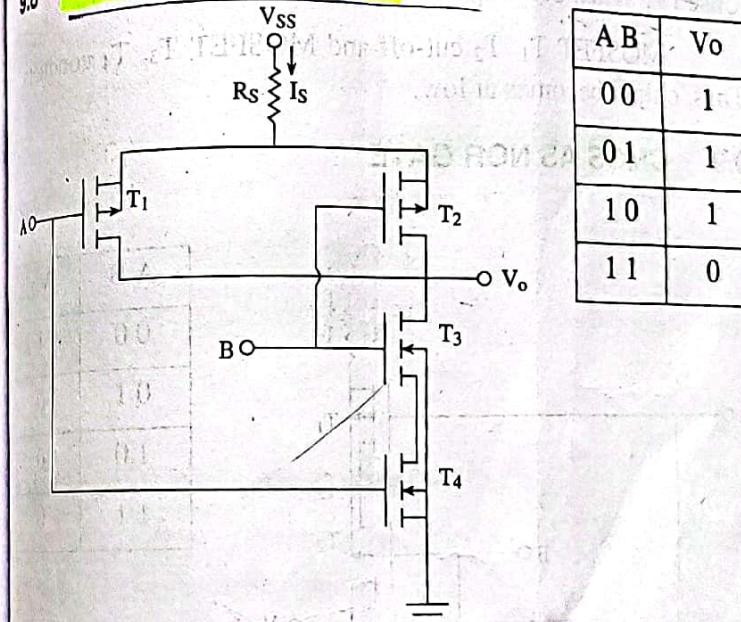


Fig. 9.3: CMOS as NAND gate

CMOS NAND gate is illustrated in diagram 9.3. Input A applied at Gate of T_1 & T_4 while input B at gate of T_2 & T_3 .

Operation:

Case I: When both input at low.

MOSEFT T₁ & T₂ conducting but MOSFET T₃ & T₄ becomes at cut-off. Hence output becomes high.

Case II: When input A at low & B at high.

MOSFET T₁, T₃ conducts and MOSFET T₂, T₄ cut-off. Hence output becomes at high.

Case III: When input A at high & B at low.

MOSFET T₁, T₃ becomes cut-off and T₂, T₄ conducts. Hence output becomes at high.

Case IV: When both inputs A and B at high.

MOSFET T₁, T₂ cut-off and MOSFET T₃, T₄ conducts. Thus, output becomes at low.

9.9 CMOS AS NOR GATE

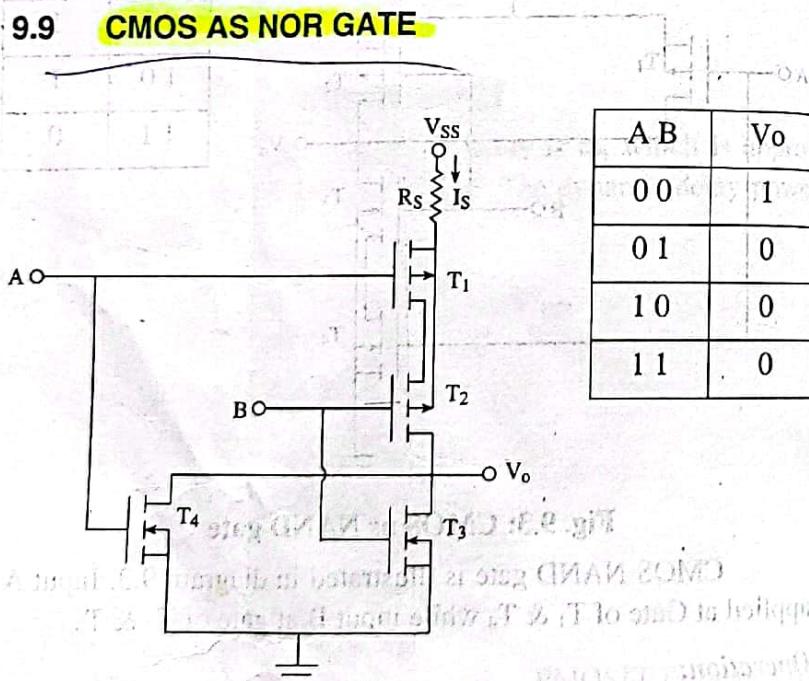


Fig. 9.4: CMOS NOR gate

A CMOS NOR gate is illustrated in diagram 9.4. Input A is Applied to gate of T₁ & T₄ and input B at gate of T₂ & T₃.

Operation:

Case I: When both input is at low.

MOSFET T₁, T₂ conducts and T₃, T₄ cut-off. Thus output becomes at high.

Case II: When input A is at low and B at high.

MOSFET T₁, T₃ conducts but T₂, T₄ cut-off. Hence output becomes at low.

Case III: When input A at high and B at low.

MOSFET T₂, T₄ conducts but T₁, T₃ cut-off. Hence output becomes at low.

Case III: When both input are at high.

MOSFET T₁, T₂ cut-off but T₃, T₄ conducts. Thus output becomes at low.

9.10 MANUFACTURE'S SPECIFICATIONS

Typical Manufacture's specification of CMOS inverter gate is listed out in Table below.

$$V_{OH}/V_{OL} = 4.99/0.01 \text{ V}$$

$$V_{IH}/V_{IL} = 3.5/1.5 \text{ V}$$

$$NMH/NML = 1.5 \text{ (approx)}/1.5 \text{ (approx)}$$

$$\text{Fan-out} = 10$$

$$tpd(LH) = 30 \text{ ns}$$

$$tpd(HL) = 30 \text{ ns}$$

$$t_r = 60 \text{ ns}$$

$$t_f = 60 \text{ ns}$$

Power dissipation = 50 nW

(Low power CMOS unit)

Propagation delay = 20 ns

(High speed CMOS)

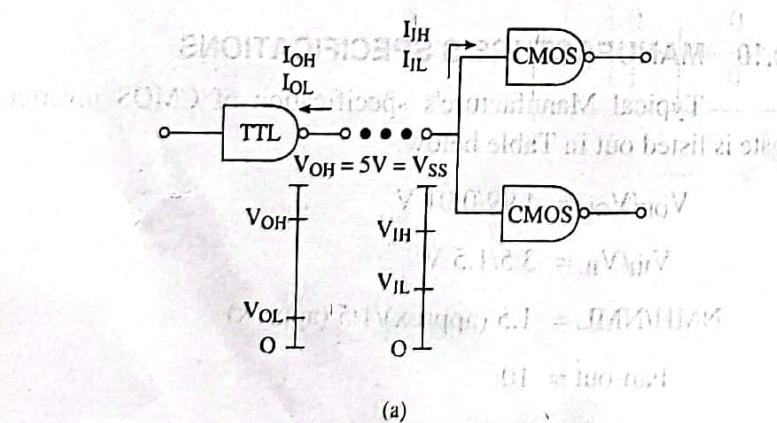
Supply = 5 Volts.

$$I_{OH}/I_{OL} = -0.5 \text{ mA}/0.4 \text{ mA}$$

$$\frac{I_{IH}}{I_{IL}} = \frac{10\text{PA}}{-10\text{PA}}$$

9.11 INTERFACING BJT AND COMOS GATES

Let us consider the Interfacing between TTL logic and CMOS logic. This is most common interfacing employed since TTL gates are the most often used logic gates. TTL as well as CMOS operates from +5 V.



(a)

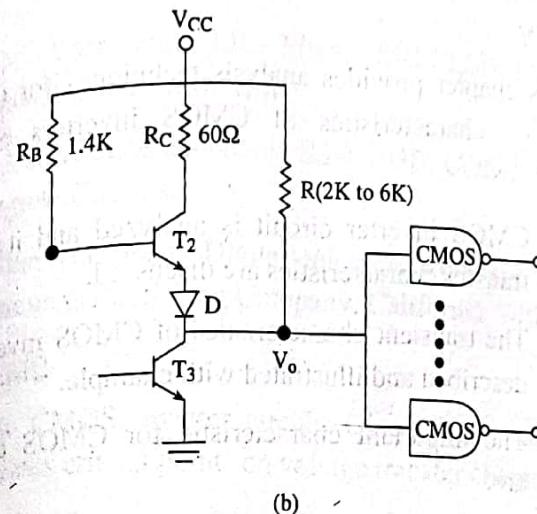


Fig. 9.5: (a) TTL driving NCMOS gates (b) TTL with passive pull up

Let us consider first the case of a TTL gate driving N-COMS gates as illustrated in diagram 9.5 (a). To operate such an arrangement having fan-out N successfully. It must require that

$$-I_{OH} (\text{TTL}) \geq N I_{IH} (\text{CMOS})$$

$$I_{OL} (\text{TTL}) \geq -N I_{IL} (\text{CMOS})$$

$$V_{OL} (\text{TTL}) \leq V_{IL} (\text{CMOS})$$

$$V_{OH} (\text{TTL}) \geq V_{IH} (\text{CMOS})$$

As it is readily verified from data and thus satisfied for any reasonable Fan-out N.

A frequently employed circuit modification used to raise V_{OH} (TTL) above 3.5 V is shown in diagram 9.5 (b), where an external resistor R has been bridged between V_{CC} and output. Typically R in the range 2 to 6 k.

SUMMARY

This chapter provides analysis techniques for the static and dynamic characteristics of CMOS inverters and gate circuits.

- CMOS inverter circuit is analyzed and its voltage transfer characteristics are discussed.
- The transient characteristics of CMOS inverters are described and illustrated with example.
- The important characteristic for CMOS discussed are:

- Fan-out
- Power dissipation

- Delay power product
- Propagation delay

- The design of NAND and NOR gate based on CMOS inverter is explained.
- Typical manufactures specifications and concept of interfacing BJT and CMOS gate are introduced & discussed.

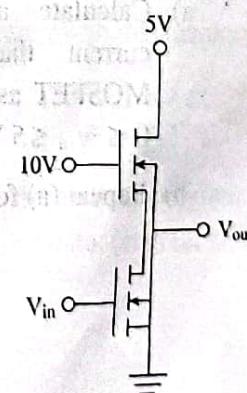
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6. Haldun Hazendar, Digital microelectronics - Benjamin/Cummings Publishing Company, California, 94065.

PROBLEMS

1. Draw CMOS inverter circuit. Discuss its operation and indicates critical points on voltage transfer characteristics.
2. For CMOS inverter, discuss the terms mentioned below.
 - a) Transient analysis for CMOS inverter.
 - b) Fan-out
 - c) Power dissipation
 - d) Delay power product
 - e) Propagation delay
3. Draw CMOS NAND and NOR gate and discuss its operation with the help of truth table.
4. For linear load inverter shown in diagram 4 below, the load device has $W/L = 1$.
 - a) Select W/L ratio of inverting transistor for $V_{OL} = 0.3$ V.
 - b) Find V_M (the point at which $V_{in} = V_{out}$) if W/L of inverter = 30, Neglect body effect.



In static RAM, the stored information's retained on it as long as the supply is 'ON'. Static RAM is faster than Dynamic RAM. Static RAM consume comparatively more power and are more expensive. CMOS Static RAM recommended for medium size of memory.

Dynamic RAM loses its content in a very short time even though the power supply is 'ON'. It stores data in the gate to source capacitor of Transistor. Due to leakage charge on these stray capacitors leaks away after a few milliseconds. Therefore, D-RAM has to be periodically refreshed usually every 2 milliseconds. It consumes less power and are cheaper. D-RAM used where large size of memory required.

10.5 READ ONLY MEMORY (ROM)

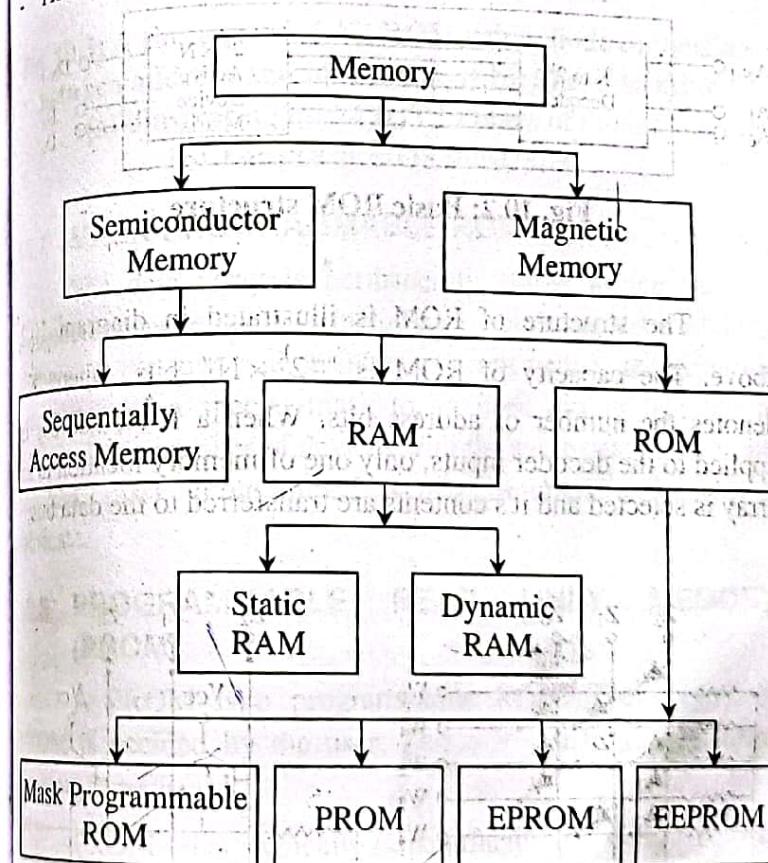
It is read only memory which is non-volatile in nature and it is used for permanent storage. It also posses Random Access Property. It contains Assembler, compiler, debugging program or any other permanent program. ROM widely used for function tables (sine, cosine, square root, logarithm, exponentials etc.), code conversion tables, multiplication, and division subroutines etc. In ROM, data bits are stored once during the chip fabrication using a process called Masking. Data stored in ROM at the time of manufacturing. The user can't write into ROM. It is not accessible.

Types of ROM

- Mask programmable ROM
- PROM
- EPROM
- EEPROM

Applications of ROM:

- Code conversion
- Look up Table
- Sequence generators
- Seven segment display
- Combinational logic Implementation.
- As a Multiplier etc.



10.6 BASIC ROM STRUCTURE

As name implies, a Read Only Memory (ROM) stores information that can be read. ROM is a combinational circuit

that consists of an array of semiconductor device such as diodes, BJT, MOS, which are interconnected to store any array of binary data, thereby realizing a prescribed set of function of same set of inputs. ROM are also random access memory with fixed data stored in all address. ROM'S are typically used in computer system for storing monitor programme and routines to run during interrupts.

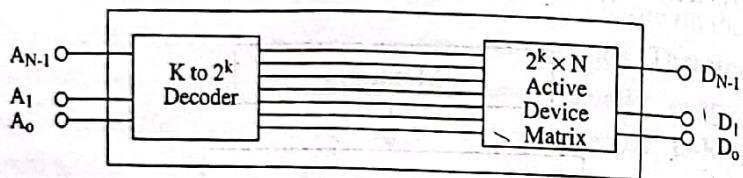
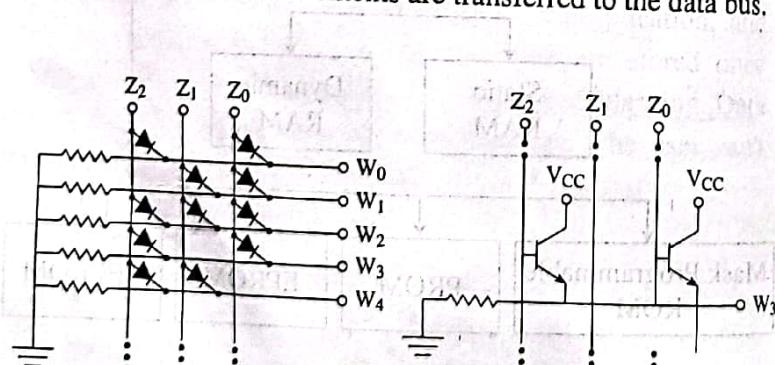
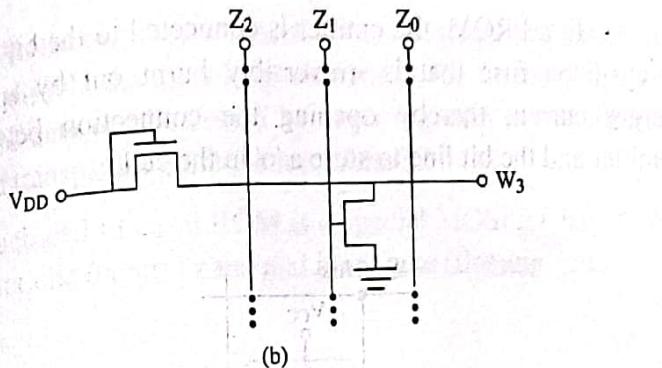


Fig. 10.2: Basic ROM structure

The structure of ROM is illustrated in diagram 10.2 above. The capacity of ROM is " $2^k \times N$ " bits, where 'K' denotes the number of address bits. When a K-bit address is applied to the decoder inputs, only one of memory location in an array is selected and its contents are transferred to the data bus.



(a)



(b)

Fig. 10.3: A three word, 5-bit ROM using diode connection
 (a) illustrating use of BJT in place of diodes
 (b) The use of MOS illustrated

10.7 MASK PROGRAMMABLE ROM

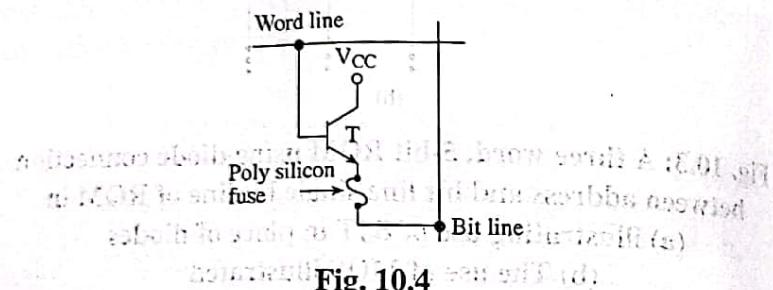
The data array is permanently stored at the time of manufacture by selectively including or omitting the switching elements at the row-column intersection of matrix, requiring the preparation of a special mask to be used during fabrication. Unless a large number of devices with the same data patterns are required, mask programmed ROMs becomes expensive to fabricate.

10.8 PROGRAMMABLE READ ONLY MEMORY (PROM)

A PROM is a programmable ROM. The content of PROM is decided by the user. The user can write permanent program in a PROM.

PROM is typically manufactured using bipolar technology, all switching elements are present in the matrix, with the connection at each intersection made by means of fusible link. These links are selectively burnt out by the user by means of PROM programmer in order to store data permanently.

In a PROM, the emitter is connected to the bit line via a polysilicon fuse that is irreversibly burnt out by applying a larger current thereby opening the connection between the emitter and the bit line to store a '0' in the cell.



Field programmable ROM offer user programmability at lower cost than mask programmed ROMs. Both the mask and field programmable ROMs have one serious limitation. A single incorrect bits of information make the entire IC useless. Moreover, it is often necessary to modify the stored data during the design cycle of the digital system.

10.9 EPROM

An EPROM is an erasable PROM. Usually, the content of memory erased by exposing EPROM to high intensity short wave ultraviolet light for 10 to 20 minutes. An UV source with wavelength of 2537 \AA is used for this purpose. The user cannot erase the content of a single memory location but in fact entire contents are erased.

The most widely used form of erasable programmable ROM is based on the special MOS device structure illustrated in diagram 10.5. The input voltage to the control gate is applied to the floating gate through a thin insulating layer of oxide.

EPROM employs a special charge storage mechanism to enable to disable the switching element in the memory matrix. Any stored data can be erased by exposing chip to intense UV light via a transparent lid at the top of the IC.

Each cell in an EPROM is a special MOSFET having 2-gates, outer one (control gate) and inner gate (floating gate).

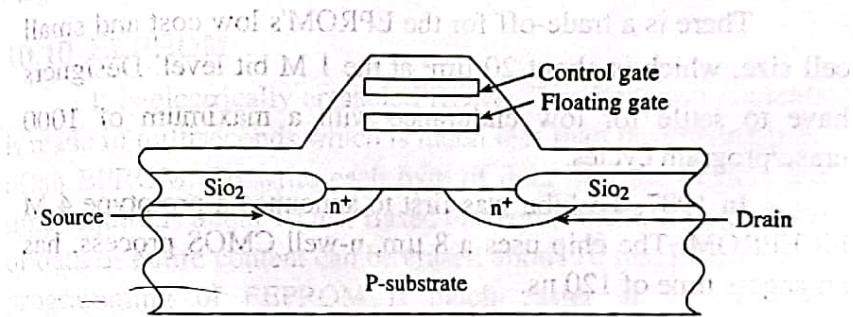


Fig. 10.5: MOS erasable programmable read only memory

When floating gate is left unchanged, the control gate acts as regular gate of N-channel MOSFET and MOSFET will conduct when its gate is energized causing storing '0'.

The floating gate MOSFET can be made non-conducting by forcing negative charges onto its floating gate. This is performed during write operation by grounding the source and energizing the drain to high voltage (16 to 20 V) and control gate to somewhat higher potential (25 to 28 V) voltage. Under this condition a conduction channel get established between drain and source.

Some of electrons traveling might migrate via the oxide layer of floating gate so negative charges get accumulates on floating gate. That causes the increase in threshold voltage of the device. Hence when floating gate holds charges, the device will not conduct. When its gate is energized, the logic '1' becomes available at data line.

The charge stored on floating gate of an EPROM device will remain on it for extremely long period of time. The charge on floating gate MOSFET can be removed by shining ultra-violet light of correct wave length on the floating gate. Electrons trapped on the floating gate acquire sufficient photon energy from UV light to overcome the inherent energy barrier of the oxide layer and relax back to the substrate.

There is a trade-off for the EPROM's low cost and small cell size, which is about $20 \mu\text{m}^2$ at the 1 M bit level. Designers have to settle for low endurance with a maximum of 1000 erase/program cycles.

In 1987, Toshiba was first to announce a prototype 4 M bit EPROM. The chip uses a $8 \mu\text{m}$, n-well CMOS process, has an access time of 120 ns.

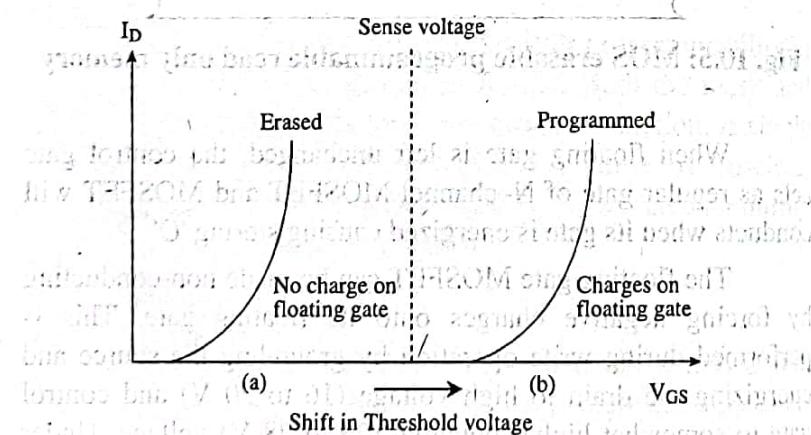


Fig. 10.6: Shifting in characteristics curve of the FAMOS due to programming

Before this is programmed, there is no charge on the floating gate and device operates as a regular n-channel enhancement MOSFET, exhibiting the transfer characteristics illustrated in diagram 10.6 (a), in which V_T is comparatively low. This state is termed as erased state.

The programming or writing is done by avalanche injection of hot electrons from the substrate via isolating oxide. To make device relatively easy to fabricate, oxide thickness maintained as 1000 \AA . Higher potential applied at control gate and between drain & source as already explained. Electrons accrete via channel. The transfer characteristic is illustrated in diagram 10.6 (b). This state is termed as programmed state.

10.10 EEPROM

It is electrically erasable PROM. The change in contents is made in milliseconds which is much less than the erasing time of an EPROM. To write each byte of data into the device, the time required is about 10 ms. Based on requirement, a single byte of data or entire content can be erased about 10 ms. Erasing and programming of EEPROM is much easier as compare to EPROM.

The metal nitride oxide semiconductor (NMOS) structures yielded the first nonvolatile memory that was called electrical alterable ROMs or EAROMs. It is illustrated in diagram 10.7.

A nitride layer is placed on top of the gate oxide and the tunneled electrons are retained at the oxide-nitride interface. On application of positive gate voltage, Electrons tunnel via thin oxide layer and captured by traps at the aforementioned interface to become stored charges. The threshold voltage shift due to stored charge. Device remains at higher V_T state corresponding to a logical '1' until a reverse gate voltage is applied to erase the memory and return device to lower V_T to represent '0'.

Disadvantage of first generation:

- Data disturbance during Read operation and loss of data overtime.

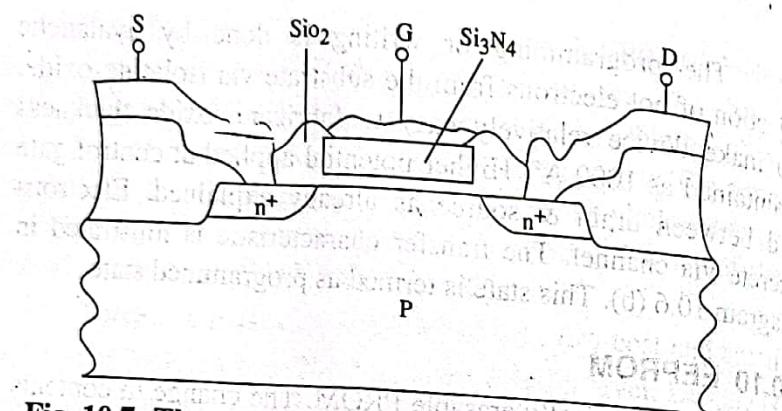


Fig. 10.7: The cross section of MNOS device used in first generation EAROMs

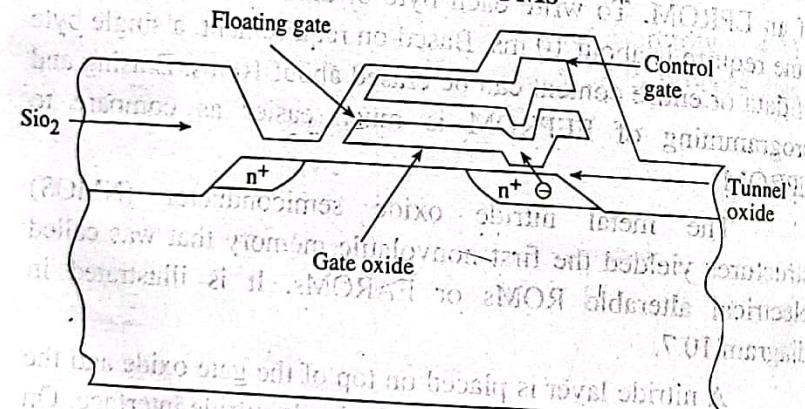


Fig. 10.8: Thin oxide double polysilicon E²PROM

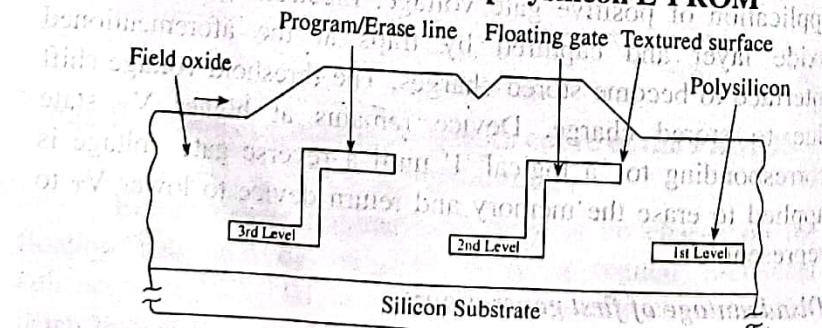


Fig. 10.9: Cross section of textured-surface triple poly E²PROM

- Require multiple supply

- Address and data require to be stable for entire cycle lasting up to 40 ms.

- Programmable only after an entire memory array or at least one page electrically erased.

The second generation thin oxide EEPROM stored data by trapping charge on floating gates using a transistor structure that resembled FAMOS used in EPROM is illustrated in diagram 10.8. This structure improves the data integrity as compared to MNOS parts. The programming or erasure of EEPROM cell requires the application of a large reversible gate field of around 10^7 V/cm on a thin gate oxide of about 100 \AA separating floating gate from the substrate. This field must be strong enough to produce a measurable current via thin oxide. At the same time, the field in interpoly silicon oxide must maintain at relatively low value to prevent unwanted transport of electrons between floating and control gates.

Programming is accomplished by tunneling electrons from floating gate to n^+ drain diffusion by grounding control gate and applying the programming voltage to the drain diffusion. Thus producing a logic '0' state in the cell.

Erasure is performed by charging the floating gate, resulting in a logic '1' state in the cell. It obtained when control gate maintained to high voltage and source, drain & substrate are all grounded.

Typical EEPROM cell, having two transistors (one used for reading and other for programming and erasure) are larger than EPROM cells. Although second generation EEPROM chips used TTL levels, they still require an externally generated high voltage pulse to alter data as well as latches to hold address and data signals.

Third generation EEPROM eliminate the external components by incorporating all of the required supporting hardware for performing function as voltage generating and

pulse shaping on the chip. They operate from a single 5 V supply, thereby removing high current typically used to alter data by charge pump circuit. They automatically perform a byte erase cycle prior to each byte write. To hold the information during the write cycle, latches are added on the address and data inputs.

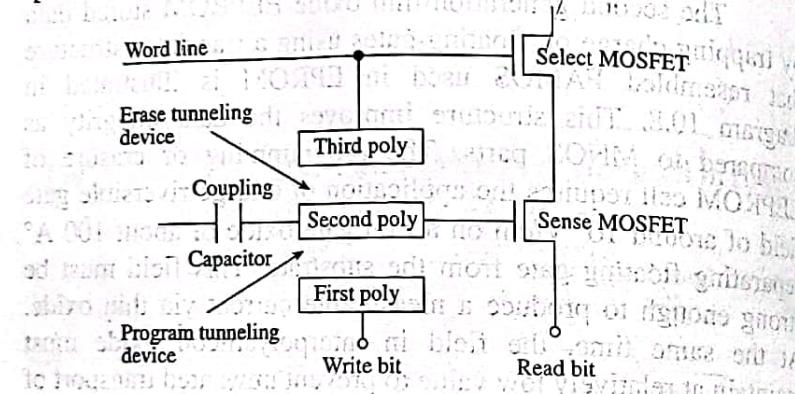


Fig. 10.10: Textured surface triple poly EEPROM cell

10.11 RAM

RAM is an array of storage cells that memorize information in binary form. As contrasted with an ROM, information can be randomly written into or readout of each storage element as required. The basic storage cell is the latch or flip-flop.

Linear Selection:

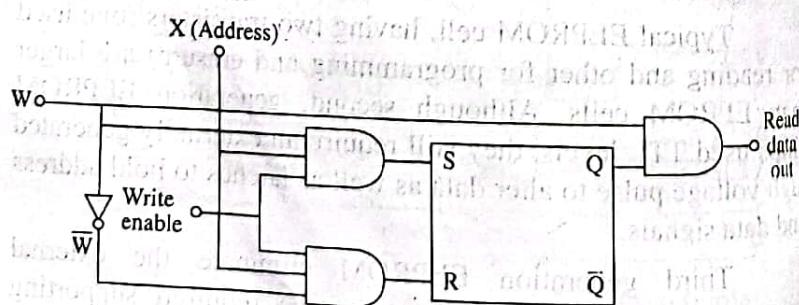


Fig. 10.11:

To read-out or write data into the cell, it is necessary that the address line $X = 1$. To write the write enable also should be high.

If the write input is at logic 1(0), the $S = 1(0)$ & $R = 0(1)$. Hence $Q = 1(0)$ and the data read – out is 1(0), corresponding to that written in.

The read/write 16 words of 8-bits each, A total of $16 \times 8 = 128$ storage cells must be used. Out if this 8 cells are arranged in a Horizontal line, all excited by a different address. In other words, the addressing is provided by exciting one of sixteen (1 of 16) lines. This type of addressing is called linear selection.

Coincident selection

A more commonly used topology is to arrange 16 memory elements in a rectangular 4×4 array, each cell now storing one bit. If one word, eight such matrix places are required, one for each of the 8 – bits in each words. Each bit is located by addressing X-address line and Y-address line.

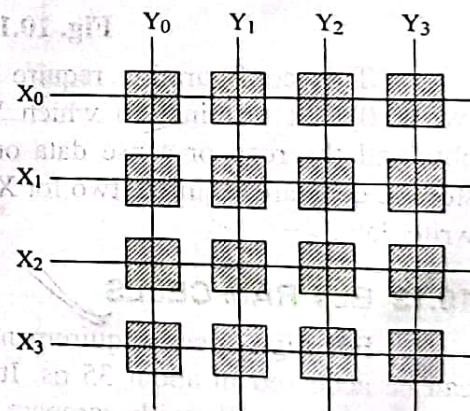


Fig. 10.12: Coincident selection

The intersection of two lines located at a point in two dimensional matrix, thus, identifying the storage cell under consideration. Such two dimensional addressing is called X-Y or coincident selection.

10.12 BASIC RAM ELEMENT

For either bipolar or MOS RAM, it is possible to construct a flop-flop which has common terminal for both writing and reading, such terminal 1, 2 as illustrated in diagram 10.13.

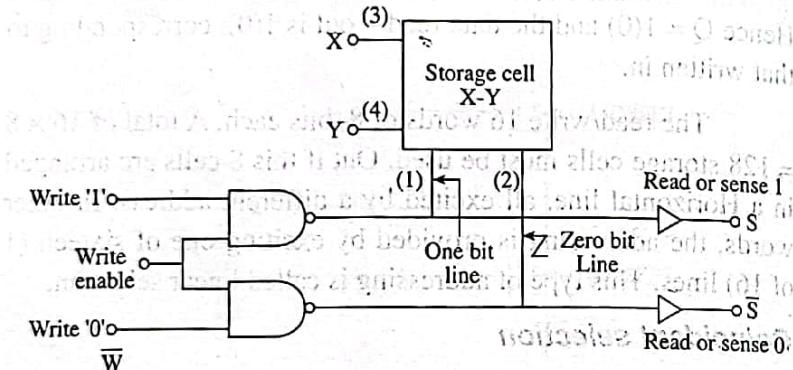


Fig. 10.13:

This configuration requires both W [write = 1] and \bar{W} [write 0]. At terminal to which W (\bar{W}) is applied, there is obtained the read or sense data outputs S (\bar{S}). Four leads for storage cells are required, two for X-Y address and two for read, write data.

10.13 BJT RAM CELLS

For high speed requirement, BJT RAM preferred, as it can be accessed in about 35 ns. It is small in size, as contains 1024 memory cells with compare to MOS RAM having 4096 memory cells.

BJT RAM memory cell is a simple flop-flop with some additional features like read, write and addressing the cell. A RAM memory cell using multi-emitter transistor is illustrated in diagram 10.14.

Let X and Y at logic 0 and Read-Write also at logic 0. Then transistor T_3 and T_4 conducts and its collector voltage becomes low. Hence diodes D_1 and D_2 do not conduct. If say that the state of flip-flop is such that T_1 conducting and T_2 OFF,

then emitter current flow in E_x and E_y . A bias voltage 0.5 V applied via R_3 to E_D . Here E_D is more positive than E_x and E_y by at least 0.2 V. Thus, E_D does not conduct. Under this conditions transistors T_5 and T_6 becomes cut-off and Data output becomes at logic 1.

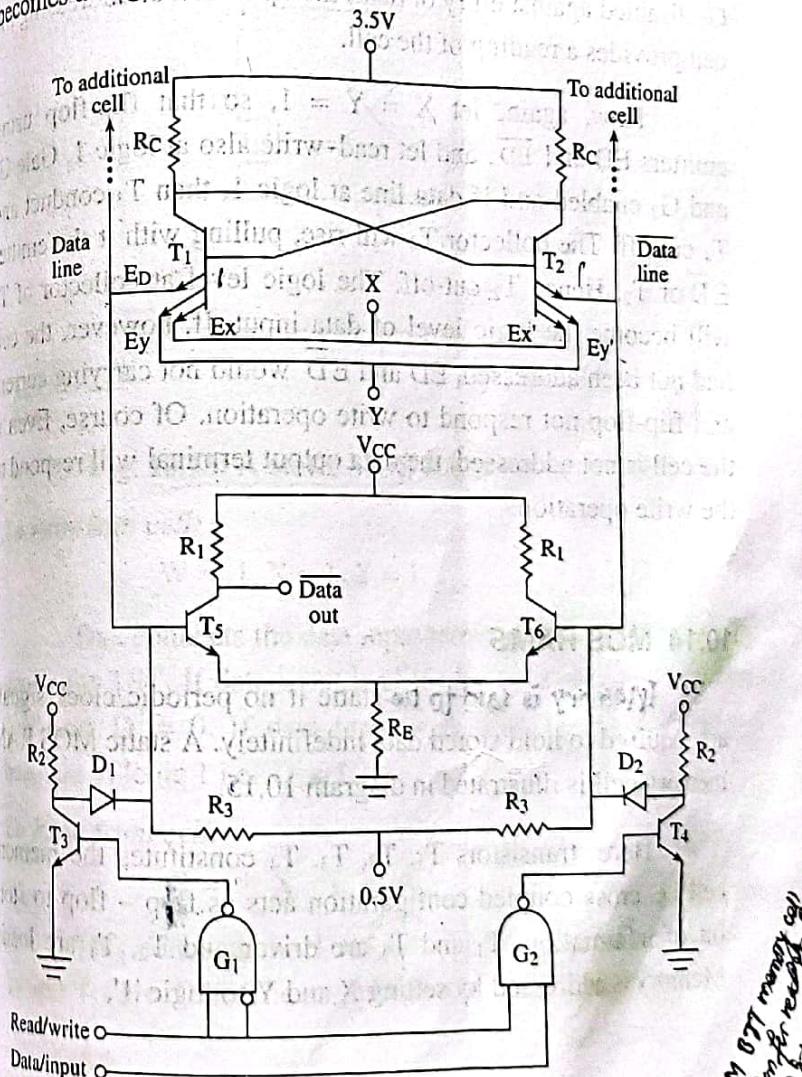


Fig. 10.14: A RAM BJT memory cell provision for reading & writing

Now, let X and Y at logic 1, the current via E_x and E_y will be diverted to ED. A component of this current flow via base of T_5 and \overline{Data} out terminal will assume same logic level present at collector of T_1 . Thus, with read-write at logic 0 (G_1 & G_2 disabled against entry of data) the operation of addressing the cell provides a reading of the cell.

How, again, let $X = Y = 1$, so that flip-flop using emitters ED and \overline{ED} , and let read-write also at logic 1. Gate G_1 and G_2 enabled and if data line at logic 1, then T_3 conduct and T_4 cut-off. The collector T_4 will rise, pulling with it the emitter \overline{ED} of T_2 . Hence T_2 cut-off. The logic level at collector of T_2 will become the logic level of data input. If, however, the cell had not been addressed, ED and \overline{ED} would not carrying current and flip-flop not respond to write operation. Of course, Even if the cell is not addressed, the data output terminal will respond to the write operation.

10.14 MOS RAMS

Memory is said to be static if no periodic clock signals are required to hold stored data indefinitely. A static MOS RAM memory cell is illustrated in diagram 10.15.

Here, transistors T_1 , T_2 , T_3 , T_4 constitutes the memory cell i.e. cross coupled configuration acts as flip-flop to store bit of information. T_1 and T_3 are driver and T_2 , T_4 are loads. Memory is addressed by setting X and Y to logic '1'.

discrete removed

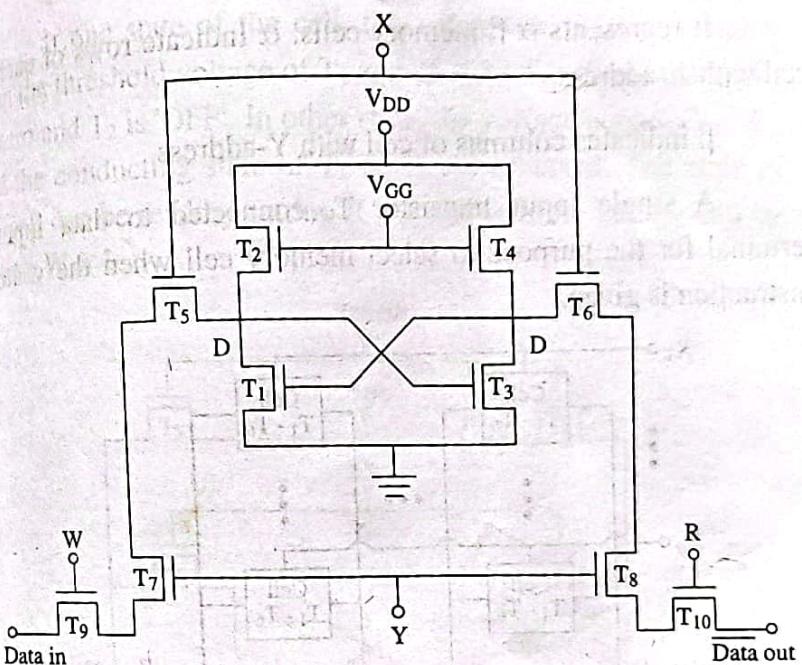


Fig. 10.15: A static MOS RAM memory cell

To write into cell:

$$W = 1, X = 1, Y = 1.$$

This connects the data input terminal to node D as T_5 , T_7 and T_9 are 'ON'. If data input is at logic 1, this causes T_3 to turn 'ON' and $\overline{D} = 0$. If data input = 0, then T_3 cut-off and \overline{D} becomes at logic 1 i.e. $\overline{D} = 1$.

To Read from cell:

$$R = 1, X = 1, Y = 1$$

This connects the \overline{Data} out-put terminal to \overline{D} , since T_6 , T_8 and T_{10} are 'ON'. The complement of data written into cell is Read.

Many memory cells connected to same input and output constitute RAM, is illustrated in diagram 10.16.

It represents $\alpha \beta$ memory cells. α Indicate rows of each cell with X-address.

β indicates columns of cell with Y-address.

A single input transistor T_9 connected to data input terminal for the purpose to select memory cell when the write instruction is given.

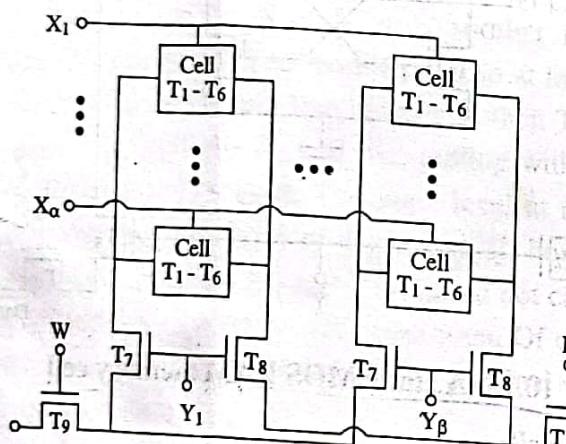


Fig. 10.16: Interconnection of cells to form a RAM

Similarly, a single output transistor T_{10} to connect the selected memory cell to Data output terminal during read operation.

10.15 DYNAMIC RAM

A Dynamic MOS RAM memory cell is illustrated in diagram 10.17. The memory cell is composed of T_1 , T_2 , T_3 & T_4 . Transistors T_7 , T_8 , T_5 & T_6 serve all the cells having same y-address.

The state of the cell is stored on stray capacitances C_1 & C_2 . These capacitors becomes accessible to data lines when T_3 , T_4 , T_7 & T_8 are all conducting making $X = Y = 1$.

If one state of the cell, the voltage across C_1 is higher than the threshold voltage of T_1 and T_1 is 'ON', voltage across C_2 is zero and T_2 is 'OFF'. In other state, the voltage across C_1 & C_2 and the conducting state of T_1 & T_2 are reversed. The state of the cell can be read by setting $R = 1$ and written into the cell by setting $W = 1$.

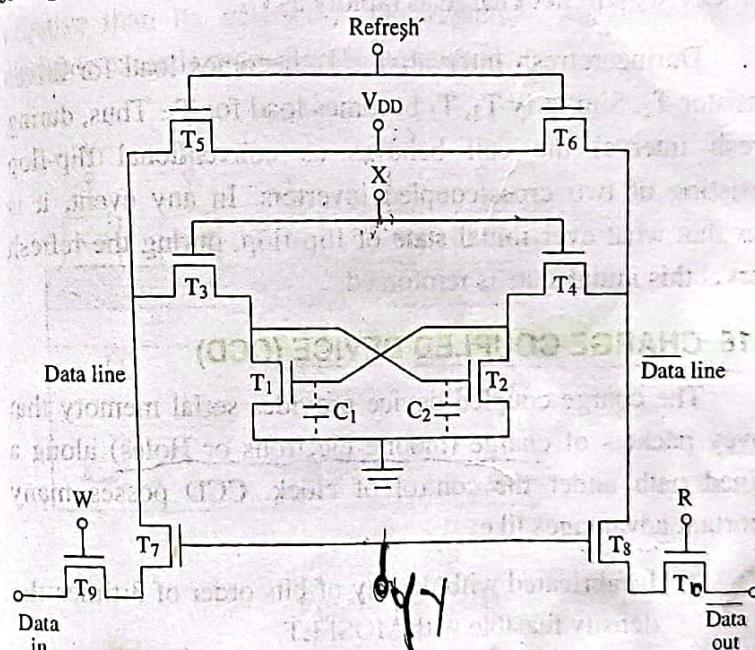


Fig. 10.17: MOS dynamic RAM cell

Refresh Operation:

The refresh operation accomplish by allowing brief access from supply voltage V_{DD} to the cell.

When X – address and refresh are simultaneously high, T_3 , T_4 , T_5 , T_6 conducts.

If initially, T_1 ON, T_2 cut-off, $V_{C_1} > VT$ and $V_{C_2} = OV$,

During refresh V_{DD} is applied via T_6 & T_4 to C_1 in parallel with T_2 . But T_2 cut-off. Hence all current from V_{DD} will directed towards C_1 , allowing C_1 to recharge, if any charge lost due to leakage.

Similarly, V_{DD} is applied to C_2 in parallel with T_1 . Since T_1 is 'ON' C_2 will not charge as rapidly as C_1 .

During refresh interval, T_4 , T_6 becomes load for driver transistor T_2 . Similarly T_3 , T_5 becomes load for T_1 . Thus, during refresh interval the cell behaves as conventional flip-flop consisting of two cross-coupled inverters. In any event, it is clear that whatever initial state of flip-flop, during the refresh interval this initial state is reinforced.

10.16 CHARGE COUPLED DEVICE (CCD)

The charge coupled device provides serial memory that convey packets of charge (mobile electrons or holes) along a defined path under the control of clock. CCD posses many important advantages like:

- It fabricated with density of bits order of 3 times the density feasible with MOSFET.
- ✓ Same speed as of MOSFET memory.
- ✓ Improved density cause lower cost.
- ✓ Less power dissipation.
- ✓ Much simpler fabrication process.

Storage of charge:

Let us consider the situation illustrated in diagram 10.18. The bottom of substrate is connected to ground i.e. maintained at OV. All metal electrodes are maintained at fixed negative

voltage. The separation between electrodes is extremely small compare to their width. If the electrode voltage is large enough in magnitude, so that it exceeds the threshold voltage of substrate, then a depletion layer is formed below the oxide layer.

If the voltage on one of metal electrode is made more negative than its neighbors, the depletion region below that electrode extends more deeply than others.

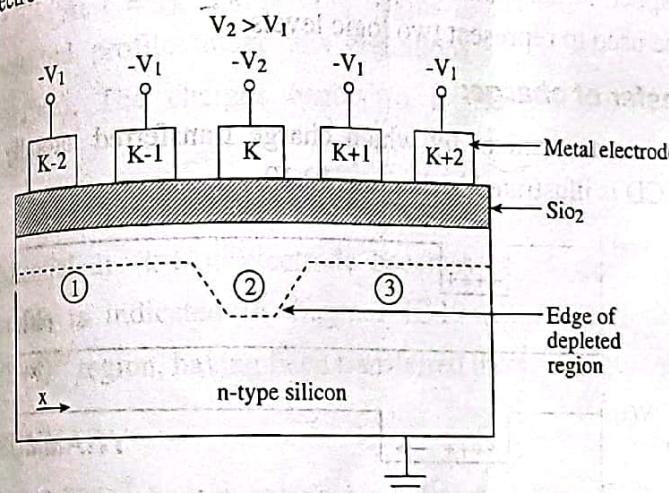


Fig. 10.18: CCD

Any charged particles 'q' in a field described by a potential $V(x)$ exerted a force F in the positive direction.

$$F = -q \frac{dv}{dx}$$

If the potential is flat, $\frac{dv}{dx} = 0 \Rightarrow F = 0$. There is no force.

In the region between (2) & (3) where $\frac{dv}{dx}$ is positive, the force is to left.

Thus, positive charge introduced into depletion region at any level is free to move within the potential well.

The larger negative potential applied to a particular electrode (k) compare to other electrodes ($k - 2, k - 1, k + 1, k + 2$), result in deeper depletion region for that electrode. If one introduce some positive charges into this region, the charge will be trapped in position. The presence or absence of such charges can be used to represent two logic levels.

Transfer of charge:

A mechanism by which charge transferred laterally in the CCD is illustrated in diagram 10.19.

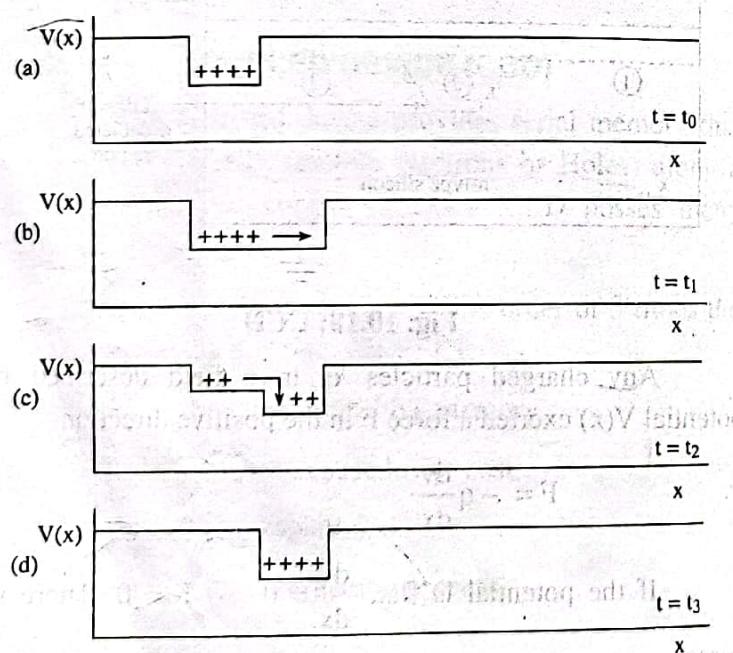


Fig. 10.19: Mechanism of charge transfer

Let at $t = t_0$, the voltage across k -electrode is $V_K = -V_2$, all other electrodes at $V = -V_1$. An extended depletion region is

formed below K -th electrode and some positive charges are introduced in this region.

At $t = t_1$, let $(k+1)^{th}$ electrode also drops to $-V_2$, then potential profile under this condition is as indicated in diagram 10.19 (b). The charges will diffuse towards right as shown by arrow.

At $t = t_2$, if V_K now begins to return to $-V_1$, Then potential profile under this conditions is shown in diagram 10.19(c). The charges begins to migrate towards $(k+1)^{th}$ region.

At $t = t_3$, Now, V_K becomes at $-V_1$ and V_{K+1} i.e. potential at $(k+1)^{th}$ electrode becomes at $-V_2$. The potential profile is indicated in diagram 10.19 (d). The charge is in $(k+1)^{th}$ region, having been transferred there from K^{th} region.

SUMMARY

This chapter begins by defining a number of special terms used in description of semiconductor memories. The student should be familiar with most of the terms used and with following ideas:

- Term "Memory" and classifications.
- Semiconductor and magnetic memory.
- Sequential access memory.
- Random access memory (static, dynamic).
- Read only memory (Including mask PROM, PROM, EPROM, EEPROM).
- ROM and RAM basic structure.

- Memory Address: Row and Column selection.
- Concept of volatile versus non volatile information storage.
- BJT RAM cell with Read and Write operation.
- MOS RAM including Read & Write operation.
- Concept and feature of static and Dynamic memory illustrated
- Dynamic MOS RAM with read, write and refresh operation
- Concept of CCD including storage of charge and transfer of charge.

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PROBLEMS

1. Discuss the various semiconductor memory types. List out differences between RAM and ROM.
2. Illustrate various features of RAM. Discuss the basic differences between static and Dynamic RAM.
3. Discuss the various ROM memory types. List out different feature of Masked ROM, PROM, EEPROM and EEPROM.
4. Draw MOS RAM memory cell and explain Read and Write operation.
5. Draw the dynamic RAM memory cell and explain Read, Write, Refresh operation in DRAM circuit.
6. Illustrate the concept of writing data into cell and erasing of data in
 - a) EEPROM.
 - b) EEPROM.
7. Discuss concept of EEPROM based on development
 - a) First generation
 - b) Second generation
 - c) Third generation

List out merits and demerits of an EEPROM.
8. Draw a RAM BJT memory cell and explain Read and Write Operation in BJT RAM circuit.

9. Discuss the features and illustrate the concept of basic structure of
 - i) ROM
 - ii) RAM
 - iii) Linear selection
 - iv) Coincident selection.
10. For Charge coupled Device memory cell, Illustrate and discuss the terms mentioned below.
 - i) concept of CCD
 - ii) Advantages of CCD
 - iii) Storage of charge in CCD
 - iv) Transfer of charge in CCD.

Analog Switches

11
Unit

11.1 INTRODUCTION

The Diodes, bipolar transistors and Filed effect transistors (both junction and Insulated gate) can be used as analog switches. Diode switches are faster than transistor switches since the storage time and capacitances associated with diodes are appreciably smaller than in transistor. Diodes, on the hand, being two terminal devices, have no control electrode and hence generally lead to more awkward circuitry than transistor (3 terminals Device). But still, where speed is at a premium, Diodes becomes the active device of choice. In addition to these, some important typical applications of switches are discussed.

11.2 ANALOG SWITCHES

Ideally, digital wave forms make abrupt transitions between two range of values. One range represent logic '1' while other represent logic '0' within each range, the exact signal level is of no significance.

Analog voltages are those whose precise value is always of significant. Analog voltage may be fixed in value or may make excursion via continuous range of values. The switches in circuit and system involving analog signals, in which the opening and closing of switch controlled by Digital wave-form, such circuits are variously termed as Analog gates, Transmission gates, linear gates, Time selection circuits etc. depending upon the purpose for which the gate is used. The switch control digital wave-form is reffered to as the gating signal, the control signal or logic input.

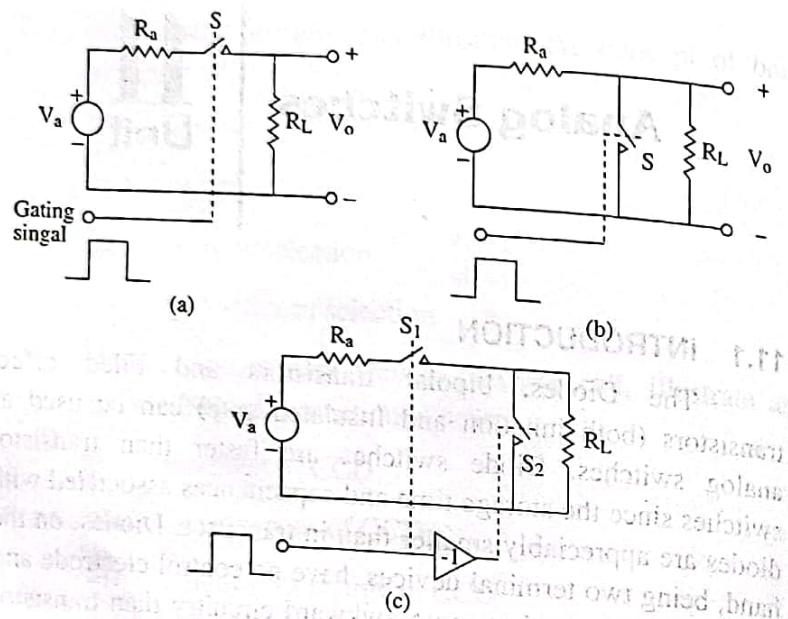


Fig. 11.1: Switch configuration (a) series switch (b) shunt switch (c) combination of series and shunt switch

Several analog gates via which one can control the transmission of analog signal 'Va' to a load 'RL' is illustrated in diagram 11.1. A gating signal which makes transition between two ranges controls the opening and closing of switch 'S'. The gating signal is a digital signal i.e. when gating signal is at logic high, the switch becomes open, and when gating signal is at low, the switch becomes closed.

The series, shunt and combination of both switch, illustrated in diagram 11.1 a, b, c above. Depending upon the particular requirement, it becomes advantageous to use either series or shunt switch arrangement.

Applications of switching circuit:

Switching circuit posses wide applications, some important applications are listed-out below.

Multiplexing

- Sample and Hold (S/H)

- Integrate and Dump

- Digital to Analog Conversion

- Parameter Control

- Maximum Voltage Decision Making Circuit etc.

11.3 DIODE TRANSMISSION GATES

Diodes, BJT, FET, can be used as analog switches. Diode switches are faster than transistor switches since the storage time and capacitance associated with diodes are appreciably smaller than in transistors.

(a) One-Diode Gate

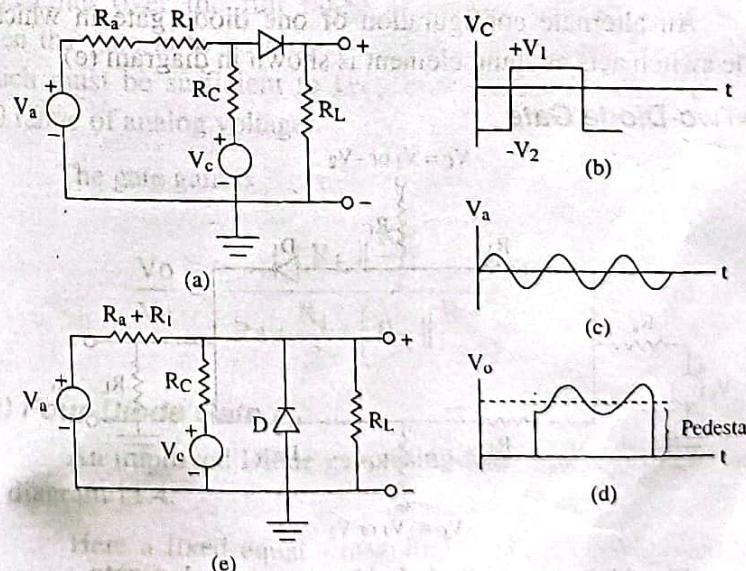


Fig. 11.2: (a) A one diode gate (b) The control voltage (c) An input wave form (d) The output wave form (e) A one diode gate in which diode acts as shunt element

One diode gate is illustrated in diagram 11.2 (a). A control voltage ' V_C ' opens and closes the gate to regulate the transmission of analog signal ' V_a '. For a typical analog voltage as shown in diagram (c), the output V_o appears as in diagram (d). The Analog waveform, when transmitted via the gate, is superimposed on a pedestal i.e. the base line of the output is different depending on whether the gate is open or closed.

The gate has a limited range of amplitude over which it would operate.

At $V_C = -V_2$, The diode D is normally cut-off. But if the peak, positive going excursion of the analog wave-form is too large, there will be transmission of these peaks.

Similarly, at $V_C = V_1$, A negative excursion of analog waveform which will too large will cut the diode OFF.

An alternate configuration of one diode gate in which diode switch acts as shunt element is shown in diagram (e).

(b) Two-Diode Gate

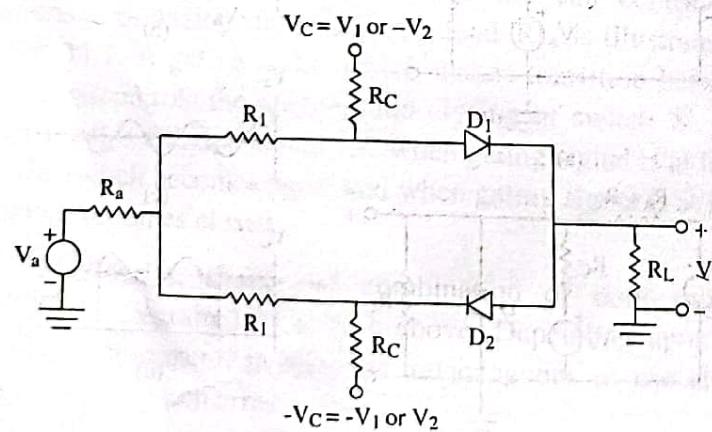


Fig. 11.3: A two diode bridge transmission gate

Two diode gate is a combination of two one diode gates of type shown in diagram 11.3. The pedestal of one diode gate

of diagram 11.2 (d) will be eliminated in two diode gate illustrated in diagram 11.3.

Here, two symmetrical voltages V_C and $-V_C$ are required. When the control voltages are at levels V_1 and $-V_1$ respectively, the diodes conduct and the analog signal ' V_a ' is transmitted to output. When control voltages are at V_2 and $-V_2$ respectively, diode do not conduct and gate is closed against transmission.

As a result of symmetry of the circuit and symmetry of control voltages, there will be no pedestal at the gate output.

The range of excursion of the voltage will determine the required control voltage level V_1 and V_2 . On the one hand, when the gate is to transmit, $V_C = V_1$ must be sufficiently positive ($-V_C = -V_1$ sufficiently negative) to maintain both diodes conducting over the full range of analog voltage. Similarly, when the gate is to be closed against transmission, $V_C = -V_2$, which must be sufficient to keep both diodes cut-off over the full range of analog voltage.

The gate gain is

$$\frac{V_o}{V_a} = \frac{R_L \parallel \frac{R_C}{2}}{R_a + R_1 + \left(R_L \parallel \frac{R_C}{2} \right)} \quad \dots \dots \text{(i)}$$

(c) Four-Diode Gate

An improved Diode gate, using four diodes is illustrated in diagram 11.4.

Here a fixed equal-magnitude voltages are applied to the resistors 'RC' while the gating voltages $+V_C$ and $-V_C$ applied via two additional diodes D_3 and D_4 .

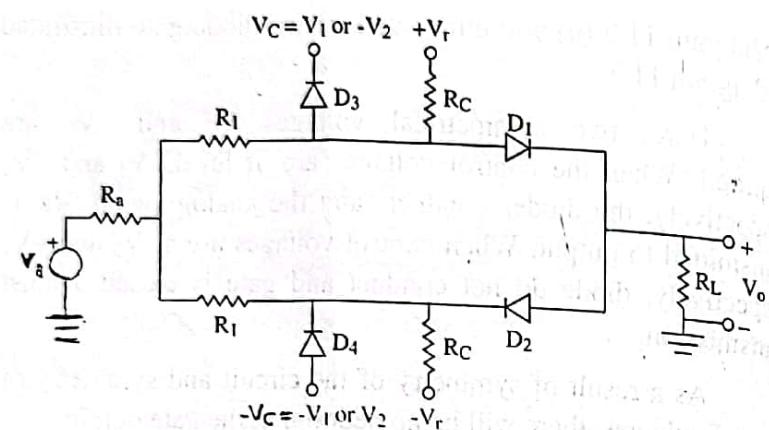


Fig. 11.4: A four diode gate

During transmission:

At $V_C = V_1$, Diodes D_3 and D_4 are cut off. The gate is then identical in form to the two diode gate except that the current via diodes D_1 and D_2 is provided by fixed reference voltages $+V_r$ and $-V_r$ rather than by control voltage. We see that output never exceed $\pm V_1$. For if V_a should increase to a value which increase V_o above V_1 , Diode D_3 will conduct clamping point a to the voltage $V_1 + 0.7$. Similarly, b would be clamped to $-V_1 - 0.7$, if V_a is too negative a voltage.

During Non transmission:

At $V_C = -V_2$, The points a and b are clamped by diodes D_3 and D_4 to $-V_2 + 0.7$ and $V_2 - 0.7$ respectively. Diodes D_1 and D_2 cut-off and remain cut off for all values of ' V_a '.

Small resistance ' R_1 ' in four diode gate yields increased gain.

Advantages:

- Gain is close to unity.
- During non-transmission, the isolation between Input and output is improved.

To eliminate an output pedestal, $+V_C$ and $-V_C$ need not be necessary equal in magnitude.

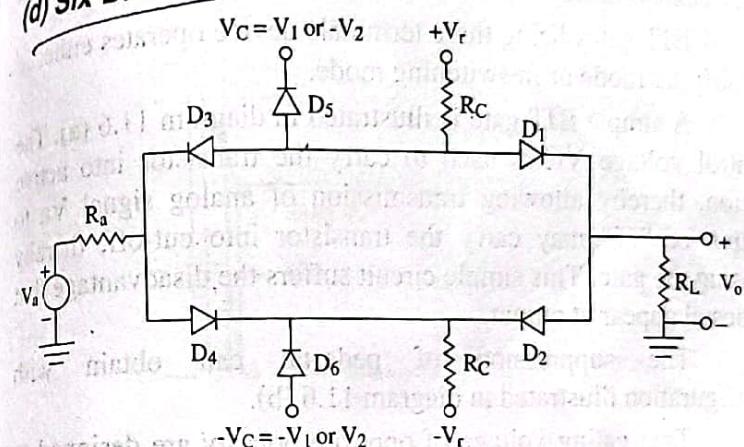
(d) Six-Diode Gate

Fig. 11.5: A six diode gate

A six diodes gate which include features of four diode gate is illustrated in diagram 11.5. When gate becomes closed against transmission, diodes D_5 and D_6 conducts and serve as clamps, back biasing all other diodes.

During transmission, diodes D_5 and D_6 are cut-off while other diodes are conducting. The advantage of the six diode case is apparent in fact that here the large voltage need appear only as a fixed voltage and not as a control signal.

From diagram 11.5 it appears that if the clamping diodes D_5 and D_6 are to remain back-biased for an analog signal of peak value V_a (max), then V_1 must be at least equal to V_a (max). On the other hand, it is also seen that in non transmission mode, Where $V_C = -V_2$, diodes D_1 and D_2 remain cut-off for all values of V_a . Thus, V_2 may be any non-negative voltage.

To summarize, we have result

$$V_1 = V_a \text{ (max)}, \quad V_2 \geq 0.$$

11.4 BJT GATES

Diode gate have advantage in terms of speed, however being two terminals device without control electrode, provides no gain.

BJT gates being three terminals device operates either in amplifying mode or in switching mode.

A simple BJT gate is illustrated in diagram 11.6 (a). The control voltage V_C is used to carry the transistor into active region, thereby allowing transmission of analog signal V_a to output or ' V_C ' may carry the transistor into cut-off, thereby closing the gate. This simple circuit suffers the disadvantage that pedestal appear at output.

The suppression of pedestal can obtain with configuration illustrated in diagram 11.6 (b).

Two gating voltage of opposite polarity are designed to keep the quiescent load current the same. When T_1 is ON and T_2 OFF (gate open) and when T_1 is OFF and T_2 ON (gate closed). This arrangement helps to eliminate pedestal.

Even with entirely symmetrical gating waveforms, objectionable spikes may appear at time of opening and closing of the gate, this is due to difficulty that one transistor ON and other OFF at the same time and to the same extent. Due to these difficulty, gate employing the transistor in the Amplifier mode are of limited applicability.

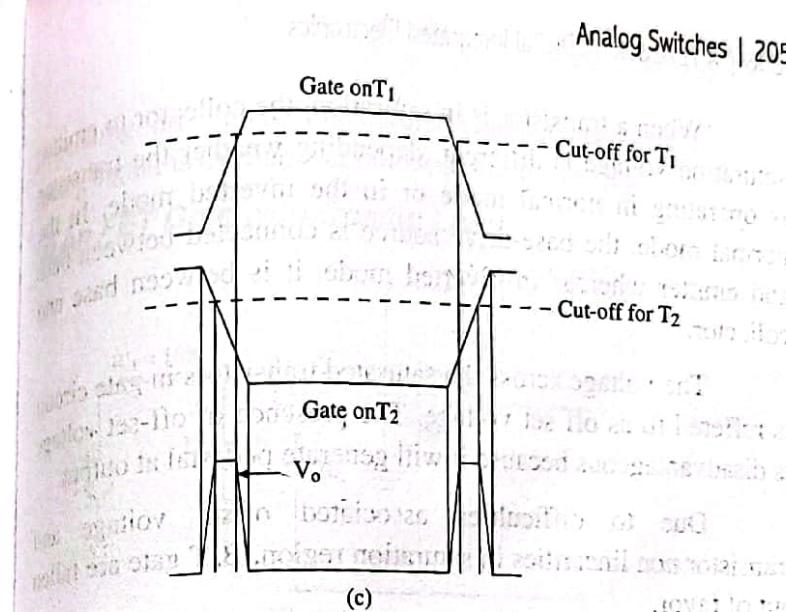
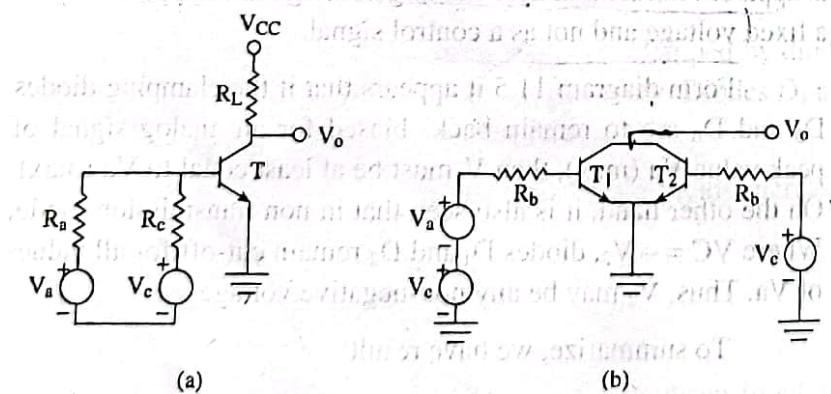


Fig. 11.6: (a) A BJT used as gate (b) two transistor used to suppress the pedestal (c) the origin of spikes in output of gate in (b)
An alternate bipolar transistor gates are illustrated in diagram 11.7(a), (b).

In diagram 11.7(a), to allow transmission, the transistor is driven to saturation by control source V_C . To restrain transmission the transistor is driven to cut-off.

In diagram 11.7(b), the transmission is allowed when the transistor is cut-off and is not allowed when transistor is in saturation.

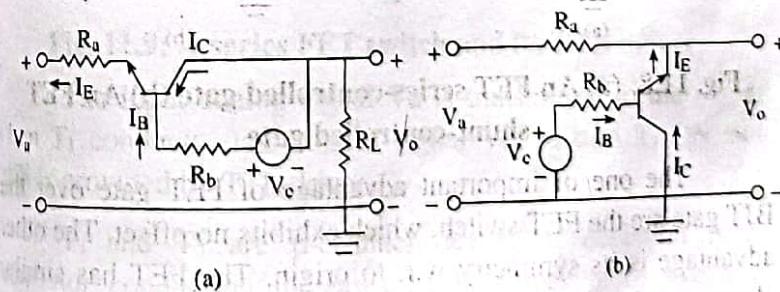


Fig. 11.7: (a) Transistor used as series element
(b) As a shunt element

When a transistor is in saturation, the collector to emitter saturation voltage is different, depending whether the transistor is operating in normal mode or in the inverted mode. In the normal mode, the base-drive source is connected between base and emitter whereas in inverted mode, it is between base and collector.

The voltage across the saturated transistors in gate circuit is referred to as offset voltage. The presence of offset voltage is disadvantageous because it will generate pedestal at output.

Due to difficulties associated offset voltage and transistor non linearities in saturation region, BJT gate are fallen out of favor.

11.5 FET GATES

A FET gate having series and shunt configuration are illustrated in diagram 11.8(a, b).

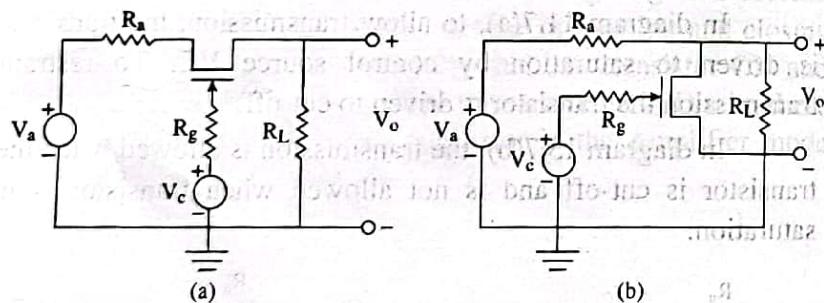


Fig. 11.8: (a) An FET series-controlled gate (b) An FET shunt-controlled gate

The one of important advantage of FET gate over the BJT gate are the FET switch, which exhibits no offset. The other advantage is its symmetry w.r.t. to origin. The FET has similar characteristics in its forward and reverse operating modes. The gating signal (control signal) is applied to the gate terminal,

Depending on signal, FET either conducts or does not and analog signal is available at output or not respectively.

(a) An FET Gate with Opamp Load

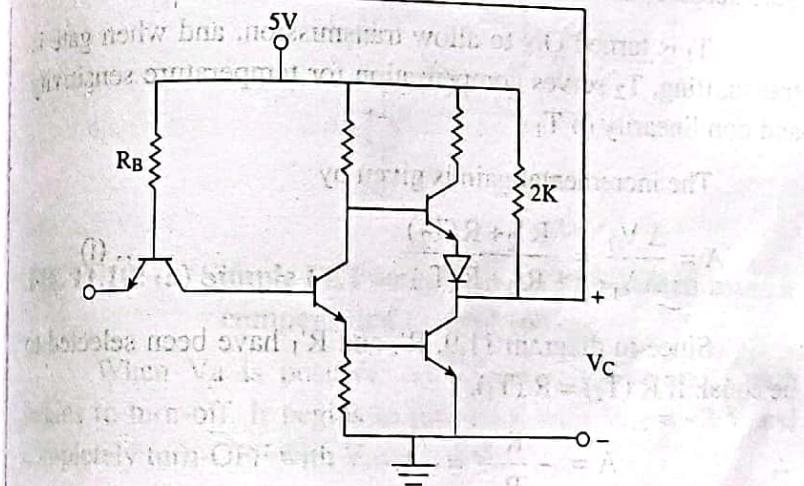
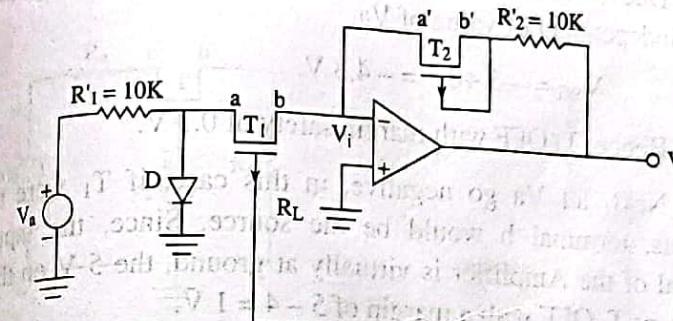


Fig. 11.9: A series FET switch and its TTL driver

The input analog signal V_a is transmitted to the output when T_1 conducts. The control signal V_c , to turn T_1 ON and OFF is provided by TTL driver.

T_1 and T_2 are p-channel device of depletion type. Transistor conduction increases as V_{GS} goes more +ve and conduction decreases as V_{GS} goes more -ve. Typically the threshold voltage V_T is $V_{SG} = -4$ V.

Let $V_C = 5$ V and V_a is positive. Then 'a' acts as source and 'b' as drain.

Due to diode 'D' the voltage at 'a' will be clamped at 0.7 V, independent of value of V_a .

$$\therefore V_{SG} = -5 + 0.7 = -4.3 \text{ V.}$$

Hence, T_1 OFF with margin safety of 0.3 V.

Next, let V_a go negative, in this case, if T_1 were to conduct, terminal 'b' would be the source. Since, the input terminal of the Amplifier is virtually at ground, the 5 V on the gate keeps T_1 OFF with a margin of $5 - 4 = 1$ V.

T_1 is turned ON to allow transmission, and when gate is transmitting, T_2 serves compensation for temperature sensitivity and non linearity of T_1 .

The incremental gain is given by

$$A = \frac{\Delta V_o}{\Delta V_i} = \frac{R'_2 + R(T_2)}{R'_1 + R(T_1)} \quad \dots \dots \text{(i)}$$

Since in diagram 11.9, R'_2 and R'_1 have been selected to be equal. If $R(T_2) = R(T_1)$,

$$\therefore A = -\frac{R'_2}{R'_1} = -1.$$

(b) FET Gate Drivers

Whether the gate device is ON or OFF, is decided by the gate to source voltage of an FET.

Let us consider the configuration illustrated in diagram 11.10 (a) which is using n-channel junction FET. The FET is fully turned ON when $V_{GS} = 0$ V, and fully turned OFF with $V_{GS} = -4$ V.

If V_C swings between OV to -4 V, Then when V_a is negative, the pn diode formed between gate and source is forward biased. Hence, maximum allowable negative voltage at the input is less than 0.6 V.

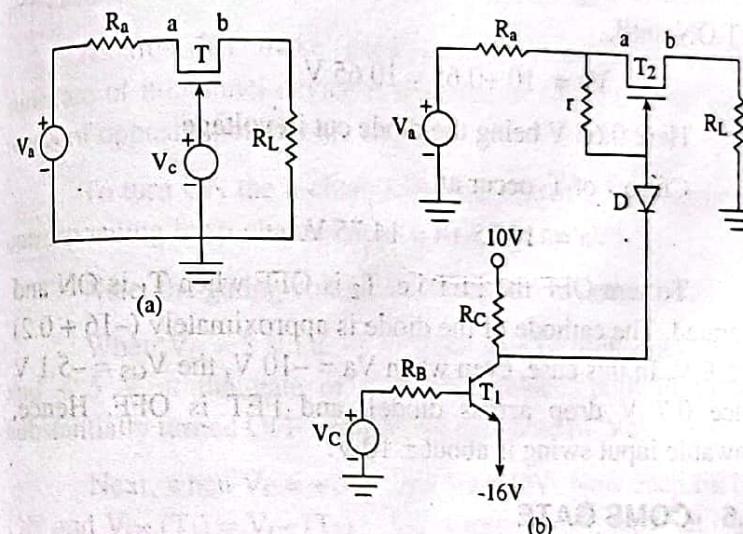


Fig. 11.10: (a) Simple FET switch (b) An FET switch using a compensated control voltage

When V_a is positive, V_{GS} goes negative and switch begins to turn-off. It begins to turn OFF with $V_{GS} = -2$ V and completely turn-OFF with $V_{GS} = -4$ V.

Thus, allowable analog input swing is about from + 2 V to - 0.4 V.

The restriction of the allowable input swing can be increased with the circuit illustrated in diagram 11.10 (b). The gate voltage is not fixed but follows the source voltage. The allowable input range with this circuit is about ± 10 V.

When T_1 is OFF and D is OFF. If V_a - ve, Terminal 'a' is source, 'b' - drain. Then

$$V_{GS} = OV$$

If V_a positive, terminal 'b' is source, 'a' drain. Then $V_{GS} > OV$, i.e. slightly +ve because, now gate is at same potential as drain.

Assuming $R_d \ll R_i$, the diode will remain OFF and the FET ON until.

$$V_a = 10 + 0.65 = 10.65 \text{ V.}$$

Here 0.65 V being the diode cut in voltage.

Cut-off of T_2 occur at

$$V_a = 10.75 + 4 = 14.75 \text{ V.}$$

To turn OFF the FET i.e. T_2 is OFF when T_1 is ON and saturated. The cathode of the diode is approximately $(-16 + 0.2) = 15.8 \text{ V}$. In this case, even when $V_a = -10 \text{ V}$, the $V_{GS} = -5.1 \text{ V}$ [since 0.7 V drop across diode], and FET is OFF. Hence, allowable input swing is about $\pm 10 \text{ V}$.

11.6 COMS GATE

A simple circuit of COMS gate is illustrated in diagram 11.11, in which a complementary-symmetry MOSFET (CMOS) has been employed.

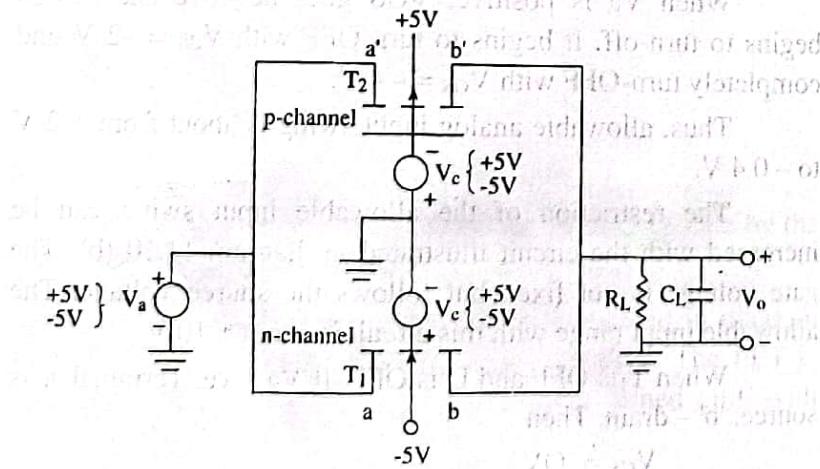


Fig. 11.11: A CMOS gate

In MOSFET, the function between "source and substrate" and between "drain & substrate" must not be allowable to be come forward biased. The substrate of n-channel devices is connected to the most negative point in the circuit and in p-channel to the most positive point in the circuit.

Assume V_a make excursions between $\pm 5 \text{ V}$, the substrate of n-channel device is returned to -5 V . Gating wave forms of opposite polarity are required.

To turn ON the n-channel device V_{GS} of 2 V is required, corresponding for p-channel device of 2 V is needed.

Note, the gating voltage levels are $+5 \text{ V}$ and -5 V .

When $V_C = 5 \text{ V}$ i.e. -5 V at the gate of n-channel device and $+5 \text{ V}$ at the gate of p-channel device, both FETs are substantially turned OFF irrespective the value of 'Va'.

Next, when $V_C = +5 \text{ V}$, and $V_a = OV$, Now each FET is ON and $V_{GS}(T_1) = V_{GS}(T_2) = 3 \text{ V}$ above cut-off. Now let input changes from OV . Then one of device will be driven towards cut-off and reaches to cut-off when source changes by 3 V . But at the same time other device will be driven further into its ON region of operation.

Over entire range of input voltage, at least one FET will be ON.

11.7 APPLICATION OF ANALOG SWITCHES

(a) Multiplexing

Most often multiplexer are used in pulse code modulation (PCM) communication systems and have many other applications as well. A two channel multiplexer with gating drive and Ring counter is illustrated in diagram 11.12, which used to turn switches T_1 to T_2 ON and OFF in sequence.

Here, Gating Amplifiers are driven by two inputs. One is the VB, Blanking signal, when VB is at low, all switches are open and Analog signals are not transmitted to the output.

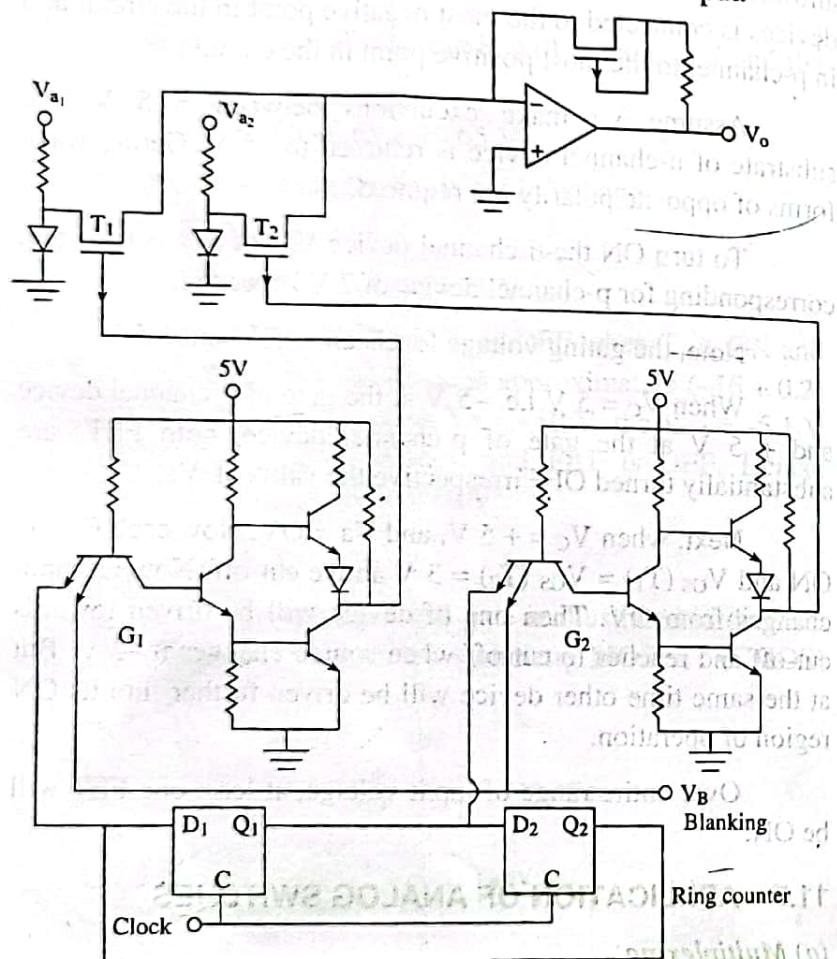


Fig. 11.12: A two channel multiplexer

The second input to each gate is the appropriate output of the ring counter, which determines the input to be transmitted to the output. The counter is so designed that only one output of the counter is in high state at any time. Hence only one switch is closed at a time.

Thus, output V_o represents the samples of $V_{a_1}(t)$ and $V_{a_2}(t)$ in succession.

(b) Maximum Voltage Decision Making Circuit

The maximum voltage decision making circuit is illustrated in diagram 11.13 (a) and its timing diagram in diagram 11.13 (b).

Here, input voltages V_1 and V_2 are to be compared and the higher magnitude voltage value has to be presented at output as V_o .

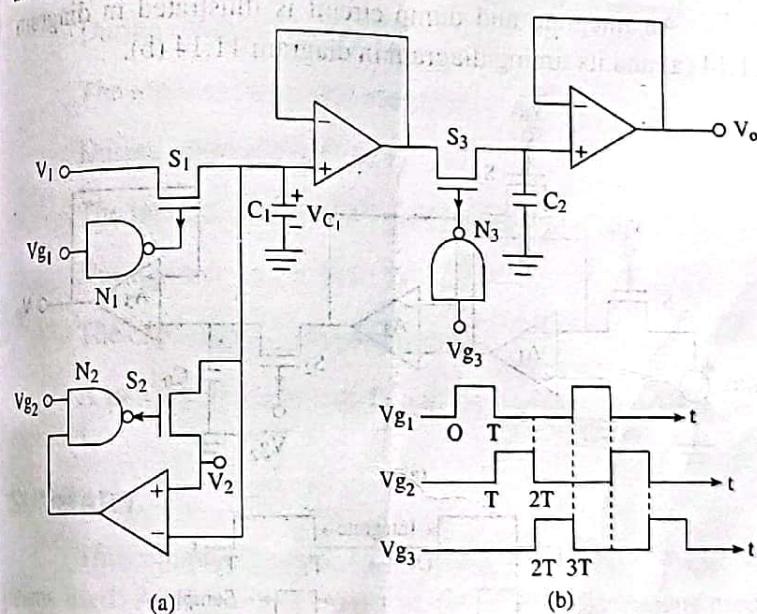


Fig. 11.13: (a) Circuit diagram (b) Timing diagram

To compare V_2 with V_1 , switch S_1 closed for time 0 to T , during time interval T to $2T$, V_2 is compared with V_1 in comparator. If $V_2 > V_1$, the comparator output becomes positive. NAND gate N_2 output becomes at logic low (0), which closes switch S_2 . Now capacitor charges to V_2 . If $V_2 < V_1$, switch S_2 remains open and capacitor voltage remains at V_1 .

At $t = 2T$, switch S_3 closes and capacitor C_2 charges to $VC_1(\text{max})$, the output voltage holds this value until $t = 3T$, at that time the voltage on C_2 changes to the new value of $VC_1(\text{max})$.

A 3-stage Ring counter can be used to generate the gate pulses vg_1 , vg_2 , vg_3 as illustrated time diagram for it in diagram 11.13(b). By extending the above concept $(N - 1)$ comparators and $(N + 1)$ gate pulses are needed to compare N -signals.

(c) An Integrate and Dump Circuit

An integrate and dump circuit is illustrated in diagram 11.14 (a) and its timing diagram in diagram 11.14 (b).

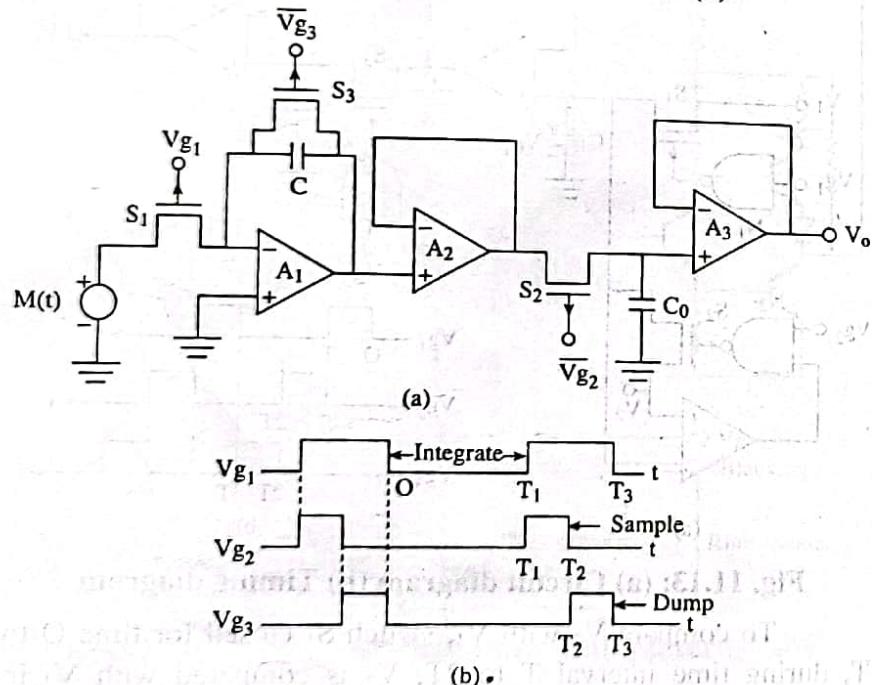


Fig. 11.14: (a) Integrate and dump circuit
(b) Timing diagram

The circuit is used to integrate the input signal for a time interval T_1 and transmit the integrated voltage to the output. But

before, each integration, the above charge stored in the capacitor must be discharged, i.e. the capacitor which stores the integrated input voltage must be dumped.

The integrate is fully capable of dumping capacitor 'C' when switch 'S₁' open and S₃ is closed, the capacitor discharge via FET switch. The integrate voltage V_i would get transmit to output when switch S₂ becomes closed.

The timing diagram for wave form V_{g₁}, V_{g₂} and V_{g₃} are illustrated in diagram 11.14(b)

During interval t = 0 to T₁,

The input voltage gets integrated.

During interval t = T₁ to T₂,

The integrator output V_i gets sampled and stored on C₀.

During interval t = T₂ to T₃,

The capacitor 'C' gets discharged.

A new cycle begins at T₃ and then entire procedure gets repeated.

SUMMARY

This chapter begins by defining a number of special terms used. Analysis and design of various configurations used in description of analog switches and its wide applications. The students must be familiar with most of the analog switches used and with following ideas.

- Analog switch, switch configuration (series and shunt switch)
- Analog gates, Transmission gate, linear gates, gating signal, control signal.

- Diode transmission gates discussed are:
 - One diode gate.
 - Two diode gate.
 - Four diode gate.
 - Six diode gate.
- Bipolar junction transistor gates discussed are:
 - Single BJT as a gate.
 - Two BJT used to suppress pedestal.
 - An alternate BJT configuration.
- Field Effect Transistor Gates discussed are:
 - FET Gate with series and shunt configuration.
 - FET gate with opamp load.
 - FET gate Driver.
 - FET switch using compensated control voltage.
- Complementary metal oxide gates discussed are
 - Illustration and configuration of a COMS Gate.
- Application of analog switches:
 - Multiplexing.
 - Maximum voltage decision making circuit.
 - Integrate and dump circuit.

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PROBLEMS

1. Discuss the Importance of these term in analog switches
 - i) Analog switch
 - ii) Analog gate, Transmission gate, linear gate
 - iii) Gating signal, Control signal.
2. For analog switch, Illustrated and discuss the concept of
 - i) Series switch
 - ii) Shunt switch
 - iii) Combination of series and shunt switch.
3. For Diode transmission gate, Illustrate and discuss the concept of
 - i) One diode transmission gate
 - ii) Two diode transmission gate
 - iii) Four diode transmission gate
 - iv) Six diode transmission gate.
4. For BJT transmission gate, Illustrate and discuss the concept of
 - i) A single BJT gate
 - ii) Two BJT gate used to suppress pedestal
 - iii) Alternate BJT series and shunt configuration.