FPGA assignment 1

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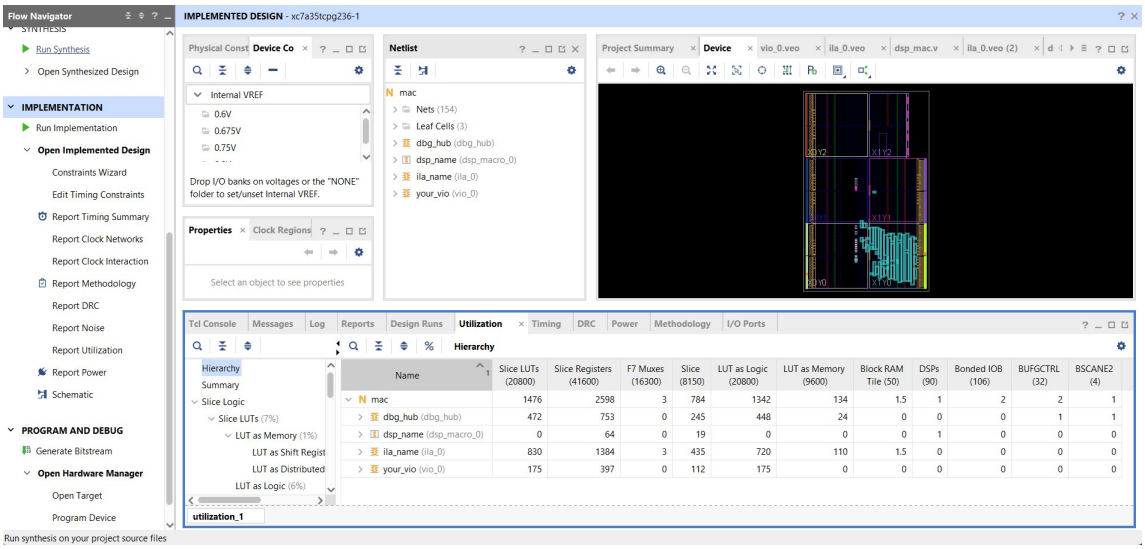
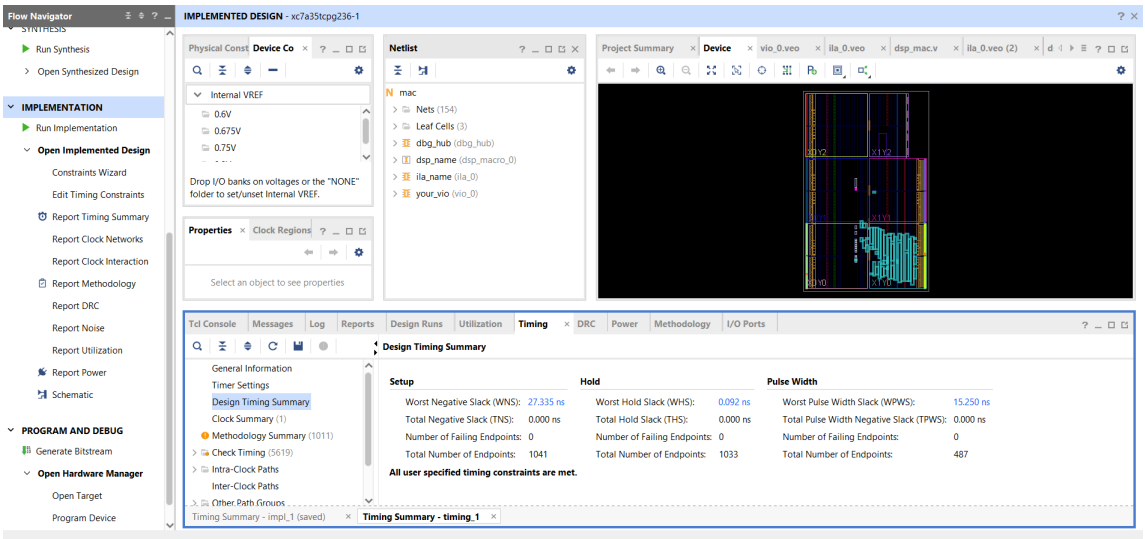
1 Question 1 - MAC-DSP

The image below represents the utilisation of the resources.



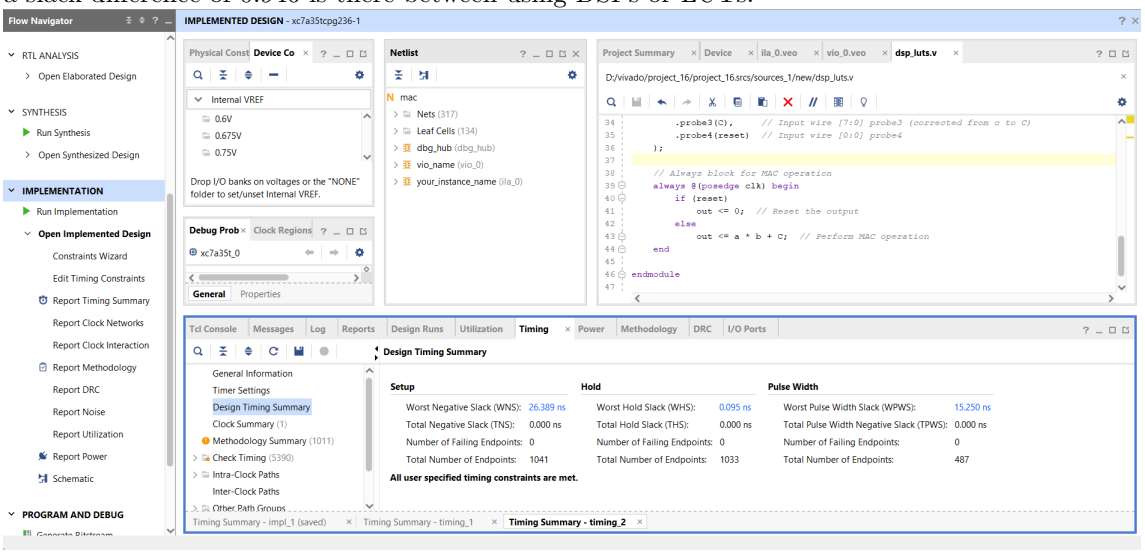
The figure gives the data that Slice Registers(64 of them) and one DSP block has been used for the MAC operation.

We can also see the timing report below.

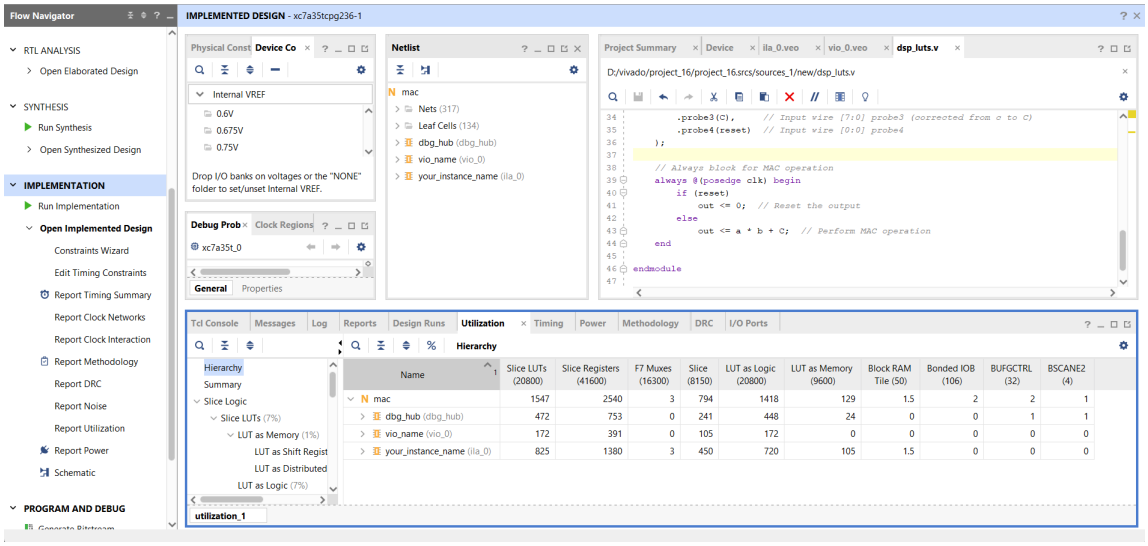


2 Question 2

a slack difference of 0.946 is there between using DSPs or LUTs.



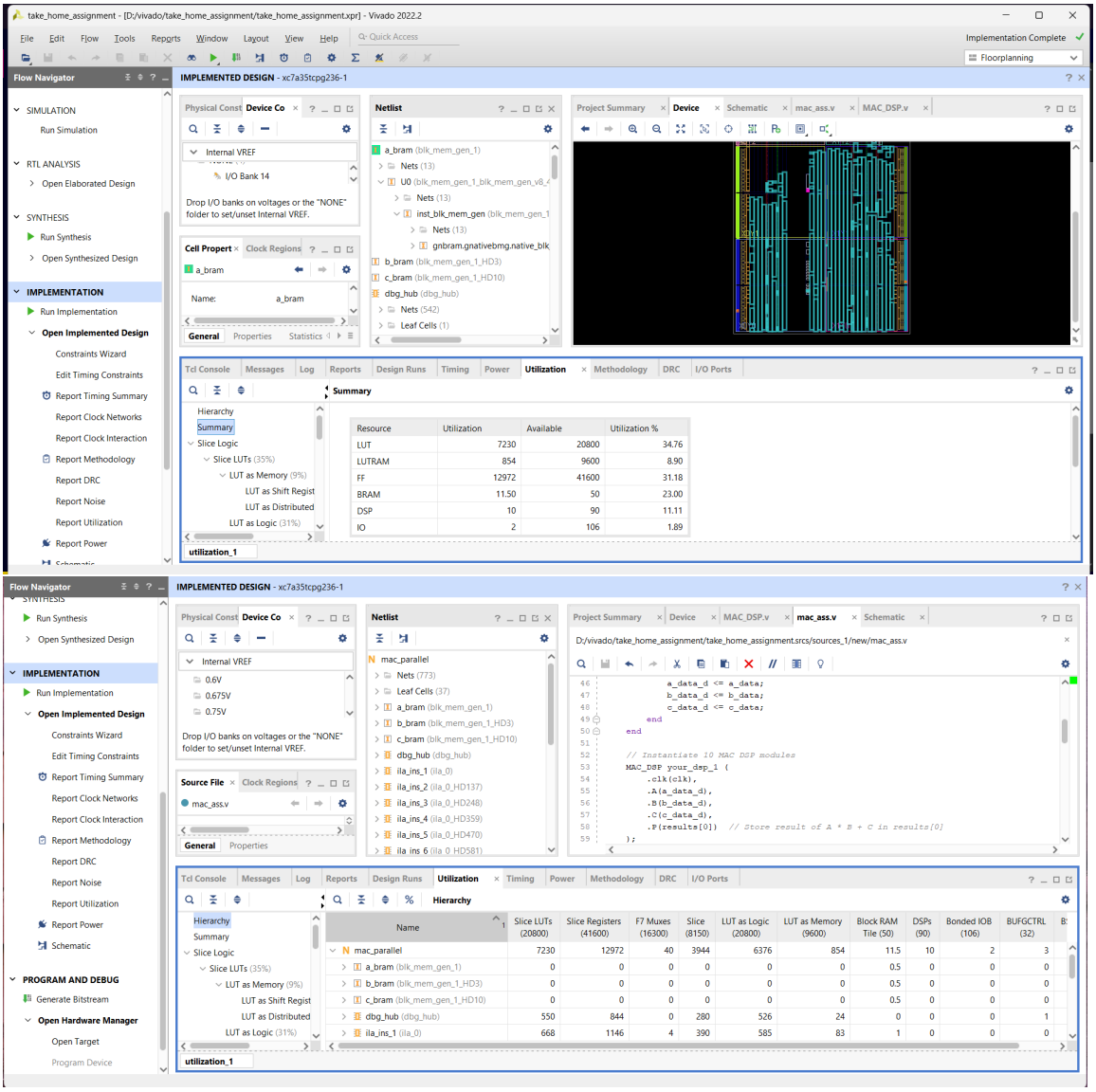
There are more LUTs used towards logic and less towards memory when we are using LUTs instead of DSPs.



3 Question 3

3.1 Part a

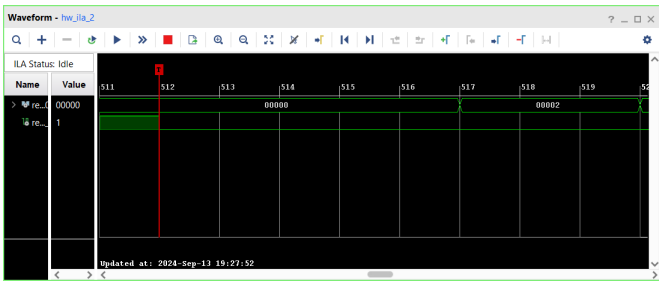
Basis3 board have 90 more DSP blocks that are available. Currently, we are using 10 DSP blocks for the MAC operations, so we can use a total of 100 DSP blocks in parallel at a time.



3.2 Part b

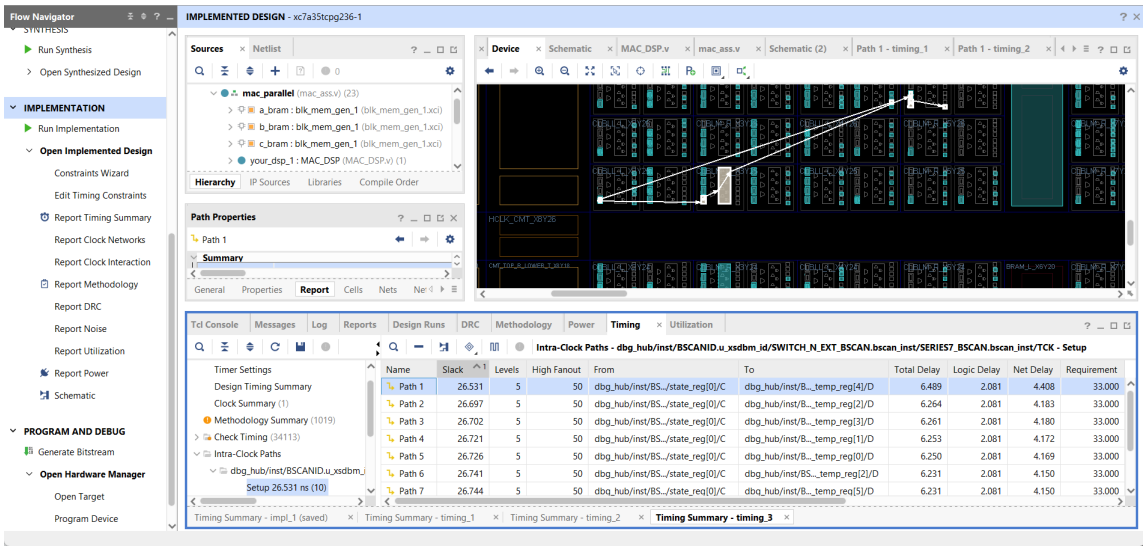
So the delay for the trigger of the 1st output is 5 clock cycle So for 10 dsp's the delay will be 50 ns. So the Throughput for 1 sec will be:-

$$Throughput = 2 * 10^{-10}$$

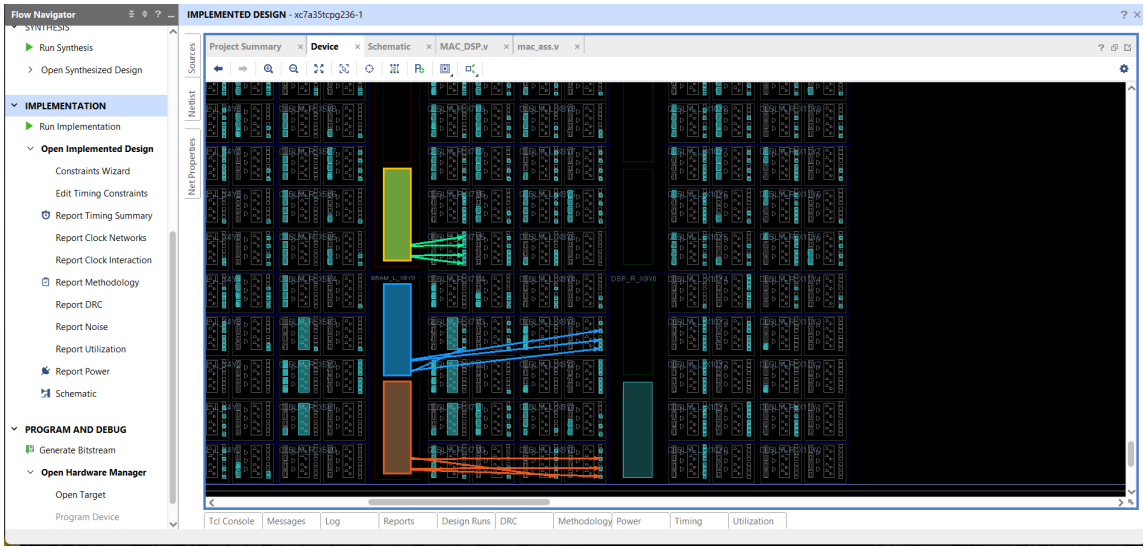


4 Question 4

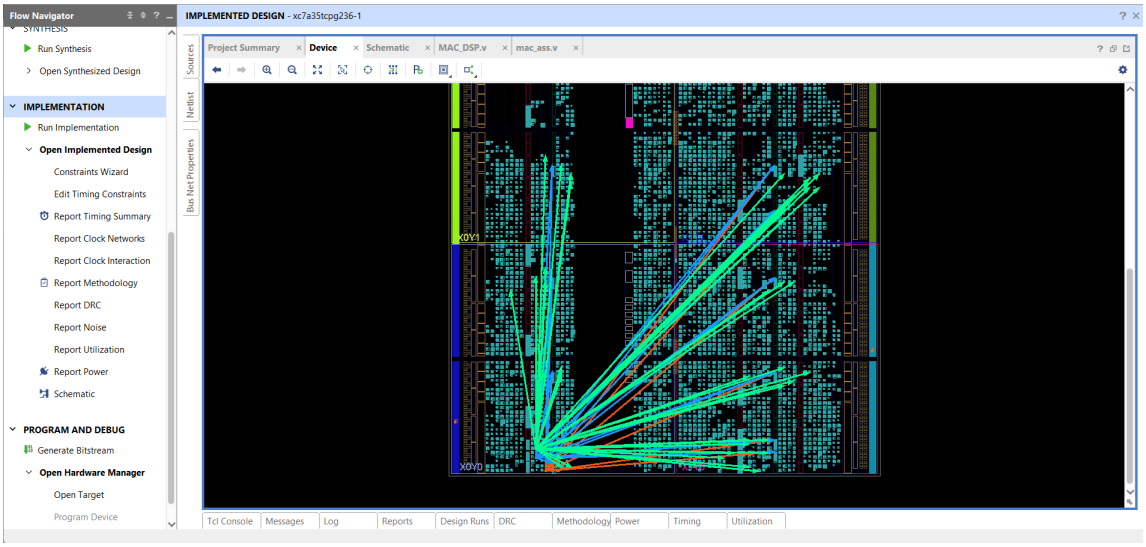
Wire Delay is the net delay of the critical path which is 4.408 for our design. We can use floorplanning principles and place related logic elements close together to shorten interconnect lengths.



BLOCK RAM'S PLACEMENT:-
These three colored blocks are the Block RAMs, the red ones being for a, blue ones being for b and yellow containing instances of c.



This diagram contains the connections between Block RAMs and DSP blocks. Three types of connections can be seen in the figure, Green ones, Blue ones and Orange ones.
Green ones connect c's BRAM to the 10 DSPs.
Blue ones connect b's BRAM to the 10 DSPs.
Orange ones connect a's BRAM to the 10 DSPs.


Flow Navigator
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Project Summary
Device
Schematic
MAC_DSP.v
mac_ass.v
Sources
Netlist
Bus Net Properties
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Utilization