

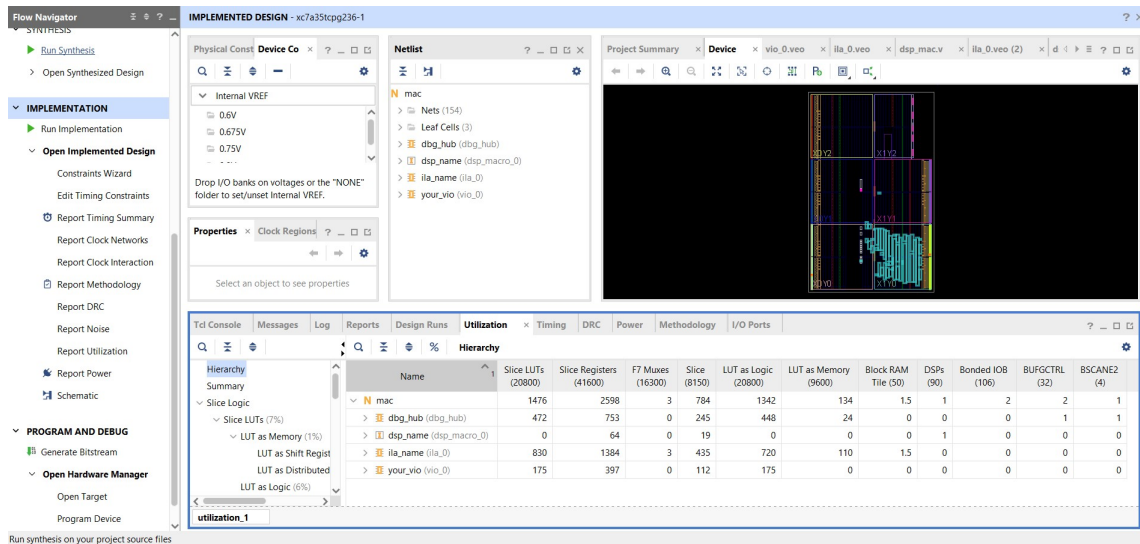
FPGA assignment 1

Siddharth Vikram(IMT2022534), Shreyas Biradar(IMT2022529), Aryaman Pathak(IMT2022513)

September 13, 2024

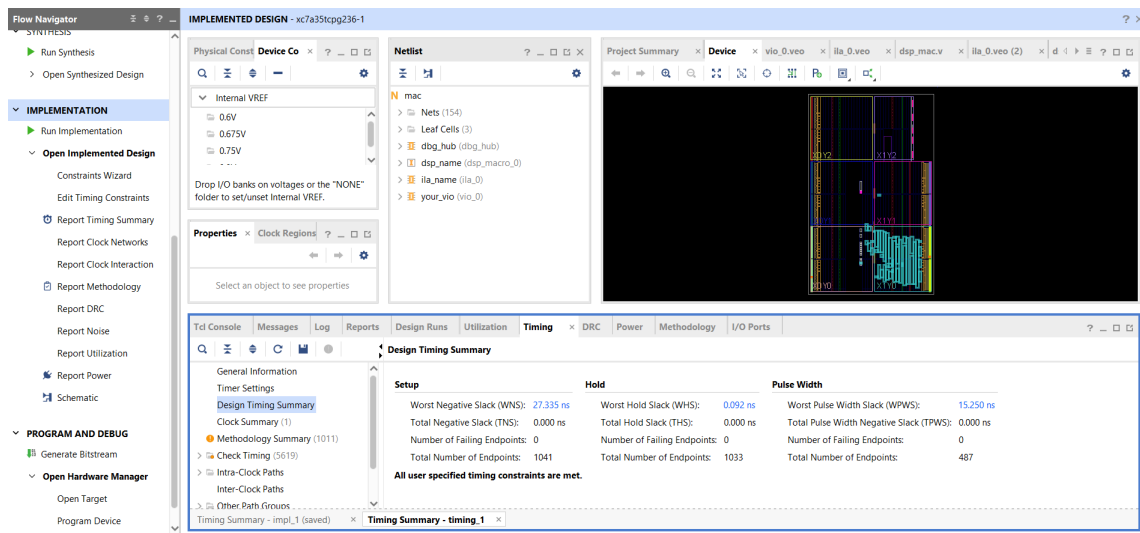
1 Question 1 - MAC-DSP

The image below represents the utilisation of the resources.



The figure gives the data that Slice Registers(64 of them) and one DSP block has been used for the MAC operation.

We can also see the timing report below.



2 Question 2

a slack difference of 0.946 is there between using DSPs or LUTs.

The screenshot shows the Xilinx Vivado IDE interface. The left sidebar contains the Flow Navigator with sections for RTL ANALYSIS, SYNTHESIS, IMPLEMENTATION, and PROGRAM AND DEBUG. The main workspace is divided into several panes: Physical Constraints, Device Constraints, Netlist, Project Summary, and a code editor showing the VHDL code for 'dsp_luts.v'. The 'Design Timing Summary' report is open, displaying the following data:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 26.389 ns	Worst Hold Slack (WHS): 0.095 ns	Worst Pulse Width Slack (WPWS): 15.250 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 1041	Total Number of Endpoints: 1033	Total Number of Endpoints: 487

Below the table, it states: "All user specified timing constraints are met."

There are more LUTs used towards logic and less towards memory when we are using LUTs instead of DSPs.

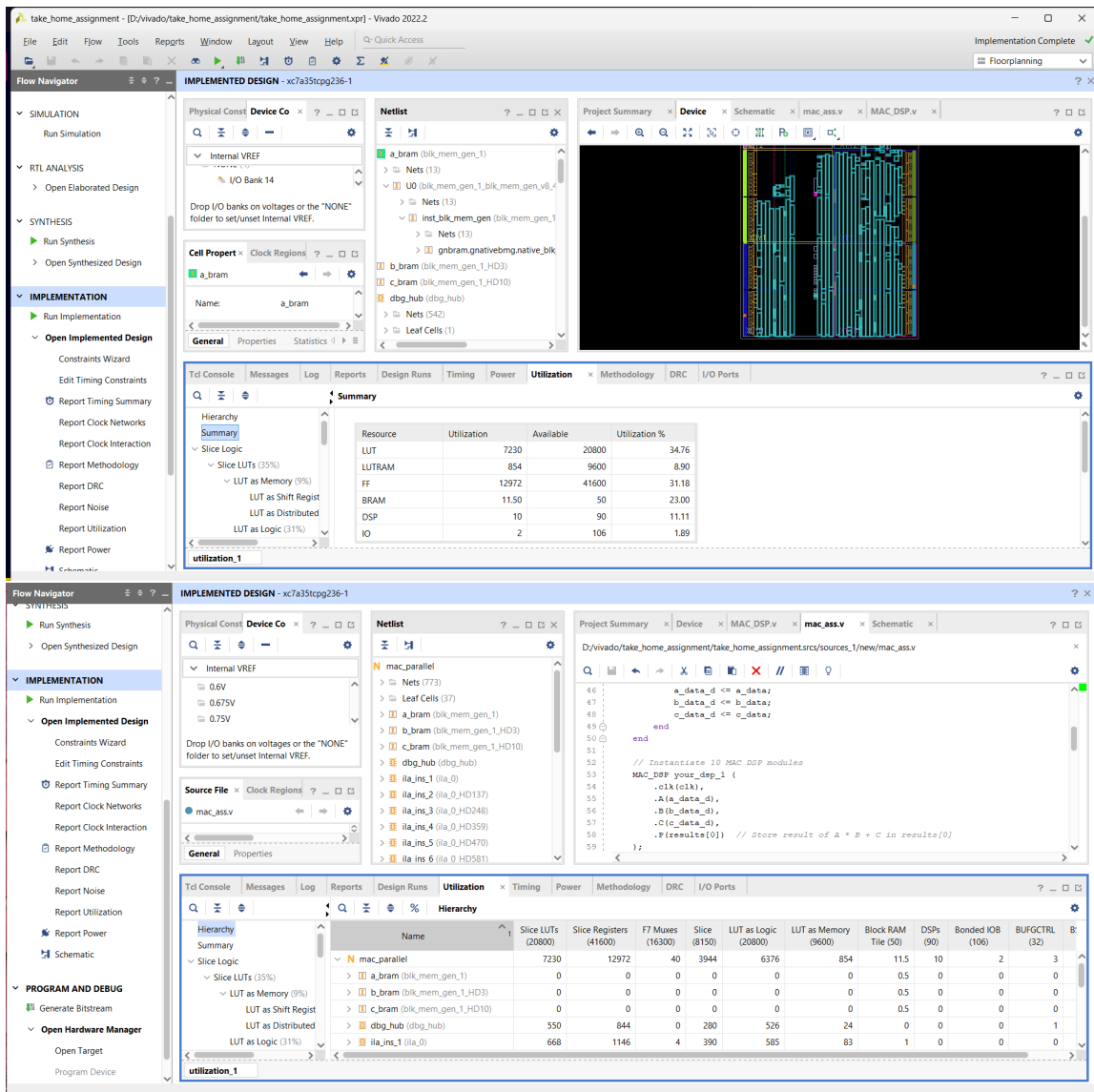
The screenshot shows the Xilinx Vivado IDE interface with the 'Utilization' report open. The report displays the following data:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANEN2 (4)
N mac	1547	2540	3	794	1418	129	1.5	2	2	1
dbq_hub (dbq_hub)	472	753	0	241	448	24	0	0	1	1
vio_name (vio_0)	172	391	0	105	172	0	0	0	0	0
your_instance_name (ila_0)	825	1380	3	450	720	105	1.5	0	0	0

3 Question 3

3.1 Part a

Basis3 board have 90 more DSP blocks that are available. Currently, we are using 10 DSP blocks for the MAC operations, so we can use a total of 100 DSP blocks in parallel at a time.



3.2 Part b

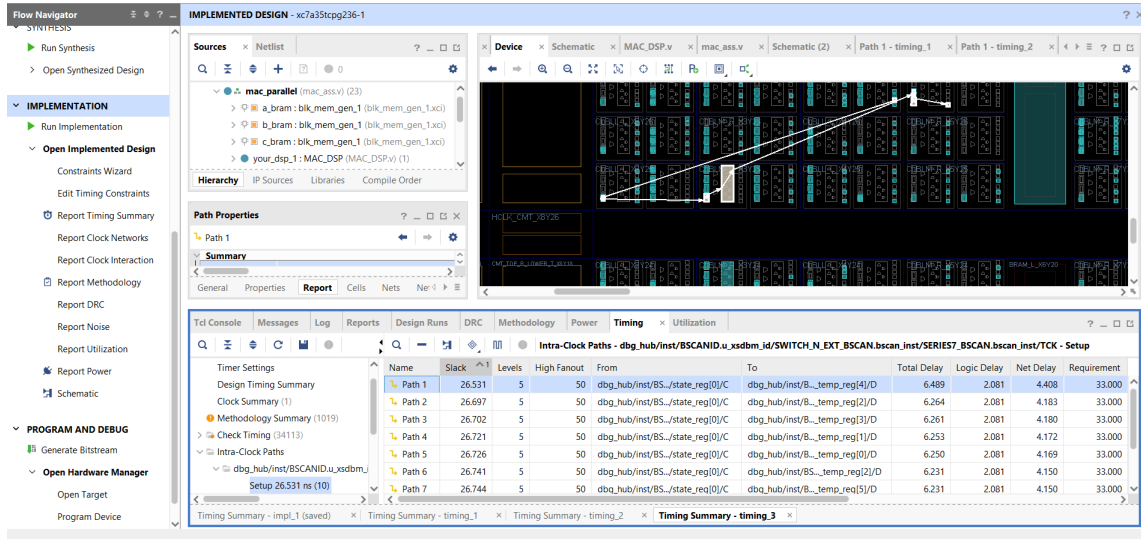
So the delay for the trigger of the 1st output is 5 clock cycle So for 10 dsp's the delay will be 50 ns.
So the Throughput for 1 sec will be:-

$$\text{Throughput} = 2 * 10^{-10}$$



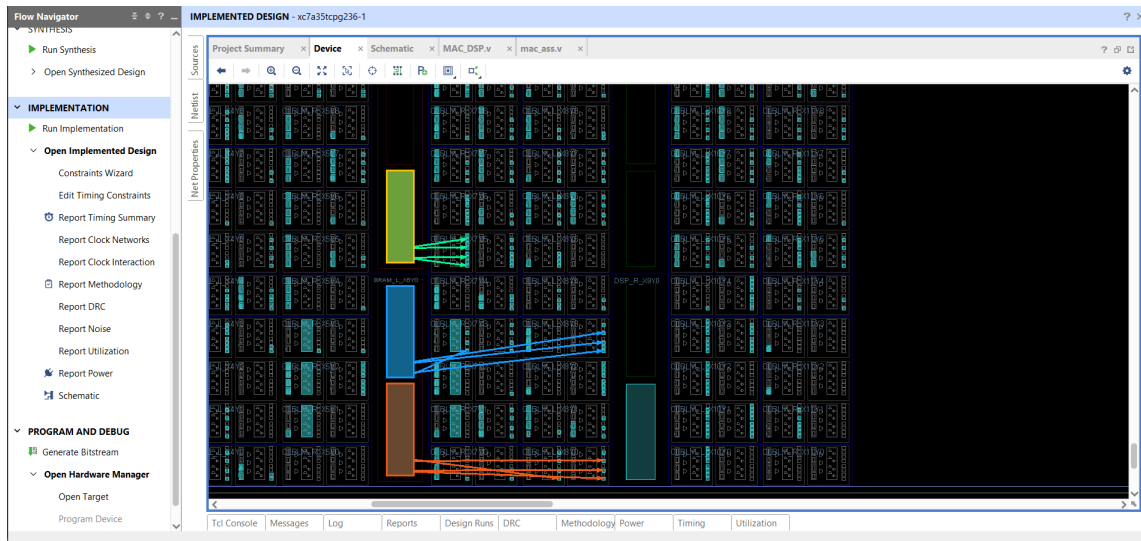
4 Question 4

Wire Delay is the net delay of the critical path which is 4.408 for our design. We can use floorplanning principles and place related logic elements close together to shorten interconnect lengths.



BLOCK RAM'S PLACEMENT:-

These three colored blocks are the Block RAMs, the red ones being for a, blue ones being for b and yellow containing instances of c.



This diagram contains the connections between Block RAMs and DSP blocks. Three types of connections can be seen in the figure, Green ones, Blue ones and Orange ones.

Green ones connect c's BRAM to the 10 DSPs.

Blue ones connect b's BRAM to the 10 DSPs.

Orange ones connect a's BRAM to the 10 DSPs.

