VL505 System design with FPGA
Sep 5 2024
Class assignment-1 (35 marks)
Duration: 1.5 hours

Create a report which should have the following:

- Your name, rollnumber
- Your group members name and roll number
- Solutions to the following questions with screenshots where necessary

A design that performs Multiply and accumulate (MAC) is provided to you along with the testbench.

1. Include a synchronous reset to the design. The MAC should be disabled when reset=1.
2. What is the maximum operating frequency of the design post implementation? (assuming ~50ps positive setup slack) Save a snapshot of this with slack. (5 marks)
3. Demonstrate the functionality of the MAC design along with the reset, on Basys3 board for the following inputs:
   1*5 + 7 = 12 (decimal). Show the output on LEDs, take the input through VIO. Show the output to the TA during the class. (10 marks)
4. Extra: Add an ILA and show the output on the ILA for two different input combinations (10 marks)
5. Eliminate the VIO. Read in 5 sets of a,b,c through a block RAM. You can use one or two r three blockRAMs. Show the output of the MAC on ILA (10 marks). Show this to the TA. Take a snapshot
6. Submit the following on LMS:
   1. Code (.v) and testbench (.v) only. Do not post entire vivado project
   2. Submit a report which contains
      1. Snapshot of slack from question 1.
      2. Max frequency achieved
      3. xdc
      4. Screenshot of the output on LEDs
      5. Screenshot of the output on ILA
      6. Screenshot for Q5