**VL505 System design with FPGA**
**Class assignment-2 (30 marks)**
**Duration: 90 minutes**

**Submission needs to be completed by the end of the class. Submissions done after the class do not carry any marks. This is a class-exam. Exam needs to be completed in the class.**

You should have a working MAC code of BlockRAM + ILA from the previous class assignment. Read in 3 sets of a,b,c through a block RAM as done in the previous class assignment.
If you do not have the Block RAM working, take the working code of the VIO+ ILA which you did in the previous class assignment. If you do not have this also working, get it to work first.

1. Now eliminate the ILA and direct the output to the 7-segment LED. The outputs for different input combinations should be displayed with a 10-12 second delay on the 7-segment. Show the demo to the TA. (20 marks)
2. Now, modify the a*b + c code to perform a + c. The inputs a and c should come from BlockRAMs. Direct the output to 7-segment and show the demo to the TA. (10 marks)

Submission:

- Submit your .v files on LMS- Write the names of your group members at the top of your .v files
- No need to upload snapshot of the FPGA board. These do not carry marks. The demo done in the class carries marks.