REV	Description	DATE	BY
A3	Production release.	10/21/2011	GC
A3A	Updated in conjunction with the release of the SRM. Typos and naming changes. No change in design.	11/5/2011	GC
A4	1. Changed supplier for the SD card connector due to availability issue. Created a dual footprint for two different parts. SD connector is now reversed, so label down is the new orientation. 2. Changed R76 from a 50 ohm to 49.9 ohm. Smaller package and lower cost. Changed footprint to 0402. 3. Changed C99 termination to DGND. 4. Added 10K pulldown to fix link speed LED. 5. Changed C7 to a 0805 package in PCB layout.	12/1/2011	GC
A5	1. Changed R219 to DNI. It was causing issues with Ethernet DHCP IP address aquisition. Will be added back in on revision A6. 2. Removed the connection of the VPP to VDD_CORE as suggested by TI.	2/3/2012	GC
A6	1. Changed R219 to installed. 2. Added R220 , a 10K pulldown to pin 18 of the SMSC PHY to allow R219 addition to work as expected.. 3. Removed the connection to the VPP pin on the processor. 4. Added R221, R218, R217, R202 to facilitate the addition of two signals, GPIO3_18 and GPIO3_19 to the expansion bus header to provide two more signals for the PRU access.. 5. Changed R210 to installed and added test point to allow the EEPROM to be programmed but with added protection to prevent corruption. Added Test Point to enable programming. 6. Moved Resistors R189 and R150 to provide more clearence around mounting hole. 7. PCB revision was changed to C2. 8. Change pullups on the boot pins to 42.2K per AM335x design team. 9. Rewired the JTAG reset signal from the optional JTAG connector. 10. R122 was removed becasue it was connectd to the wrong pin on the SMSC LAN8710. 11. R172 was removed due to a spurious reset generated by the FT2232 when under CCS, the target was connected.	5/10/2012	GC
A6A	1. Corrected typo on page 8 for correct pin on LAN8710A for MODE2 function.	6/28/2012	GC

PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3
4	PROCESSOR 2 OF 3
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	MEMORY
8	ETHERNET AND USB HOST
9	USB CONCENTRATOR
10	SERIAL AND JTAG
11	EXP CONN, uSD, AND LDO

NOTE: PCB Revision for this board is Rev C2.

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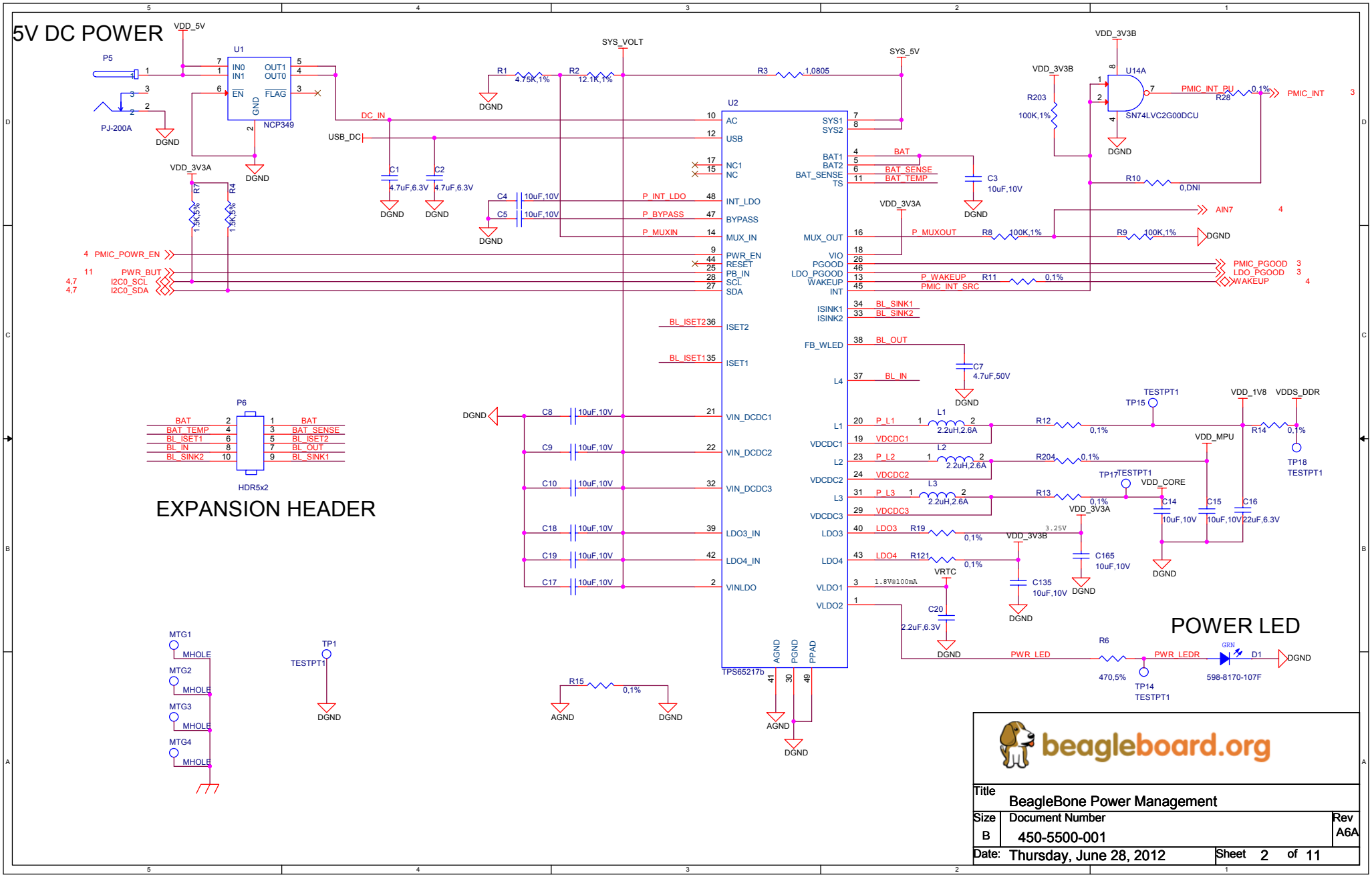
5V DC POWER
VDD_5V
P5
PJ-200A
U1
NCP349
IN0
IN1
EN
GND
OUT1
OUT0
FLAG
DGND
VDD_3V3A
R7
R4
1.5K,5%
DC_IN
USB_DC
C1
C2
4.7uF,6.3V
SYS_VOLT
R1
4.75K,1%
R2
12.1K,1%
R3
1,0805
SYS_5V
U2
AC
USB
NC1
NC
INT_LDO
BYPASS
MUX_IN
PWR_EN
RESET
PB_IN
SCL
SDA
ISET2
ISET1
VIN_DCDC1
VIN_DCDC2
VIN_DCDC3
LDO3_IN
LDO4_IN
VINLDO
TPS65217b
AGND
PGND
PPAD
C4
C5
10uF,10V
P_INT_LDO
P_BYPASS
P_MUXIN
PMIC_POWR_EN
PWR_BUT
I2C0_SCL
I2C0_SDA
BL_ISET2
BL_ISET1
C8
C9
C10
C18
C19
C17
SYS1
SYS2
BAT1
BAT2
BAT_SENSE
TS
MUX_OUT
VIO
PGOOD
LDO_PGOOD
WAKEUP
INT
ISINK1
ISINK2
FB_WLED
L4
BAT
BAT_SENSE
BAT_TEMP
C3
10uF,10V
P_MUXOUT
R8
100K,1%
R9
P_WAKEUP
R11
0,1%
PMIC_INT_SRC
BL_SINK1
BL_SINK2
BL_OUT
BL_IN
C7
4.7uF,50V
VDD_3V3B
U14A
SN74LVC2G00DCU
R203
100K,1%
PMIC_INT_PU
R28
PMIC_INT
R10
0,DNI
AIN7
PMIC_PGOOD
LDO_PGOOD
WAKEUP
P6
HDR5x2
BAT
BAT_TEMP
BL_ISET1
BL_IN
BL_SINK2
BAT_SENSE
BL_ISET2
BL_OUT
BL_SINK1
EXPANSION HEADER
L1
L2
L3
2.2uH,2.6A
P_L1
P_L2
P_L3
VDCDC1
VDCDC2
VDCDC3
R12
R204
R13
TESTPT1
TP15
TP17
TP18
VDD_1V8
VDDS_DDR
VDD_MPU
VDD_CORE
R14
C14
C15
C16
10uF,10V
22uF,6.3V
LDO3
LDO4
R19
R121
VRTC
1.8V@100mA
3.25V
C165
C135
C20
2.2uF,6.3V
VLDO1
VLDO2
PWR_LED
R6
470,5%
PWR_LEDR
D1
GRN
598-8170-107F
TP14
POWER LED
MTG1
MTG2
MTG3
MTG4
MHOLE
TP1
R15
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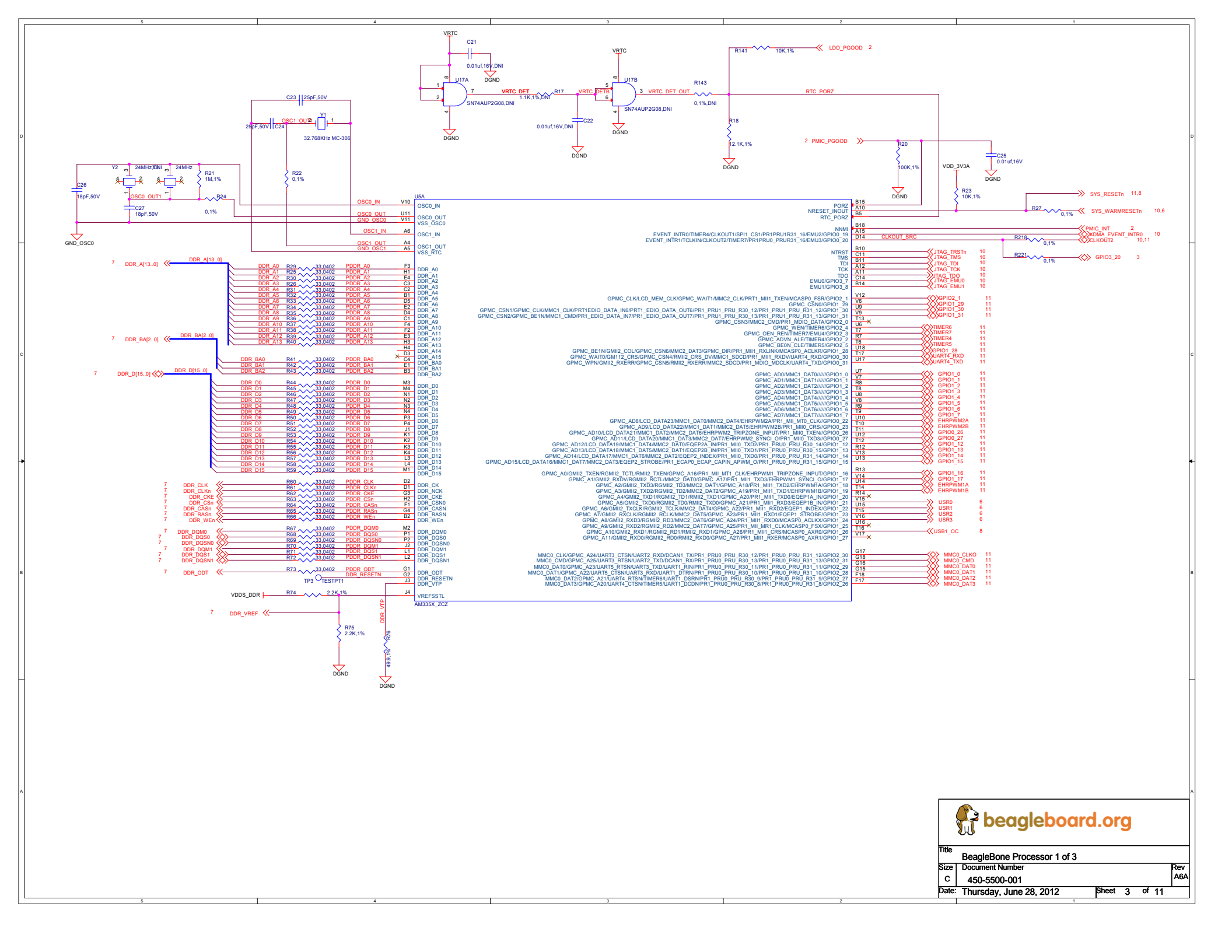
VRTC
C21
0.01uf,16V,DNI
DGND
U17A
SN74AUP2G08,DNI
VRTC_DET
R17
1.1K,1%,DNI
U17B
VRTC_DETB
VRTC_DET_OUT
R143
0,1%,DNI
C22
0.01uf,16V,DNI
R141
10K,1%
LDO_PGOOD 2
RTC_PORZ
R18
12.1K,1%
2 PMIC_PGOOD
R20
100K,1%
VDD_3V3A
C25
0.01uf,16V
R23
10K,1%
C23 25pF,50V
C24 25pF,50V
Y1
32.768KHz MC-306
OSC1_OUT
Y2 24MHz,DNI
24MHz
R21
1M,1%
R22
0,1%
R24
0,1%
C26
18pF,50V
C27
18pF,50V
GND_OSC0
OSC0_IN
OSC0_OUT
GND_OSC0
OSC1_IN
OSC1_OUT
GND_OSC1
U5A
OSC0_IN
OSC0_OUT
VSS_OSC0
OSC1_IN
OSC1_OUT
VSS_RTC
PORZ
NRESET_INOUT
RTC_PORZ
SYS_RESETn 11,8
R27
0,1%
SYS_WARMRESETn 10,6
NMI
EVENT_INTR0/TIMER4/CLKOUT1/SPI1_CS1/PR1PRU1R31_16/EMU2/GPIO0_19
EVENT_INTR1/TCLKIN/CLKOUT2/TIMER7/PR1PRU0_PRUR31_16/EMU3/GPIO0_20
PMIC_INT 2
XDMA_EVENT_INTR0 10
CLKOUT2 10,11
CLKOUT_SRC
R218
0,1%
R221
0,1%
GPIO3_20 3
NTRST
TMS
TDI
TCK
TDO
EMU0/GPIO3_7
EMU1/GPIO3_8
JTAG_TRSTn 10
JTAG_TMS 10
JTAG_TDI 10
JTAG_TCK 10
JTAG_TDO 10
JTAG_EMU0 10
JTAG_EMU1 10
DDR_A[13..0]
DDR_A0 R29 33,0402 PDDR_A0 F3
DDR_A1 R25 33,0402 PDDR_A1 H1
DDR_A2 R39 33,0402 PDDR_A2 E4
DDR_A3 R26 33,0402 PDDR_A3 C3
DDR_A4 R31 33,0402 PDDR_A4 C2
DDR_A5 R32 33,0402 PDDR_A5 B1
DDR_A6 R33 33,0402 PDDR_A6 D5
DDR_A7 R34 33,0402 PDDR_A7 E2
DDR_A8 R35 33,0402 PDDR_A8 D4
DDR_A9 R36 33,0402 PDDR_A9 C1
DDR_A10 R37 33,0402 PDDR_A10 F4
DDR_A11 R38 33,0402 PDDR_A11 F2
DDR_A12 R39 33,0402 PDDR_A12 E3
DDR_A13 R40 33,0402 PDDR_A13 H3
DDR_BA[2..0]
DDR_BA0 R41 33,0402 PDDR_BA0 C4
DDR_BA1 R42 33,0402 PDDR_BA1 E1
DDR_BA2 R43 33,0402 PDDR_BA2 B3
DDR_D[15..0]
DDR_D0 R44 33,0402 PDDR_D0 M3
DDR_D1 R45 33,0402 PDDR_D1 M4
DDR_D2 R46 33,0402 PDDR_D2 N1
DDR_D3 R47 33,0402 PDDR_D3 N2
DDR_D4 R48 33,0402 PDDR_D4 N3
DDR_D5 R49 33,0402 PDDR_D5 N4
DDR_D6 R50 33,0402 PDDR_D6 P3
DDR_D7 R51 33,0402 PDDR_D7 P4
DDR_D8 R52 33,0402 PDDR_D8 J1
DDR_D9 R53 33,0402 PDDR_D9 K1
DDR_D10 R54 33,0402 PDDR_D10 K2
DDR_D11 R55 33,0402 PDDR_D11 K3
DDR_D12 R56 33,0402 PDDR_D12 K4
DDR_D13 R57 33,0402 PDDR_D13 L3
DDR_D14 R58 33,0402 PDDR_D14 L4
DDR_D15 R59 33,0402 PDDR_D15 M1
DDR_CLK R60 33,0402 PDDR_CLK D2
DDR_CLKn R61 33,0402 PDDR_CLKn D1
DDR_CKE R62 33,0402 PDDR_CKE G3
DDR_CSn R63 33,0402 PDDR_CSn H2
DDR_CASn R64 33,0402 PDDR_CASn F1
DDR_RASn R65 33,0402 PDDR_RASn G4
DDR_WEn R66 33,0402 PDDR_WEn B2
DDR_DQM0 R67 33,0402 PDDR_DQM0 M2
DDR_DQS0 R68 33,0402 PDDR_DQS0 P1
DDR_DQSN0 R69 33,0402 PDDR_DQSN0 P2
DDR_DQM1 R70 33,0402 PDDR_DQM1 J2
DDR_DQS1 R71 33,0402 PDDR_DQS1 L1
DDR_DQSN1 R72 33,0402 PDDR_DQSN1 L2
DDR_ODT R73 33,0402 PDDR_ODT G1
DDR_RESETN G2
TP3 TESTPT1
DDR_VTP J3
VDDS_DDR R74 2.2K,1%
DDR_VREF
R75 2.2K,1%
R76 49.9,1%
DDR_VTP
DGND
AM335X_ZCZ
GPMC_CLK/LCD_MEM_CLK/GPMC_WAIT1/MMC2_CLK/PRT1_MII1_TXEN/MCASP0_FSR/GPIO2_1
GPMC_CSN0/GPIO1_29
GPMC_CSN1/GPMC_CLK/MMC1_CLK/PRT1EDIO_DATA_IN6/PRT1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30
GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31
GPMC_CSN3/MMC2_CMD/PR1_MDIO_DATA/GPIO2_0
GPMC_WEN/TIMER6/GPIO2_4
GPMC_OEN_REN/TIMER7/EMU4/GPIO2_3
GPMC_ADVN_ALE/TIMER4/GPIO2_2
GPMC_BEON_CLE/TIMER5/GPIO2_5
GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28
GPMC_WAIT0/GMII2_CRS/GPMC_CSN4/RMII2_CRS_DV/MMC1_SDCD/PR1_MII1_RXDV/UART4_RXD/GPIO0_30
GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MDIO_MDCLK/UART4_TXD/GPIO0_31
GPIO2_1 11
GPIO1_29 11
GPIO1_30 11
GPIO1_31 11
TIMER6 11
TIMER7 11
TIMER4 11
TIMER5 11
GPIO1_28 11
UART4_RXD 11
UART4_TXD 11
GPMC_AD0/MMC1_DAT0//////GPIO1_0
GPMC_AD1/MMC1_DAT1//////GPIO1_1
GPMC_AD2/MMC1_DAT2//////GPIO1_2
GPMC_AD3/MMC1_DAT3//////GPIO1_3
GPMC_AD4/MMC1_DAT4//////GPIO1_4
GPMC_AD5/MMC1_DAT5//////GPIO1_5
GPMC_AD6/MMC1_DAT6//////GPIO1_6
GPMC_AD7/MMC1_DAT7//////GPIO1_7
GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2A/PR1_MII_MT0_CLK//GPIO0_22
GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/PR1_MII0_CRS//GPIO0_23
GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN//GPIO0_26
GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/EHRPWM2_SYNCI_O/PR1_MII0_TXD3//GPIO0_27
GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12
GPMC_AD13/LCD_DATA18/MMC1_DAT5/MMC2_DAT1/EQEP2B_IN/PR1_MII0_TXD1/PR1_PRU0_PRU_R30_15/GPIO1_13
GPMC_AD14/LCD_DATA17/MMC1_DAT6/MMC2_DAT2/EQEP2_INDEX/PR1_MII0_TXD0/PR1_PRU0_PRU_R31_14/GPIO1_14
GPMC_AD15/LCD_DATA16/MMC1_DAT7/MMC2_DAT3/EQEP2_STROBE/PR1_ECAP0_ECAP_CAPIN_APWM_O/PR1_PRU0_PRU_R31_15/GPIO1_15
GPIO1_0 11
GPIO1_1 11
GPIO1_2 11
GPIO1_3 11
GPIO1_4 11
GPIO1_5 11
GPIO1_6 11
GPIO1_7 11
EHRPWM2A 11
EHRPWM2B 11
GPIO0_26 11
GPIO0_27 11
GPIO1_12 11
GPIO1_13 11
GPIO1_14 11
GPIO1_15 11
GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16
GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/PR1_MII1_TXD3/EHRPWM1_SYNCI_O/GPIO1_17
GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/PR1_MII1_TXD2/EHRPWM1A/GPIO1_18
GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/PR1_MII1_TXD1/EHRPWM1B/GPIO1_19
GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20
GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21
GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22
GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23
GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24
GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25
GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/PR1_MII1_CRS/MCASP0_AXR0/GPIO1_26
GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27
R13
R14
V14
U14
T14
R15
V15
U15
T15
V16
U16
T16
V17
GPIO1_16 11
GPIO1_17 11
EHRPWM1A 11
EHRPWM1B 11
USR0 6
USR1 6
USR2 6
USR3 6
USB1_OC 8
MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30
MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31
MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29
MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28
MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27
MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26
G17
G18
G16
G15
F18
F17
MMC0_CLKO 11
MMC0_CMD 11
MMC0_DAT0 11
MMC0_DAT1 11
MMC0_DAT2 11
MMC0_DAT3 11
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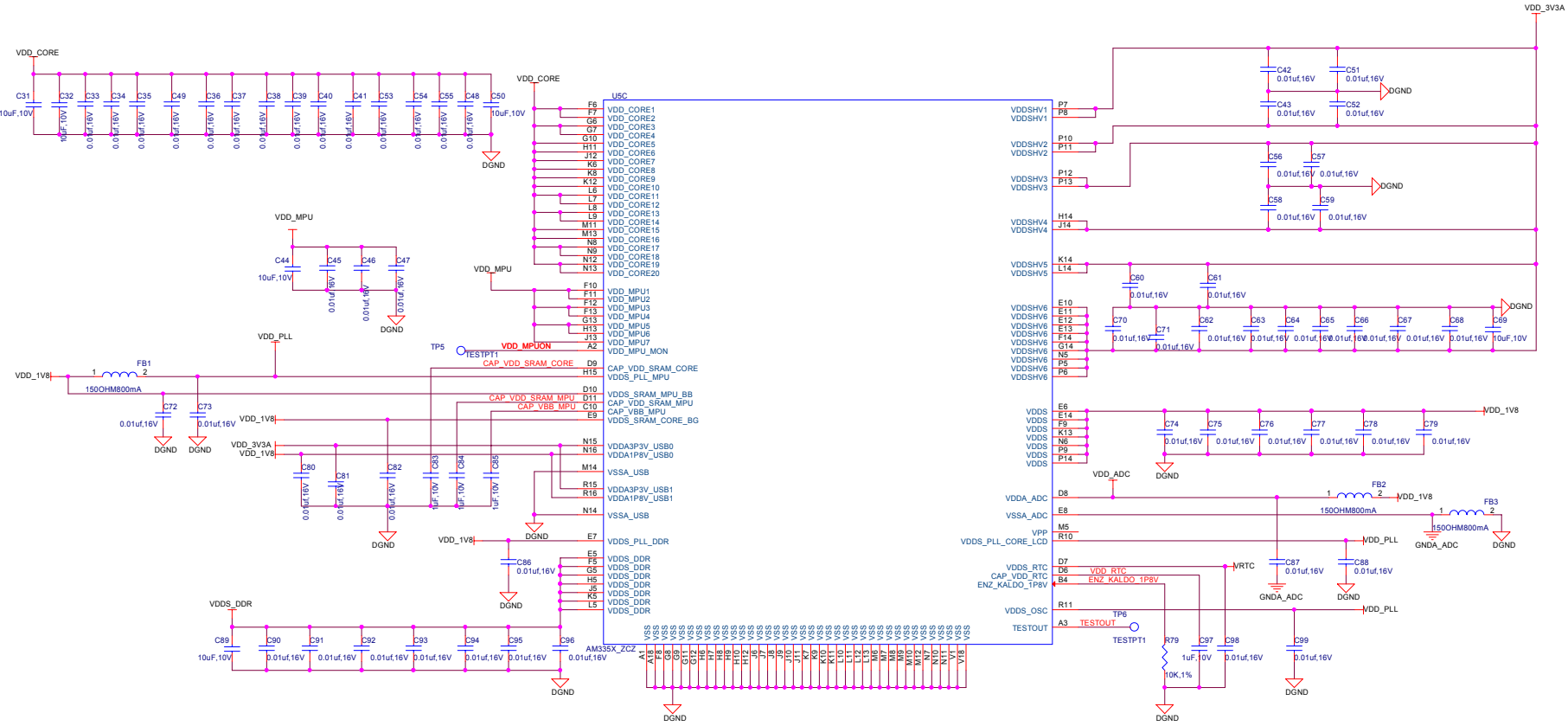

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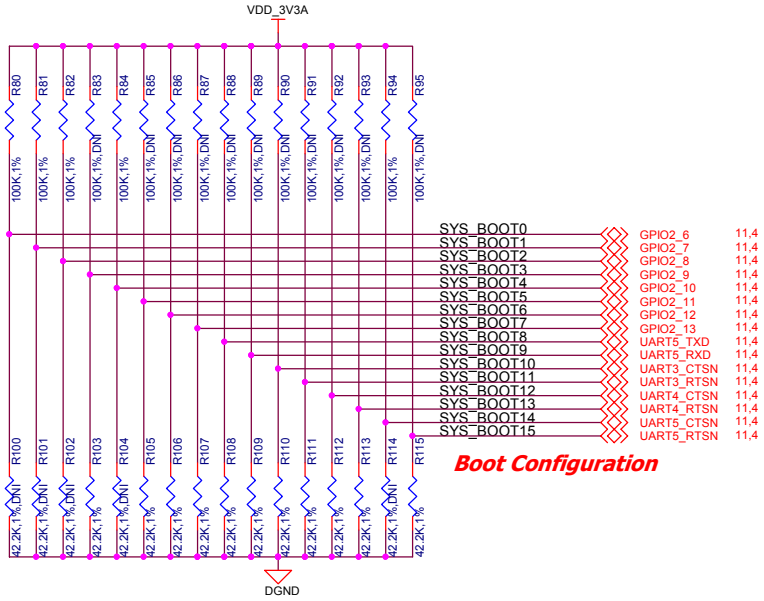
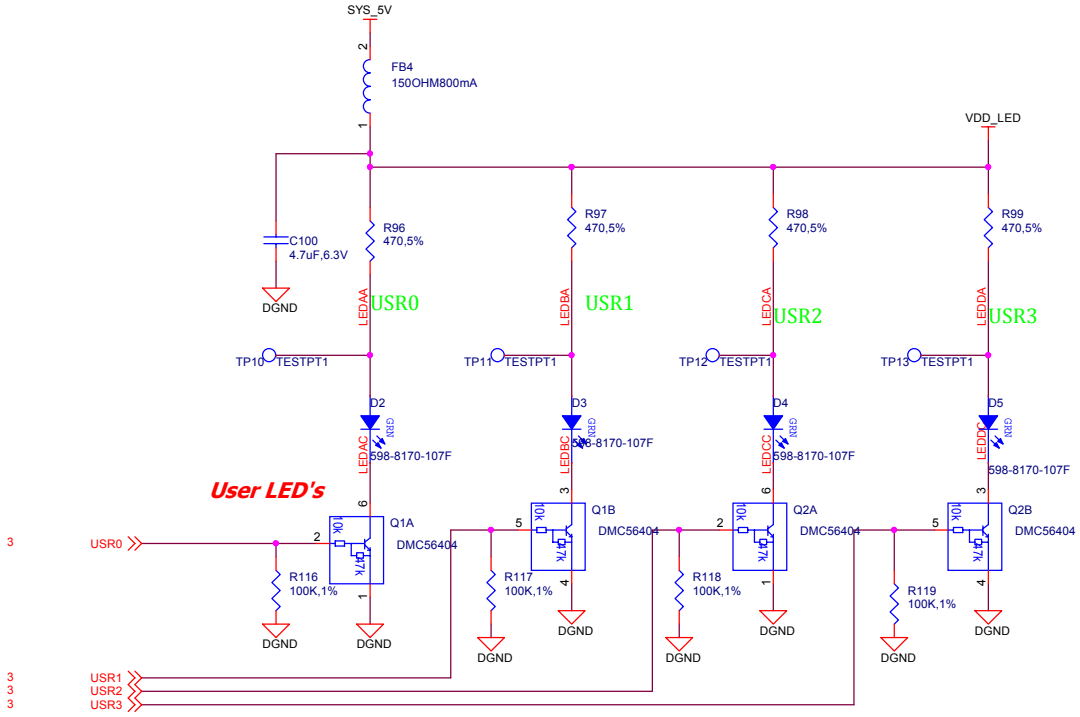
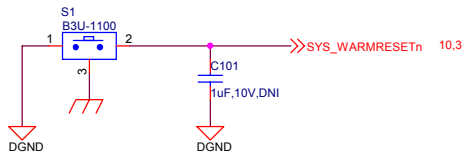


BOOT ORDER....MMC....SPI....UART....USB.....24MHZ



RESET BUTTON



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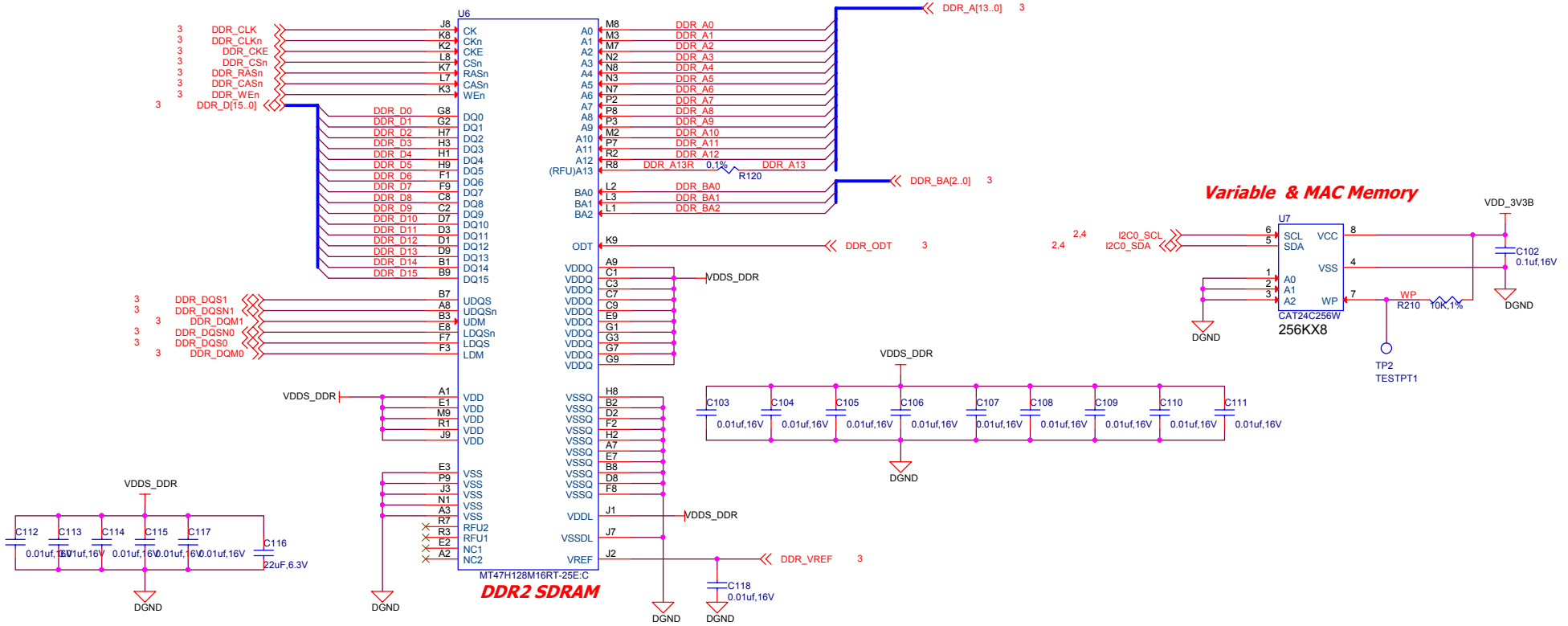

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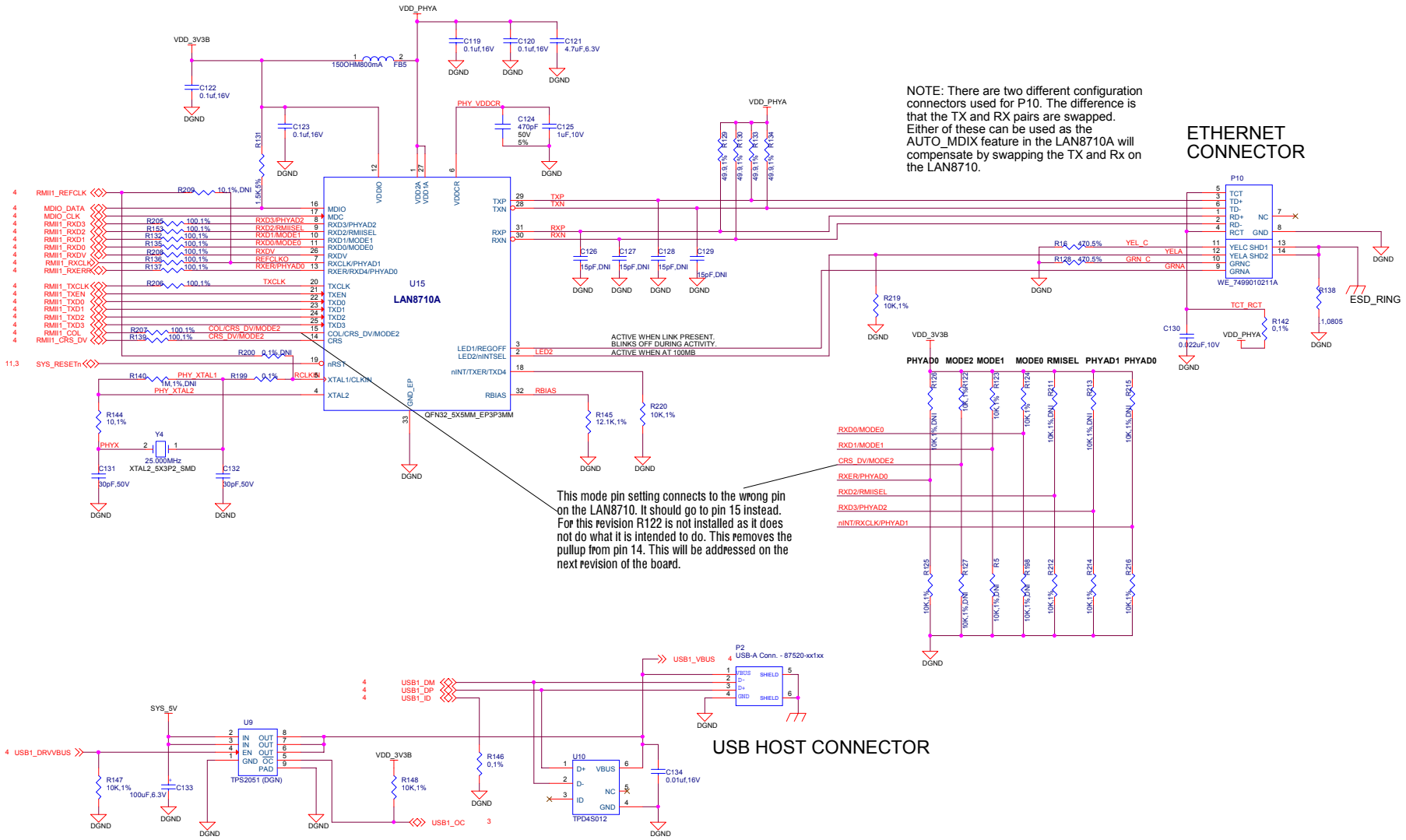

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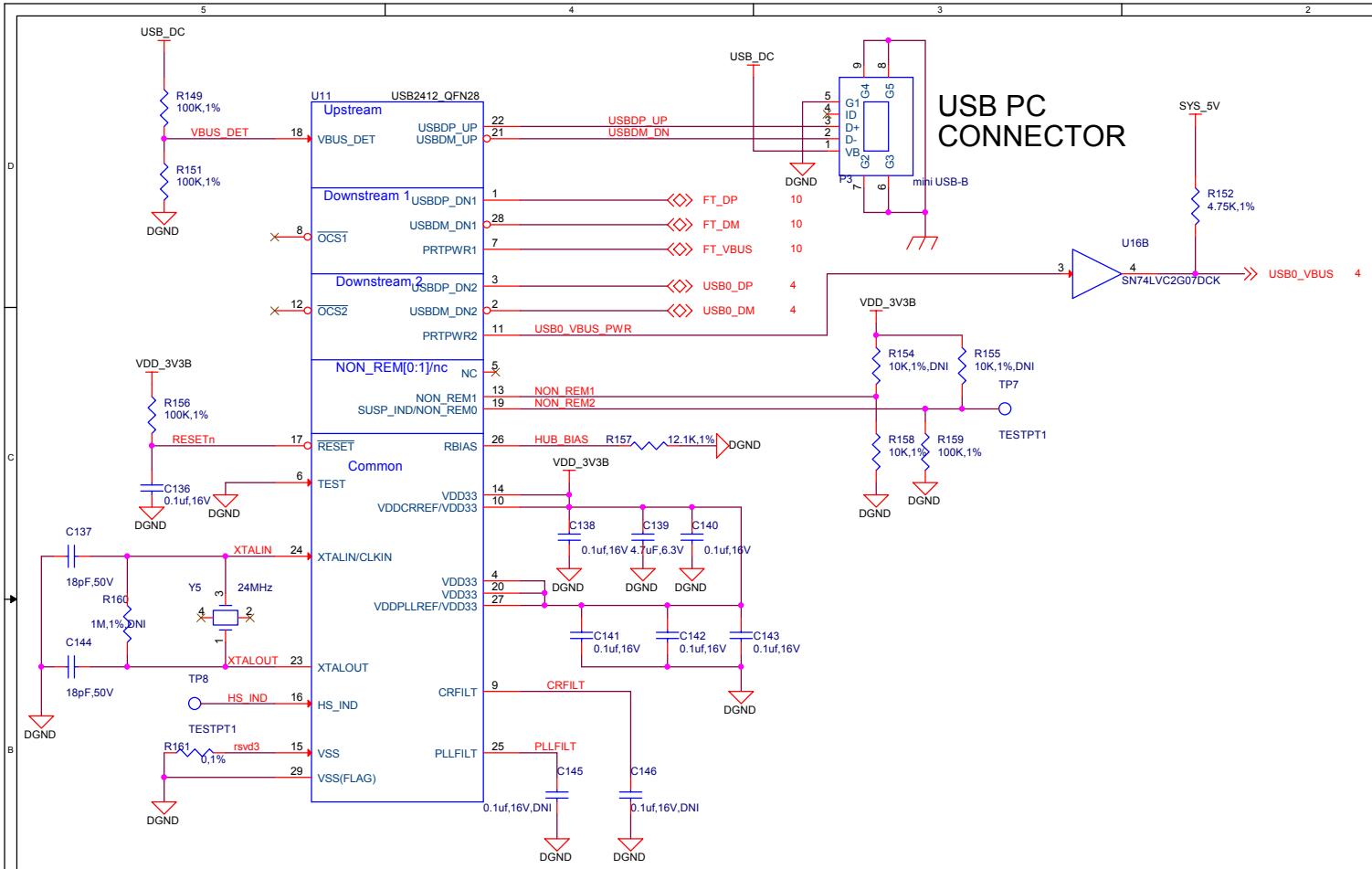

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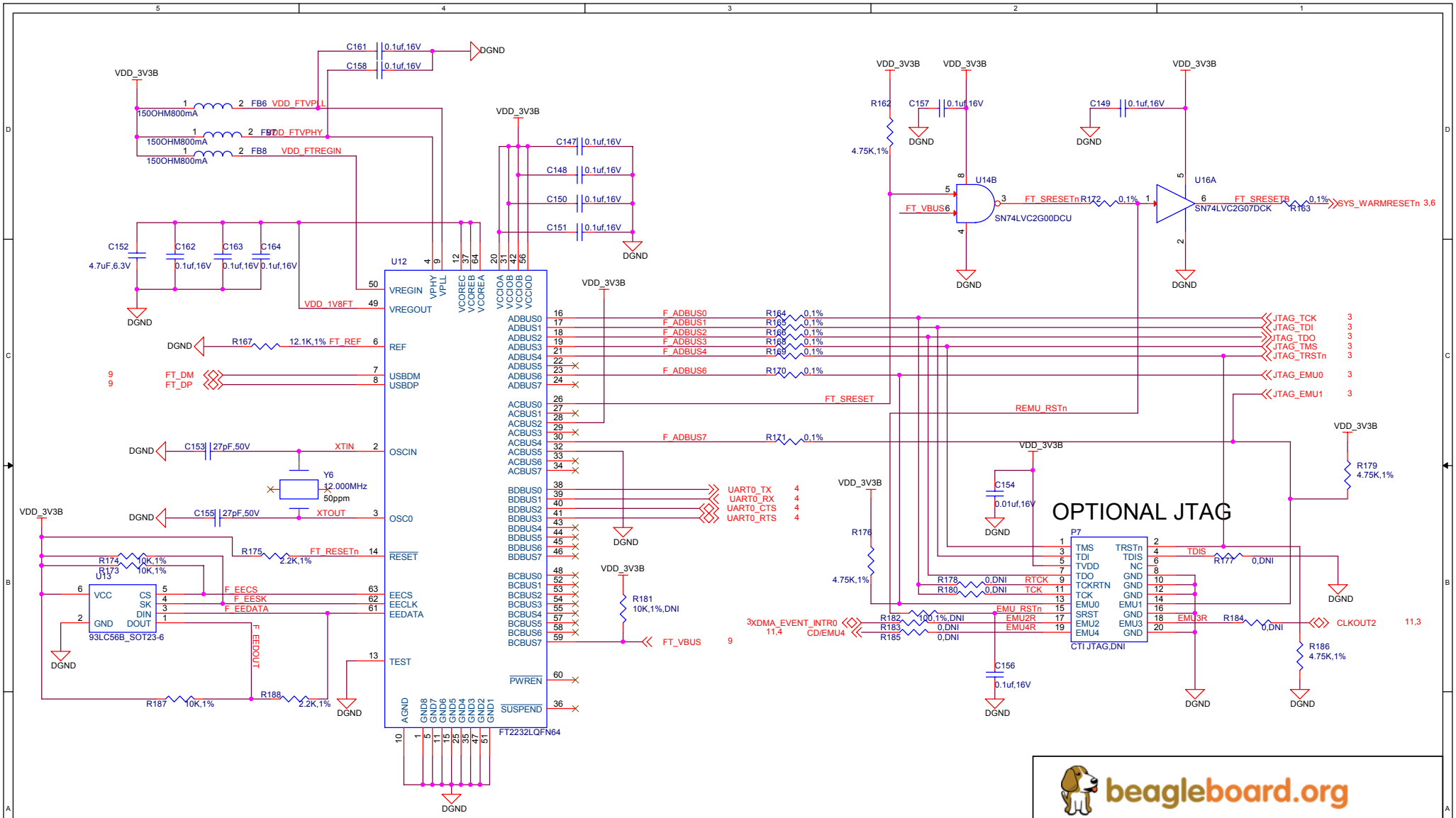
C161 0.1uf,16V
C158 0.1uf,16V
DGND
VDD_3V3B
150OHM800mA
FB6 VDD_FTVPLL
FB7 VDD_FTVPHY
FB8 VDD_FTREGIN
C152 4.7uF,6.3V
C162 0.1uf,16V
C163 0.1uf,16V
C164 0.1uf,16V
U12
VREGIN
VREGOUT
VDD_1V8FT
REF
R167 12.1K,1% FT_REF
USBDM
USBDP
FT_DM
FT_DP
C153 27pF,50V
XTIN
Y6
12.000MHz
50ppm
C155 27pF,50V
XTOUT
OSCIN
OSC0
RESET
FT_RESETn
R175 2.2K,1%
R174 10K,1%
R173 10K,1%
U13
93LC56B_SOT23-6
VCC
GND
CS
SK
DIN
DOUT
F_EECS
F_EESK
F_EEDATA
EECS
EECLK
EEDATA
EEDOUT
TEST
R187 10K,1%
R188 2.2K,1%
C147 0.1uf,16V
C148 0.1uf,16V
C150 0.1uf,16V
C151 0.1uf,16V
VPHY
VPLL
VCOREC
VCOREB
VCOREA
VCCIOA
VCCIOB
VCCIOC
VCCIOD
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
PWREN
SUSPEND
AGND
GND8
GND7
GND6
GND5
GND4
GND3
GND2
GND1
FT2232LQFN64
F_ADBUS0
F_ADBUS1
F_ADBUS2
F_ADBUS3
F_ADBUS4
F_ADBUS6
F_ADBUS7
R164 0,1%
R165 0,1%
R166 0,1%
R168 0,1%
R169 0,1%
R170 0,1%
R171 0,1%
FT_SRESET
UART0_TX
UART0_RX
UART0_CTS
UART0_RTS
R181 10K,1%,DNI
FT_VBUS
R162 4.75K,1%
C157 0.1uf,16V
C149 0.1uf,16V
U14B
SN74LVC2G00DCU
FT_VBUS
FT_SRESETn
R172 0,1%
U16A
SN74LVC2G07DCK
FT_SRESETR
R163 0,1%
SYS_WARMRESETn
REMU_RSTn
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRSTn
JTAG_EMU0
JTAG_EMU1
C154 0.01uf,16V
R176 4.75K,1%
R179 4.75K,1%
OPTIONAL JTAG
P7
TMS
TDI
TVDD
TDO
TCKRTN
TCK
SRST
EMU0
EMU2
EMU4
TRSTn
TDIS
NC
GND
EMU1
EMU3
R177 0,DNI
R178 0,DNI
R180 0,DNI
RTCK
TCK
EMU_RSTn
EMU2R
EMU4R
R182 100,1%,DNI
R183 0,DNI
R185 0,DNI
XDMA_EVENT_INTR0
CD/EMU4
CTI JTAG,DNI
C156 0.1uf,16V
R184 0,DNI
CLKOUT2
R186 4.75K,1%
EMU3R
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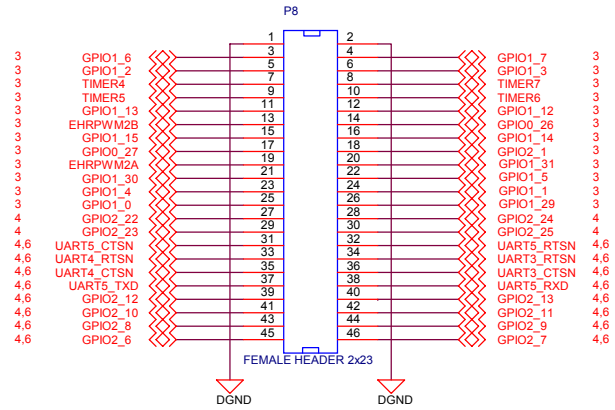
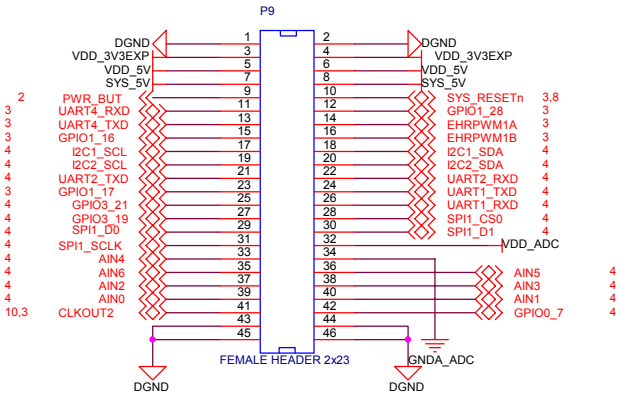
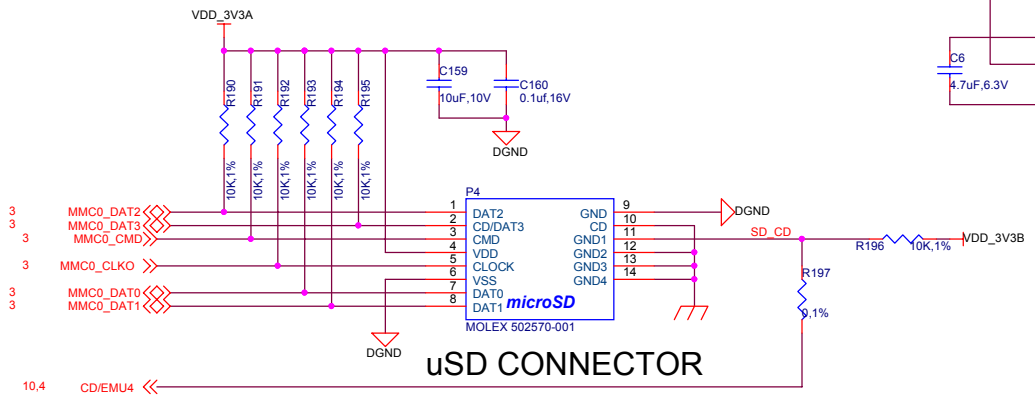


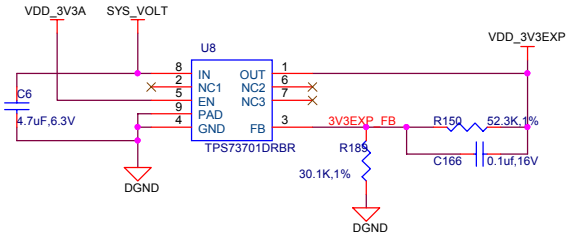
EXPANSION HEADER



EXPANSION HEADER



uSD CONNECTOR



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