

REV	Description	DATE	BY
A3	Production release.	10/21/2011	GC
A3A	Updated in conjunction with the release of the SRM. Typos and naming changes. No change in design.	11/5/2011	GC
A4	1. Changed supplier for the SD card connector due to availability issue. Created a dual footprint for two different parts. SD connector is now reversed, so label down is the new orientation. 2. Changed R76 from a 50 ohm to 49.9 ohm. Smaller package and lower cost. Changed footprint to 0402. 3. Changed C99 termination to DGND. 4. Added 10K pulldown to fix link speed LED. 5. Changed C7 to a 0805 package in PCB layout.	12/1/2011	GC
A5	1. Changed R219 to DNI. It was causing issues with Ethernet DHCP IP address aquisition. Will be added back in on revision A6. 2. Removed the connection of the VPP to VDD_CORE as suggested by TI.	2/3/2012	GC
A6	1. Changed R219 to installed. 2. Added R220 , a 10K pulldown to pin 18 of the SMSC PHY to allow R219 addition to work as expected.. 3. Removed the connection to the VPP pin on the processor. 4. Added R221, R218, R217, R202 to facilitate the addition of two signals, GPIO3_18 and GPIO3_19 to the expansion bus header to provide two more signals for the PRU access.. 5. Changed R210 to installed and added test point to allow the EEPROM to be programmed but with added protection to prevent corruption. Added Test Point to enable programming. 6. Moved Resistors R189 and R150 to provide more clearance around mounting hole. 7. PCB revision was changed to C2. 8. Change pullups on the boot pins to 42.2K per AM335x design team. 9. Rewired the JTAG reset signal from the optional JTAG connector. 10. R122 was removed because it was connectd to the wrong pin on the SMSC LAN8710. 11. R172 was removed due to a spurious reset generated by the FT2232 when under CCS, the target was connected.	5/10/2012	GC
A6A	1. Corrected typo on page 8 for correct pin on LAN8710A for MODE2 function.	6/28/2012	GC

PAGE NO.	SCHEMATIC PAGE
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8	ETHERNET AND USB HOST
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10	SERIAL AND JTAG
11	EXP CONN, uSD, AND LDO

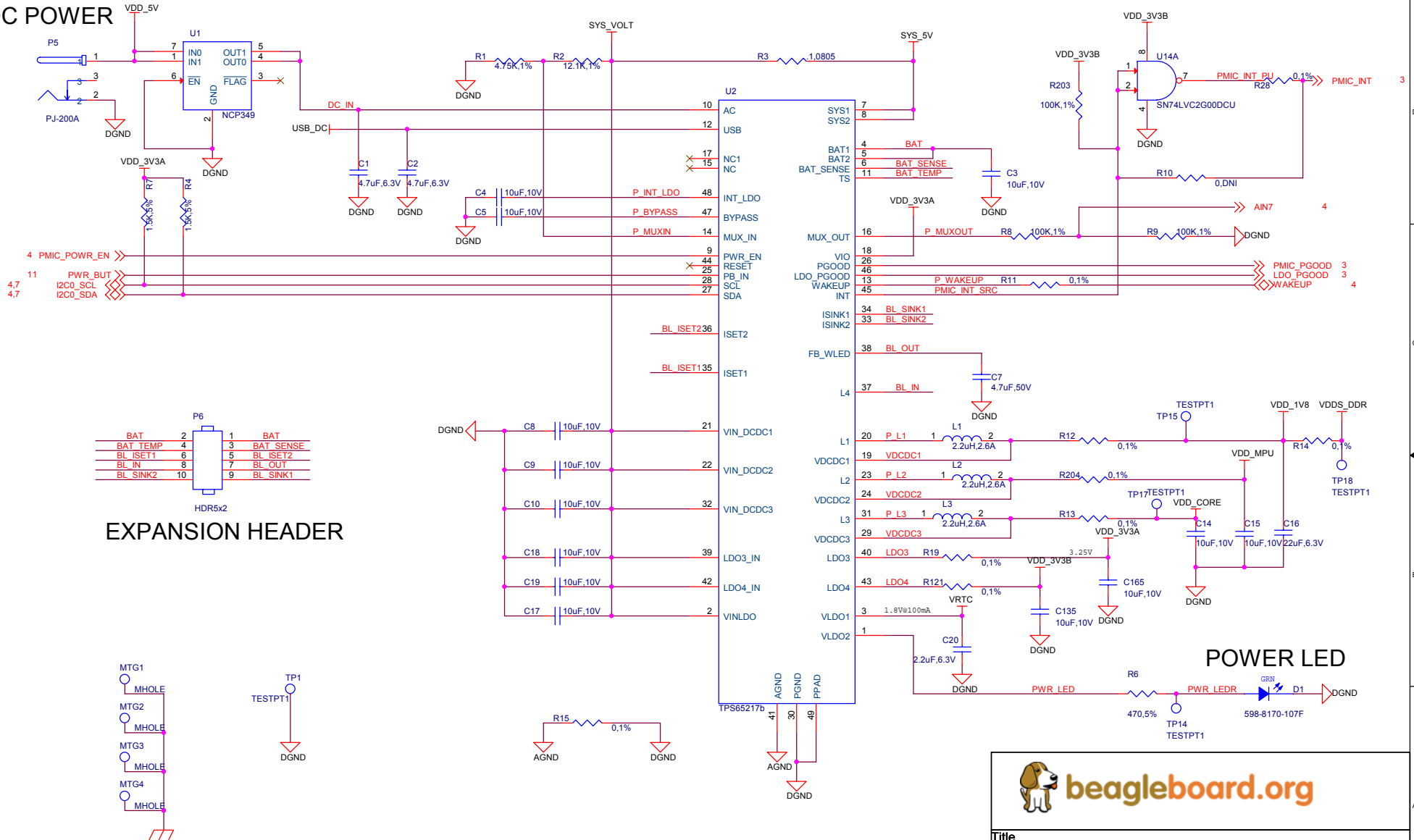
NOTE: PCB Revision for this board is Rev C2.

This schematic is **\*NOT SUPPORTED\*** and DOES NOT constitute a reference design. Only "community" support is allowed via resources at [BeagleBoard.org/discuss](http://BeagleBoard.org/discuss).

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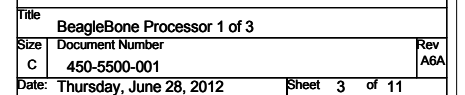
 <b>beagleboard.org</b>		
Title	BeagleBone Cover Page	
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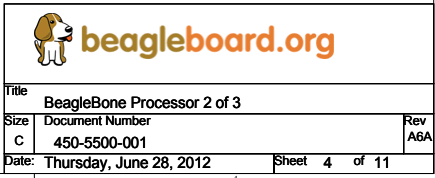
# 5V DC POWER

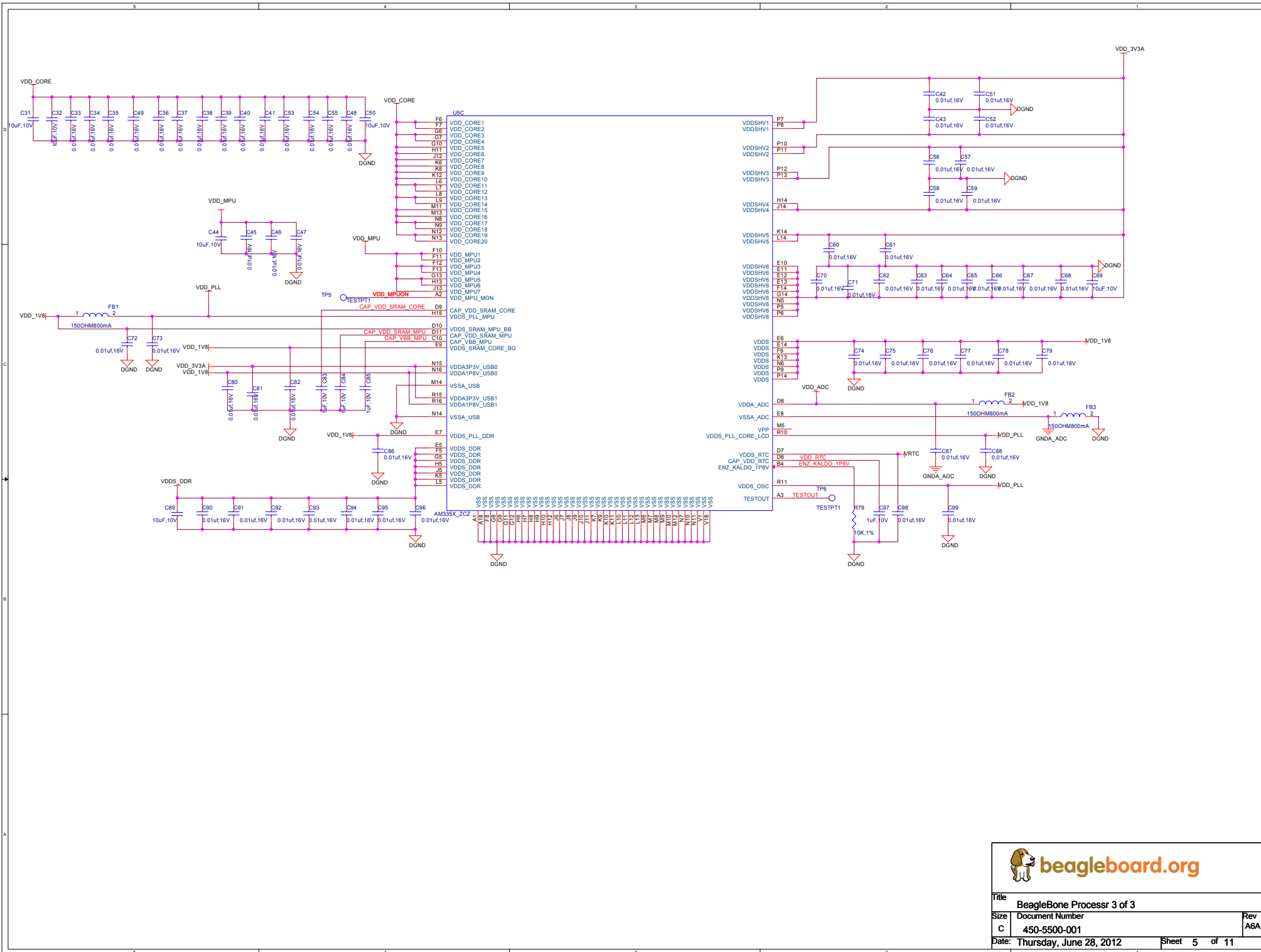


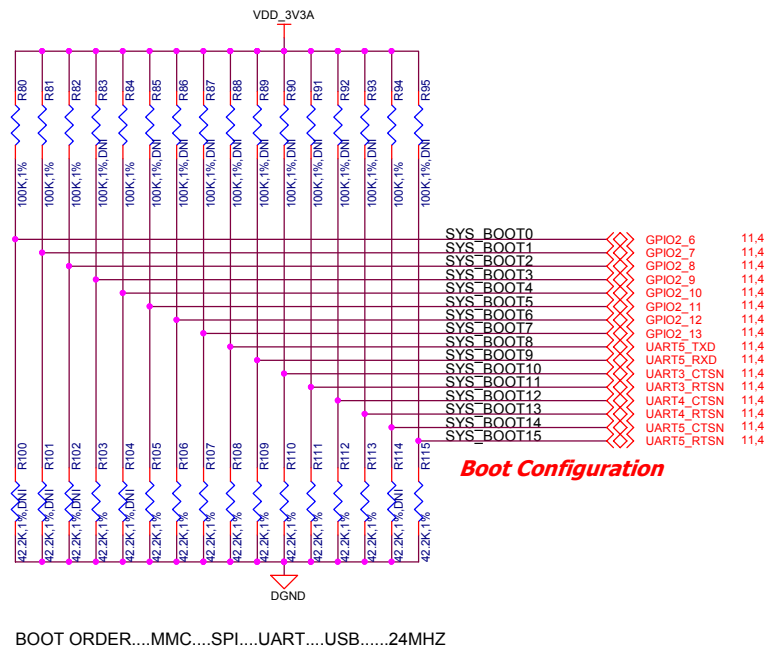
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Title		
BeagleBone Power Management		
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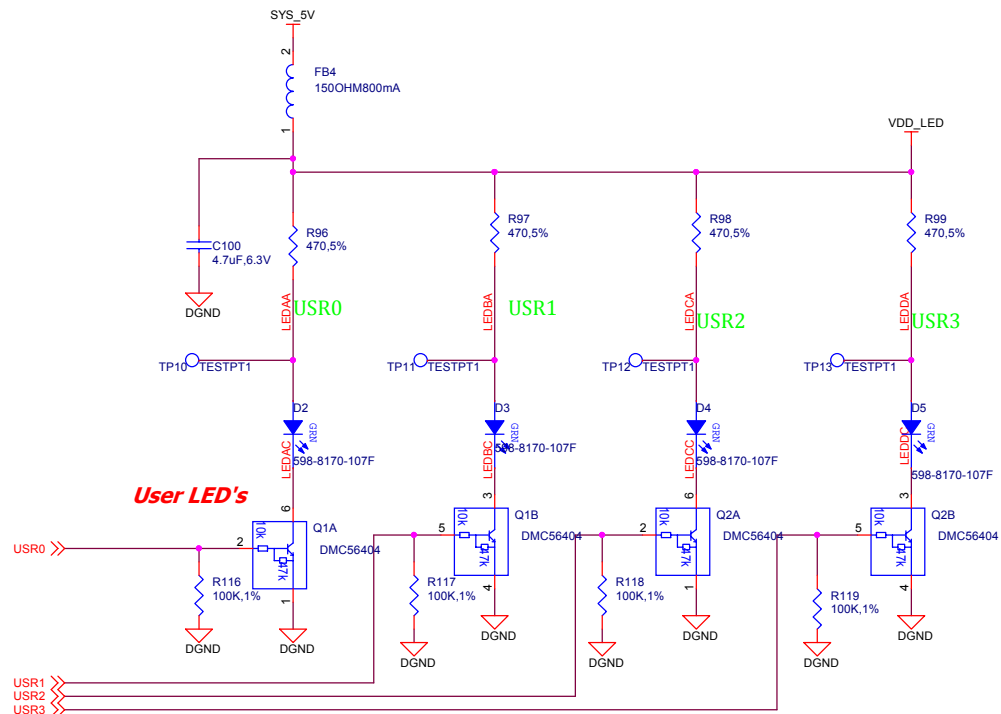




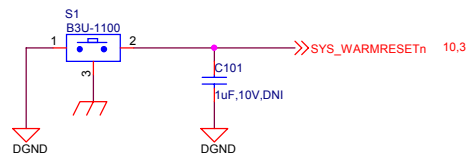




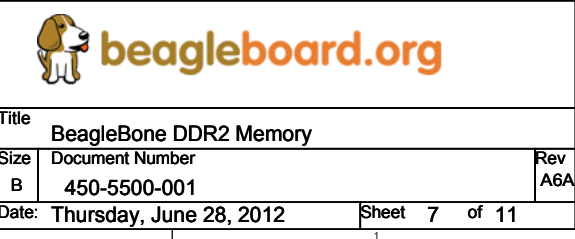
BOOT ORDER.....MMC.....SPI.....UART.....USB.....24MHZ

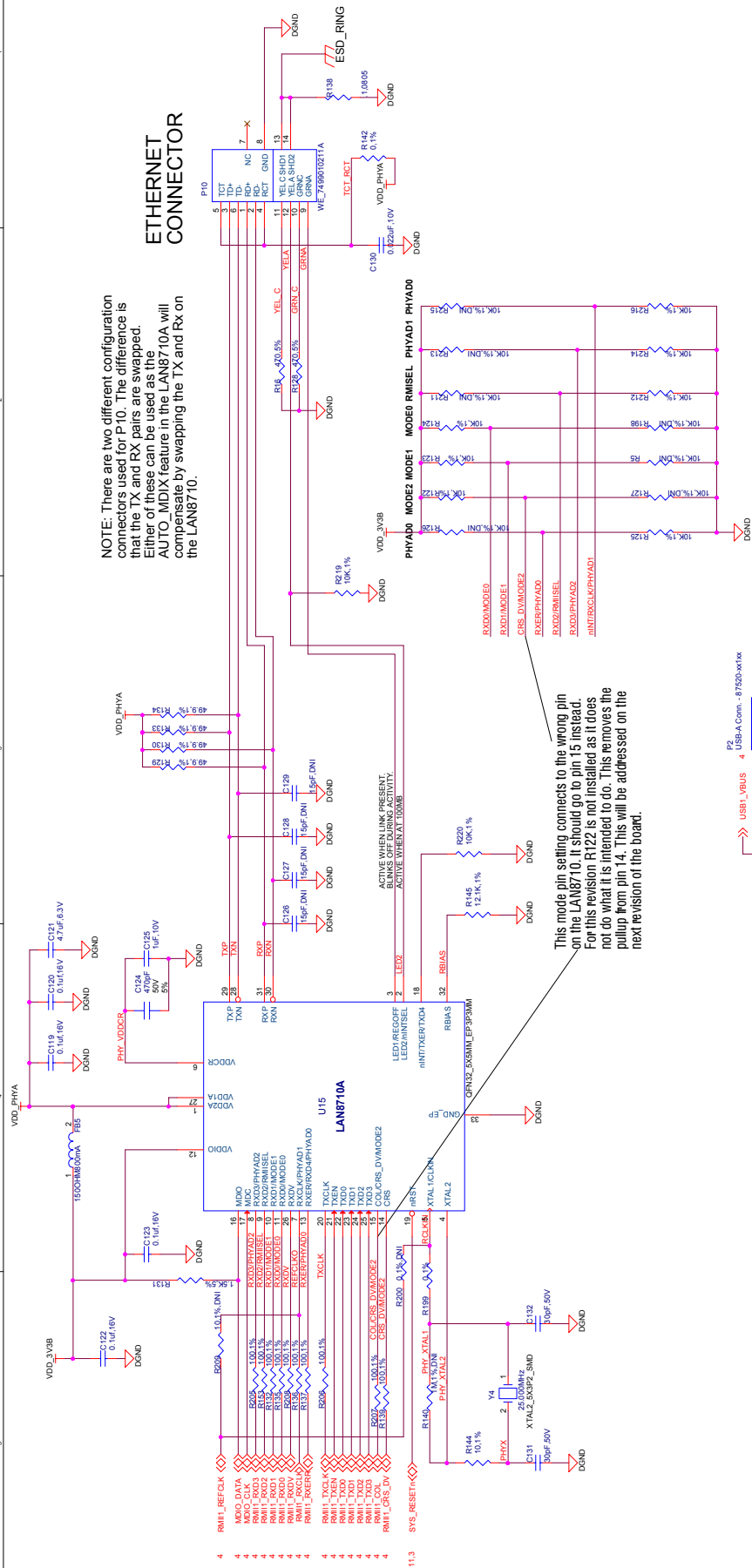


## RESET BUTTON

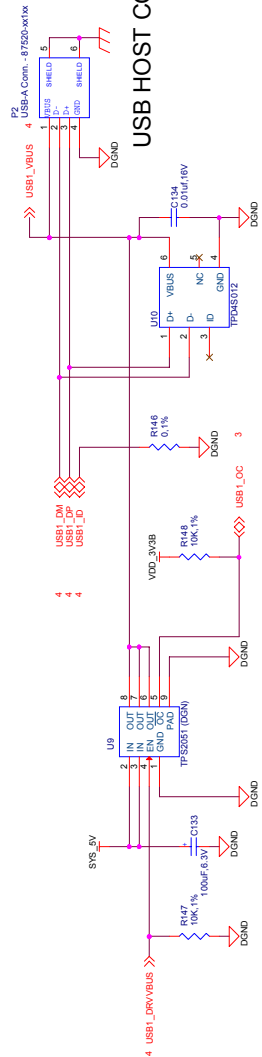


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BeagleBone LED, Configuration and Reset		
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## USB HOST CONNECTOR

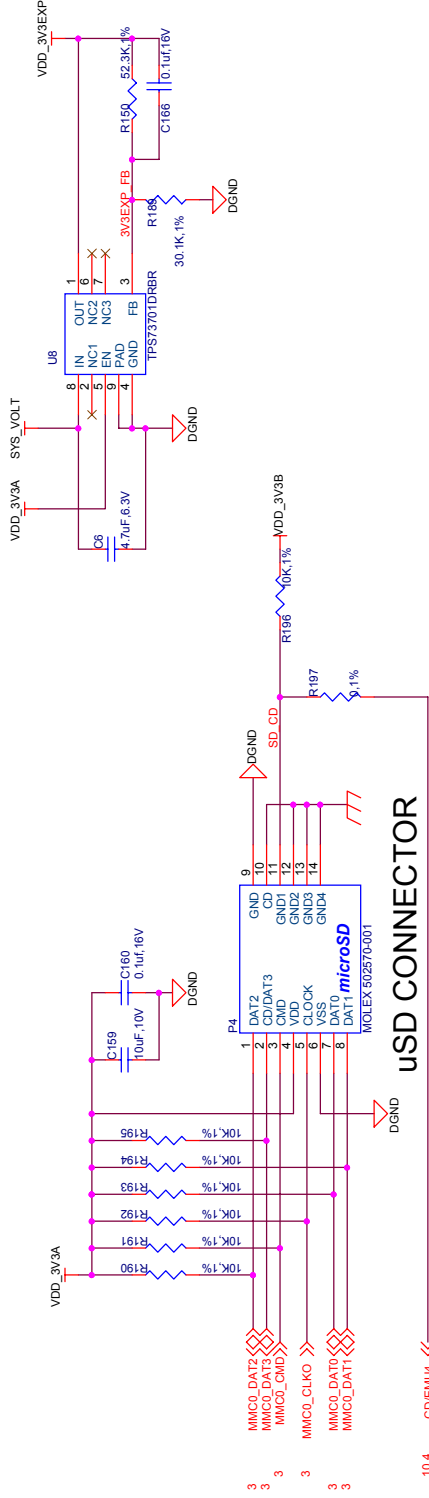
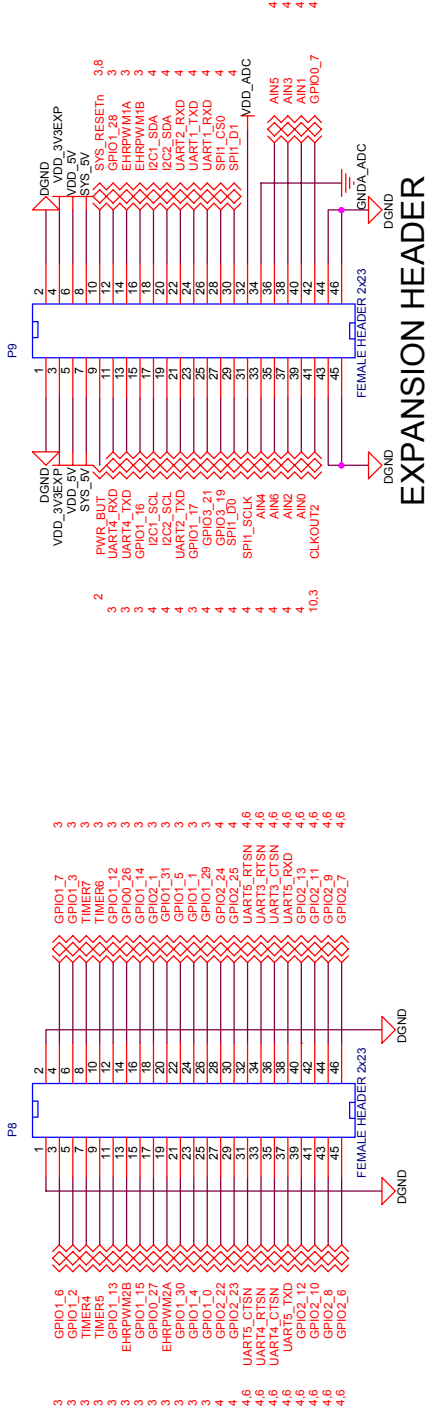


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BeagleBone Expansion Headers, SD/MMC and LDO		
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