Biren Gami

+91-6354514473 | gamibiren@gmail.com | Linkedin | GitHub

Education

- **Sardar Vallabhbhai National Institute Of Technology** — Surat, Gujarat
  Bachelor of Technology in Electronics and Communications; CGPA: 7.9/10 — *December. 2021 – May. 2025*
- **Shree Ram Vidhyalaya** — Palanpur, Gujarat
  Higher Secondary Education; Percentage: 93.38/100 — *July. 2019 – March. 2021*

Projects

- **Cadence Virtuoso: 8-Bit Manchester Carry chain adder** — Oct, 2024 - Nov, 2024
  - Designed and simulated 8-bit Manchester carry chain adder for faster speed in **180nm** technology node.
  - Performed **Schematic** and **Layout** Design for different blocks like **XOR**, **AND**,**Inverter**, **Generate and Propagate**.
  - Performed (**DRC**) and (**LVS**) Verification for all the cells created.
  - Performed **RC Extraction**, **Pre Layout**, and **Post Layout** simulation.
- **Systolic Array Architecture on FPGA** — May, 2024 - June, 2024
  - Designed a systolic array architecture for 3x3 matrix multiplication of 32-bit floating-point numbers.
  - Achieved multiplication output in 9 clock cycles, 3x faster than the 27 cycles required for typical sequential multiplication.
- **Xilinx Vivado: 8x8 Wallace Tree Multiplier** — March, 2024 - April, 2024
  - Designed and implemented a **Wallace Tree multiplier** architecture optimized for **Speed** using structural modelling.
  - Conducted **Pre-synthesis** simulation for **functional verification**.
  - Conducted **Post-synthesis** analysis to evaluate area utilization, power consumption, and timing characteristics.
  - Generated the bitstream file and demonstrated the logic on the **Basys3** FPGA device.
- **Mini Projects: Digital Design using Verilog.** — Jan, 2024 - Feb, 2024
  - Designed and verified FIFO, single/dual Port RAMs for the memory operations.
  - Implemented and tested the working of vending machine and sequence detectors using Mealy and Moore Finite State Machines.

Co-Curricular and Achievements

- Executive,Drishti-A Revolutionary Concept(Technical Club of SVNIT)
- Qualified the 1st and 2nd rounds of **ROBOCON-2023** with 94.7/100 and 85/100 grade respectively.
- Participated in **Grand Finale at National Level Robotics Competition ROBOFEST3.0** - conducted by **Government of Gujarat** and secured a grant of 2.5Lac rupees as Prize Money.

Technical Skills

- **VLSI and Embedded Fundamentals**: Analog Layout Design, Digital Logic Design, STA, HDL Proficiency, Processor Architecture(RISC-V)
- **Languages**: Verilog HDL, Verilog A, C, Python, Embedded C
- **Softwares**: Cadence Virtuoso, Xilinx Vivado, LTSpice, NGSpice, Atmel AVR, Proteus, MATLAB