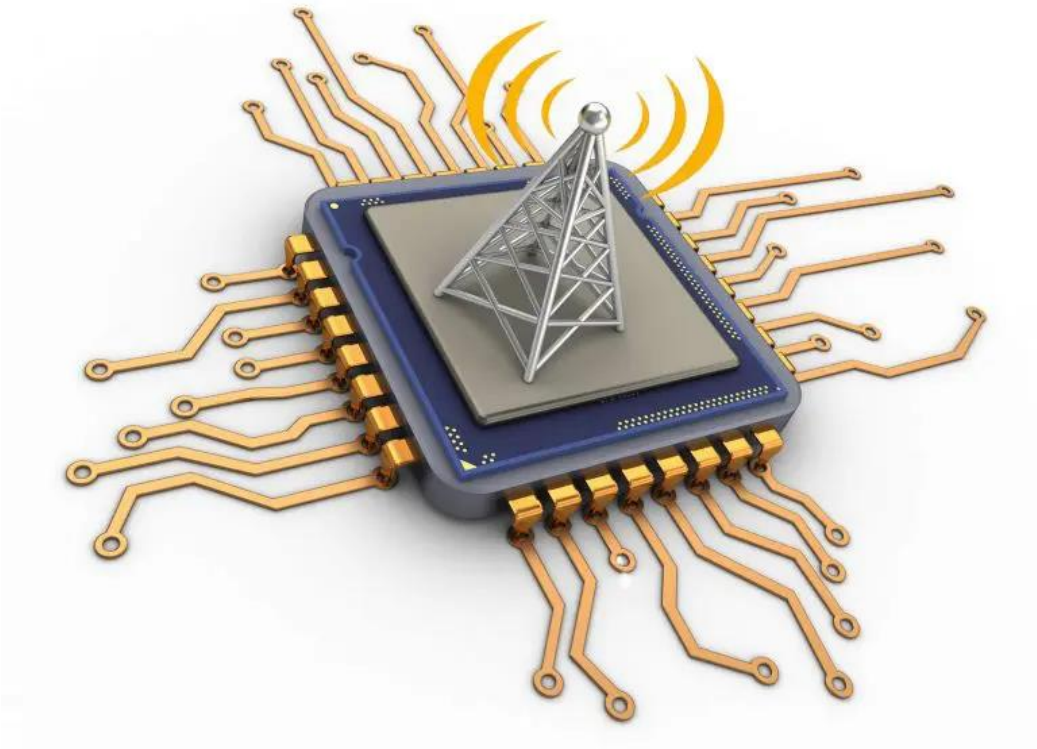
COOK-BOOK OF Two Stage Op-Amp



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1. Motivation:

This Cook-Book present the design conduct that is to be followed for the designing of the Two-Stage Operational amplifier. The need of 2-Stage Opamp over single stage differential amplifier (5-transitor OTA) is caused by the demand for the higher gain. Because of its immunity to environmental noise, it has gain immense popularity in analog circuit.

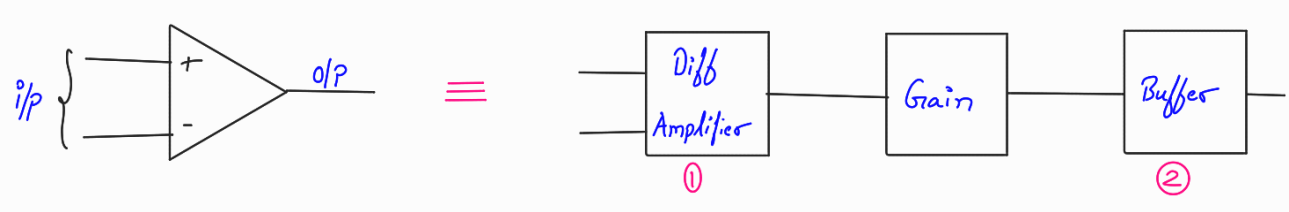


Figure 1: Disintegration of Op-amp

(1) Differential Amplifier of 40dB gain is not suitable to make a negative feedback amplifier so it is followed by the Gain block as a second stage but if we make an Op-Amp without a (2) Buffer stage the it is simply called a Transconductance Amplifier.

Hence, we will be designing the three blocks in stages and analyze it stepwise basis.

2. Design Requirement:

A) Technology: UMC 180nm process

B) Supply Voltage (V_{dd}) = 1.8 V

C) Voltage gain (A_v) = 1000 (60dB)

D) Load Capacitor (C_L) = 2pF

E) Input Common mode range (ICMR) = Max: +1.6V & Min: -0.8V

F) Slew Rate (SR) = 20V/usec

G) Power Dissipation < 300 uW

H) Gain Bandwidth Product (GBW) = 30 MHz

I) Phase Margin (PM) $\geq 60°$

This project aims to achieve a typical design requirement. Although following the cook-book, any design need similar to this can be achieved with proper tuning.

3. Two Stage Op-Amp Topology:

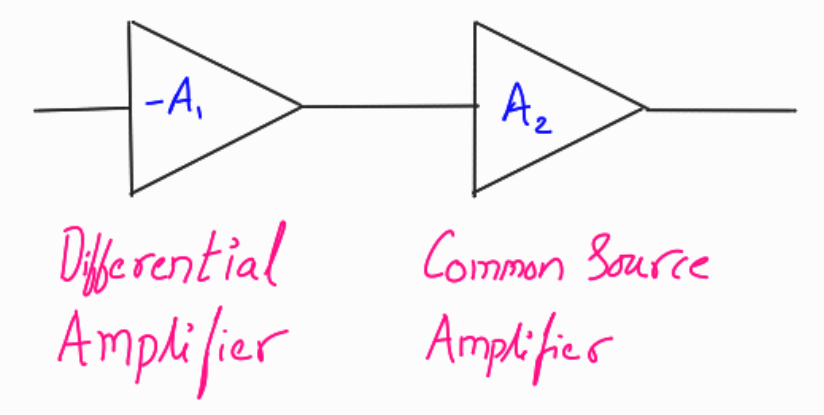


Figure 2: Block diagram of Op-amp topology

Now for the Common source amplifier we have two option two choose from a) NMOS Common Source b) PMOS Common Source

We are using PMOS CS Amplifier as a 2nd stage for a competent headroom *[Ref: Which transistor type to use for the second stage? By Dr. Nagendra Krishnapura, Course: Analog Circuits, IIT Madras]*

We can make more stages, having more gain E.g.: 5 stages without any issues of head room but the issue arises because of the increasing poles.

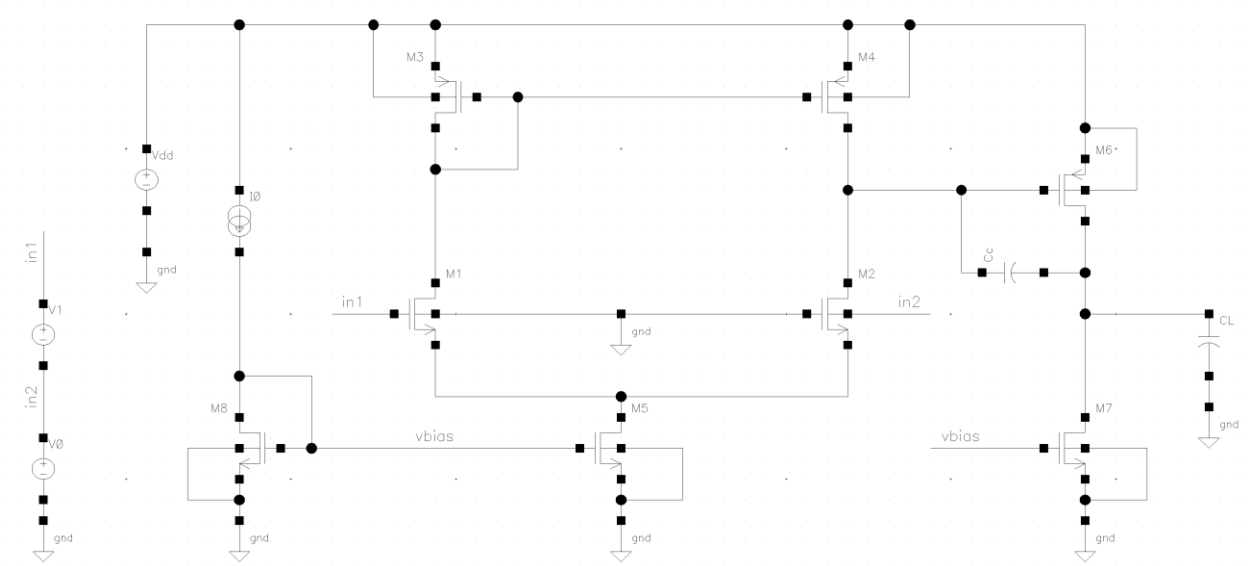


Figure 3: Proposed Two Stage Op-Amp topology

We want to achieve Positive gain out of 2nd stage hence, we switched the sign in 1st stage (in1 = -ve & in2 = +ve) such that negative from 1st stage and one more negative from Common source results in total positive gain.

4. Small signal model of Two Stage Op-Amp:

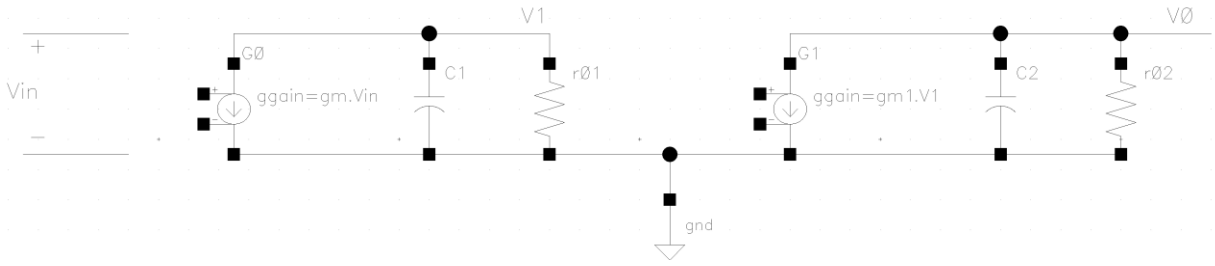


Figure 4: Small signal model

Where,

C_1 = parasitic capacitances of 1st stage, E.g., C_{DS} of M2 and M4

& $C_2 \approx C_L$ ($\because C_L$ is much bigger compared to the parasitic of 2nd stage Amplifier)

Two stage Op-Amp is a two-pole system,

$$P_1 = \frac{1}{r_{01}.C_1} \text{ and } P_2 = \frac{1}{r_{02}.C_L}$$

 # Bode Plot

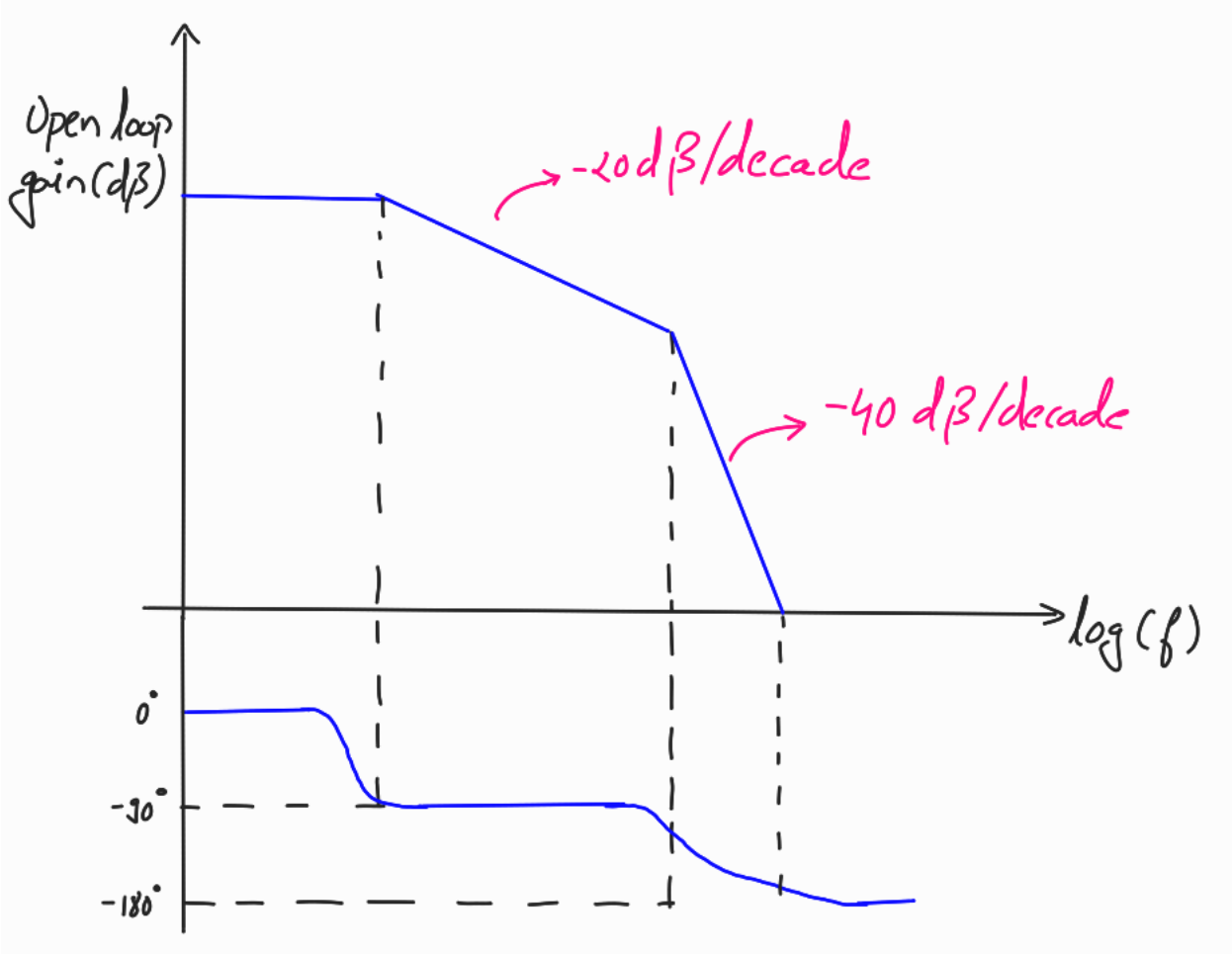


Figure 5: Bode Plot

We can see the phase margin is very close to zero.

By definition,

$$Phase\ Margin(PM) = (Phase\ crossover\ frequency\ at\ -180°) - (Unity\ Gain\ Crossover\ frequency)$$

A) PM = Positive => Stable System

B) PM = 0 => Marginally Stable System

C) PM = Negative => Unstable System

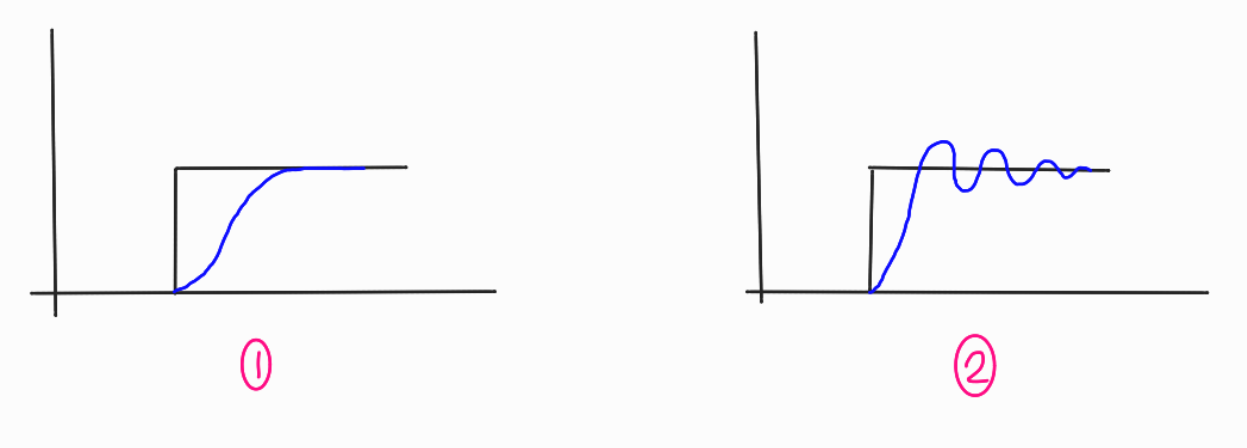


Figure 6: (1) Good Phase Margin (2) Bad Phase Margin

If the system has a Bad Phase Margin is, then Ringing effect will arise in the system. For removing the ringing effect, we need a phase margin of minimum 45°.

To be in a safe side Phase Margin of 60° is needed which is also specified in a Design Requirement.

5. Compensation Method:

With the aim of having good Phase Margin let us do the comprehensive analysis of the two-pole system.

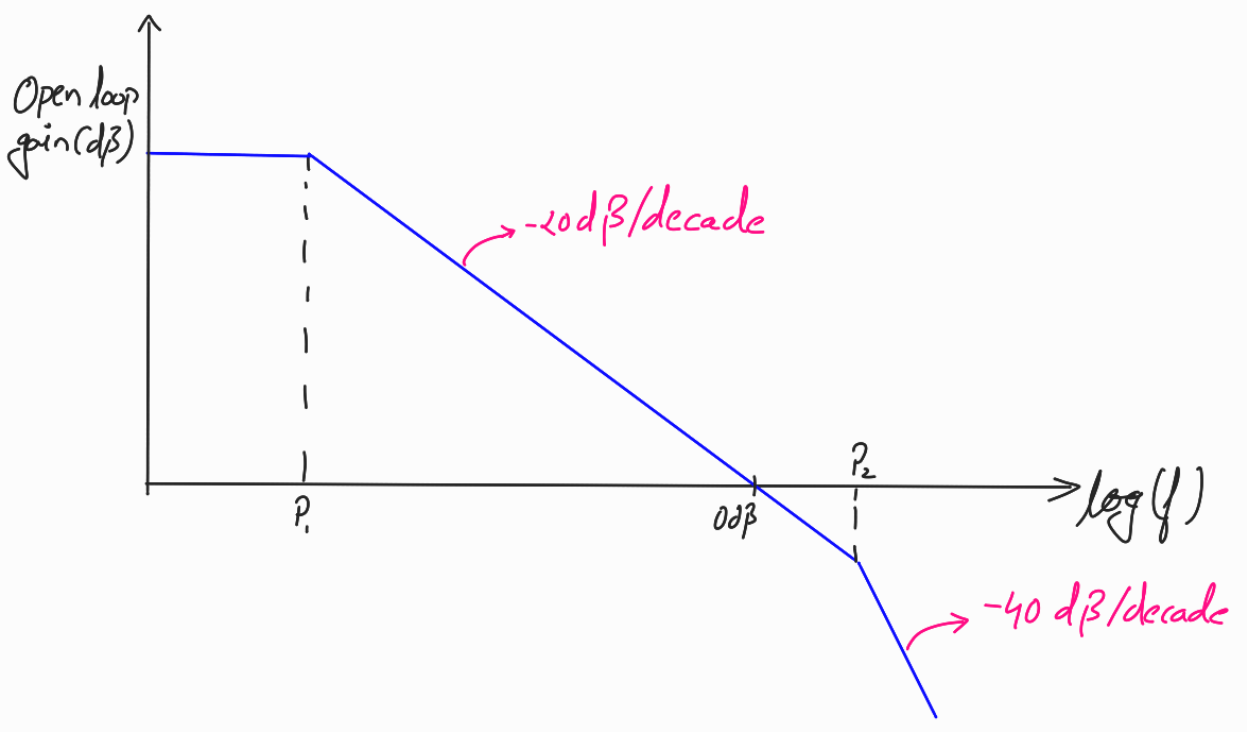


Figure 7: Shifting of Poles

The proposed idea is to move the Pole P_1 or P_2 in such a way that the gain crosses 0dB before the Pole P_2. And effectively since P_2 is very far away will not have any effect.

Hence, in this way we have a Single pole system even if 2 poles exist.

We have,

$$P_1 = \frac{1}{r_{01}.C_1} \text{ and } P_2 = \frac{1}{r_{02}.C_L}$$

Now, since C_L is a Load Capacitance which is design specified hence over which we don't have much control.

Therefore, the plan is to increase the value of C_1 such that the 1st Pole can be moved to the left side.

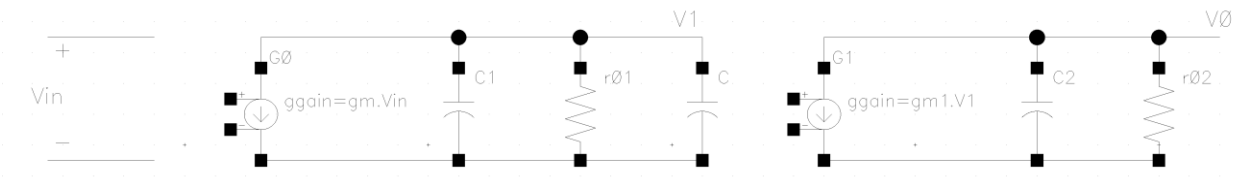


Figure 8: Shifting of P_1 using a Big Fat Capacitor (C)

Now the 1st pole will effectively become, $P_1 = \frac{1}{r_{01}.(C_1+C)}$

The 1st pole has shifted towards left thereby achieving our primary goal.

But, to avoid the use of Big Fat Capacitor we can utilize the Miller effect.

Miller's Theorem:

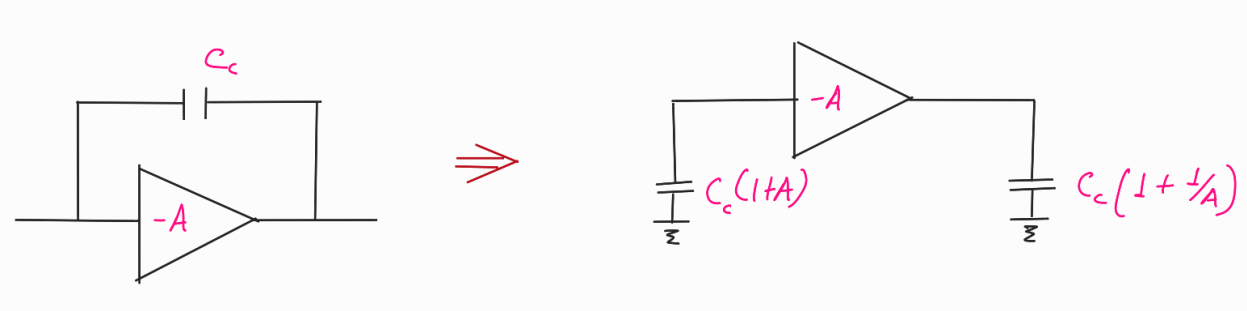


Figure 9: Miller Effect

Miller effect arises when there are two paths from input to the output then the impedance of one path can be divided into the input part and the output part.

Using Miller's theorem to convert the circuit of figure 9.

Then the input capacitance: $C_{in} = C_c(1 + A)$

And this effect is called "Miller Multiplication" of the capacitor.

Hence, small capacitor can be equated as big capacitor with the aid of Miller Multiplication hence saving some area for layout design.

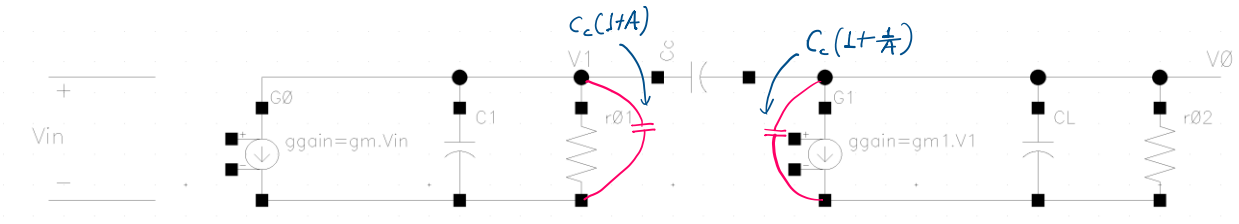


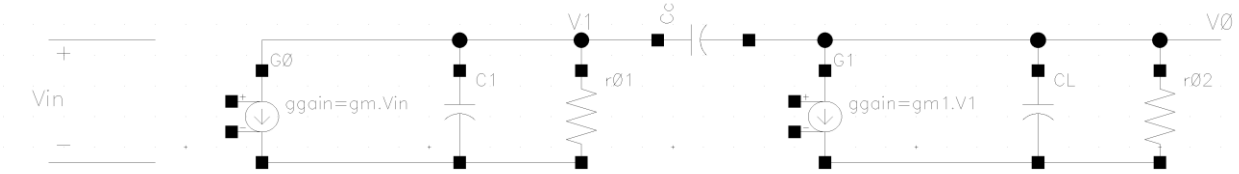
Figure 10: Coupling Capacitor for Miller Multiplication

6. Some Important parameters of Operational Amplifier:

There are few parameters of Op-Amp which needs to be reviewed before the design steps.

Transfer Function:

Let us derive the transfer function of the two-stage op-amp:

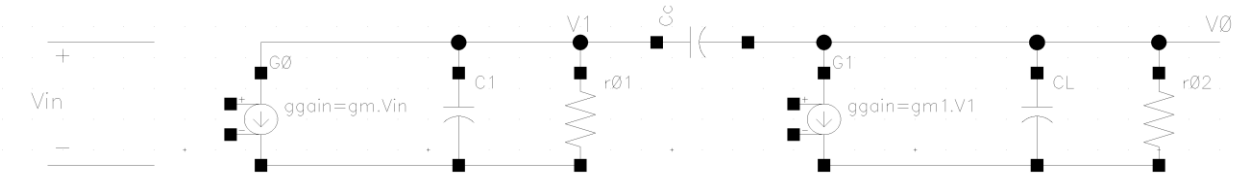


But we cannot apply miller theorem here because of:

A) Pole Splitting: arises due to the byproduct of Miller frequency compensation.

B) Zero: At high frequency Coupling Capacitor 'C_c' will behave as a short.

Hence Miller Theorem cannot be applied to derive the transfer function, so only way to derive a transfer function is by manual method.



Applying chain rule;

$$\frac{V_0}{V_{in}} = \frac{V_1}{V_{in}} \times \frac{V_0}{V_1} \tag{1}$$

From the figure;

$$\frac{V_1}{\frac{1}{sC_1}} + \frac{V_1}{R_1} + g_m V_{in} + \frac{V_1 - V_0}{\frac{1}{sC_c}} = 0$$

$$V_1 = \frac{V_0 sC_c R_1 - g_m R_1 V_{in}}{1 + sR_1(C_1 + C_c)} \tag{2}$$

Again, from the figure;

$$\frac{V_0}{\frac{1}{sC_2}} + \frac{V_0}{R_2} + g_{m1} V_1 + \frac{V_0 - V_1}{\frac{1}{sC_c}} = 0$$

$$V_0 = \frac{V_1(sC_c - g_{m1})}{\left[s(C_2 + C_c) + \frac{1}{R_2}\right]} \tag{3}$$

Now, substituting equation (3) in (2) and finally in (1) we get;

$$\therefore \frac{V_0}{V_{in}}$$

$$= \frac{g_m R_1 g_{m1} R_2 \left(1 - \frac{sC_c}{g_{m1}}\right)}{s^2[R_1R_2(C_1C_2 + C_1C_c + C_2C_c)] + s\left[R_2(C_c + C_2) + R_1(C_c + C_1) + C_c g_{m1} R_1 R_2 + 1\right]}$$

For General Expression of two pole system;

$$\frac{V_0}{V_{in}} = \frac{A_{DC}\left(1 - \frac{s}{z}\right)}{\left(1 + \frac{s}{P_1}\right).\left(1 + \frac{s}{P_2}\right)}$$

$$\frac{V_0}{V_{in}} = \frac{A_{DC}\left(1 - \frac{s}{z}\right)}{1 + s\left(\frac{1}{P_1} + \frac{1}{P_2}\right) + s^2\left(\frac{1}{P_1P_2}\right)} \qquad (4)$$

Let us do some approximations for simplicity;

$$\because P_2 \gg P_1$$

So,

$$\frac{1}{P_1} + \frac{1}{P_2} \approx \frac{1}{P_1}$$

Hence from equation 4;

Coefficient of $s = \frac{1}{P_1}$

Coefficient of $s^2 = \frac{1}{P_1 P_2}$

Therefore, from the transfer function;

$$P_1 \approx \frac{1}{g_{m1} R_2 R_1 C_c} \tag{5}$$

$$P_1 P_2 \approx \frac{1}{R_1 R_2 (C_1 C_2 + C_1 C_c + C_2 C_c)} \tag{6}$$

Substituting (5) in (6) we get;

$$P_2 \approx \frac{g_m}{C_2} \tag{7}$$

Again, from the transfer function;

$$z = \frac{g_{m1}}{C_c} \tag{8}$$

Where, z is the zero location.

$$A_{DC} = g_m R_1 . g_{m1} R_2 \tag{9}$$

Where, A_{DC} is the dc gain of Op-Amp

We know,

$$Gain\ Bandwidth\ product = DC\ gain \times first\ pole$$

Hence from equation (5) and (9)

$$GBW = \frac{g_m}{C_c} \tag{10}$$

Slew Rate (SR):

Slew rate is a rate of change of the output. Basically, it is a measure of how quickly the output can change considering it's limiting factor.

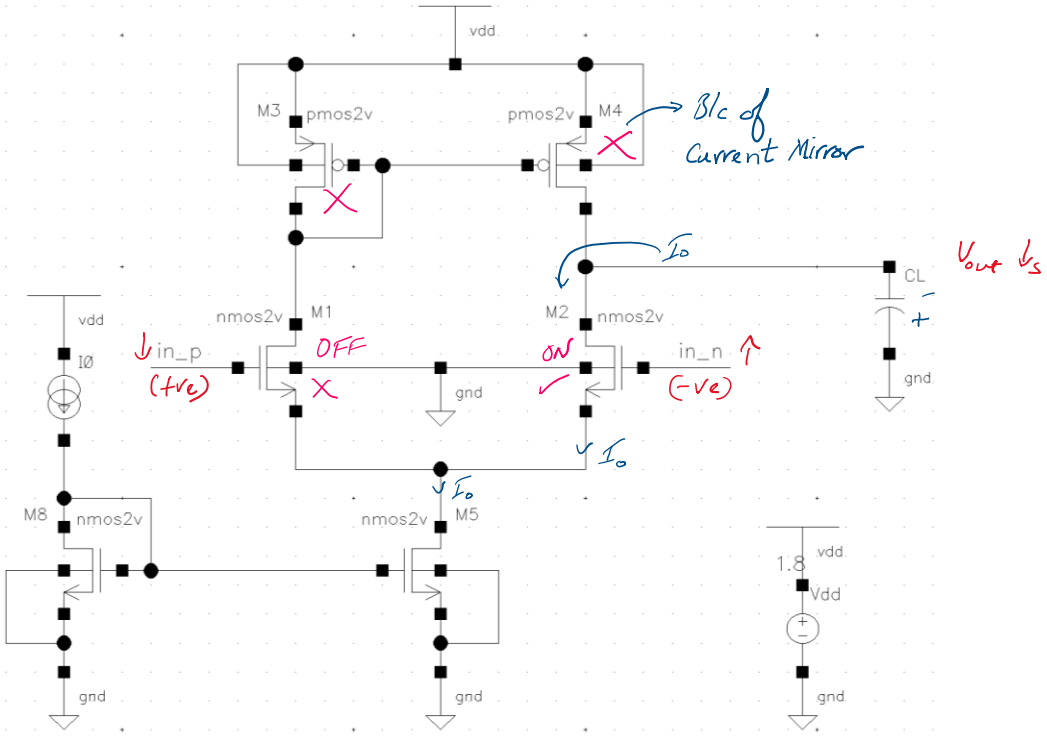


Figure 11: Single stage Op-Amp

If V_in_n is increased and if V_in_p is decreased we measure the output and observe how quickly it changes to determine the slew rate of the system. Limiting factor: M1 is completely turned Off

M2 is completely turned On.

But for a two stage Op-amp minor change needs to be done:

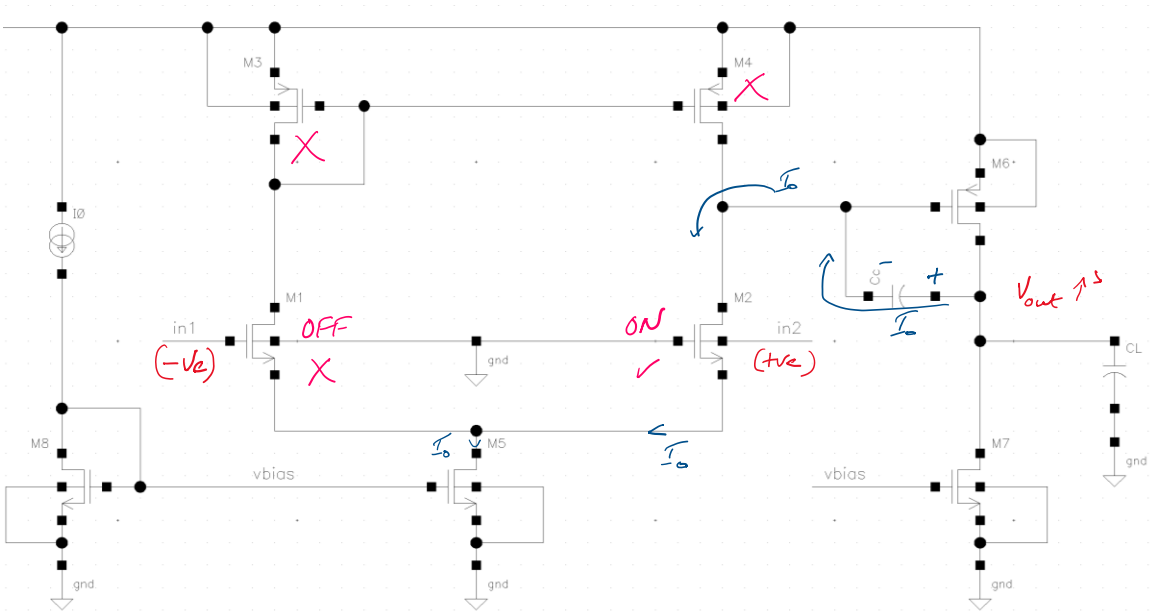
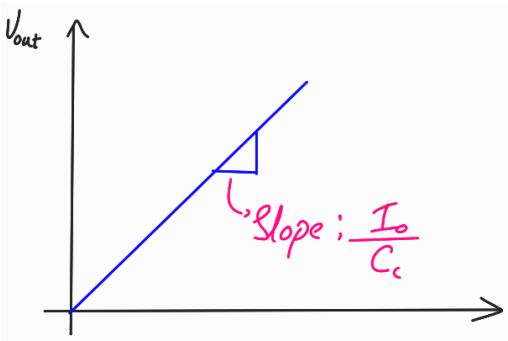


Figure 12: Two stage Op-Amp

A) CASE I:

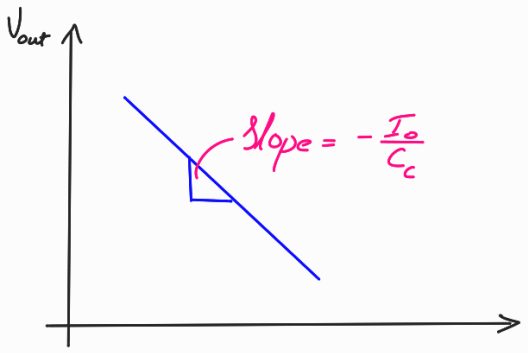
The right side of the Op-Amp is kept positive because if we increase the voltage of M2 the drain will be decreased and again the inverting stage is created by M6 (since it's a CS amplifier). So, output voltage will be increasing. Hence, because of flow of current I_0 through C_c;



$$\therefore SR = \frac{I_0}{C_c}$$

B) CASE II:

If M1 is ON and M2 is off and all the current is flowing through M1 then current will flow through current mirror into C_c.



$$\therefore SR = -\frac{I_0}{C_c}$$

Hence for a two-stage op-amp;

$$\therefore |SR| = \frac{I_0}{C_c} \tag{11}$$

Phase Margin:

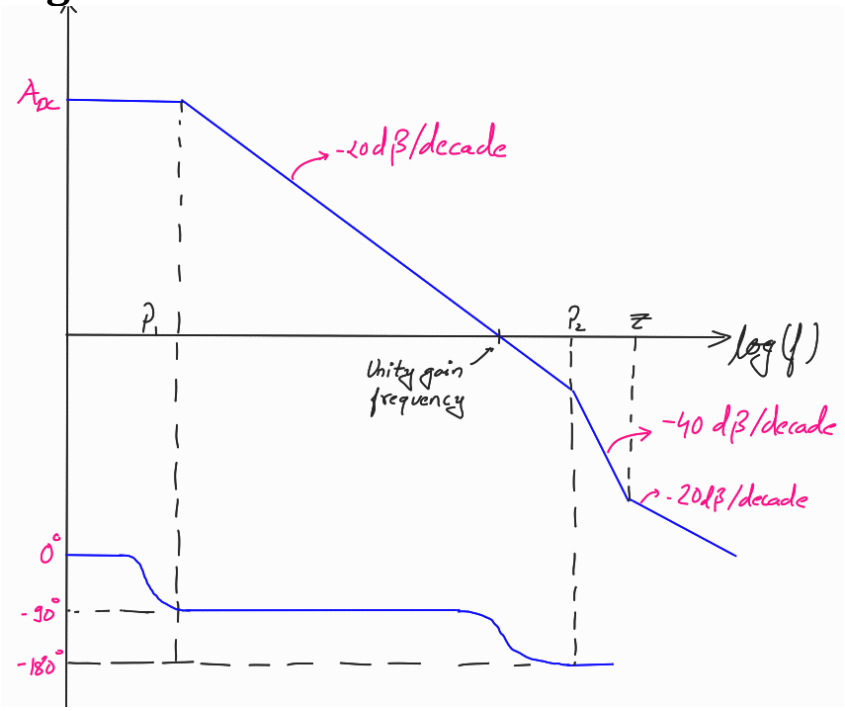


Figure 12: Bode Plot of Two stage Op-Amp

In our design GBW/ unity gain frequency will be between phase -90° to -180°. If unity gain frequency is very close to 180°, which will cause phase margin to decrease.

Note: Phase difference <45° is not acceptable because in such case there will be ringing effect.

The preferred value of phase margin is 60°.i.e., if P_2 is moving towards the unity gain frequency then our phase margin will decrease.

Let us take a factual assumption;

$$z \geq 10 \times GBW \tag{12}$$

Then from our Transfer Characteristics;

$$\angle \frac{V_0}{V_{in}} = -\tan^{-1}\left(\frac{\omega}{z}\right) - \tan^{-1}\left(\frac{\omega}{P_1}\right) - \tan^{-1}\left(\frac{\omega}{P_2}\right)$$

Since we are interested in phase and frequency at unity gain frequency (GBW) so replacing, $\omega = GBW$

$$\angle \frac{V_0}{V_{in}} = -\tan^{-1}\left(\frac{GBW}{z}\right) - \tan^{-1}\left(\frac{GBW}{P_1}\right) - \tan^{-1}\left(\frac{GBW}{P_2}\right)$$

Now substituting (12) in above equation we get,

$$\angle \frac{V_0}{V_{in}} = -\tan^{-1}\left(\frac{1}{10}\right) - \tan^{-1}(A_{DC}) - \tan^{-1}\left(\frac{GBW}{P_2}\right) \tag{13}$$

$$\therefore PM = 84.29\tan^{-1}\left(\frac{GBW}{P_2}\right) \tag{14}$$

Since we want PM above 60° so by substituting in equation (14) we get the condition as;

$$P_2 \geq 2.2 \times GBW \tag{15}$$

Even if ringing effect is not much dominant above 45° yet to have better stability and to be in the safe side phase margin of above 60° is preferred.

Now substituting the value of GBW and P_2 in (15) we get;

$$\frac{g_{m1}}{C_2} \geq 2.2 \frac{g_m}{C_c} \tag{16}$$

Again, to ensure our factual assumption of (12),

$$z = 10 \times GBW$$

$$\frac{g_{m1}}{C_c} = 10. \frac{g_m}{C_c}$$

$$g_{m1} = 10. g_m \tag{17}$$

Now, substituting (17) in (16) and $C_2 = C_L$

$$C_c \geq 0.22 \times C_L \tag{18}$$

Hence, this is the required condition for phase margin >60°

7. Cook-Book of Two Stage Operational Amplifier:

Steps:

7.1. Find I_5 from Slew rate from the design specification.

7.2. Find C_c from the phase margin condition.

7.3. Find M_1, M_2 aspect ratio from GBW.

7.4. Find M_3, M_4 aspect ratio from ICMR (Max).

7.5. Find M_5 aspect ratio from ICMR (Min).

7.6. Find M_6 aspect ratio from the phase margin condition.

7.7. Find M_7 aspect ratio.

Note: L_{min} possible=180nm but we will be taking at least L=500nm because using a short channel causes a channel length modulation.

7.1 Calculate I_5 from slew rate:

We know from (11);

$$|SR| = \frac{I_5}{C_c}$$

Hence, substituting the data from design specification we get,

$$\therefore I_5 = 20\mu A \qquad (19)$$

7.2 Calculate C_c:

We have from equation (18)

$$C_c \geq 0.22 \times C_L$$

Hence, substituting the data from design specification we get,

$$C_c \geq 440 \text{ fF}$$

Since, the above condition is a minimum possible value for having phase margin=60° so accounting for parasitic capacitance also let's give;

$$\therefore C_c = 800fF \qquad (20)$$

7.3 Calculate M_1, M_2 aspect ratio from GBW:

We know from equation (10);

$$g_m = GBW \times C_c \times 2\pi$$

Hence, substituting the data from design specification we get,

$$\therefore g_m = 160\mu \qquad (21)$$

We have,

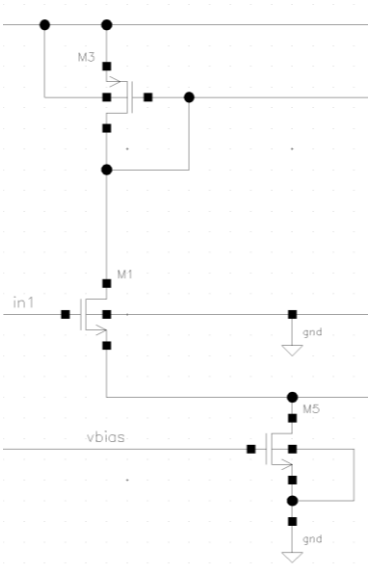
$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_m^2}{\mu_n C_{ox}.2I_D}$$

We know, for M_1 and M_2 => $2I_D = I_5$

Hence, by substituting equation (19), (21) we get;

$$\therefore \left(\frac{W}{L}\right)_{1,2} \approx 5 \tag{22}$$

7.4 Calculate M_3, M_4 aspect ratio from ICMR(Max):



For M_1 to be in saturation,

$$V_d > V_g - V_{t1}$$

$$V_g < V_d + V_{t1}$$

Hence, gate voltage can go as high by one threshold value over the drain voltage.

So,

$$\therefore V_{in(\max)} = V_{d1} + V_{t1} \tag{23}$$

And,

$$\therefore V_{d1} = V_{DD} - V_{sg3} \tag{24}$$

We know,

$$\therefore I_3 = \frac{\mu_p C_{ox} \left(\frac{W}{L}\right)}{2} \left(V_{gs} - V_t\right)^2 \tag{25}$$

$$\therefore V_{gs3} = \left[\sqrt{\frac{2I_{D3}}{\beta_p}} + |V_{t3}|\right] \tag{26}$$

Hence, substituting (26) in (24)

$$\therefore V_{D1} = V_{DD} - \left[\sqrt{\frac{2I_{D3}}{\beta_p}} + |V_{t3}|\right] \tag{27}$$

Substituting (27) in (23) we get;

$$ICMR_{max} \leq \left[V_{DD} - \left(\sqrt{\frac{2I_3}{\beta}} + |V_{t3}|\right)\right]_{min} + V_{t1(\min)}$$

$$ICMR_{max} \leq V_{DD} - \sqrt{\frac{2I_3}{\beta}} - |V_{t3}|_{max} + V_{t1(\min)}$$

$$\frac{2I_D}{\mu_p C_{ox}\left(\frac{W}{L}\right)_3} = \left[V_{DD} - ICMR_{max} - |V_{t3}|_{max} + V_{t1(min)}\right]^2$$

$$\therefore \left(\frac{W}{L}\right)_3 = \frac{2I_{D3}}{\mu_p C_{ox}\left[V_{DD} - ICMR_{max} - |V_{t3}|_{max} + V_{t1(min)}\right]^2} \tag{28}$$

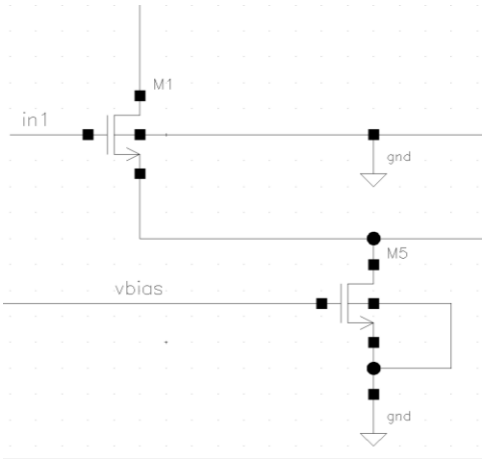
From the 5-transistor OTA cook book we have;

a) $\mu_p C_{ox} = 60\mu$, b) $\mu_n C_{ox} = 300\mu$, c) $V_{t3max} = 0.51$, d) $V_{t1min} = 0.47$

Hence, substituting the data from design specification and above in (28) we get,

$$\therefore \left(\frac{W}{L}\right)_{3,4} \approx 14 \tag{29}$$

7.5 Calculate M_5 aspect ratio from ICMR(Min):



For M_5 to be in saturation,

$$V_{d5} > V_{g5} - V_{t5}$$

Let, V_{dsat5} be voltage to keep M_5 in saturation.

We can observe that if V_{in} decreases as an effect drain voltage of M_5 decreases which might push M_5 in triode region.

So,

$$\therefore V_{in(\min)} = V_{gs1} + V_{dsat5} \tag{30}$$

$$ICMR_{min} \leq \left[\sqrt{\frac{2I_{d1}}{\beta_1}} + |V_{t1}|\right]_{max} + V_{dsat}$$

$$V_{dsat} \geq ICMR_{min} - \sqrt{\frac{2I_{d1}}{\mu_n C_{ox}.\left(\frac{W}{L}\right)_1}} - |V_{t1}|_{max} \tag{31}$$

Hence, substituting from design specification and $V_{t1max} = 0.59$

We get,

$$V_{dsat} = 94.6\, mV$$

Generally, we prefer the voltage across M_5 least 100mV because if V_{ds} of M_5 is very less then we have to make a very big MOSFET (Ref: Equation (32)) to ensure that it is in saturation.

But from (31) we cannot change $ICMR_{min}$ neither $V_{t1(max)}$ so only thing that can change is β_1 value. Hence if we increase the $\left(\frac{W}{L}\right)_1$ of M_1 then voltage drop across M_1 will be less which will help us get more voltage across M_5.

Hence let us consider,

$$\therefore \left(\frac{W}{L}\right)_{1,2} \approx 6$$

Hence, again substituting in (31) we get,

$$V_{dsat} = 105\, mV$$

$$\therefore I_{D5} = \frac{\mu_p C_{ox} \left(\frac{W}{L}\right)_5}{2} (V_{dsat})^2 \qquad (32)$$

Hence, by substituting all the values we get;

$$\therefore \left(\frac{W}{L}\right)_5 \approx 12$$

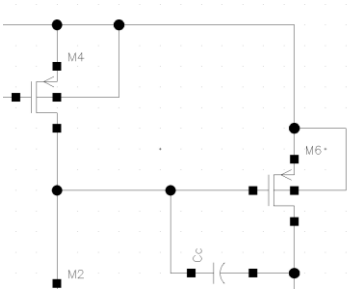
7.6 Calculate M_6 aspect ratio:

We know from equation (16);

$$g_{m1} \geq 10.\, g_m$$

Since, g_{m1} is the gain of second stage of op-amp which is g_{m6}. Hence, by substituting we get,

7.7 Calculate M_7 aspect ratio:



From the figure;

$$\frac{I_6}{I_4} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}$$

Now, by substituting all the values in the above condition we get,

$$I_6 = 125\mu A \qquad (33)$$

From the Figure;

$$\frac{I_7}{I_5} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5}$$

Now, by substituting all the values in the above condition we get,

$$\therefore \left(\frac{W}{L}\right)_7 = 75 \qquad (34)$$

8. Results:

Hence, substituting all the derived parameters in proposed two stage Op-Amp topology Figure 3 we got following frequency and phase plot i.e., Bode plot.

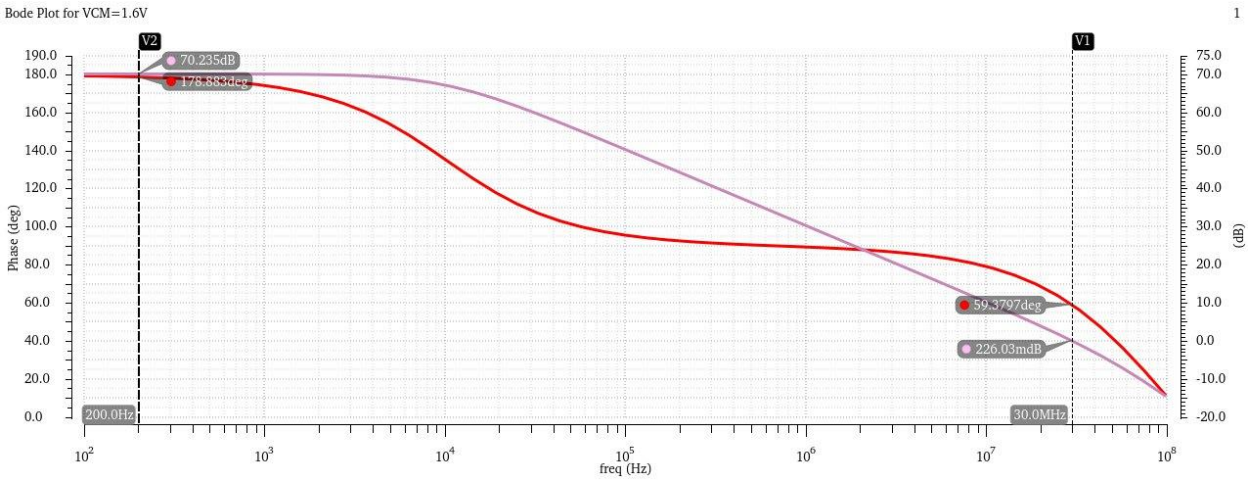


Figure 13: Bode Plot of Two stage Op-Amp

Therefore,

- Voltage gain (A_v) ≈ 70 dB
- Gain Bandwidth Product (GBW) = 30MHz
- Phase Margin (PM) =59.38 ≈ 60
- Power Dissipation = 122 u W

Also, the other defined design requirement was met.