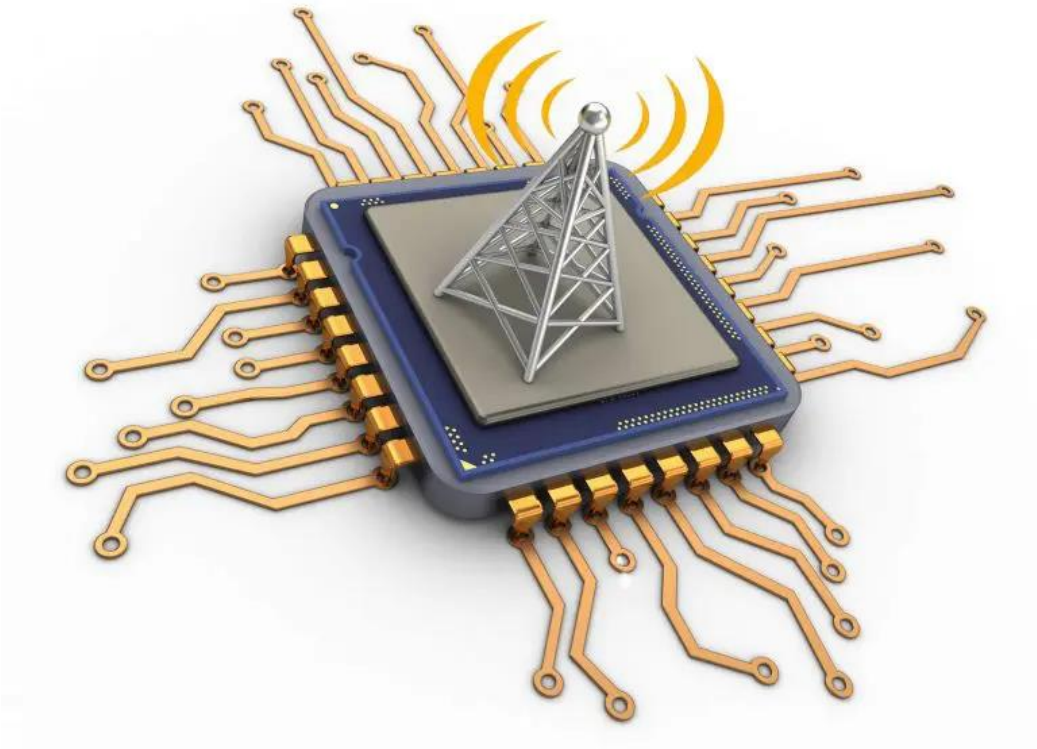
COOK-BOOK OF Bandgap Voltage Reference



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1. Motivation:

This Cook-Book present the design conduct that is to be followed for the designing of the Bandgap Voltage reference (BGR). It is a major building block of Integrated circuit as it is very essential for a circuit to be immune to effect of temperature change. The functionality of BGR is to give a constant reference voltage which is independent of temperature and supply voltage.

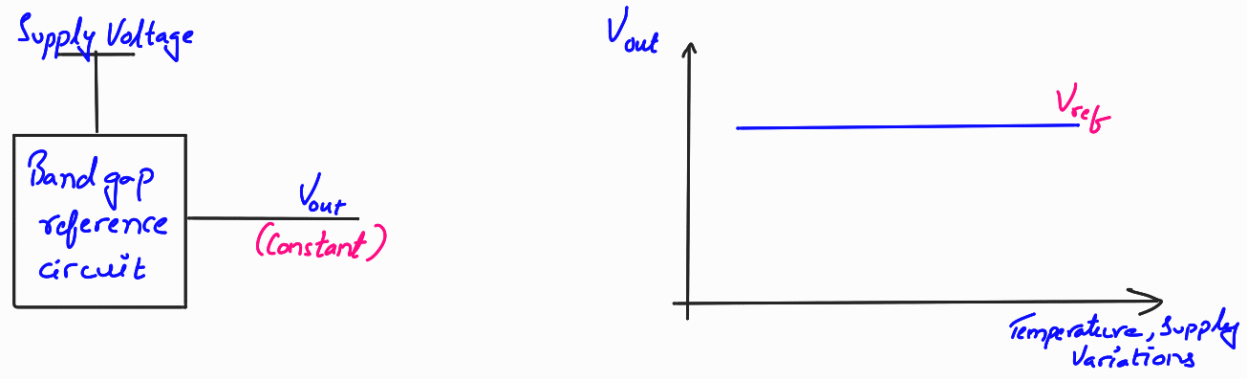


Figure 1: Bandgap reference functionality

Process variations is also one of the parameters which effect $V_{ref.}$

Applications: IN LDO, Buck, Boost Converter, Regulator, ADC, DAC or any of analog or RFIC circuits.

The standard temperature variation an integrated circuit is expected to withstand is: -40℃ to 125℃

Hence, Bandgap reference is a circuit which will give constant output voltage (V_{ref}) with respect to temperature and supply variations.

Important Parameters of BGR:

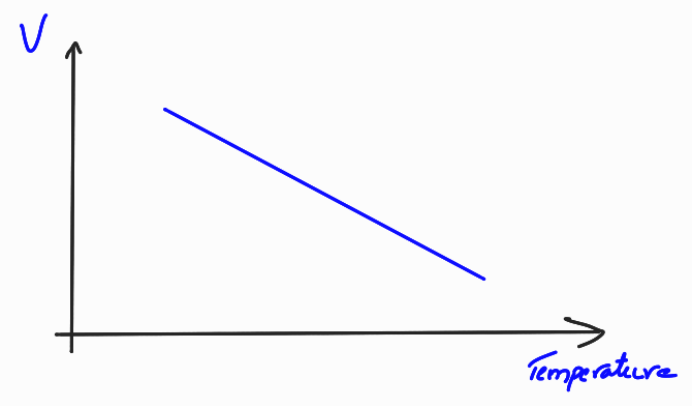
A) Temperature variations: More prevailing than others

B) Supply variations

2. Temperature Variations:

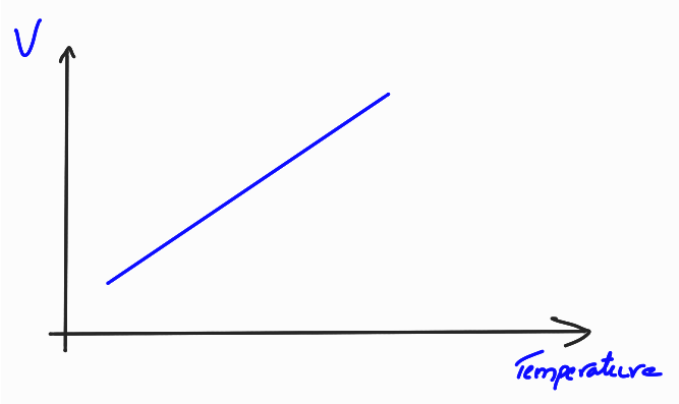
Generally, a circuit behaves in two ways under the effect of temperature:

A) CTAT (Complementary to absolute temperature):



Circuit whose voltage or current decreases with the increase in temperature are called CTAT circuits.

B) PTAT (Proportional to absolute temperature):



Circuit whose voltage or current increases with the increase in temperature are called PTAT circuits.

Now, we can make a constant voltage reference, cancelling the effect of temperature by combining CTAT and PTAT circuits.

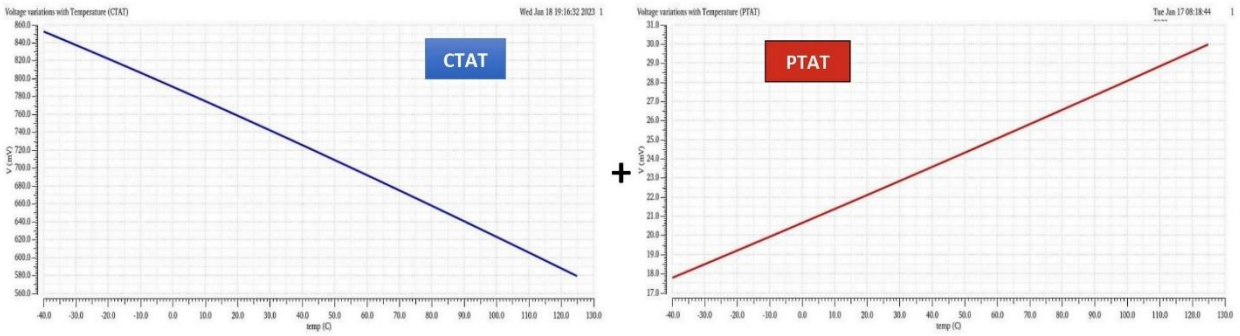


Figure 2: Combining CTAT and PTAT together

But it is not applicable to any PTAT or CTAT since the slope of CTAT and PTAT differs and adding them up will not cancel their nature.

Thus, we need to scale the CTAT and PTAT so that they cancel each other as depicted in given block diagram representation.

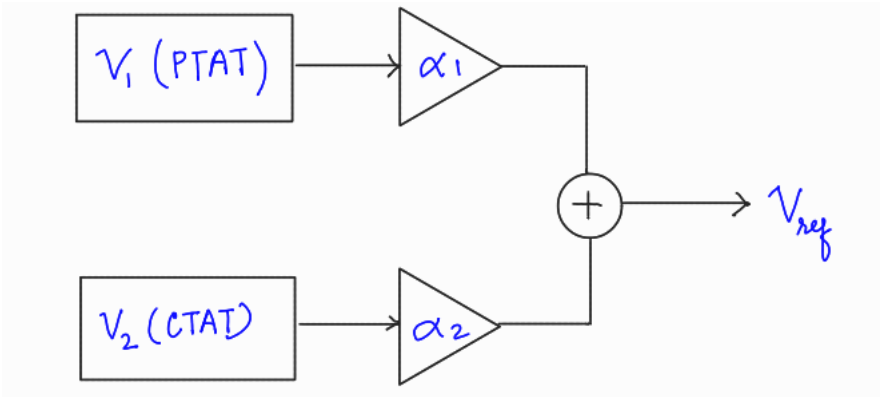


Figure 3: Block diagram of BGR

Hence, Bandgap reference can be mathematically represented as;

$$\alpha_1 . PTAT + \alpha_2 . CTAT = Constant\ Voltage \qquad (1)$$

Where, α_1 and α_2 are scaling factors.

3. CTAT Design:

The circuit in which voltage decreases with increase in temperature is called CTAT. If biased current is applied across a diode, it behaves as a CTAT provided the bias current is constant in nature.

Hence by the definition, if a constant current is passed through a diode, then the voltage decreases at the rate of -1.6mV/°C with respect to temperature.

According to the definition of CTAT, the proposed circuit is sketched.

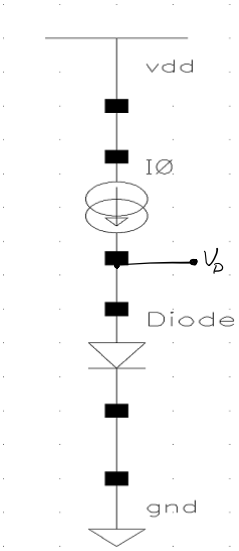


Figure 4: Proposed CTAT circuit

Condition;

I_0= constant w.r.t temperature and supply variations

(to be discussed how to achieve the constant current)

We know the diode equation is given as;

$$I_0 = I_s . e^{\frac{V_D}{V_t}}$$

Where, V_t = thermal voltage =26mV @ 300K

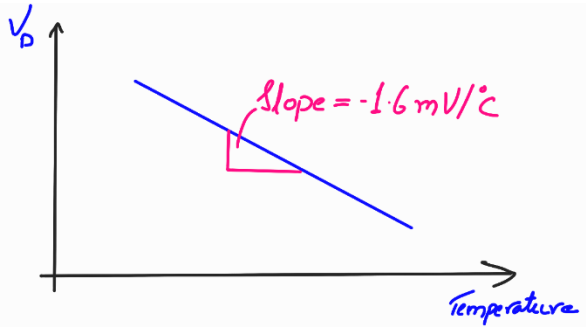
I_s= saturation/scaled current

& V_D =Voltage across the diode

To find V_D from the diode equation;

$$\frac{I_0}{I_s} = e^{\frac{V_D}{V_t}}$$

$$V_D = V_t . ln\left(\frac{I_0}{I_s}\right) \quad (2)$$



If the constant current is passed through a diode, then the voltage across a diode (V_D) with respect to temperature is of slope -1.6mV/°C.

Hence,

$$\frac{dV_D}{dT} = -1.6\text{mV/°C}$$

& We know,

$$V_t = \frac{kT}{q} \qquad (3)$$

Since from (3) $V_t \propto T$ is a PTAT

From equation (2) V_t is PTAT (very weak) and $ln\left(\frac{I_0}{I_s}\right)$ is CTAT (very strong)

Hence, if overall nature is to be considered the CTAT term is more dominating ergo V_D effective nature is CTAT.

Differentiating equation (3) with respect to temperature;

$$\frac{dV_t}{dT} = \frac{k}{q} \qquad (4)$$

Since, I_0 is constant with respect to temperature;

$$\frac{dI_0}{dT} = 0 \qquad (5)$$

We know that Saturation current is given as;

$$I_s = b.T^{(4+m)} exp\left[-\frac{E_g}{kT}\right] \quad (6)$$

Where,

b: proportionality constant, E_g = energy band gap of silicon,

m: -3/2 & k = Boltzmann constant.

Differentiating equation (6) with respect to temperature and simplifying;

$$\frac{dI_s}{dT} = I_s.\left[\frac{4+m}{T} + \frac{E_g}{kT^2}\right] \quad (7)$$

Finally differentiating equation (2) with respect to temperature and substituting (4), (5) & (7)

$$\frac{dV_D}{dT} = \frac{dV_t}{dT}.ln\left(\frac{I_0}{I_s}\right) + V_t.\frac{dln\left(\frac{I_0}{I_s}\right)}{dT}$$

$$\frac{dV_D}{dT} = \frac{V_D - (4+m)V_t - \frac{E_g}{q}}{T} \quad (8)$$

Therefore, equation (8) is the final expression for the slope of CTAT i.e., rate of change of diode voltage with respect to temperature.

Now, substituting the values at 300K and V_D = 0.75

$$\frac{dV_D}{dT} = \frac{0.75 - \left(4 - \frac{3}{2}\right) \times 26mV - 1.2}{300}$$

$$\therefore \frac{dV_D}{dT} \approx -1.66mV/°C$$

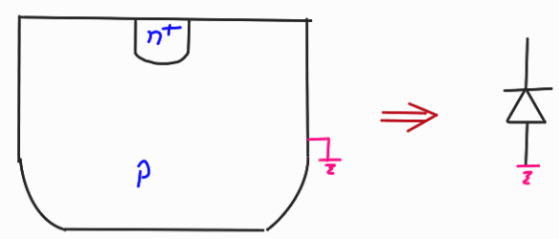
Proved.

Q) How to make a diode in a CMOS process?

= We know that diode is essentially a P-N junction device. There are few methods to achieve few of them are mentioned below:

A) 1st Method:

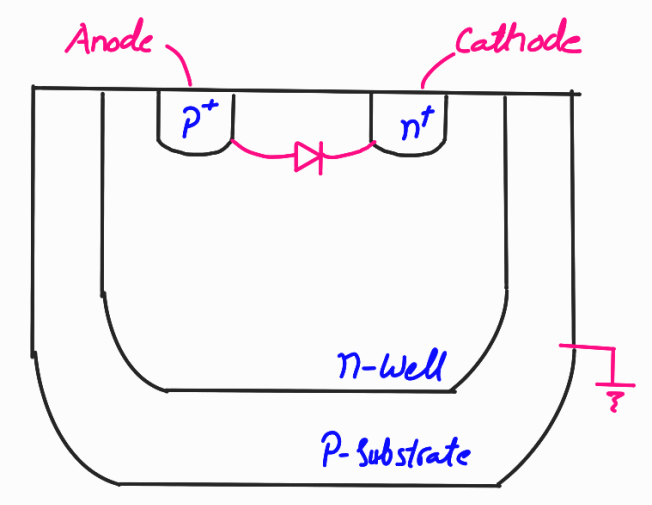
In standard CMOS we have a p-substrate.



If we make a n^+ implant in a p-substrate we get a diode. But in this design, we have p-substrate always connected to ground.

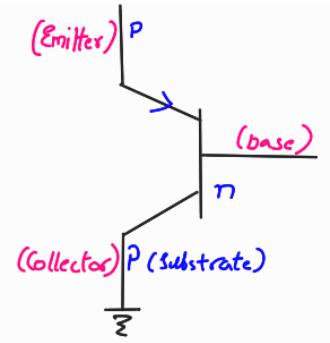
Instead, we want cathode (n) part of the diode to be grounded for making CTAT circuit.

B) 2nd Method:



In the pursuit of making a diode using CMOS process, here in this method first we put a n-well in p-substrate again over which p^+ & n^+ implant is done.

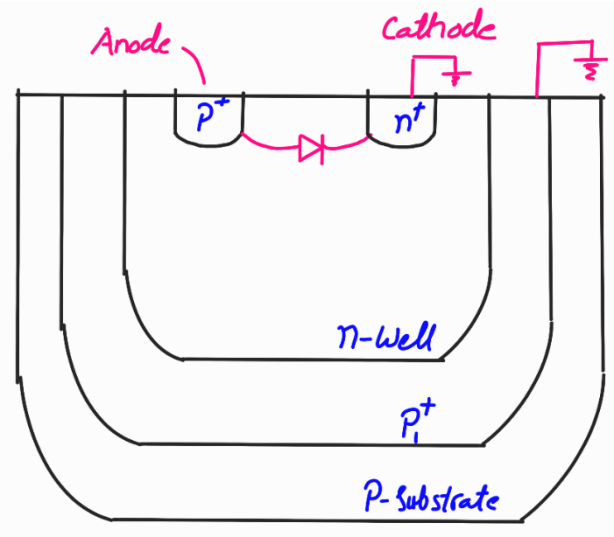
Unlike in a 1st method here anode & cathode of diode is free to connect anywhere.



But the structure formed by a 2nd method will form a p-n-p transistor which is essentially a parasitic BJT and in which large emitter-collector flows because of which all of our current will be flowing to the substrate but we wanted to make emitter-base as diode and make a current flow through that.

In a CMOS circuit same substrate is connected together as common substrate so any current creeping to the substrate will affect the other circuit present in the ICs. Hence, because of the formation of a parasitic BJT this design method is not applicable.

C) 3rd Method:



In contrast to the previous method in this design the current flowing from the p+ towards the substrate is collected by the p_1^+ and it is connected to the ground.

Thus because of the implant of p_1^+ in this design it is stopping the current from creeping into the substrate. Furthermore, for our CTAT design we wanted cathode to be grounded. Hence, 3rd type of method can be used to make our CTAT.

Schematic Diagram:

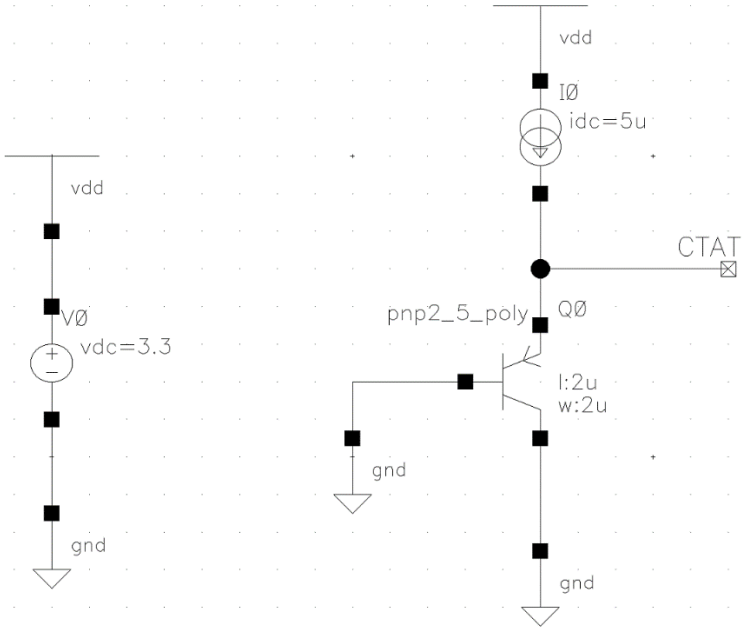


Figure 5: Schematic diagram of CTAT circuit

In our design, we have implemented diode using a BJT (pnp) with the current source in the emitter terminal replicating the proposed circuit in Figure 4. To implement the practically realizable circuit, we will be replacing the ideal current source by a current mirror in our design of band gap reference circuit.

Results:

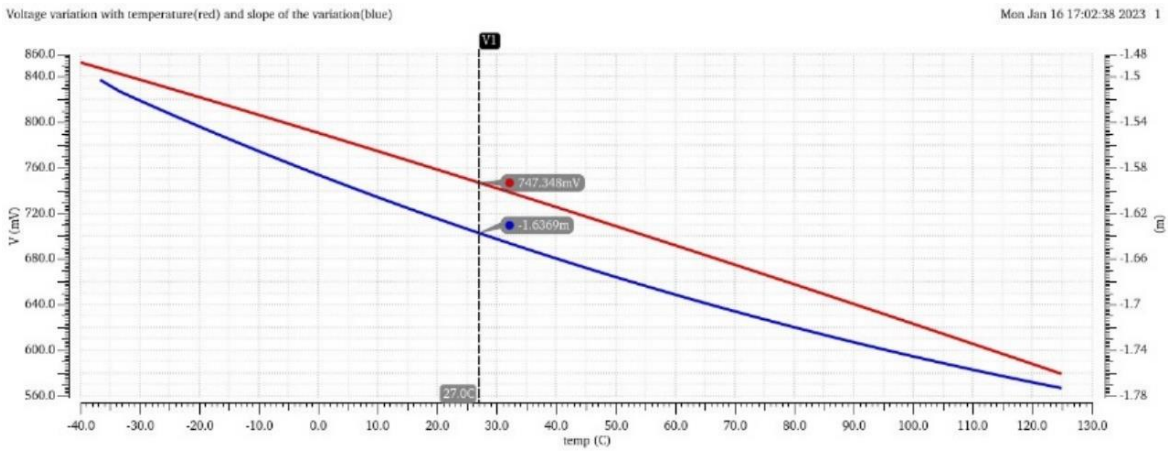


Figure 6: Characteristics of CTAT circuit

From the figure 6 we observed that as temperature increases, voltage decreases. Hence, we can conclude that CTAT is realized. Additionally, the slope of voltage w.r.t temperature (blue graph) is approximately -1.6 mV/°C with variations from -1.5 mV/°C to -1.78 mV/°C.

4. PTAT Design:

The circuit in which voltage increases with increase in temperature is called PTAT.

From the equation (3) we have $V_t \propto T$ which is a PTAT. Now, in order to extract the PTAT behavior of V_t from the circuit.

We have from equation (2);

$$V_D = V_t . ln\left(\frac{I_0}{I_s}\right)$$

The second term is CTAT because of the strong independence of I_s on temperature. Hence, we need to somehow cancel the CTAT part from V_D so that we get PTAT nature only.

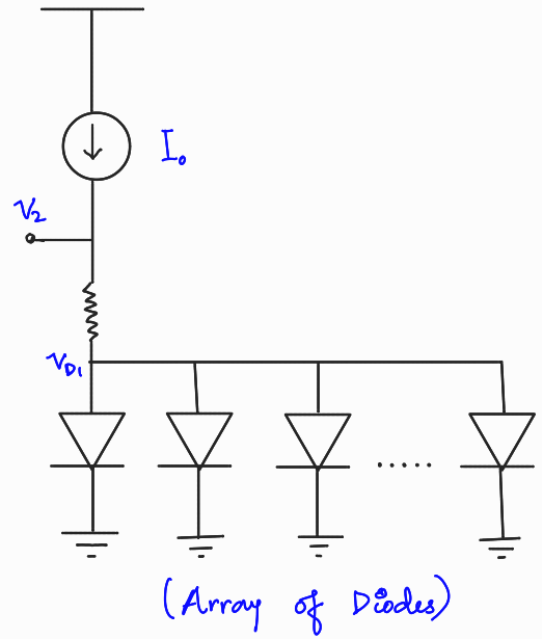


Figure 7: Array of diodes in parallel.

Diode equation is given as;

$$I = I_s . e^{\frac{V_D}{V_t}}$$

For array of diodes;

$$\therefore I_0 = n . I = nI_s . e^{\frac{V_D}{V_t}}$$

$$\therefore V_{D1} = V_t . ln\left(\frac{I_0}{nI_s}\right) \quad (9)$$

Subtracting equation (9) from (2) we get;

$$V_D - V_{D1} = V_t \left[ln\left(\frac{I_0}{I_s}\right) - ln\left(\frac{I_0}{nI_s}\right)\right]$$

$$\therefore V_D - V_{D1} = V_t \, ln(n) \quad (10)$$

Hence, the equation (10) has an ideal PTAT nature with proportional dependence on V_t thus with Temperature.

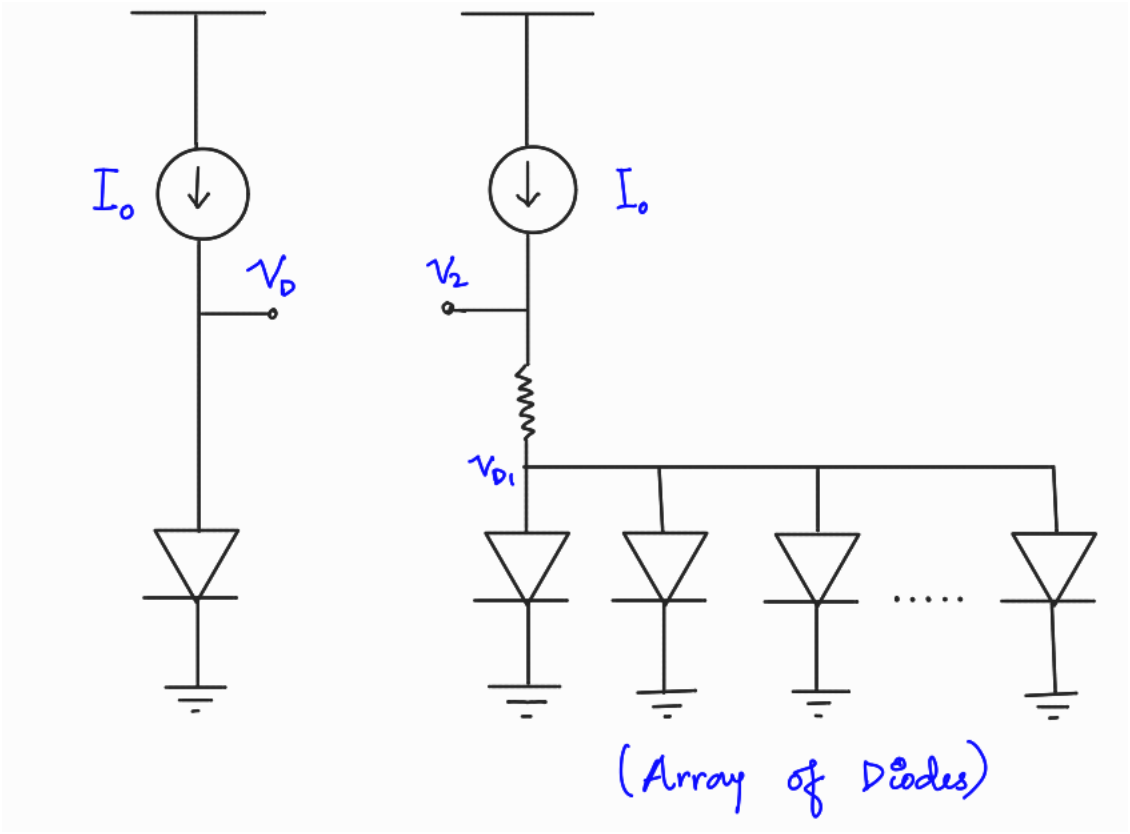


Figure 8: Proposed PTAT circuit.

Hence from the above proposed circuit if V_D -V_{D1} is extracted, then we

will achieve our PTAT nature. Alternatively, we can make $V_D = V_2$ and simply by extracting the voltage across the resistor we will get PTAT nature circuit.

If $V_D = V_2$ then,

$$V_D = I_0 R + V_{D1}$$

$$\therefore I_0 R = V_D - V_{D1} = V_t \ln(n) \quad (11)$$

Therefore, we got voltage across the resistor as PTAT.

Now, in order to make V_D and V_2 at same potential equal current must flow through both the branches.

To achieve our objective of equal current we can either use:

A) Current Mirror

B) Op-Amp

A) Current Mirror:

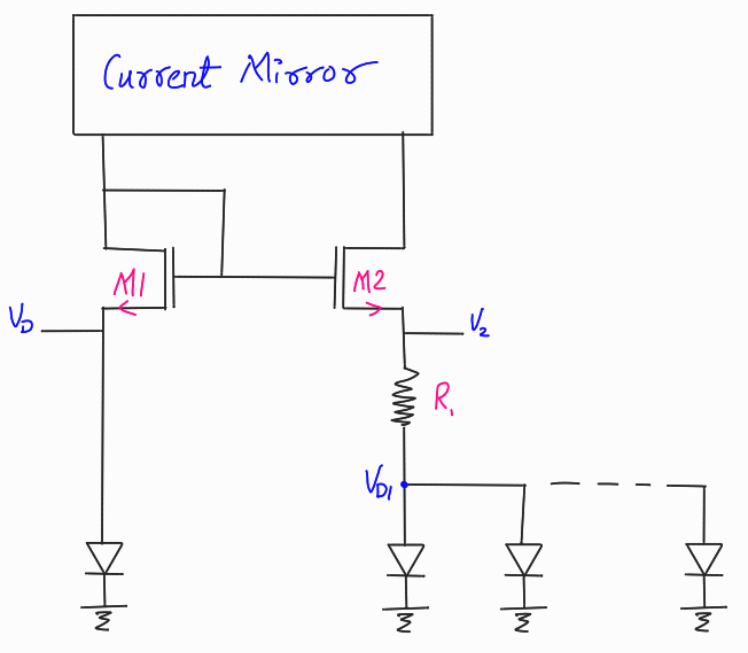


Figure 8: PTAT circuit with current mirror.

If

$$I_{DM1} = I_{DM2}$$

$$(V_{gs1} - V_t)^2 = (V_{gs2} - V_t)^2$$

$$V_{gs1} = V_{gs2}$$

As, V_g is equal in both transistors being in a common mode. Now in order to ensure $V_{s1} = V_{s2}$

$$i.e., V_D = V_2$$

Hence, current mirror will force the two branches to have an equal current that in turn ensures $V_D = V_2$

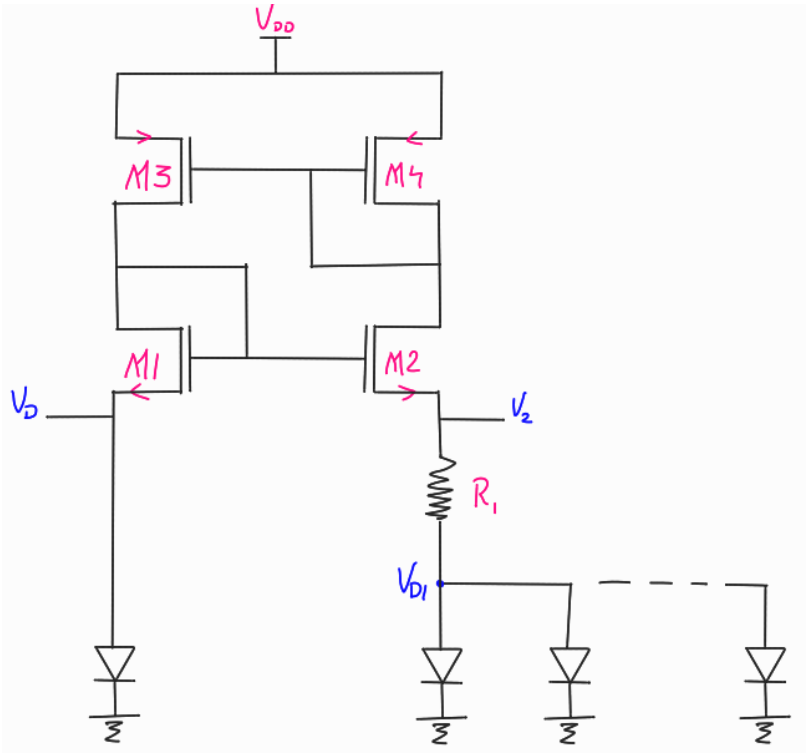


Figure 9: PTAT circuit with current mirror.

We need to ensure that dimension of all the MOSFET are equal so that equal current will flow through both the branches.

Here, two current mirror is used to satisfy two conditions A) Equal current through both branches & B) Same voltage at the source node of NMOS. And when $V_D = V_2$ then

$$I_0 R = V_2 - V_{D1} = V_D - V_{D1}$$

Hence, from equation (10) the resistor R_1 of figure 1 will behave as PTAT.

Separating a PTAT in a different branch:

Since, the PTAT resistor is above all the diode and is difficult to operate with when layout is done. Hence for that we can duplicate the current in another branch as shown in below design:

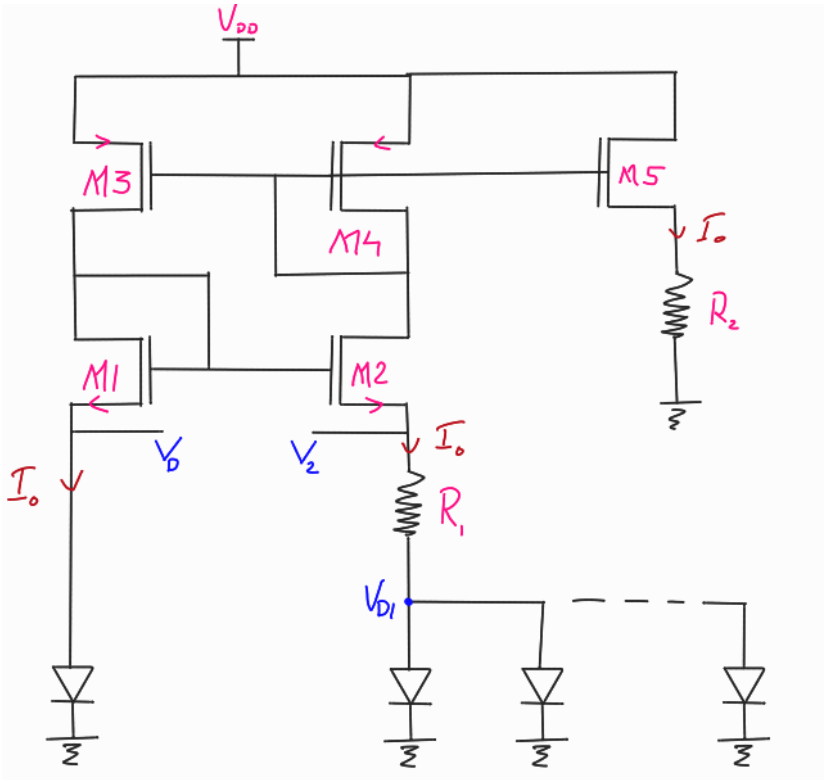


Figure 10: PTAT circuit.

From equation (11) we have;

$$I_0 R_1 = V_t \ln(n)$$

$$I_0 = \frac{V_t \ln(n)}{R_1}$$

From the figure (10) we have;

$$\therefore V_{R2} = I_0 . R_2$$

$$\therefore V_{R2} = \frac{R_2}{R_1} V_t \ln(n) \quad (12)$$

Hence, the voltage across the resistor R_2 is pure 'PTAT'

In the equation (1) we needed a scaled PTAT so that we can adjust it to get cancelled with the CTAT, from equation (12)

$$\therefore V_{R2} = \alpha_1 V_t \quad (13)$$

Hence, by adjusting R_2, R_1 and the number of diodes in parallel 'n' we can adjust the value of α_1. In our design we will be using only two diodes.

Finding the slope of PTAT:

Differentiating equation (11) with respect to temperature we get;

$$\frac{dV_{R2}}{dT} = \frac{R_2}{R_1} \ln(n) \frac{dV_t}{dT}$$

Hence, substituting equation (4) and keeping $R_2/R_1 = 1$ for now;

$$\therefore \frac{dV_{R2}}{dT} \approx 60\ \mu V/^{\circ}\mathrm{C}$$

Schematic Diagram:

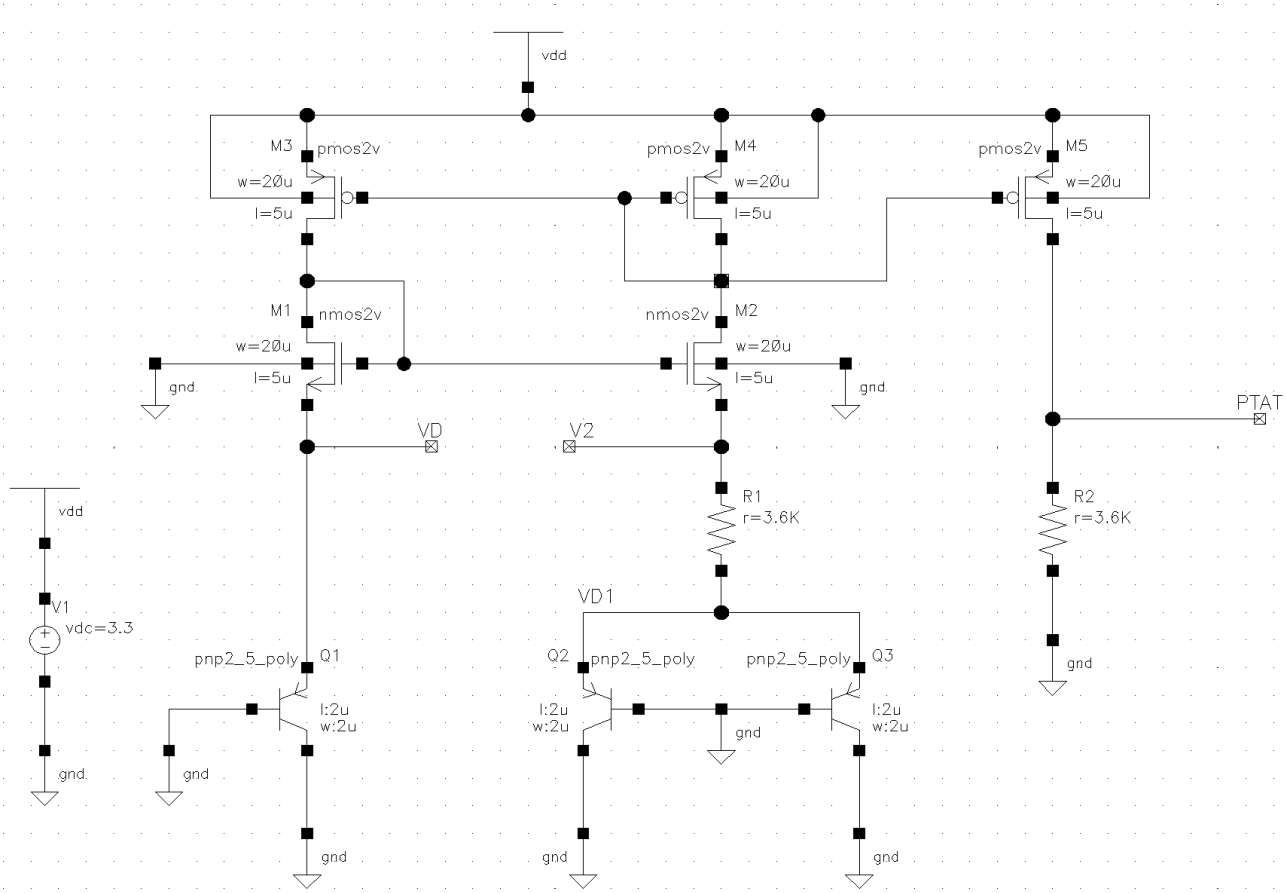


Figure 11: Schematic diagram of PTAT circuit

In CMOS technology BJT behaves like a diode when its base and collector terminals are shorted to ground. So in our design, we have implemented diode using a BJT (pnp) with the current source in the terminal replicating the proposed circuit. And also, to implement the practically realizable circuit, we have replaced the ideal current source by a current mirror while designing schematic of PTAT.

Result:

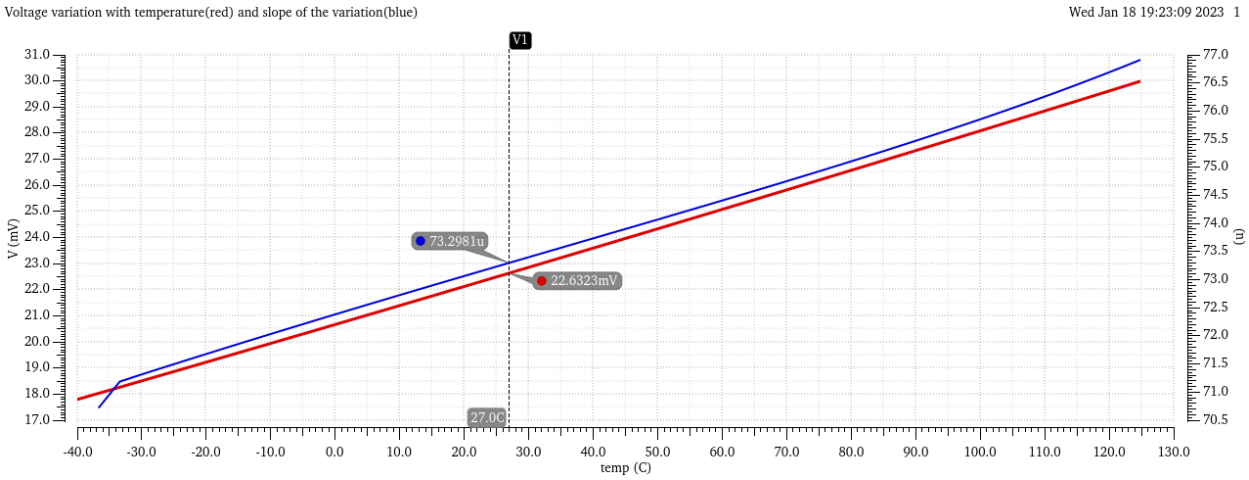


Figure 12: Characteristics of PTAT circuit

From the figure (12) we observed that as temperature increases, voltage increases. Hence, we can conclude that PTAT is realized. Additionally, the slope of voltage with respect to temperature (blue graph) is approximately 73.29 µV/°C with variations from 71 µV/°C to 77 µV/°C.

5. BGR design with current mirror:

Now to get voltage reference;

$$V_{ref} = PTAT + CTAT$$

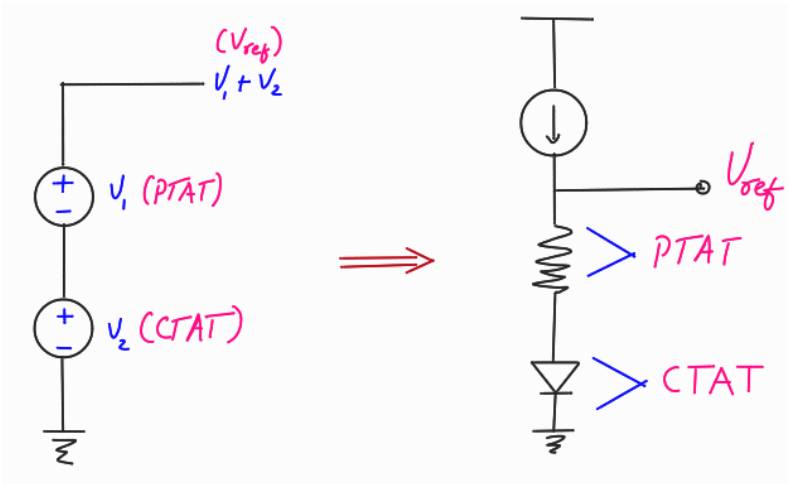


Figure 13: Combining CTAT and PTAT

Hence, combining CTAT and PTAT and making a schematic diagram;

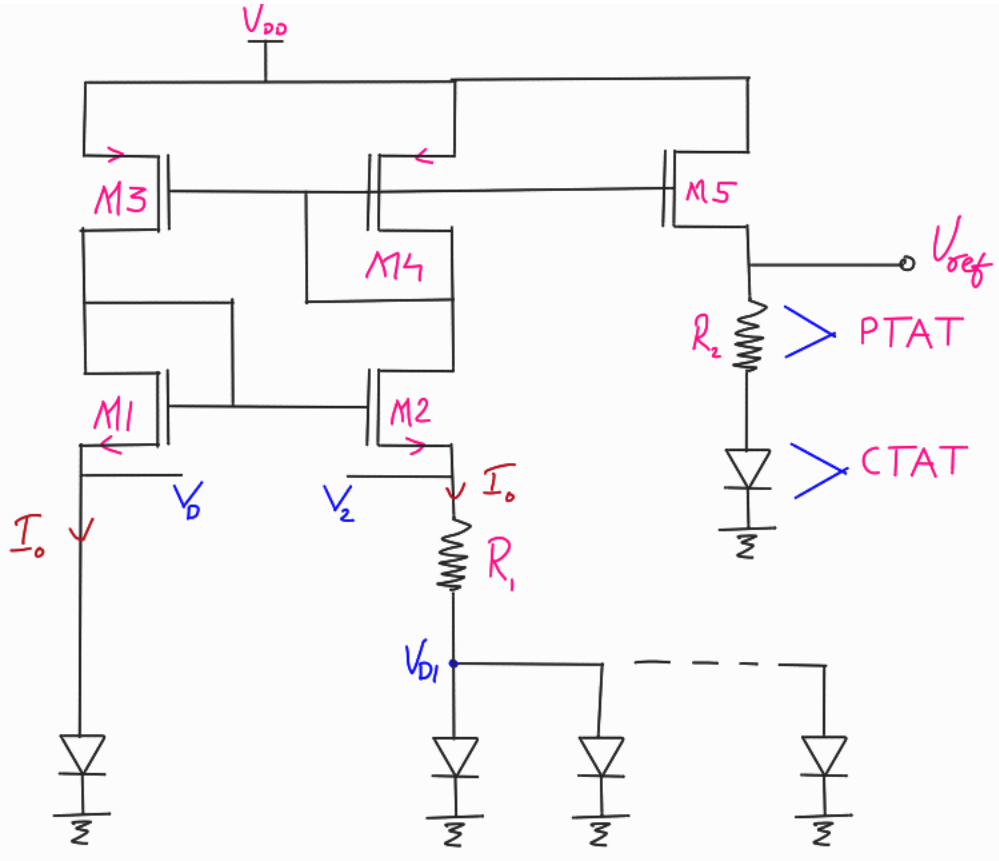


Figure 14: Proposed BGR circuit.

By the definition of CTAT we know that constant current needs to flow through the diode but PTAT current is flowing through the 3rd arm.

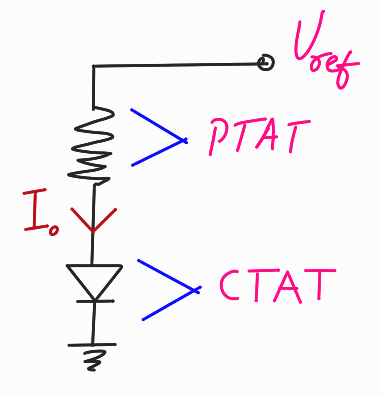


Figure 15: Current through 3rd arm.

Here,

$$I_0 = \frac{V_t . \ln(n)}{R_1}$$

But I_0 is PTAT not a constant. Now to see the effect of PTAT current on diode.

We know from equation (2);

$$V_D = V_t . ln\left(\frac{I_0}{I_s}\right)$$

But here figure (14) I_0 is not a constant. V_t is weak PTAT and I_s is strong CTAT.

Differentiating V_D with respect to temperature,

$$\frac{dV_D}{dT} = \frac{d\left[V_T\left(ln(I_0) - ln(I_s)\right)\right]}{dT}$$

$$\frac{dV_D}{dT} = V_t\left[\frac{1}{I_0}\frac{dI_0}{dT} - \frac{1}{I_s}\frac{dI_s}{dT}\right] + \left[ln(I_0) - ln(I_s)\right]\frac{dV_t}{dT} \quad (14)$$

To find $\frac{dI_0}{dT}$,We know that,

$$\therefore I_0 = \frac{\ln(n)}{R_1} V_t \quad (15)$$

$$\frac{dI_0}{dT} = \frac{ln(n)}{R_1} . \frac{V_t}{T}$$

Again, substituting equation (15) we get;

$$\therefore \frac{dI_0}{dT} = \frac{I_0}{T} \quad (16)$$

Now, substituting equation (16), (7) & (4) in equation (14),

$$\therefore \frac{dV_D}{dT} = \frac{V_D - (3+m)V_t - \frac{E_g}{q}}{T} \quad (17)$$

In compare to equation (8) when I_0 is constant and equation (17) when I_0 is PTAT both the equation is almost identical. To validate the CTAT nature of diode with PTAT current flow let us substitute the value in equation (17);

$$\frac{dV_D}{dT} = \frac{0.75 - \left(3 - \frac{3}{2}\right) \times 26mV - 1.2}{300}$$

$$\therefore \frac{dV_D}{dT} \approx -1.63mV/°C$$

Here, negative sign indicates that if temperature increases the voltage decreases so still, we are getting a CTAT nature even if the current through the diode is PTAT.

Conclusion: There is not much difference in $\frac{dV_D}{dT}$ even being current PTAT.

Design of α_1 & α_2:

We have,

$$CTAT\ slope = \frac{dV_D}{dT} \approx -1.6mV/°C$$

$$PTAT\ slope = \frac{dV_t}{dT} \approx 60\ \mu V/°C$$

$$V_{ref} = \alpha_1 . V_t + \alpha_2 . V_D$$

As we need, $\frac{dV_{ref}}{dT} = 0$ so;

$$\alpha_1 . 60\ \mu V/℃ - \alpha_2 . 1.6\ mV/℃ = 0$$

Since, the slope of PTAT is less than that of CTAT so let's increase the PTAT to completely cancels the CTAT voltage. Hence, $\alpha_2 = 1$

$$\alpha_1 = \frac{1.6\ mV}{60\ \mu V}$$

$$\therefore \alpha_1 = 26.67$$

We have from equation (12) and above;

$$V_{ref} = \frac{R_2}{R_1} \ln (n) . V_t + V_D$$

$$\therefore V_{ref} = 26.67 \times V_t + V_D$$

Substituting the values we get,

$$\therefore V_{ref} = 1.39 \approx 1.2\ V$$

Is the standard bandgap reference voltage.

Note: In general, in layout point of view n=8 diodes are used for matching purpose and to avoid systematic mismatch. But for schematic n=2 works fine.

Example Design:

We have, I_0 = 5 uA and we know $I_0 = \frac{\ln(n)}{R_1} V_t$

So,

$$R_1 = \frac{\ln(n)}{I_0} V_t$$

Hence, substituting values we get $\therefore R_1 = 3.6\ k\Omega$

We have, $\alpha_1 = \frac{R_2}{R_1} \ln(n)$

So,

$$R_2 = \frac{\alpha_1 . R_1}{\ln(n)}$$

Hence, substituting values we get $\therefore R_2 = 138.51\ k\Omega$

R_2 can be swept with the range of values such that PTAT and CTAT nature perfectly cancels each other.

Schematic Diagram:

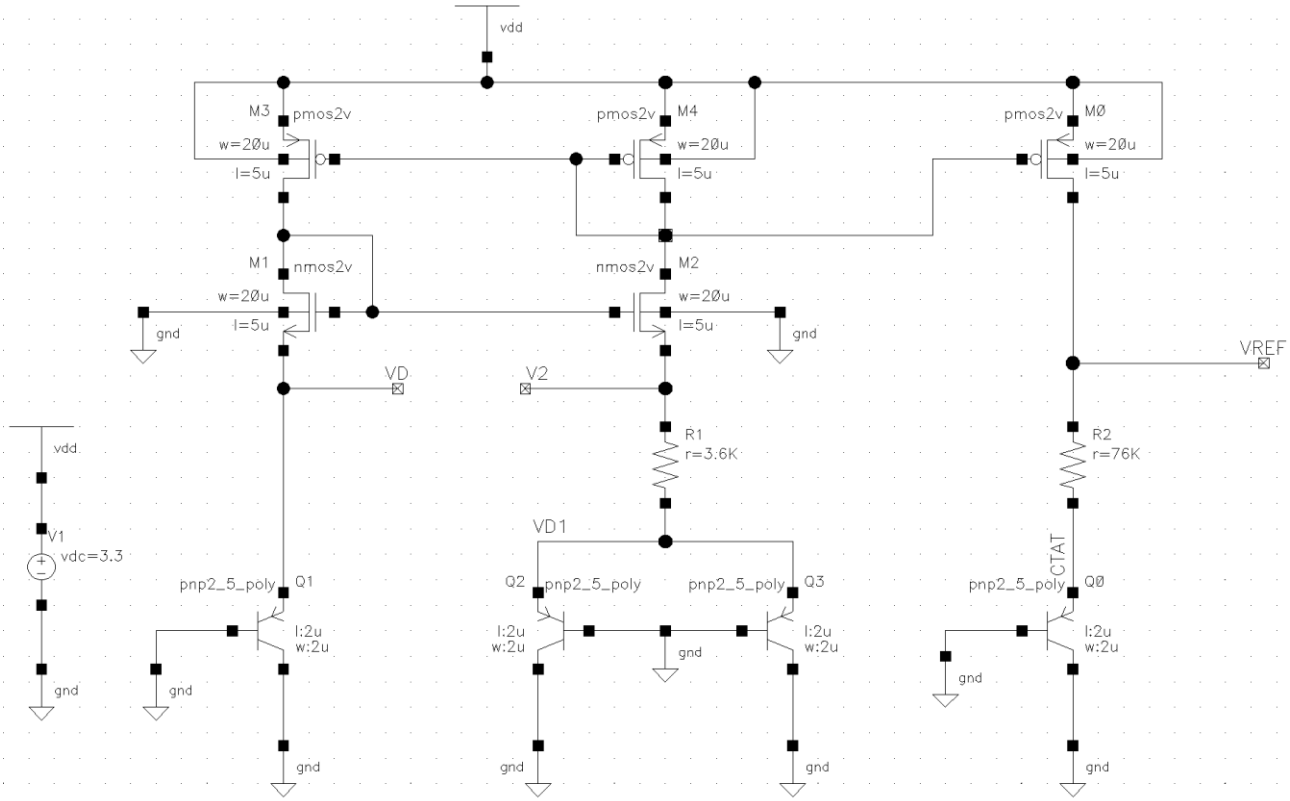


Figure 16: Schematic diagram of BGR circuit

The figure (16) depicts the schematic diagram for BGR by combining CTAT and PTAT using current mirror circuit as current source.

Result:

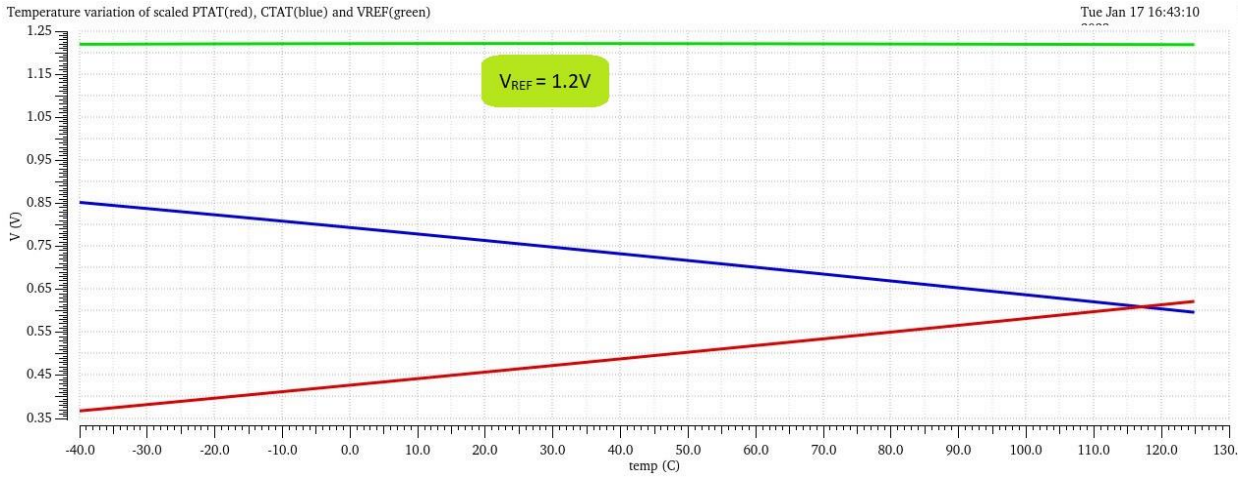


Figure 17: Temperature variation of CTAT, PTAT & V_{REF}

Hence, by adding scaled CTAT and PTAT we obtained a band gap reference of ≈ 1.2 V

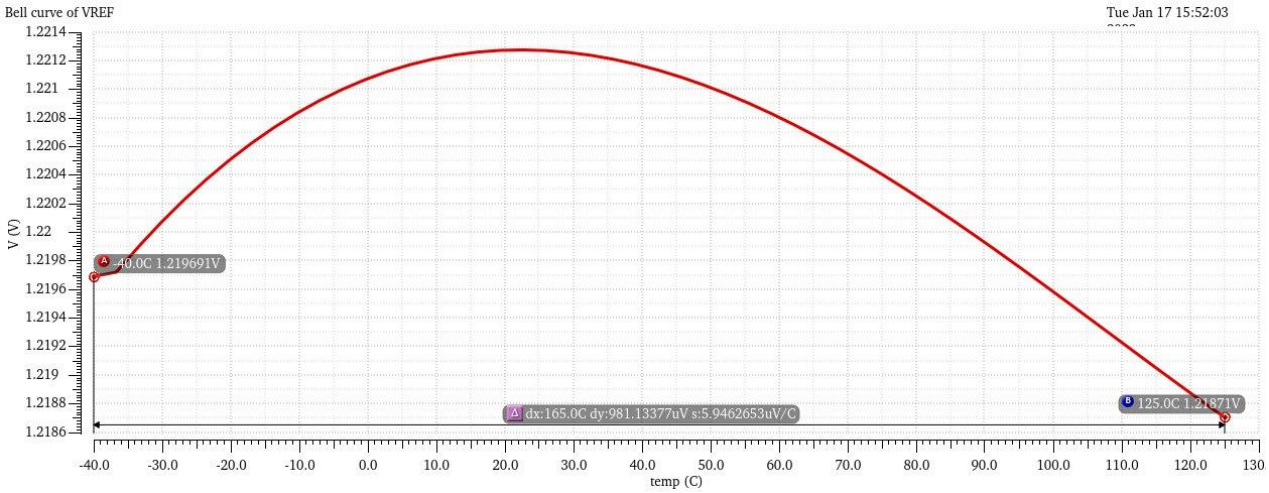


Figure 18: Bell curve of V_{REF}

When we zoomed in the graph of V_{REF}, it looks like a bell-shaped curve with maximum variation 981 uV. And we are getting such bell-curve because our CTAT and PTAT are not exact straight lines.

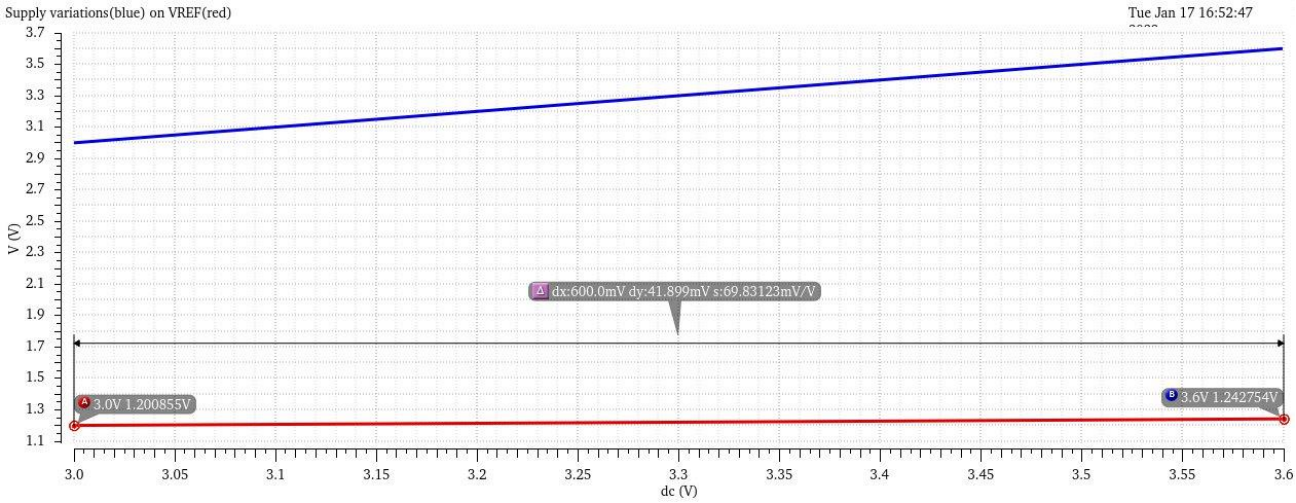


Figure 19: Supply variations on V_{REF}

When evaluated with supply variation, we got 41 mV deviation over 0.6V. Furthermore, if supply voltage and temperature variations is to be reduced, we need to use complex cascode mirror. Yet again using a cascode structure demands for higher supply voltage so trade-off is to be done as your requirement.