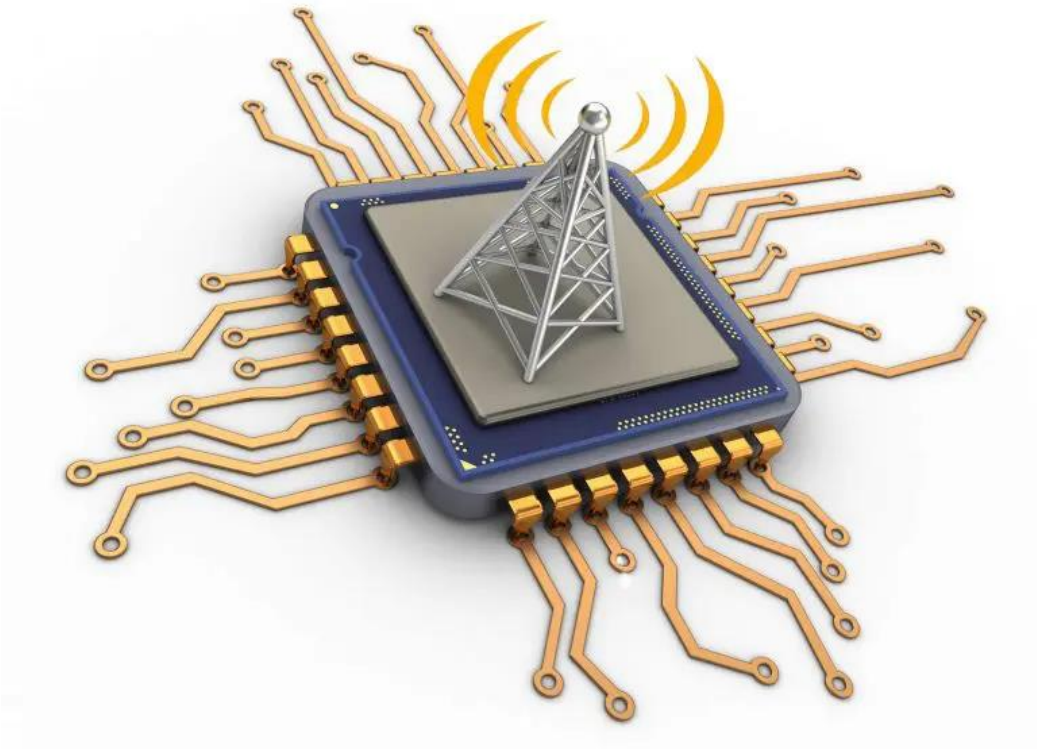
COOK-BOOK OF Two Stage Op-Amp



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1. Motivation:

This Cook-Book present the design conduct that is to be followed for the designing of the Two-Stage Operational amplifier. The need of 2-Stage Opamp over single stage differential amplifier (5-transitor OTA) is caused by the demand for the higher gain. Because of its immunity to environmental noise, it has gain immense popularity in analog circuit.

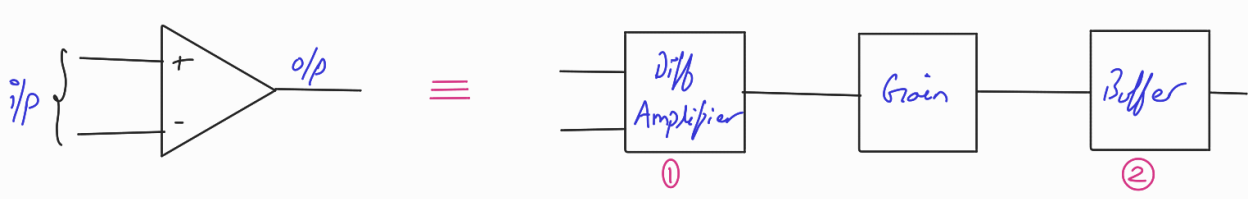

Figure 1: Disintegration of Op-amp

(1) Differential Amplifier of 40dB gain is not suitable to make a negative feedback amplifier so it is followed by the Gain block as a second stage but if we make an Op-Amp without a (2) Buffer stage the it is simply called a Transconductance Amplifier.

Hence, we will be designing the three blocks in stages and analyze it stepwise basis.

2. Design Requirement:

A) Technology: UMC 180nm process

B) Supply Voltage (V_{dd}) = 1.8 V

C) Voltage gain (A_v) = 1000 (60dB)

D) Load Capacitor (C_L) = 2pF

E) Input Common mode range (ICMR) = Max: +1.6V & Min: -0.8V

F) Slew Rate (SR) = 20V/usec

G) Power Dissipation < 300 uW

H) Gain Bandwidth Product (GBW) = 30 MHz

I) Phase Margin (PM) $\geq 60°$

This project aims to achieve a typical design requirement. Although following the cook-book, any design need similar to this can be achieved with proper tuning.

3. Two Stage Op-Amp Topology:

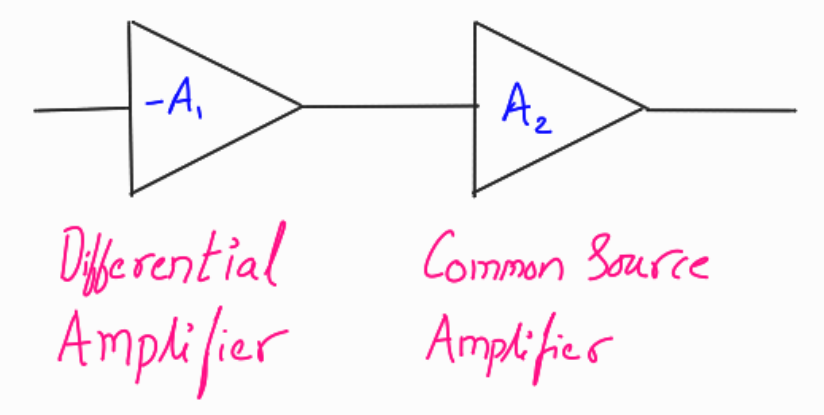

Figure 2: Block diagram of Op-amp topology

Now for the Common source amplifier we have two option two choose from a) NMOS Common Source b) PMOS Common Source

We are using PMOS CS Amplifier as a 2nd stage for a competent headroom *[Ref: Which transistor type to use for the second stage? By Dr. Nagendra Krishnapura, Course: Analog Circuits, IIT Madras]*

We can make more stages, having more gain E.g.: 5 stages without any issues of head room but the issue arises because of the increasing poles.

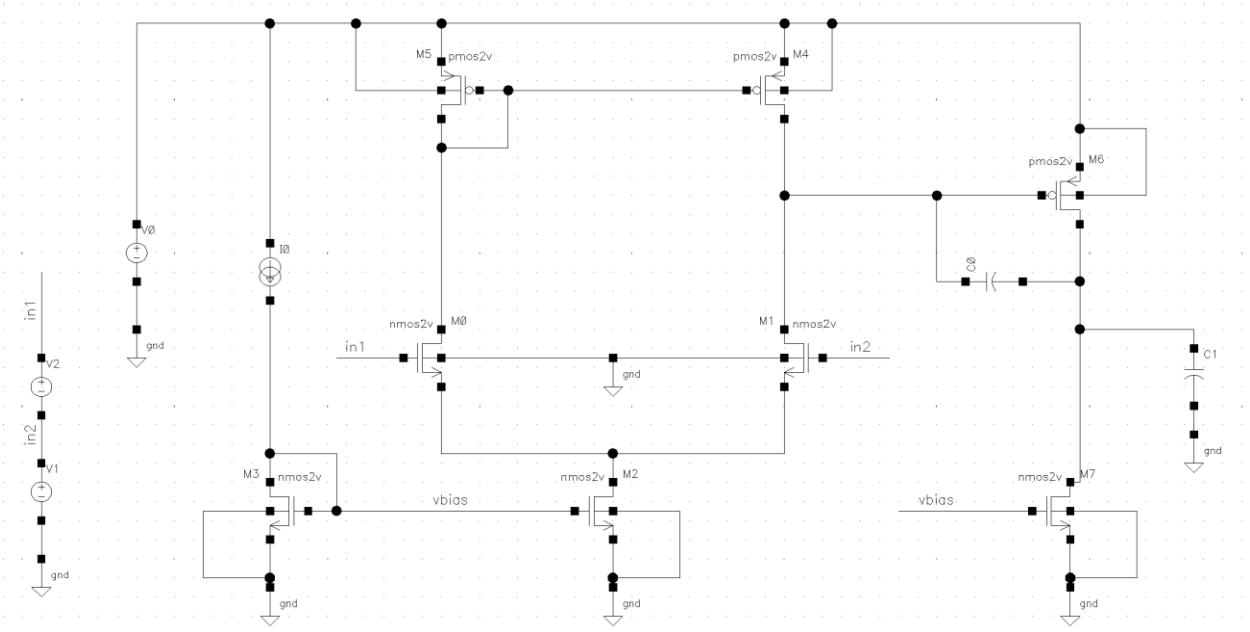

Figure 3: Proposed Two Stage Op-Amp topology

We want to achieve Positive gain out of 2nd stage hence, we switched the sign in 1st stage (in1 = -ve & in2 = +ve) such that negative from 1st stage and one more negative from Common source results in total positive gain.

4. Small signal model of Two Stage Op-Amp:

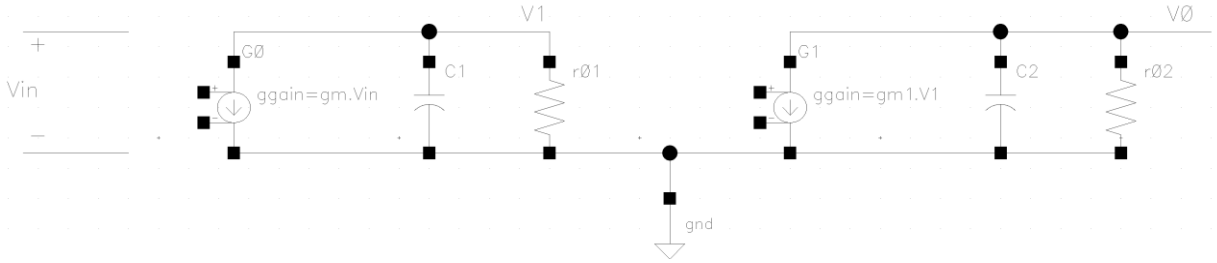

Figure 4: Small signal model

Where,

C_1 = parasitic capacitances of 1st stage, E.g., C_{DS} of M2 and M4

& $C_2 \approx C_L$ ($\because C_L$ is much bigger compared to the parasitic of 2nd stage Amplifier)

Two stage Op-Amp is a two-pole system,

$$P_1 = \frac{1}{r_{01}.C_1} \text{ and } P_2 = \frac{1}{r_{02}.C_L}$$

 # Bode Plot

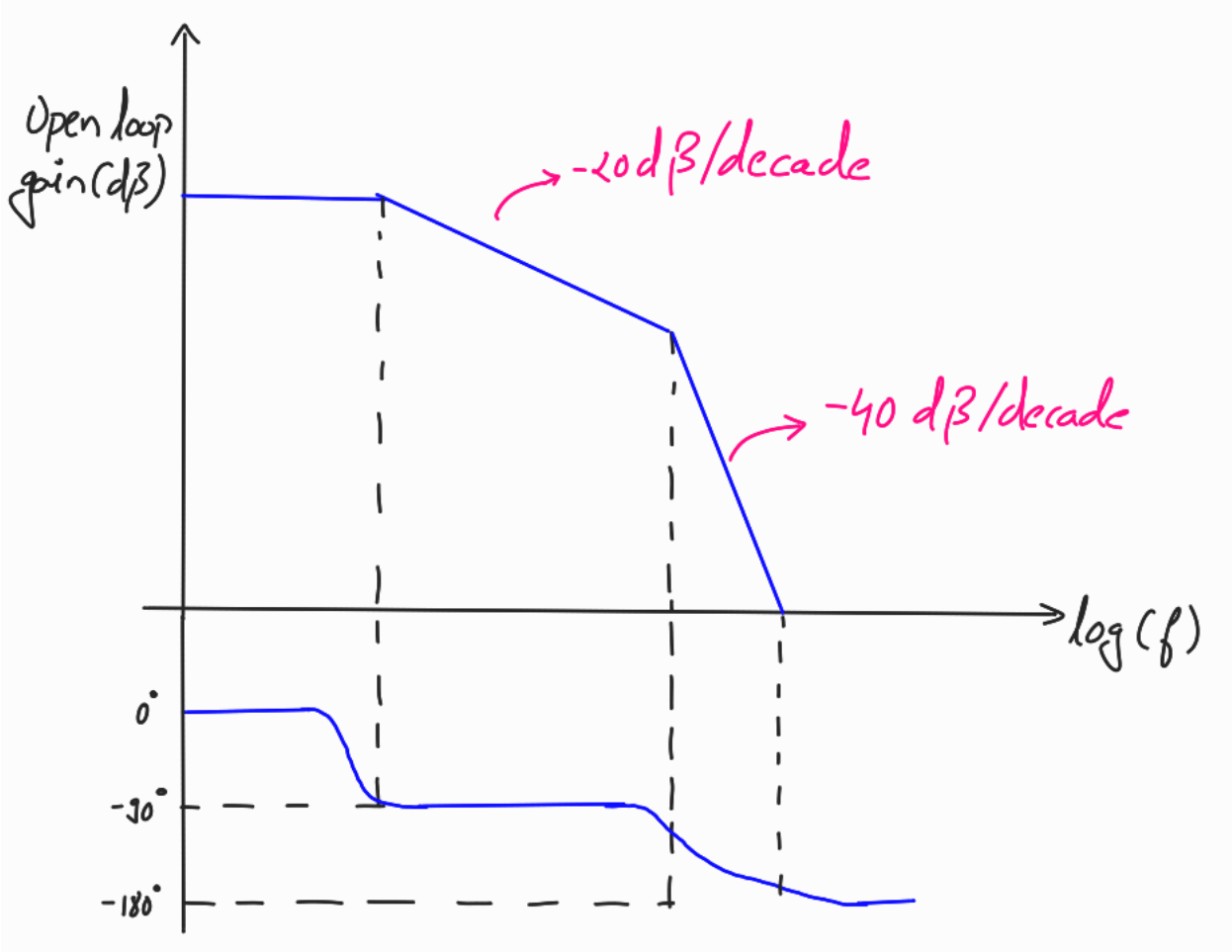

Figure 5: Bode Plot

We can see the phase margin is very close to zero.

By definition,

$$Phase\ Margin(PM) = (Phase\ crossover\ frequency\ at\ -180°) - (Unity\ Gain\ Crossover\ frequency)$$

A) PM = Positive => Stable System

B) PM = 0 => Marginally Stable System

C) PM = Negative => Unstable System

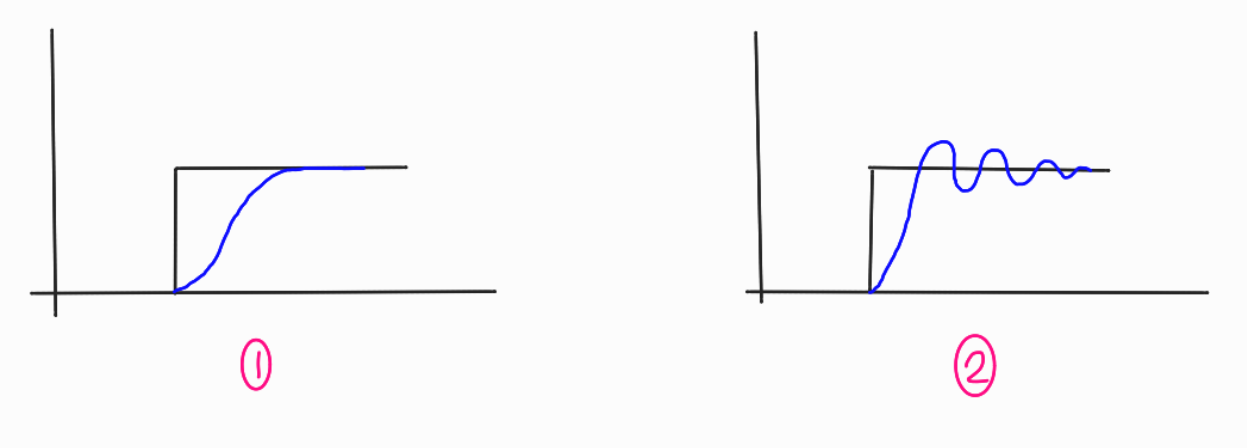

Figure 6: (1) Good Phase Margin (2) Bad Phase Margin

If the system has a Bad Phase Margin is, then Ringing effect will arise in the system. For removing the ringing effect, we need a phase margin of minimum 45°.

To be in a safe side Phase Margin of 60° is needed which is also specified in a Design Requirement.

5. Compensation Method:

With the aim of having good Phase Margin let us do the comprehensive analysis of the two-pole system.

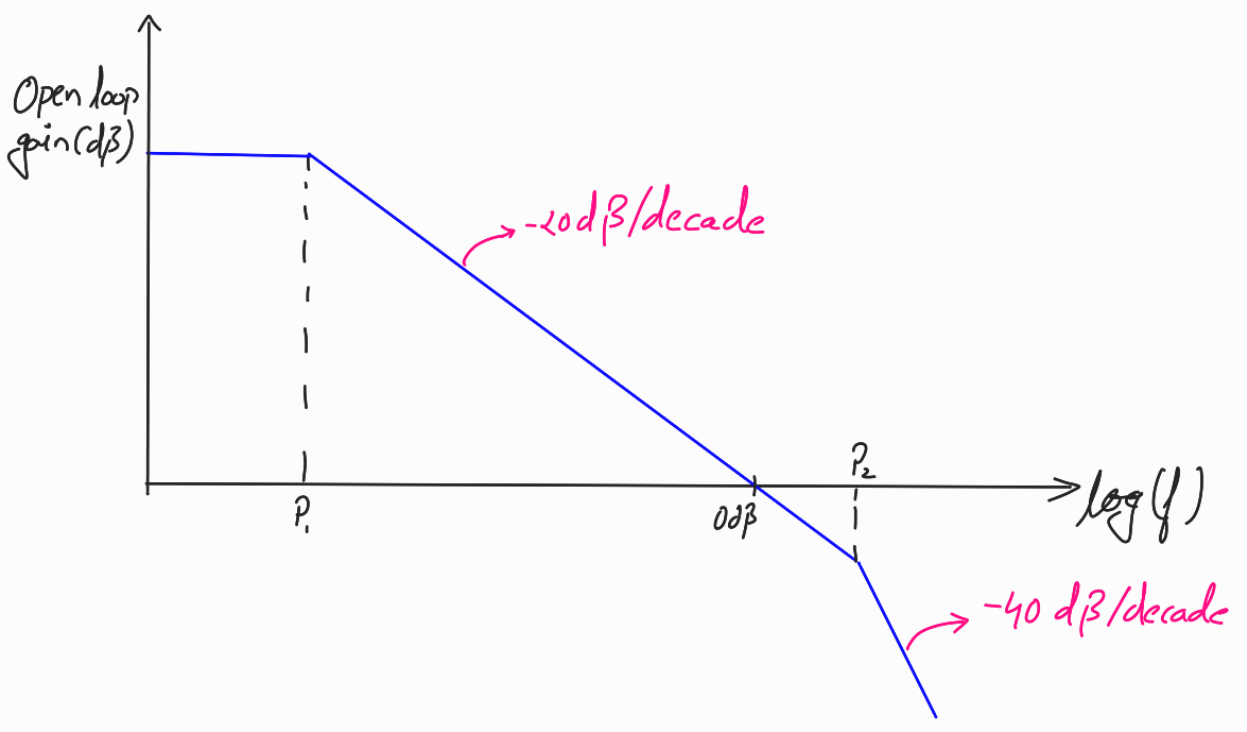

Figure 7: Shifting of Poles

The proposed idea is to move the Pole P_1 or P_2 in such a way that the gain crosses 0dB before the Pole P_2. And effectively since P_2 is very far away will not have any effect.

Hence, in this way we have a Single pole system even if 2 poles exist.

We have,

$$P_1 = \frac{1}{r_{01}.C_1} \text{ and } P_2 = \frac{1}{r_{02}.C_L}$$

Now, since C_L is a Load Capacitance which is design specified hence over which we don't have much control.

Therefore, the plan is to increase the value of C_1 such that the 1st Pole can be moved to the left side.

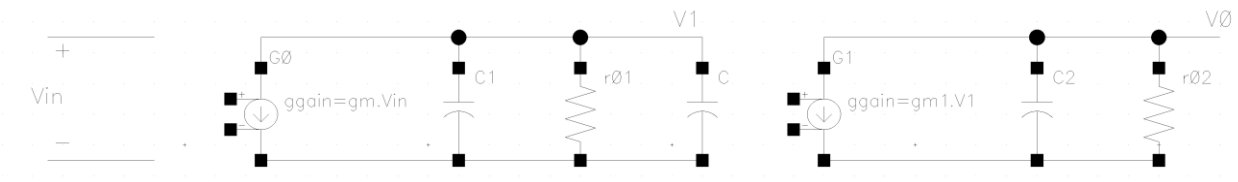

Figure 8: Shifting of P_1 using a Big Fat Capacitor (C)

Now the 1st pole will effectively become, $P_1 = \frac{1}{r_{01}.(C_1+C)}$

The 1st pole has shifted towards left thereby achieving our primary goal.

But, to avoid the use of Big Fat Capacitor we can utilize the Miller effect.

Miller Effect:

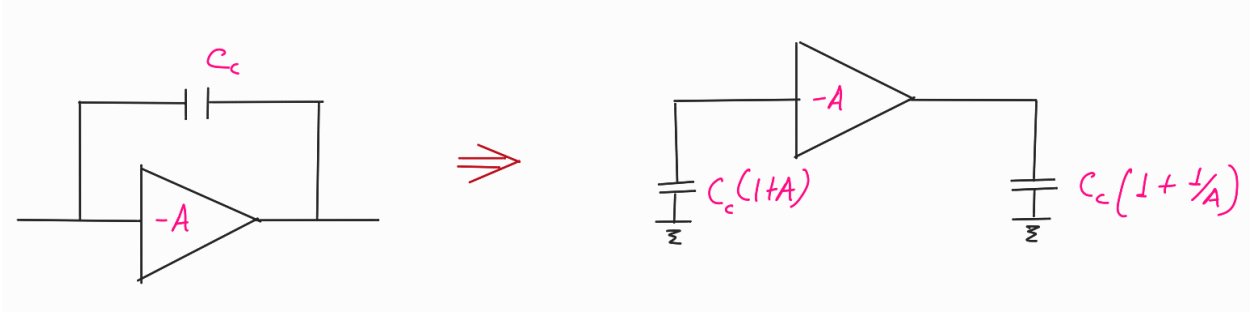

Figure 9: Miller Effect