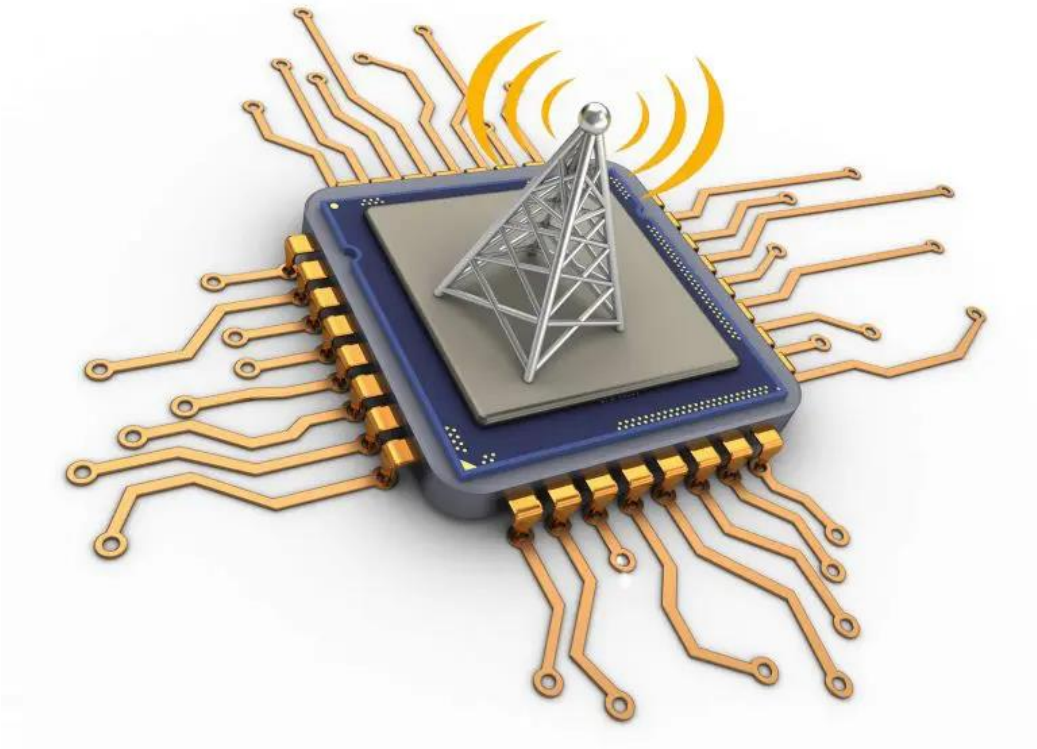
COOK-BOOK OF DIFFERENTIAL AMPLIFIER



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1. Motivation:

This Cook-Book present the design conduct that is to be followed for the designing of the differential amplifier. The need of Differential amplifier over single ended amplifier is caused by the dependence of current drawn to the circuit on V_{DD} which corrupts the signal. Because of its immunity to environmental noise, it has gain immense popularity in analog circuit.

The use of Differential Amplifier can be found in various Analog, RFIC/Mixed-Signal as an essential part of complex circuits. Hence the design knowledge of differential amplifier is crucial to understand the working of IC's.

2. Design Requirement:

A) Technology: UMC 180nm process
B) Supply Voltage (V_{dd}) = 1.8 V
C) Voltage gain (A_v) = 100 (40dB)
D) Load Capacitor (C_L) = 10pF
E) Input Common mode range (ICMR) = Max: +1.6V & Min: -0.8V
F) Slew Rate (SR) = 5V/usec
G) Power Dissipation < 3mW
H) Gain Bandwidth Product (GBW) = 5MHz

This project aims to achieve a typical design requirement. Although following the cook-book, any design need similar to this can be achieved with proper tuning.

3. Differential Amplifier Topology:

There are different types of differential amplifier topology available which have scope to achieve the set design requirement. This project is using 5 transistor “operational transconductance amplifier” (OTA) which provides better gain compared to other. As this project aims to have higher gain than specified in design requirement, 5 transistor OTA is preferred.

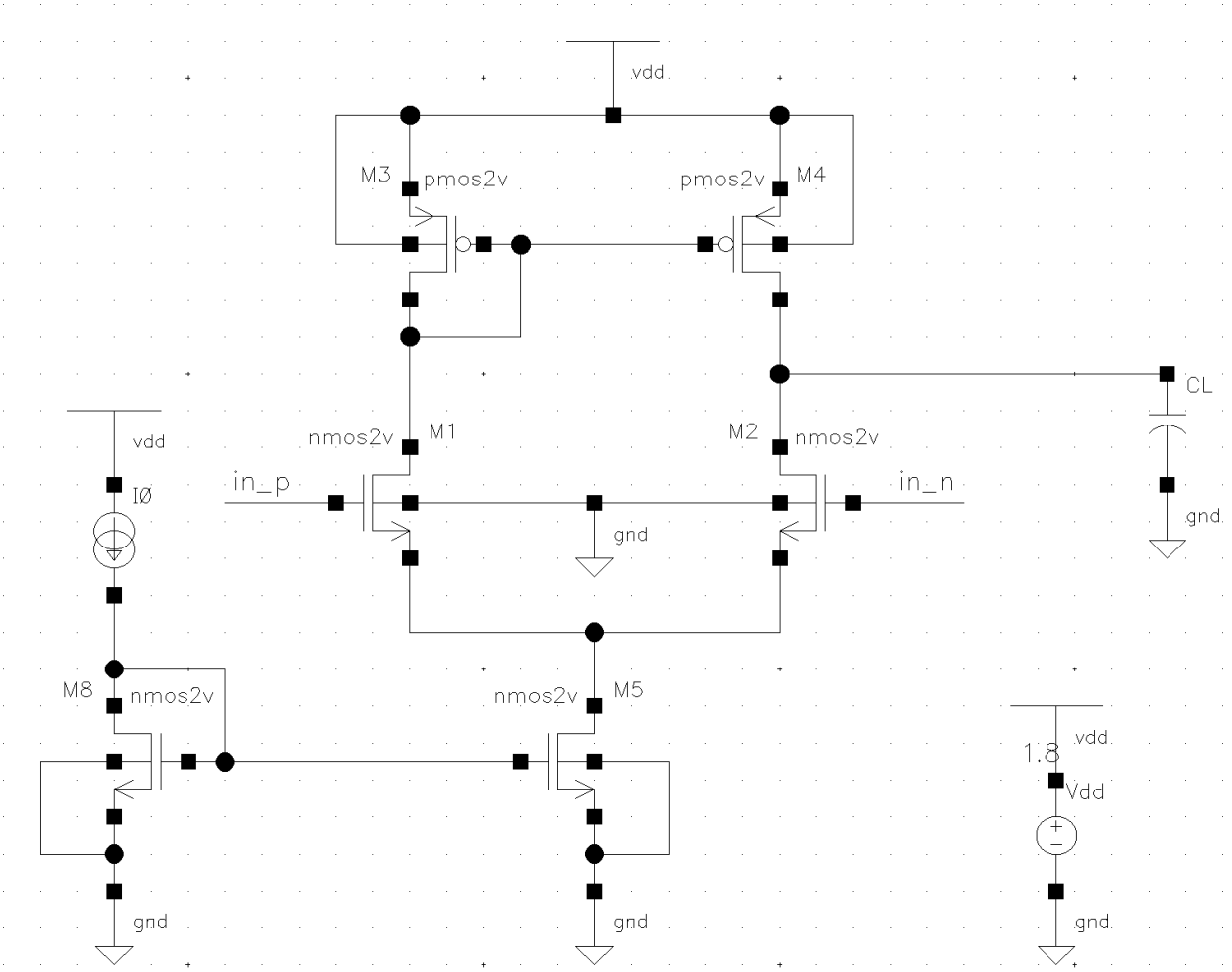


Figure 1: Proposed differential amplifier topology

Note:

- Body of PMOS is connected to highest potential and NMOS to lowest potential
- Try to follow the same terminology & nomenclature to avoid confusion.

Now as a designer we have to make sure that all the MOSFET's are in saturation and simultaneously meet the design requirement of differential amplifier.

4. Cook-Book of Differential Amplifier:

Steps:

4.1. Find I_0 from Slew rate from the design specification.

4.2. Find M_3, M_4 aspect ratio from ICMR (Max).

4.3. Find M_1, M_2 aspect ratio from GBW.

4.4. Find M_5 aspect ratio from ICMR (Min).

4.5. Find M_8 aspect ratio from I_0 & M_5.

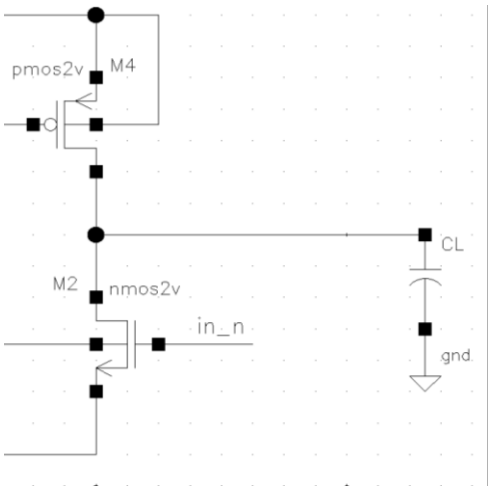
4.1. Calculate I_0 from Slew rate:

Slew Rate (SR): is the maximum rate of change of voltage or current w.r.t time.

Slew rate is present when one half circuit is completely OFF and another half is completely ON. Let us assume that M4 and M2 are completely ON.

a) For charging of the capacitor, M4 is responsible assuming that current flowing through M4 is more than I_0

b) For discharging of the capacitor, M2 is responsible, assuming that current flowing through M2 is less than I_0



As we have assumed that M4 and M2 side is only ON but another half circuit is off. Now since M4 is current mirrored with M3 no current is going to flow through the M4 there upon capacitor is going to discharged.

As we know,

$$I = C\frac{dV}{dt} \tag{1}$$

$$\therefore \frac{dV}{dt} = \frac{I}{C} \tag{2}$$

Also, by the definition of Slew Rate,

$$Slew\ Rate(SR) = \frac{dV}{dt} \tag{3}$$

$$SR = \frac{I_0}{C_L} \tag{4}$$

$$\therefore I_0 = SR\,.\,C_L \tag{5}$$

Thus, I_0 is successfully calculated from slew rate.

For our design:

Given, SR = 5V/usec & C_L = 10pF

By substituting in equation (5) we get,

$$I_0 = 50\ uA$$

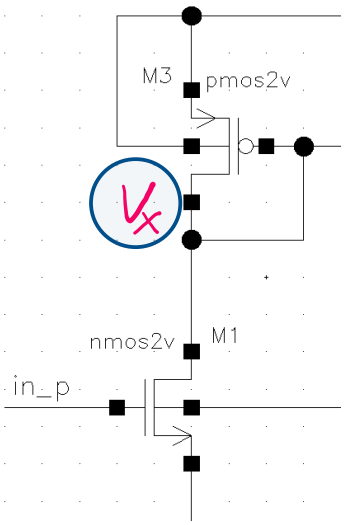
Hence, we need 50 uA current flowing through M5 and 25 uA current is going to flow through the branches of differential amplifier.

4.2. Calculate M_3, M_4 aspect ratio from ICMR (Max):

Since, the dimension of M3 and M4 is same let us take half circuit for easy analysis.

For M1 to be in Saturation,

$$V_x > V_{in} - V_{th1}$$



Considering extreme case i.e., $V_{in} = ICMR(Max)$

$$V_x > ICMR(+) - V_{th1}$$

For M3 to be in saturation,

$$V_{DS3} = V_{DD} - ICMR(+) + V_{th1} \qquad (6)$$

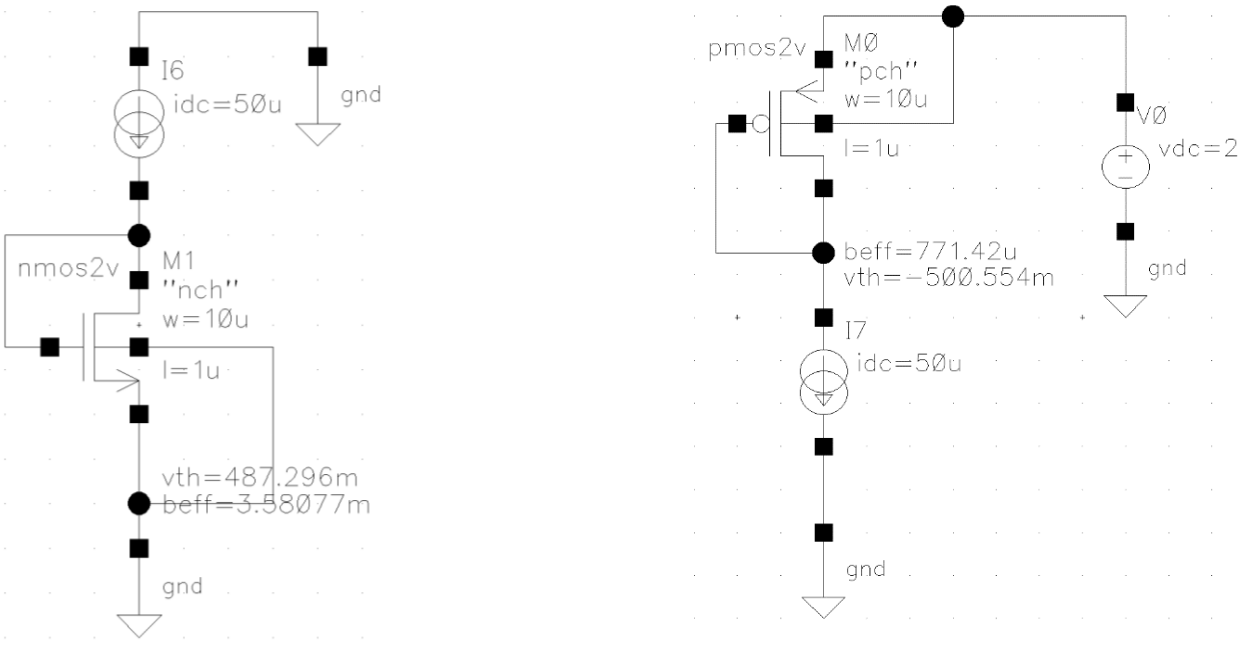
Where, $V_{DD} = 1.8\,V$, $ICMR(+) = 1.6\,V$ and $I_0 = 25\,uA$.

In order to calculate $\left(\frac{W}{L}\right)_3$: Finding V_{th1} and $u_n C_{ox}$ using simulation and then solving saturation current equation of M3.

To Calculate V_{th1} & $u_n C_{ox}$ using Simulation:

To avoid channel length modulation "λ"

Taking Length (L) = 1 um even if L_{min} = 0.18 um.



a) b)

Figure 2: a) NMOS pushing current b) PMOS pulling current

We have taken $\left(\frac{W}{L}\right)_{eff} = 10$ for both NMOS and PMOS

We know, For PMOS

$$\beta_{eff} = u_p C_{ox} \left(\frac{W}{L}\right)_{eff} \quad (7)$$

Then substituting, $\left(\frac{W}{L}\right)_{eff}$ and β_{eff} from simulation in equation (7)

$$u_p C_{ox} = \frac{uA}{V^2}$$

We know, For NMOS

$$\beta_{eff} = u_n C_{ox} \left(\frac{W}{L}\right)_{eff} \quad (8)$$

Then substituting, $\left(\frac{W}{L}\right)_{eff}$ and β_{eff} from simulation in equation (8)

$$u_n C_{ox} = \frac{uA}{V^2}$$

Also from Simulation,

$$V_{thn} = 0.487\ V$$

$$V_{thp} = 0.5V$$

Finally Calculating the aspect ratio of M3 and M4 using saturation current equation:

$$I_{DS3} = \frac{u_p C_{ox} \frac{W}{L}}{2} [V_{gs} - V_t]^2 \qquad (9)$$

4.3. Calculate M_1, M_2 aspect ratio from GBW product:

Drawing small signal model of right half circuit of 5 transistor OTA,

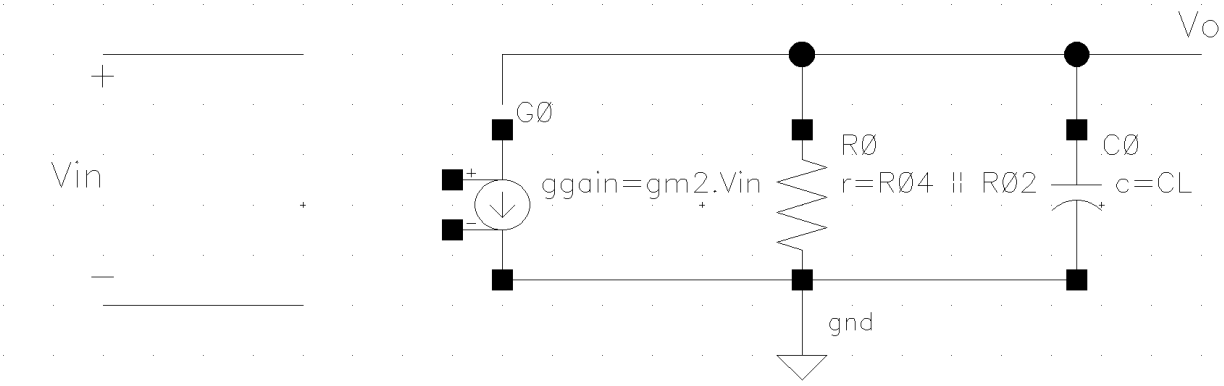


Figure 3: Small signal model of Differential amplifier

Applying KCL,

$$\frac{V_0}{R_{04}||R_{02}} + \frac{V_0}{\frac{1}{sC_2}} + g_m V_{in} = 0 \tag{10}$$

$$\frac{V_0}{V_{in}} = \frac{-g_m(r_{02}||r_{04})}{1 + sC_2(r_{02}||r_{04})} \tag{11}$$

Thus, from the transfer function we can tell it is a single pole system.

Where,

$$DC\ gain = \ g_{m2}(r_{02}||r_{04}) \tag{12}$$

$$First\ Pole(P_1) = \frac{1}{(r_{02}||r_{04})C_L} \tag{13}$$

So,

$$GBW = DC\ gain \times First\ Pole \tag{14}$$