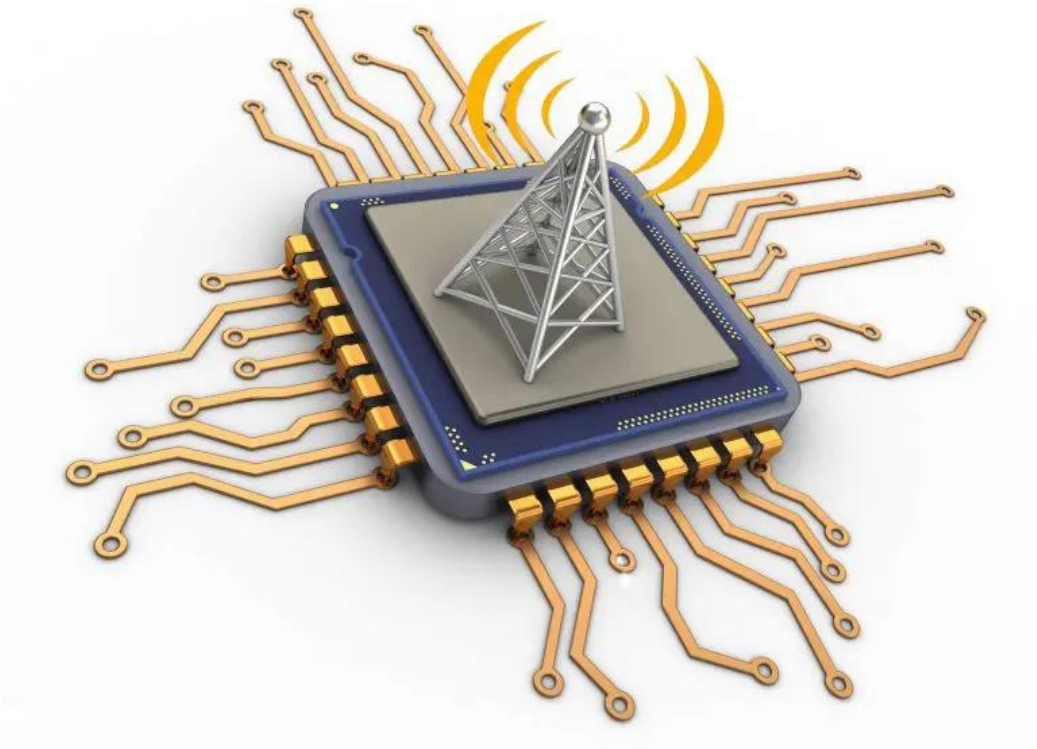
# COOK-BOOK OF NARROWBAND LNA




## Report Presented by:

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## 1. CS Stage with Inductive Degeneration:

In the pursuit to find best design topology for LNA, we have concluded Inductive degeneration LNA to be our strategy in week 5 report.

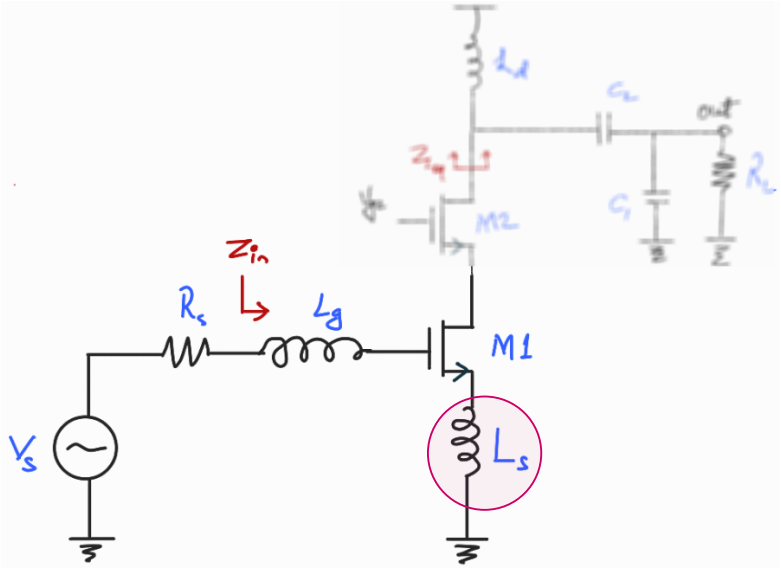



**Figure 1:** CS Amplifier with Inductive Degeneration as LNA

Till now we have just made a Low noise Trans-conductor i.e., we have converted the voltage to the current but the gain of the device shown in Figure 1, doesn't come up to the mark of our LNA requirement.

## 2. Complete LNA: Cascode Topology:

For contentment of gain requirement, we can have multiple transistors in Cascode Topology.

Why Cascode?

- Reduces Miller effect on $M_1$. (Miller effect in MOSFET accounts for an increase in input Capacitance i.e., $C_{gs}$ caused by the gain of the amplifier)
- Provides good reverse isolation. ($S_{12}$ is low)

- Amplifier is <u>unilateral</u> (signal only flows from input to output)
- Allows the input match to be independent of the output match.

Our strategy is to, have a cascode device on the drain of $M_1$ , put a load at the drain of $M_2$ which will be matched to have a maximum power transferred.

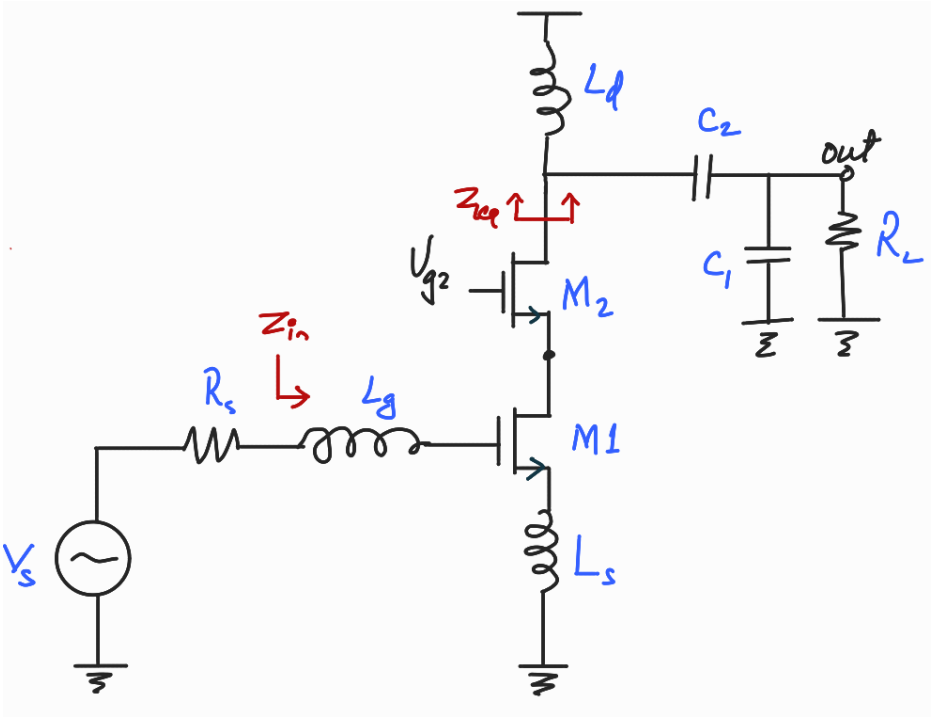


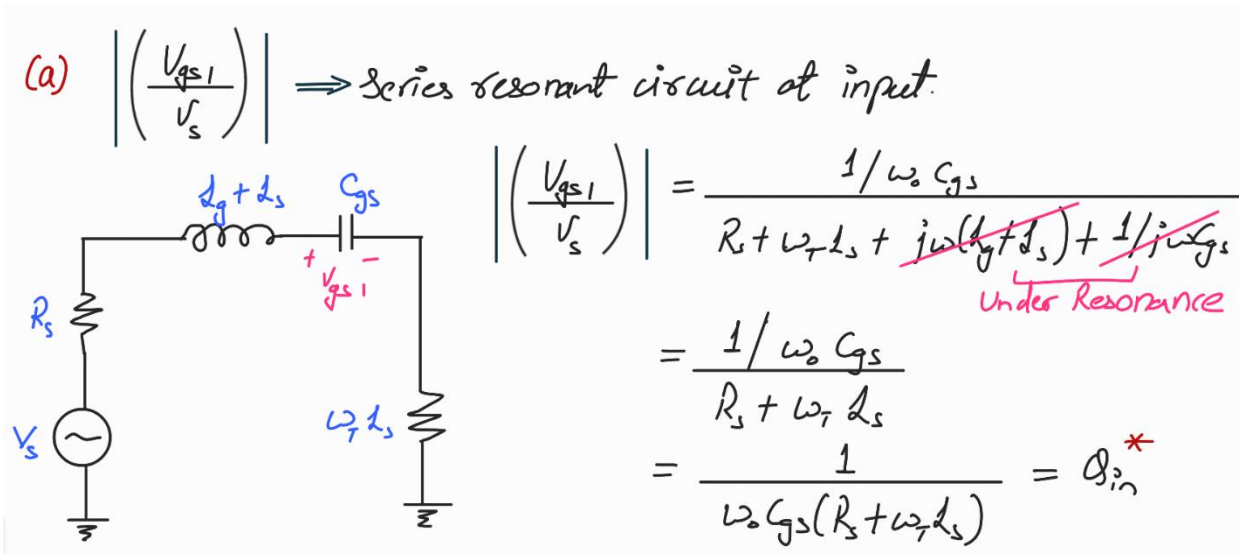

**Figure 2:** A Complete LNA: Cascode Topology

## 3. Gain Analysis of Cascode LNA:

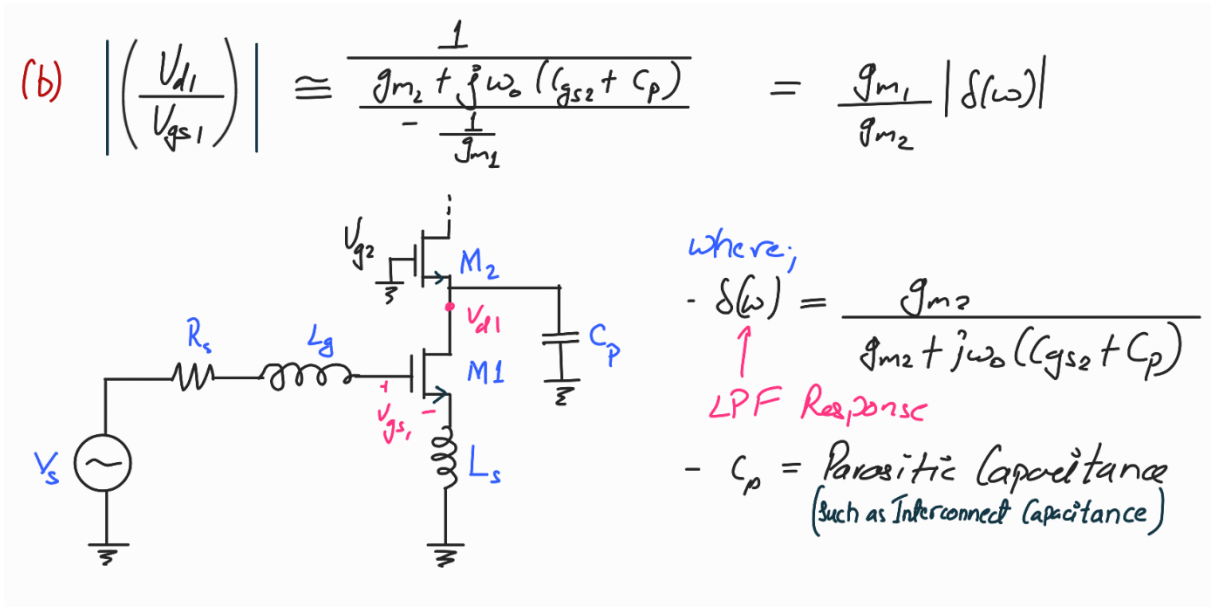
Let's divide gain analysis in stages, for easier computation of total gain.

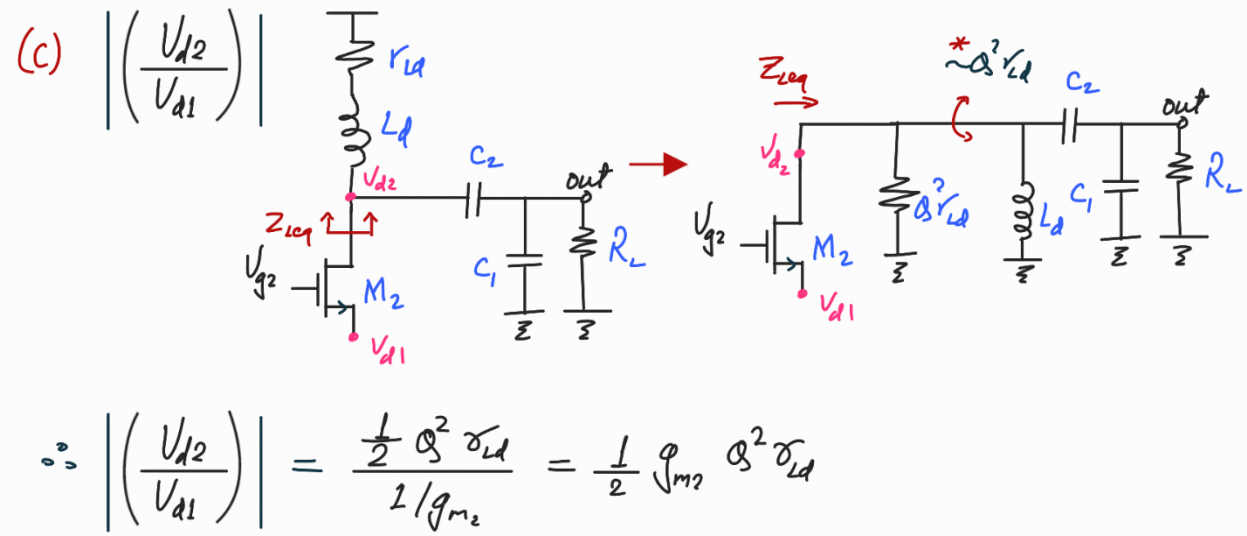
$$|A_v| = \left|\left(\frac{V_{gs1}}{V_s}\right)\left(\frac{V_{d1}}{V_{gs1}}\right)\left(\frac{V_{d2}}{V_{d1}}\right)\left(\frac{V_{out}}{V_{d2}}\right)\right|$$

(a) (b) (c) (d)



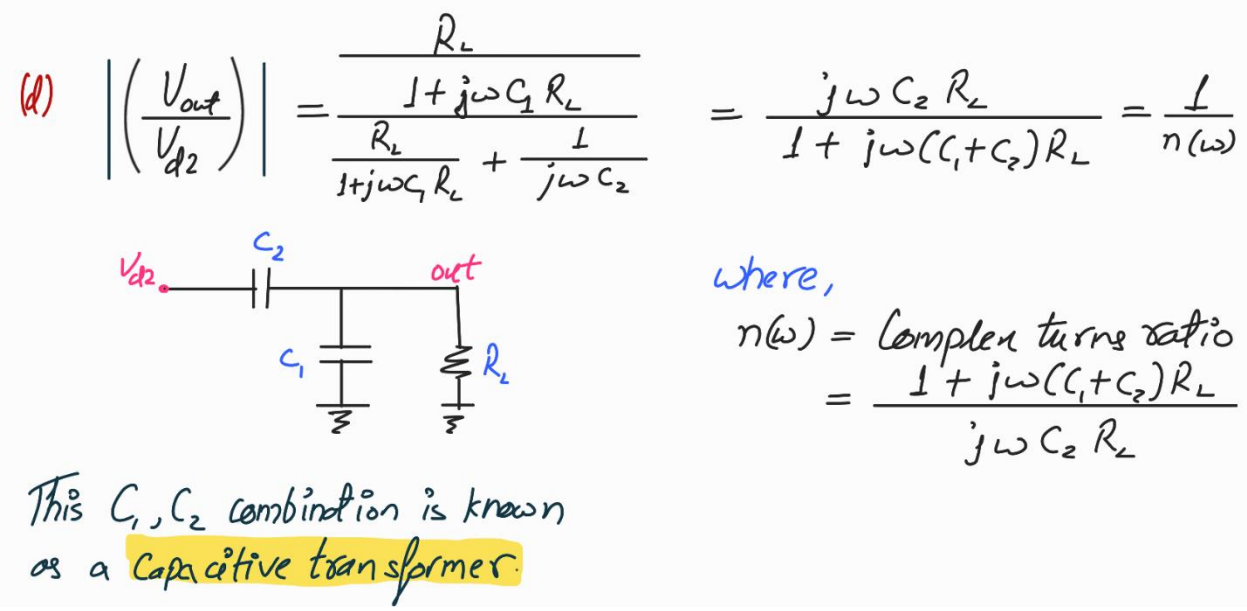

*$Q_{in}$ of input resonance circuit tends to give us voltage amplification. And it sounds like a free gain but it comes with a cost of Bandwidth. But if narrowband is needed we get nice gain characteristics for sure.






Where, $r_{Ld}$ is a parasitic resistance of a practical indictor $L_d$.

*After series parallel conversion (ref week8) of $r_{Ld}$ to $Q^2 r_{Ld}$ comparatively it is very small so it become dominant. So, we will match the Load resistance $R_L$ with $Q^2 r_{Ld}$ which makes $Z_{Leq} = 0.5 * Q^2 r_{Ld}$




Wont the $C_1$ of capacitive transformer drain all the RF signal to ground?

= No, because $n(\omega) \to 1 + \frac{C_1}{C_2}$ when, $\omega \to \infty$ So the capacitive transformer is actually Independent of frequency.

## Final Gain Expression

Substituting the previous four expressions.

$$|A_v| = (Q_{in})\left(\frac{g_{m1}}{g_{m2}}|\delta(\omega)|\right)\left(\frac{1}{2}g_{m2}Q_{Ld}^2\gamma_{Ld}\right)\left(\frac{1}{|n(\omega)|}\right)$$

$$= \frac{1}{2}Q_{in}g_{m1}Q_{Ld}^2\gamma_{Ld}\left|\frac{\delta(\omega)}{n(\omega)}\right|$$

Substituting $Q_{in}$ & $Q^2\gamma = Q\omega_0 L_d$ & $\omega_T = \frac{g_m}{C_{gs}}$

$$\boxed{|A_v| = \frac{1}{2}\left(\frac{\omega_T Q_{Ld} L_d}{R_s + \omega_T L_s}\right)\left|\frac{\delta(\omega)}{n(\omega)}\right|}$$

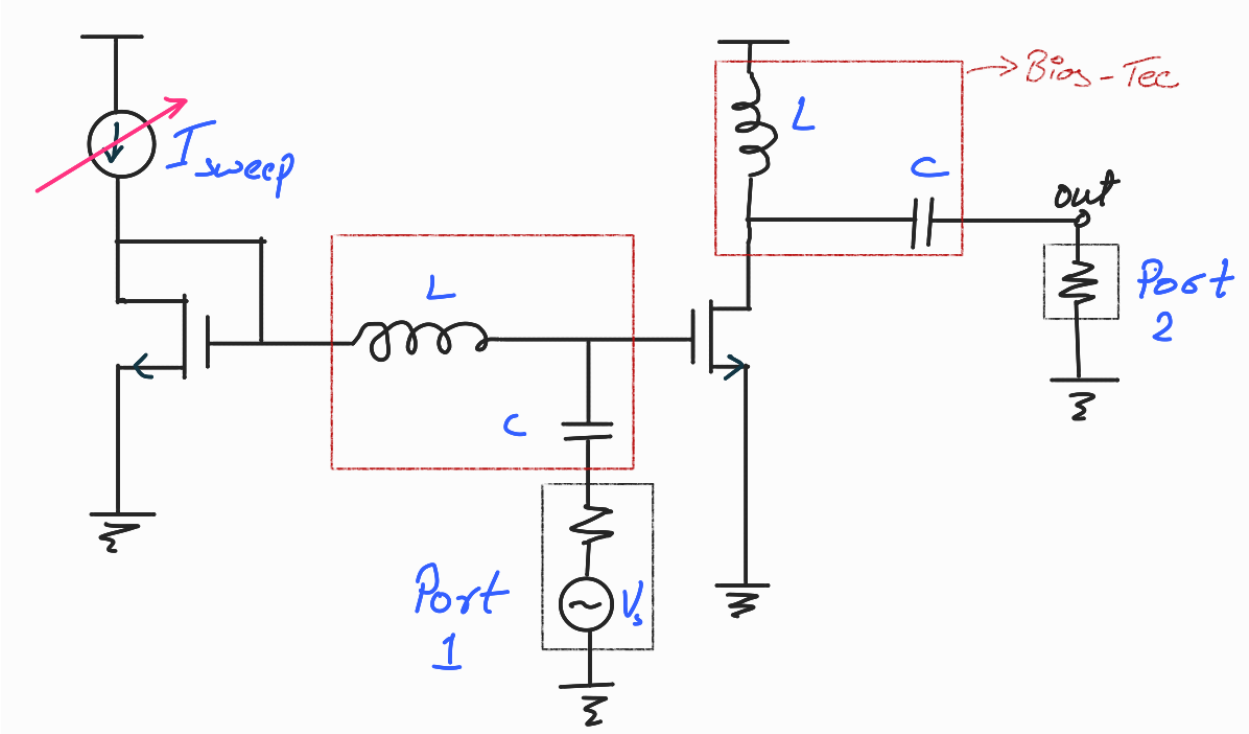
**Ways to maximize Gain:**

- Maximize $\omega_T$
  - We can make $\omega_T$ larger by making device larger which improves $g_{m1}$ but $Q_{in}$ is going to degrade because $C_{gs}$ will also increase.
  - So, we will keep the size same but increase the current with biasing then $Q_{in}$ remains the same but $g_m$ goes up so does $\omega_T$
- Maximize inductor quality factor ($Q_{Ld}$)
- Maximize $L_d$
- Maximize $\delta(\omega)$, meaning resonate out $C_p$
- Trade-off $S_{11}$ for increased $S_{21}$ i.e., reduce value of $L_s$
  - The purpose of source degenerated inductor $L_s$ is to match with 50Ω which will give me great $S_{11}$ but as a last resort we can decrease $L_s$ as a trade-off between $S_{21}$ and $S_{11}$

## 4. Cookbook of Unilateral (Cascode) Source-Degenerated LNA:

This procedure is for Narrow-Band LNA's.

1. Create current mirror circuit with bias-T's and sweep bias to find optimum current for $NF_{min}$



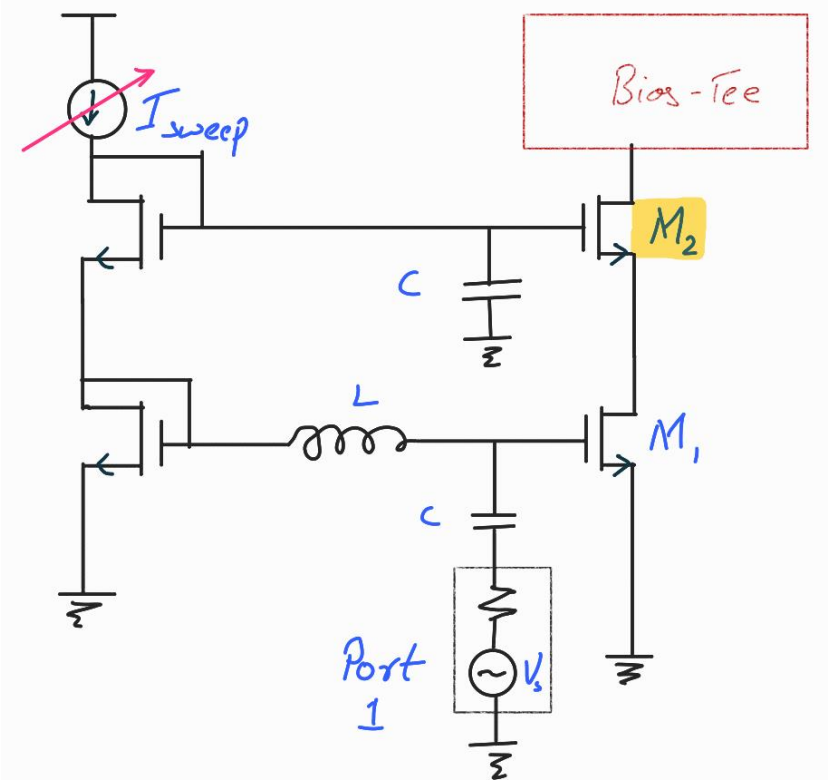

Where, L and C will be kept as 1H and 1F respectively.

- Bias-Tee is there to block RF with inductor and block DC with capacitor.

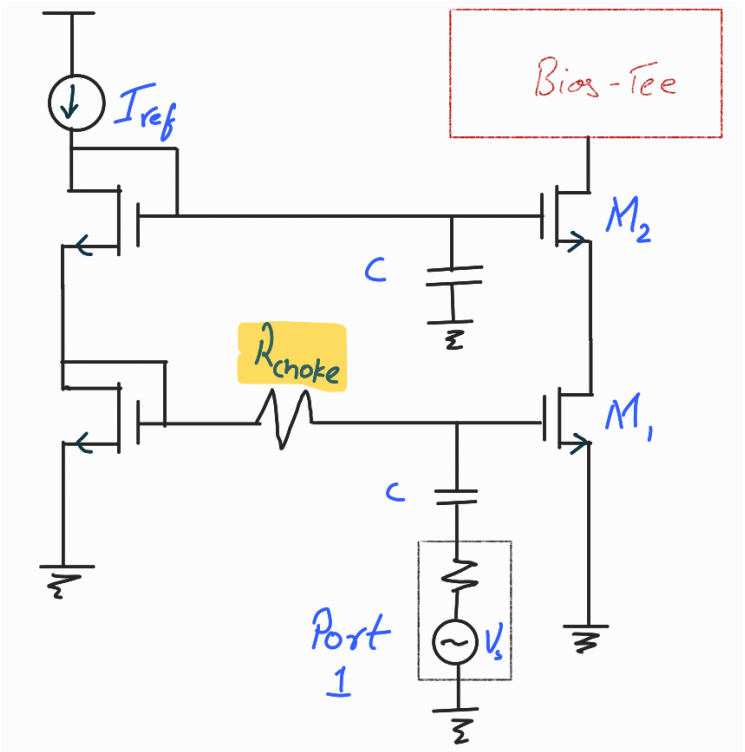
- Now simulate single finger FET and sweep bias current to find optimum current density range for minimum noise i.e., plot $NF_{min}$ vs $I_{ref}$

2. Add cascode($M_2$)

   - Add cascode device($M_2$) nominally of same size as $M_1$. You can alter the size for better performance later. We could have gone for cascode in 1st step only but now we can know how much noise is cascode presenting and repeat the same

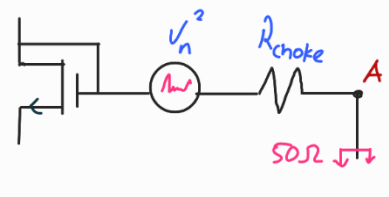



3. Update bias network (use resistive choke rather than $L_{big}$ in I/P only)



- Finalize bias network design, nominally a cascode current mirror coupled to $M_1$ through a moderate-value resistor (~5 kΩ).

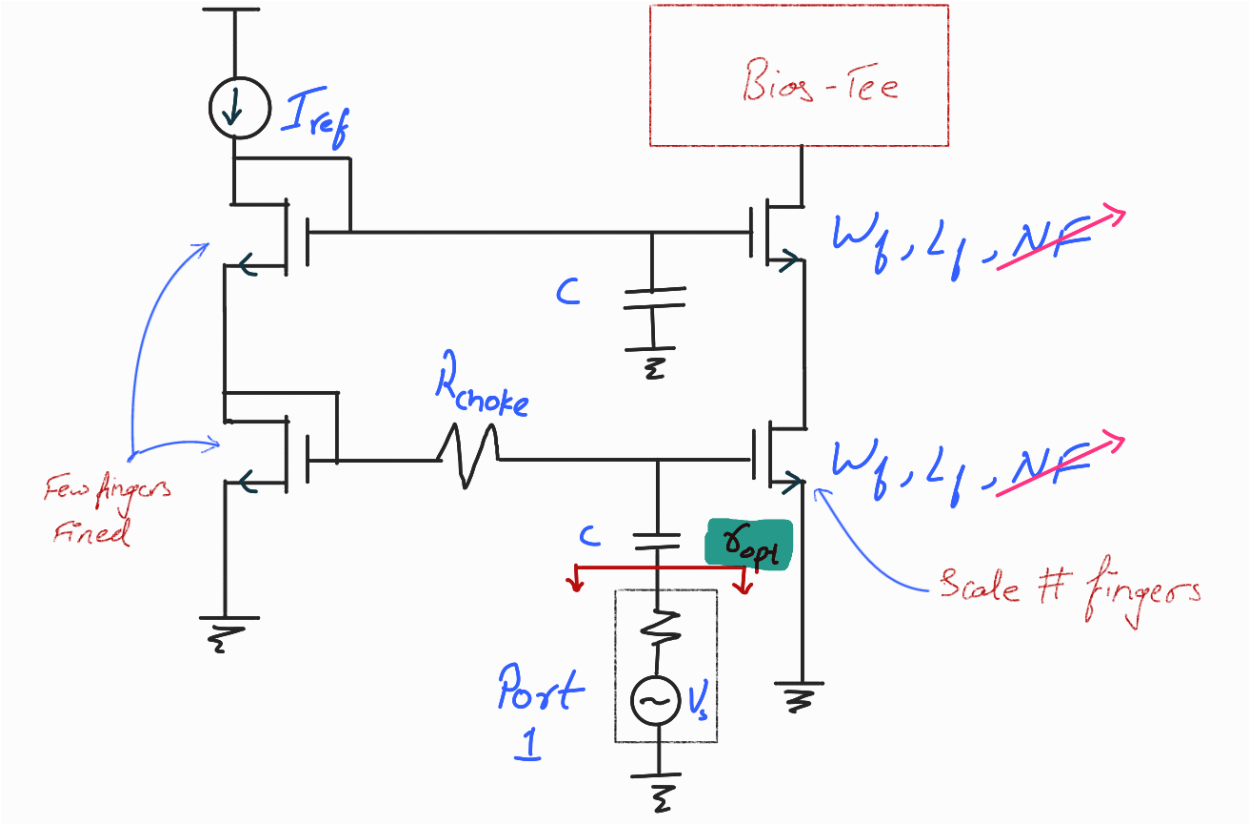
Wait won't this resistor ($R_{choke}$) create a noise?

= Yes, It will 

And is very less as $V_A=\frac{V_n^2\times 50}{5K+50}$

But if you decrease the size of $R_{choke}$ the noise factor will increase.

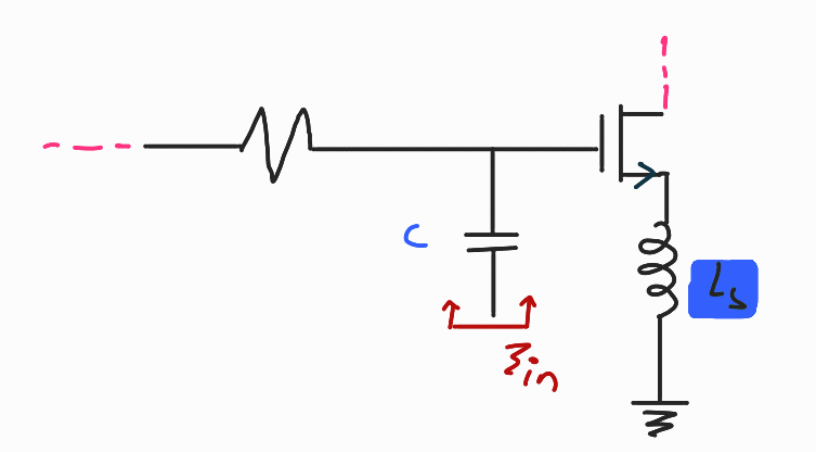
## 4. Scale size to get $R_{opt}$ (Noise Match)




- Scale the number of fingers until $R_{opt}$ (optimum noise resistance) is close to 50 Ω. The cascoded transistor $M_2$ is kept as same size as $M_1$

- Plot fingers vs $R_{opt}$ plot to find the optimum value for fingers

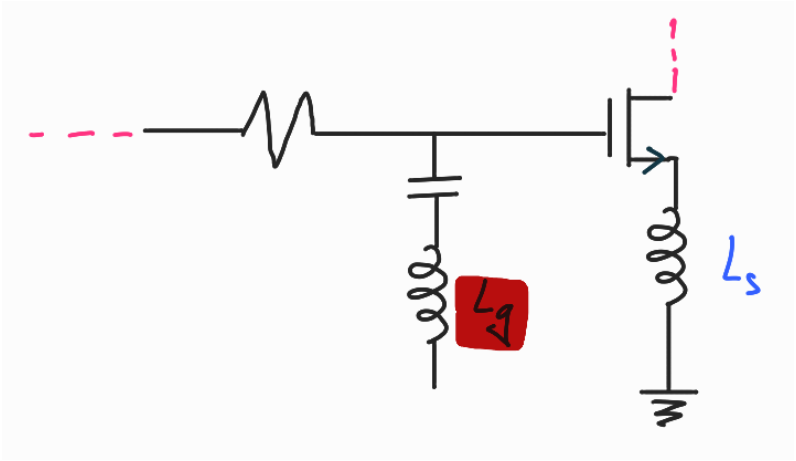
## 5. Add $L_s$ to generate real $Z_{in}$ (Power match)

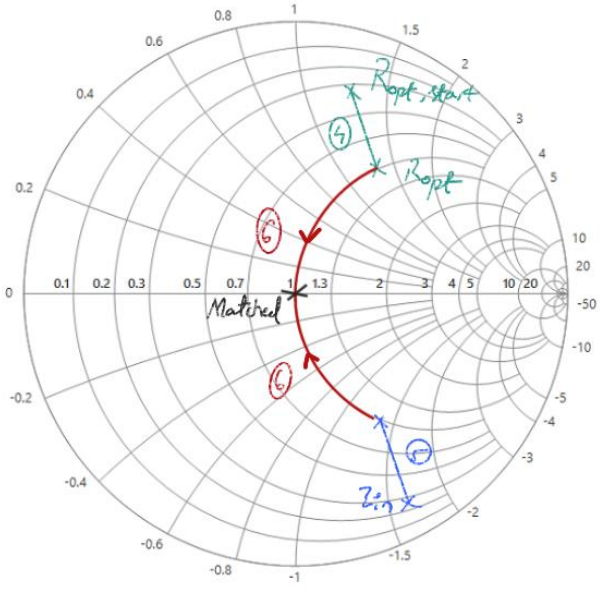



- Add degeneration inductor ($L_s$) to provide real input impedance close to 50 Ω. Degeneration can be either on-chip spiral or bond wire.

- This step gives me optimum power match i.e., Re [$Z_{in}$]=50 Ω

## 6. Add $L_g$ to complete input match




- So, step 4 will bring $R_{opt}$ to constant 50Ω circle and step 5 will bring Re [$Z_{in}$] to constant 50Ω circle.

- And finally step 6 will bring both $R_{opt}$ and Re [$Z_{in}$] to matched condition.

7. Design $L_d$ spiral inductor. Add parasitic resistor
8. Simulate output impedance $Z_{out}$ and design output matching network ($C_1$ and $C_2$).
9. Simulate $IIP_3$ and $P_{1dB}$ and compare with requirement, increase bias current as required.
10. Simulate all specifications over process, voltage, temperature (PVT)

    - Note that the PVT simulations can/should be embedded with each step to ensure all along that the design is sufficient. This can be achieved with parametric simulation.