DE-10 Standard Altera

-Setup

-Download and Quartus Prime II 2023.1 from Intel website

- https://www.intel.com/content/www/us/en/software-kit/795126/intel-quartus-prime-standard-edition-design-software-version-23-1-for-linux.html

User manual

https://ftp.intel.com/Public/Pub/fpgaup/pub/Intel_Material/Boards/DE10-Standard/DE10_Standard_User_Manual.pdf

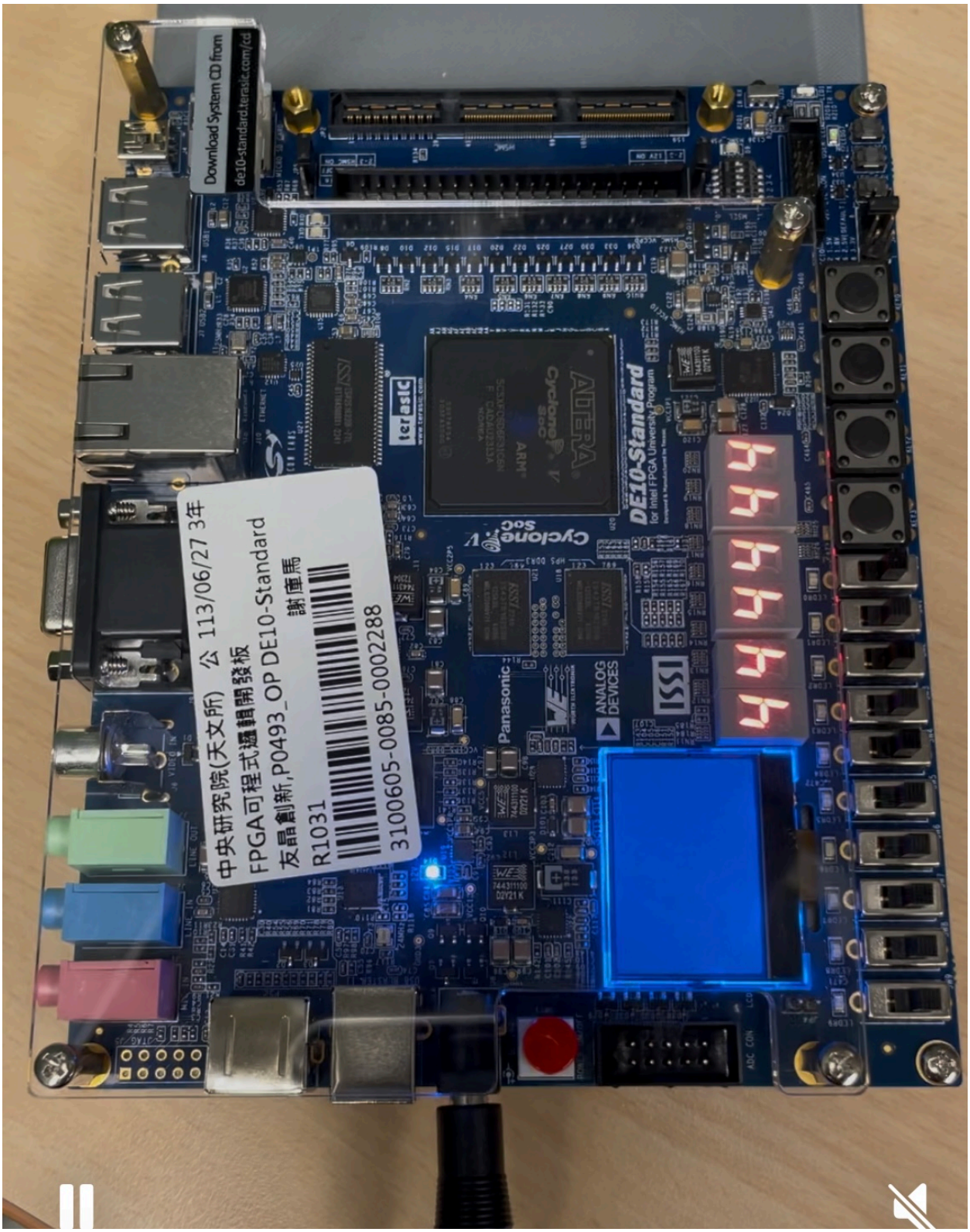
Power On

- Connect the 12v power cable to the power source (Blue color D14 LED glow]
- Connect UART cable to USB port of your system computer
- Set up Dip switch MSEL[4:0] to 10010

Note: There are 6 dip switch. 6th switch doesn’t matter. 5th switch (written 4 in board) is 1 and 0, 0, 1, and last swithc means switch 0 is 0.

- If you count from switch 0 to 5 (written on the board), the configuration is 01001.

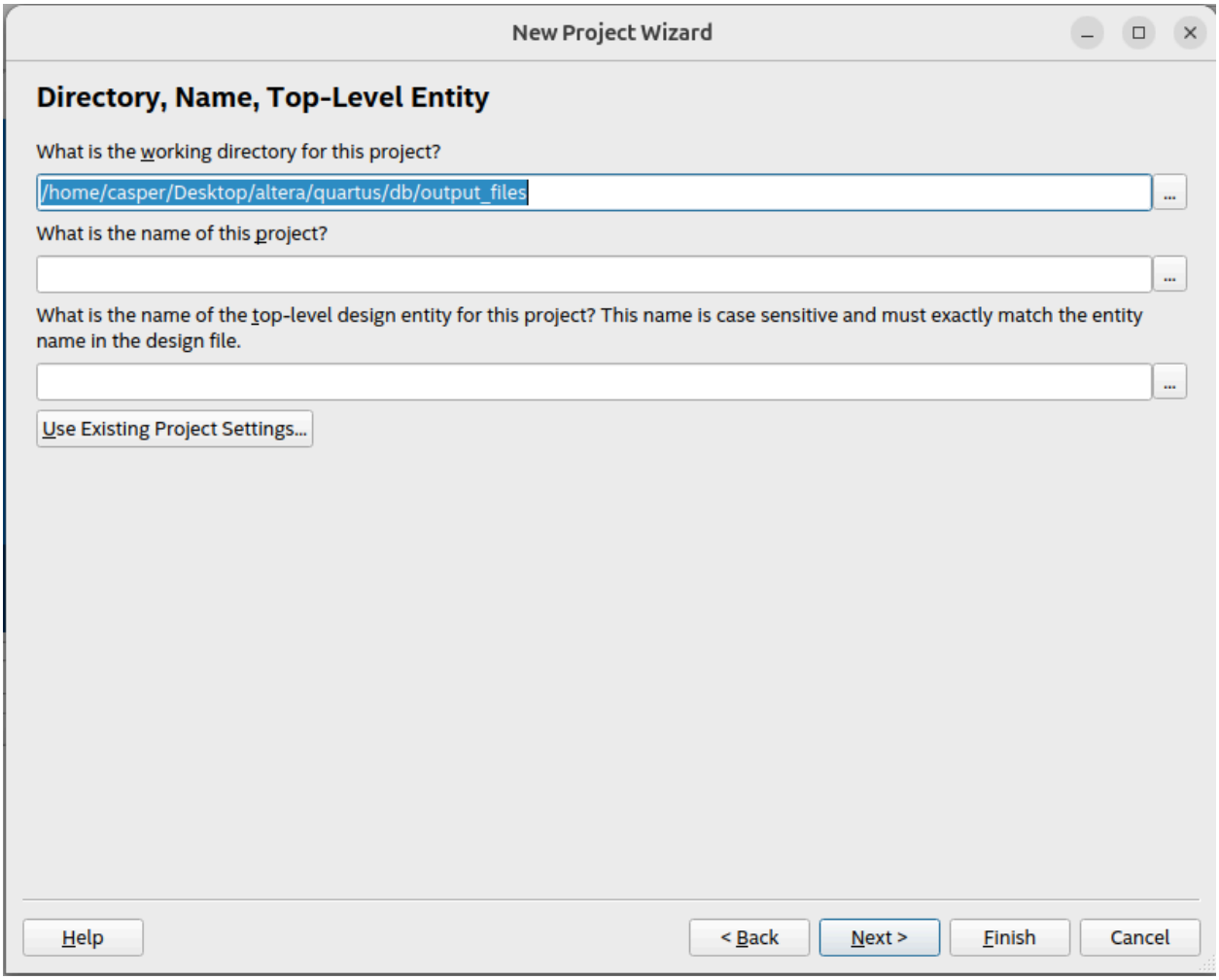
Turn on the FPGA, you will see continuously blinking LEDs and white LED. Still the big blue LED is glown but nothing displays.

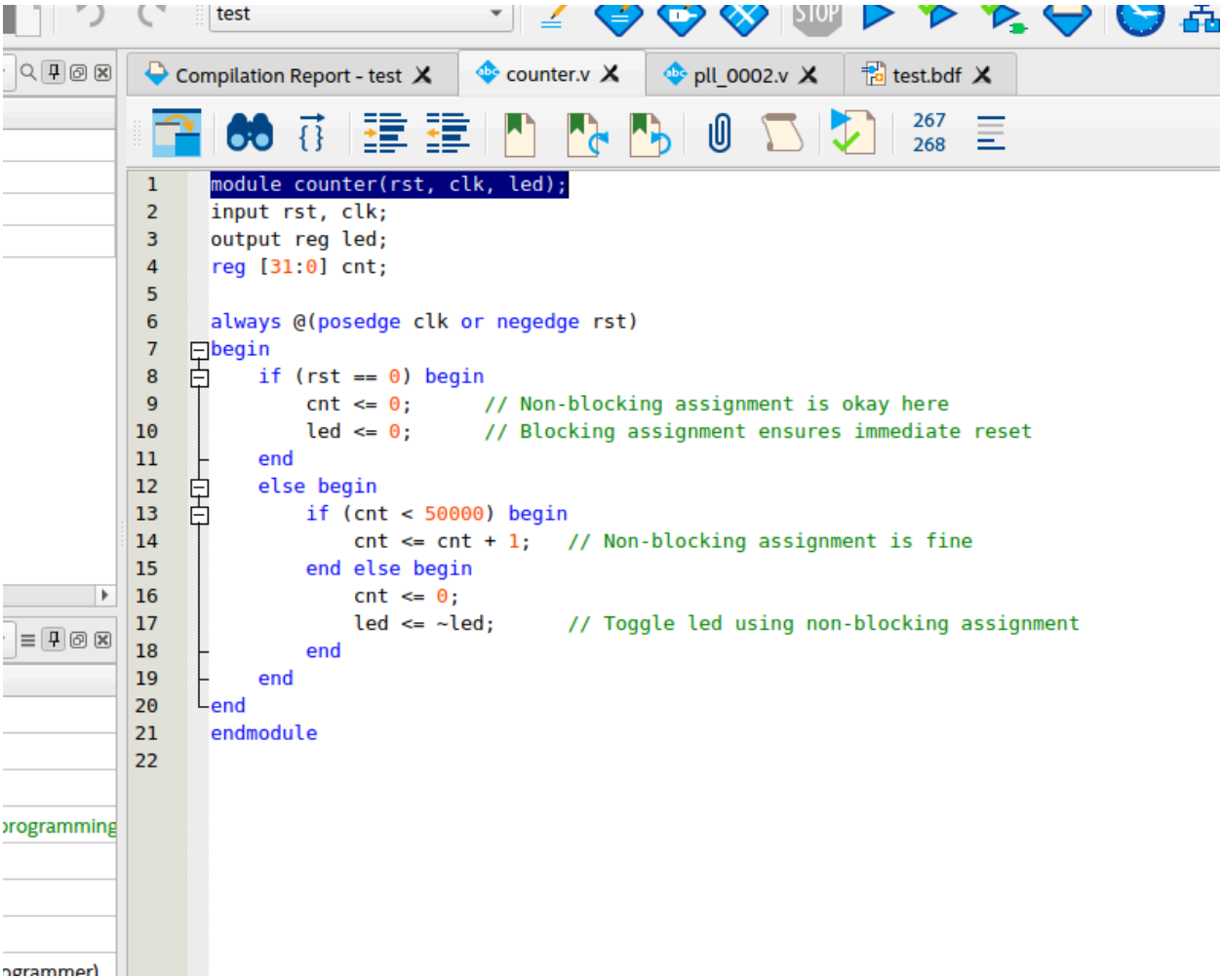

Download System CD from
de10-standard.terasic.com/cd
中央研究院(天文所) 公 113/06/27 3年
FPGA可程式邏輯開發板
友晶創新,P0493_OP DE10-Standard
謝庫馬
R1031
3100605-0085-0002288
DE10-Standard
for Intel FPGA University Program
Cyclone V SoC
ALTERA
ARM
terasIC
Panasonic
ANALOG DEVICES
ISSI

Quartus prime Standard II 23.1

After downloading and installing Quartus, let's check a simple LED blink using Verilog

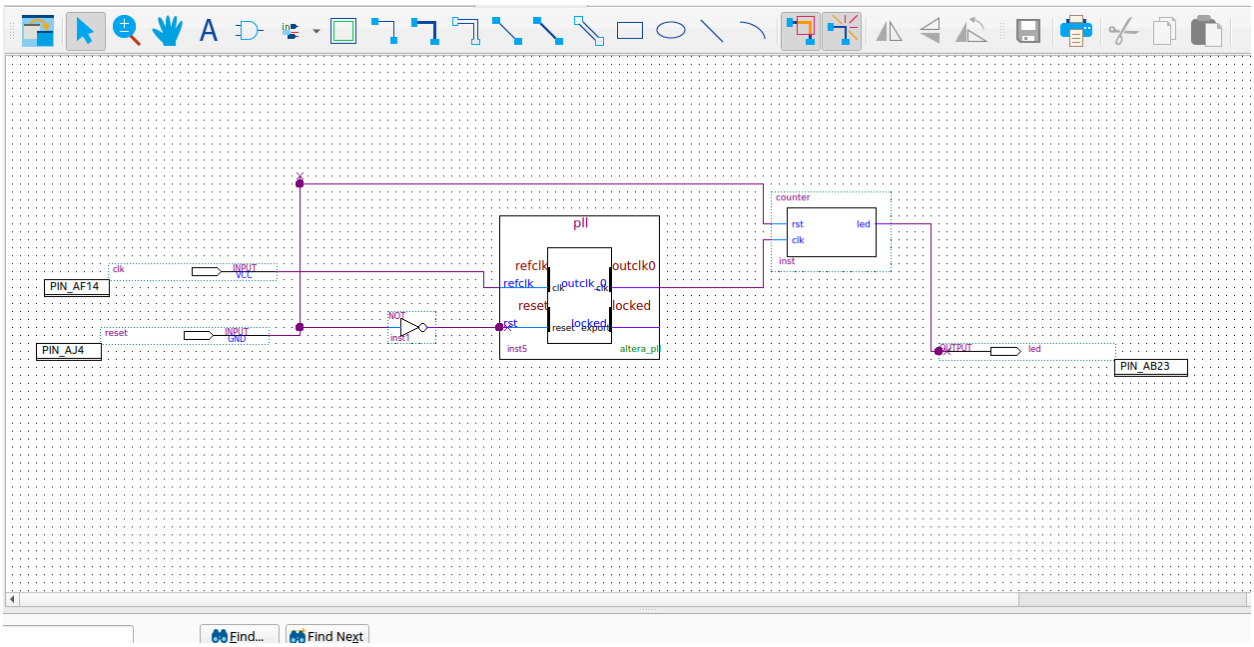
- Open Quartus Prime and make a simple Verilog file example: counter.v



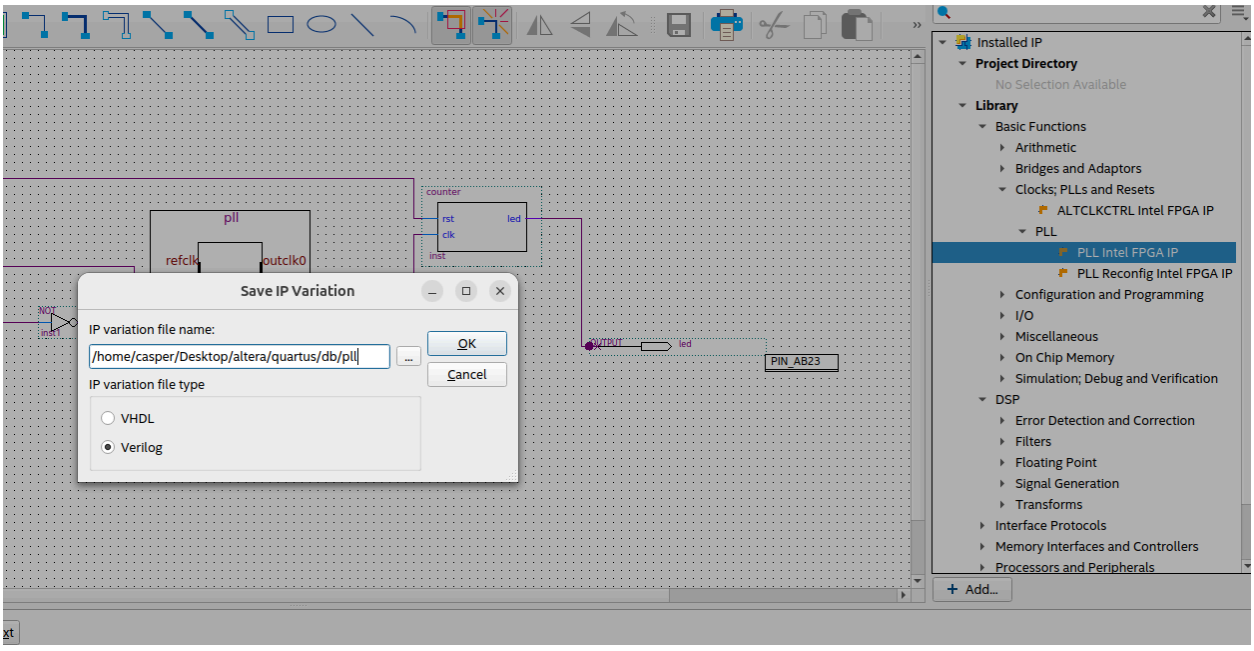


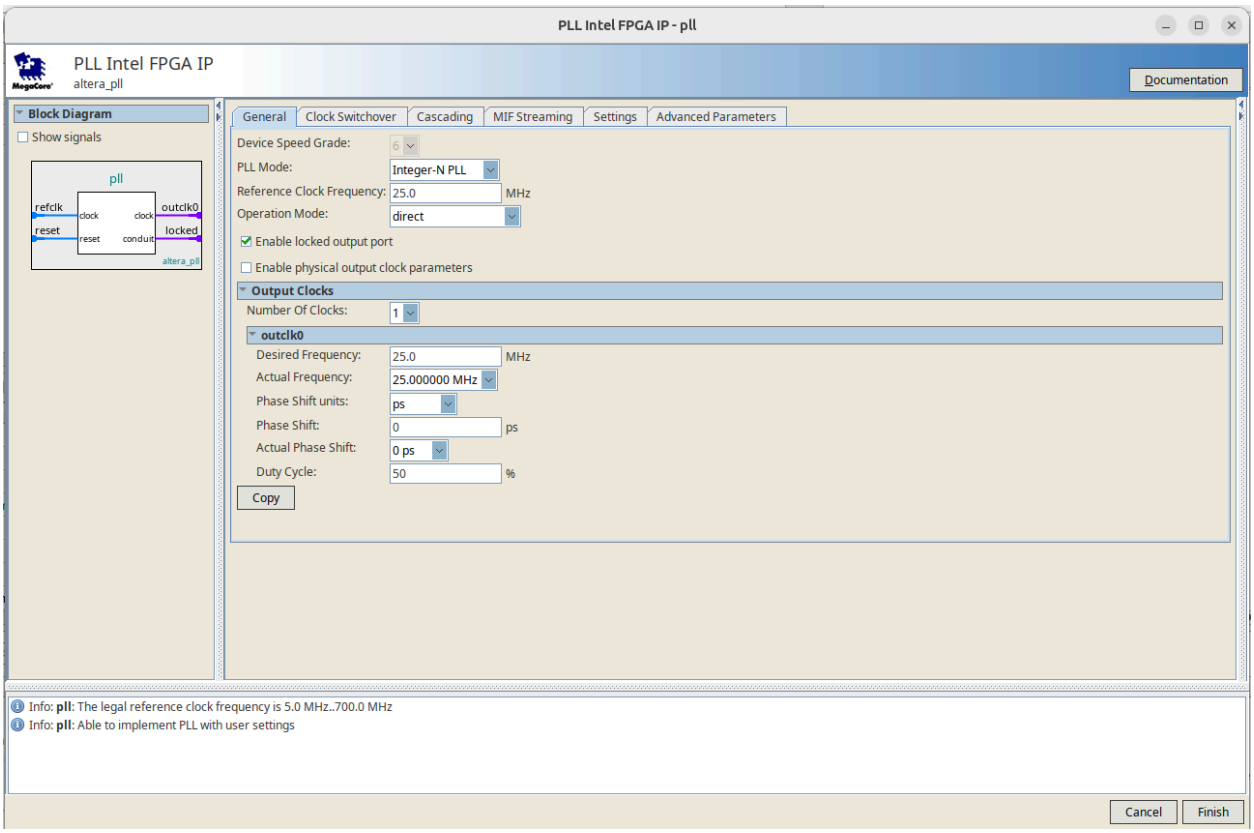
After writing the code, we have to create the symbol of the code.

- After successfully compile and run
- Click the (.vhd/.v) file and click create/update, and then select Create symbol files for current files. Quartus will give you successfully create symbol file.
- Click File, go to New, in Design file, click Block Diagram/Schematic file
- Create a diagram and double-click the screen to bring it back to the GUI interface



- On the top right corner, Library, There is Clk, PLLs and resets, click PLL. We have to design PLL for this diagram.





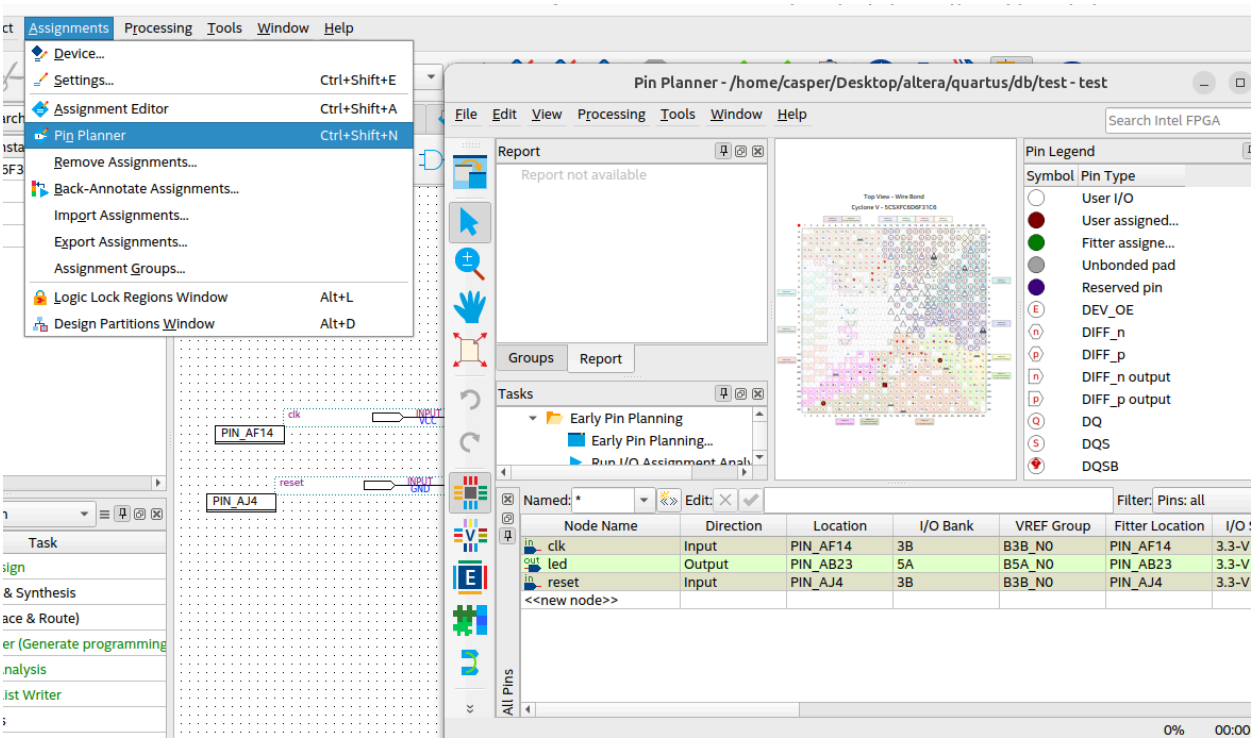
- Click finish and bring it to the GUI by clicking twice in the screen.

In Verilog, we have three ports defined. Two inputs rst, clk, and one output led. Next phase is to connect them and PIN them in the chips.

PINNING CHIP

- We use a chip planner to pin them.

In the Assignment section, there is the Pin Planner. We have to pin the chip from where it will input the signal and from where it will output the signal to blink or glow LEDs.



Input clk is taking input pin AF14, led is output, assigned AB23 (2nd led) and reset is AJ4

Figure 3.17 Connections between the LEDs and the Cyclone V SoC FPGA

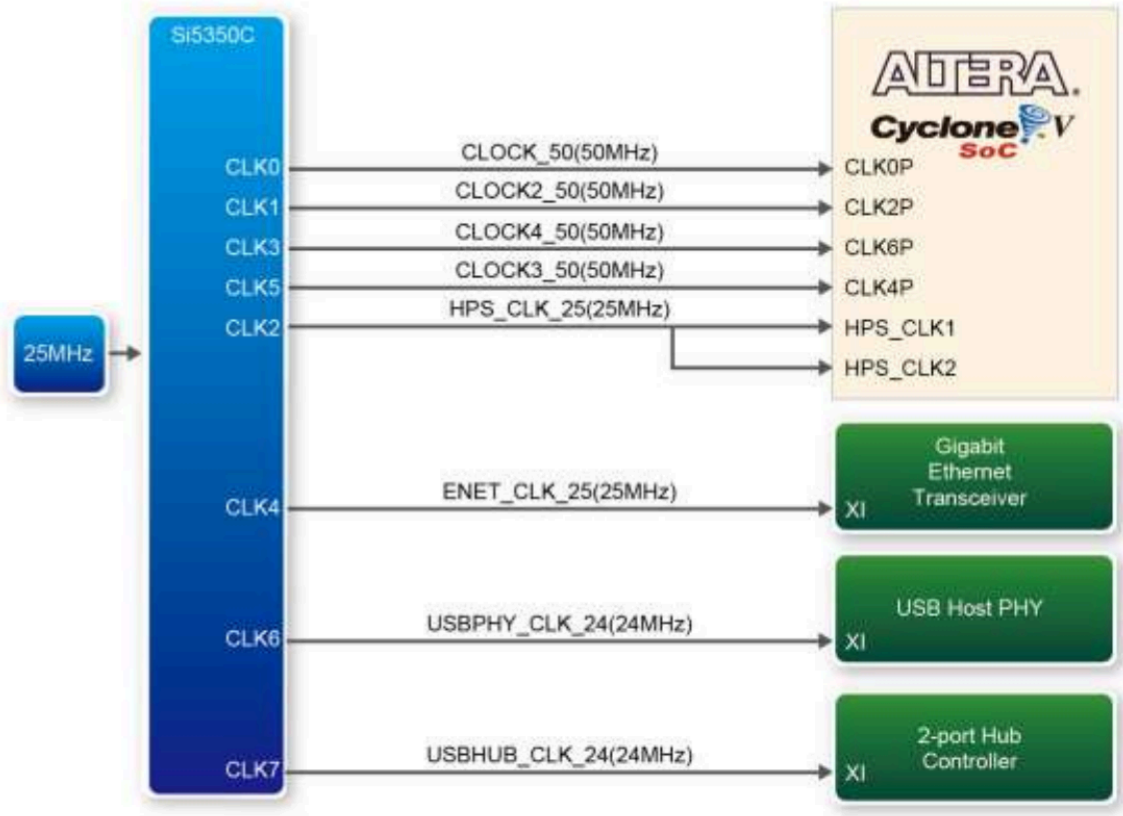


Figure 3-13 Block diagram of the clock distribution on DE10-Standard

Table 3-5 Pin Assignment of Clock Inputs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
CLOCK_50	**PIN_AF14**	**50 MHz clock input**	**3.3V**
CLOCK2_50	**PIN_AA16**	**50 MHz clock input**	**3.3V**
CLOCK3_50	**PIN_Y26**	**50 MHz clock input**	**3.3V**
CLOCK4_50	**PIN_K14**	**50 MHz clock input**	**3.3V**
HPS_CLOCK1_25	**PIN_D25**	**25 MHz clock input**	**3.3V**
HPS_CLOCK2_25	**PIN_F25**	**25 MHz clock input**	**3.3V**

ClOCK_50 is connected to pin AF14

circuit.

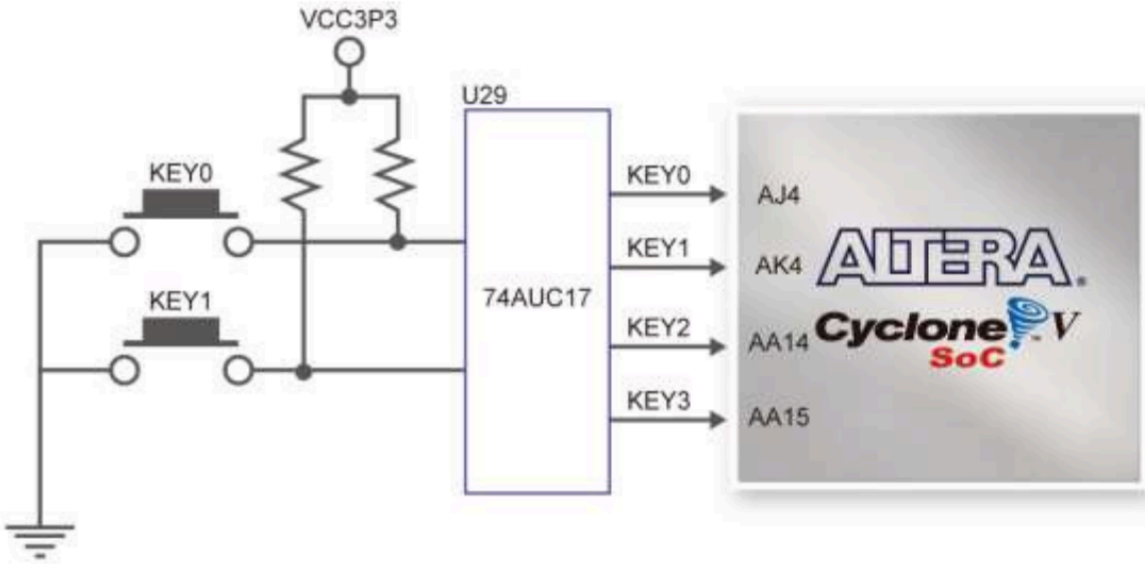
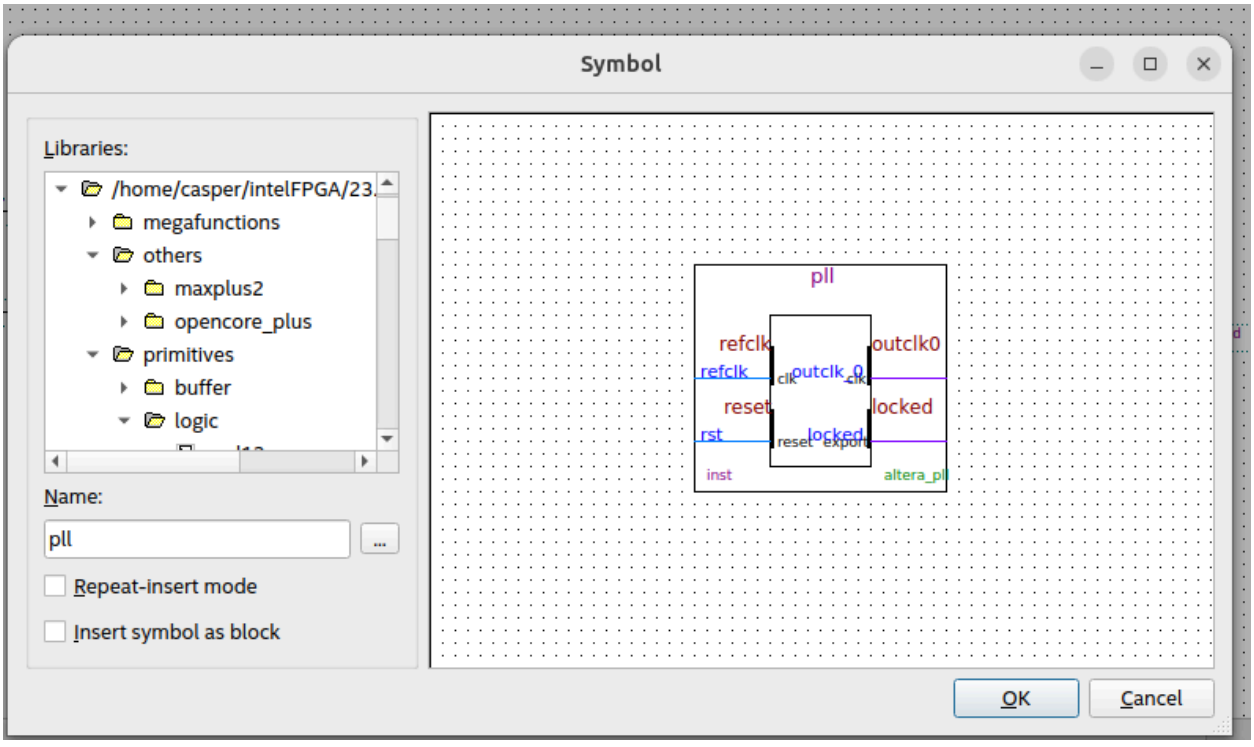


Figure 3-14 Connections between the push-buttons and the Cyclone V SoC FPGA

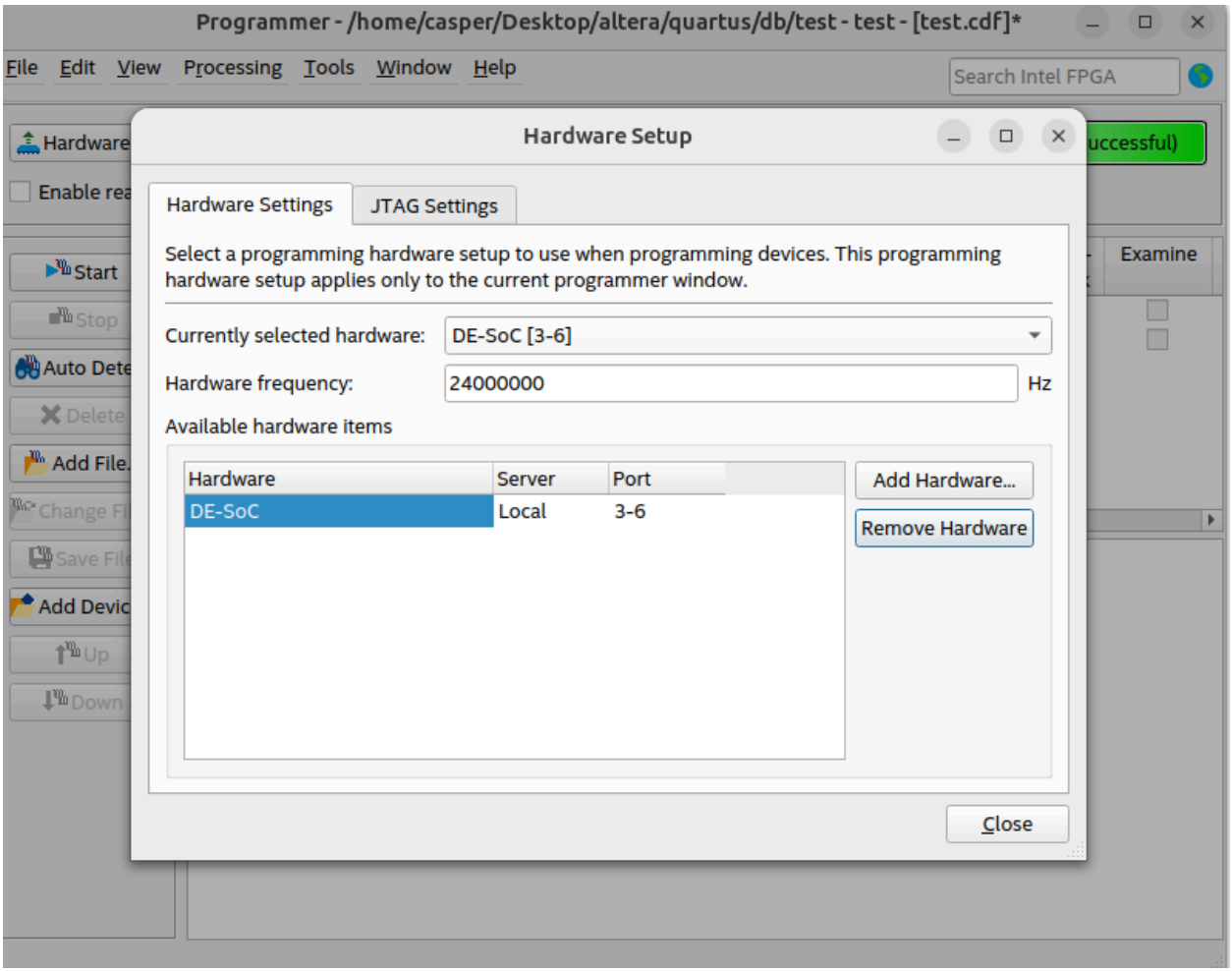
Push buttons are connected to AJ4 and they are low enable and grounded. So we have to negate reset.

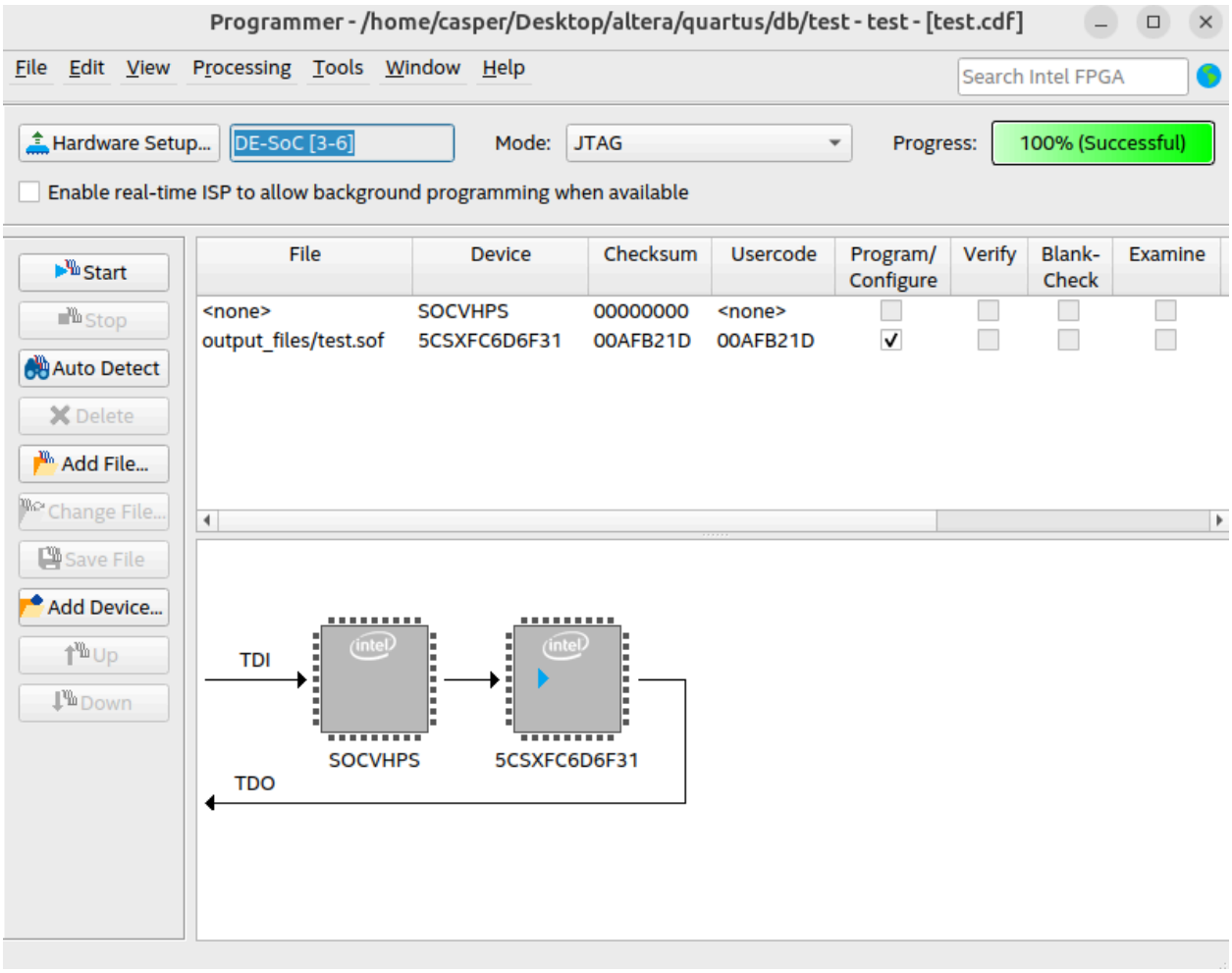


From primitive download not gate.

- similarly from logic and pins download two inputs and one output.
- Reset is set GND and CLK is set VCC

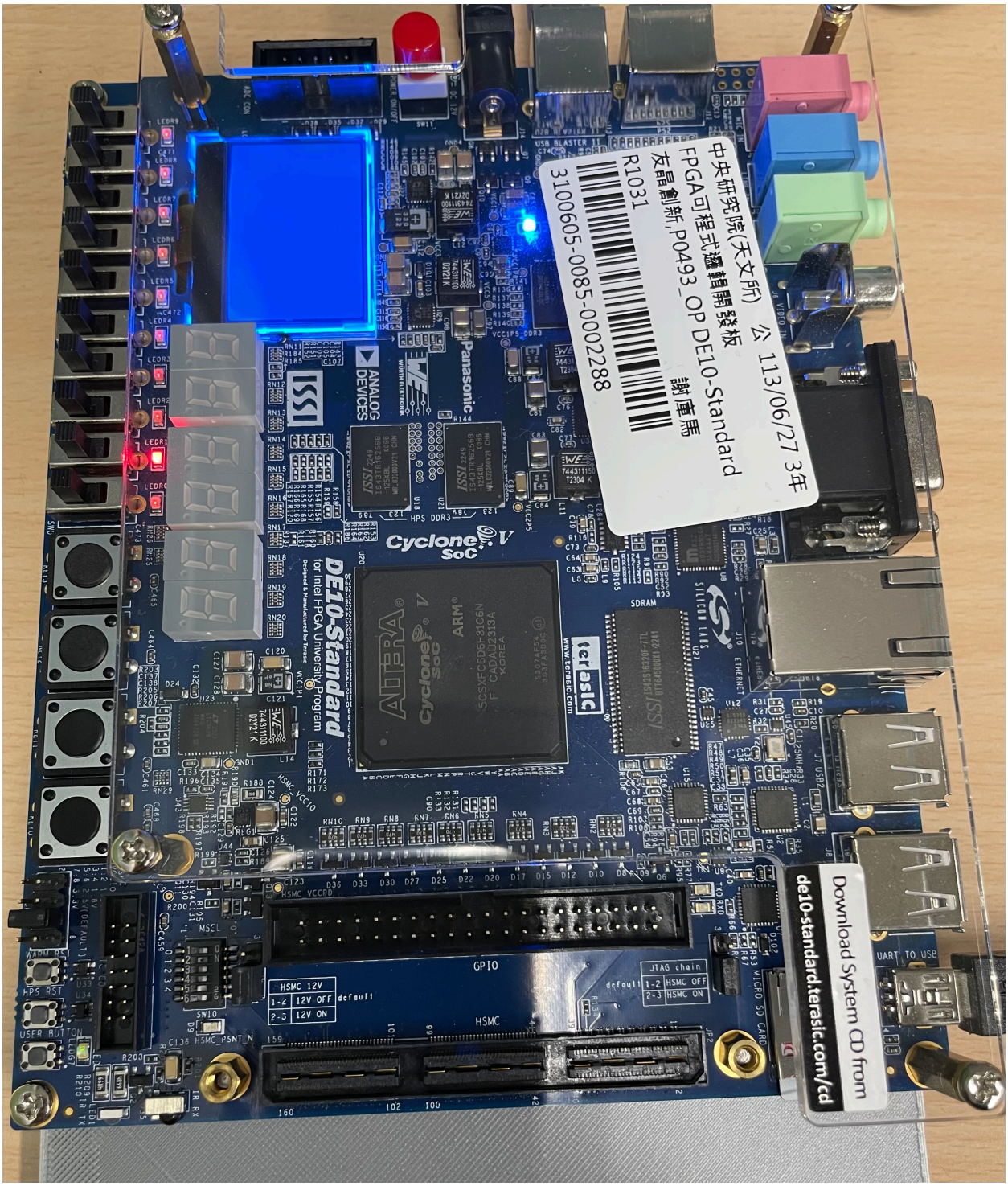
Go to hardware setup and check your device





select the connection and file name. Select the device name cyclon v and 5CSXFC6D6F31 and press start.

Then you will see second LED (LEDR1)on DE-10 standard blinking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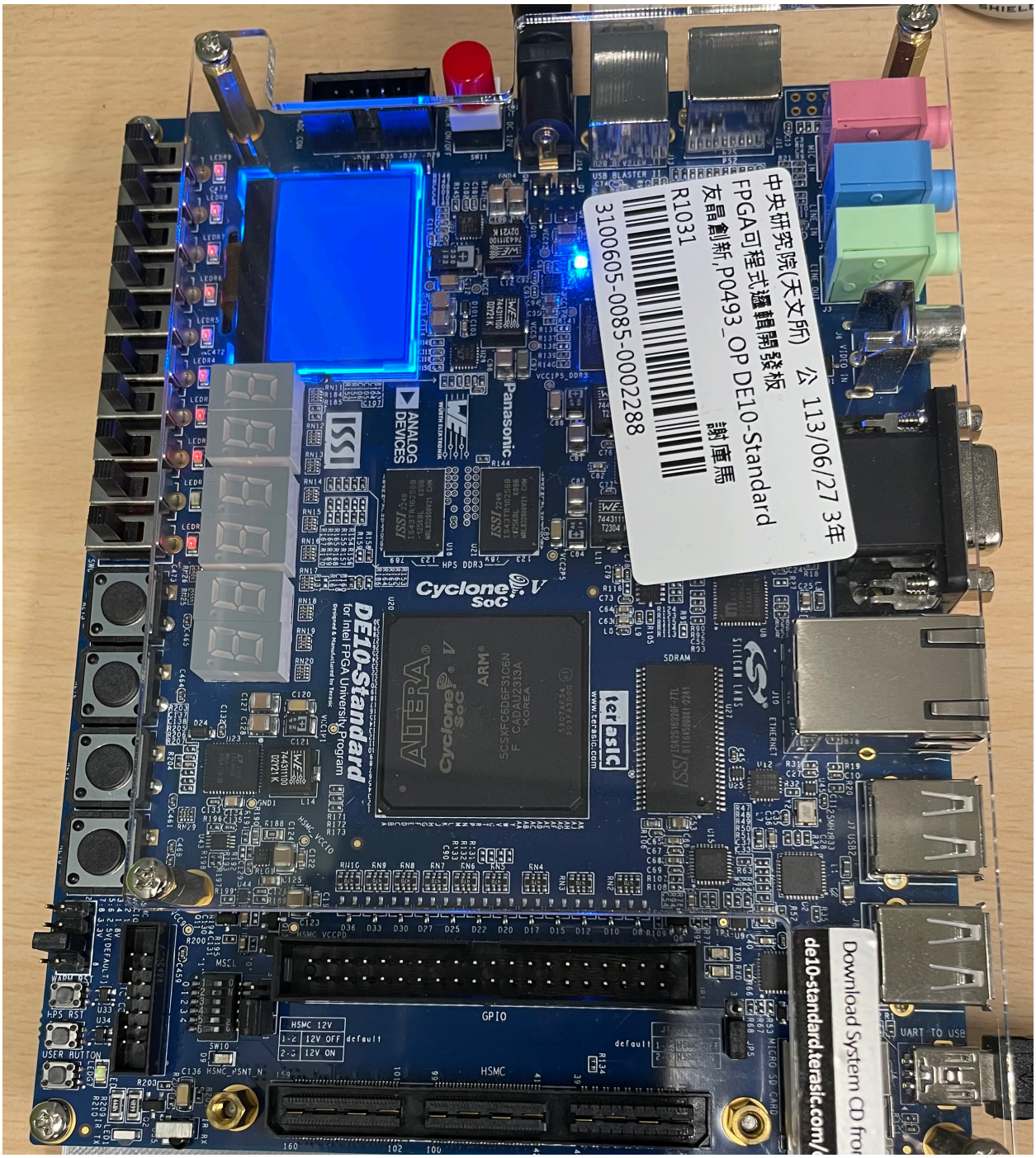
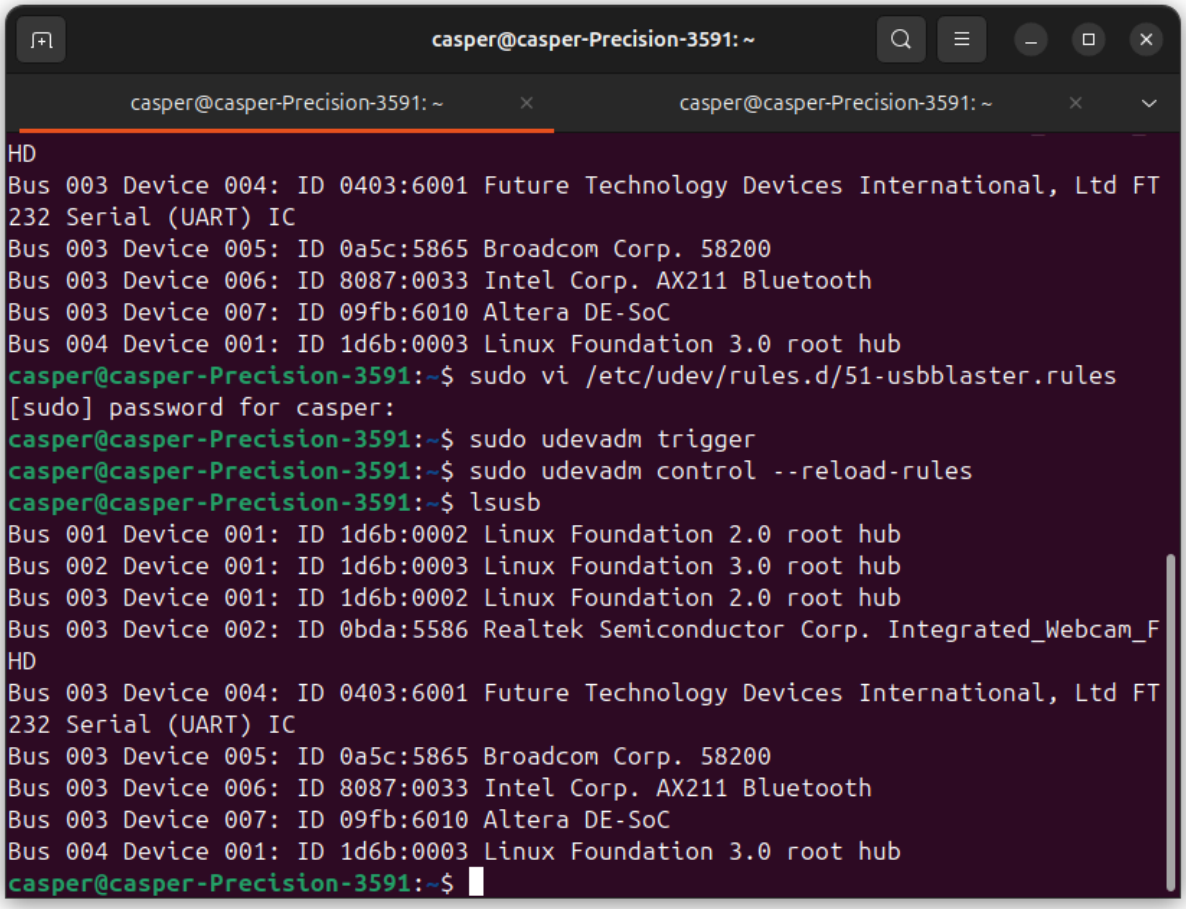


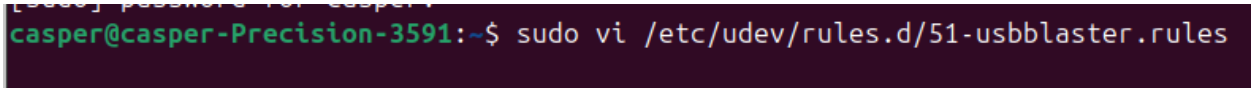
Note

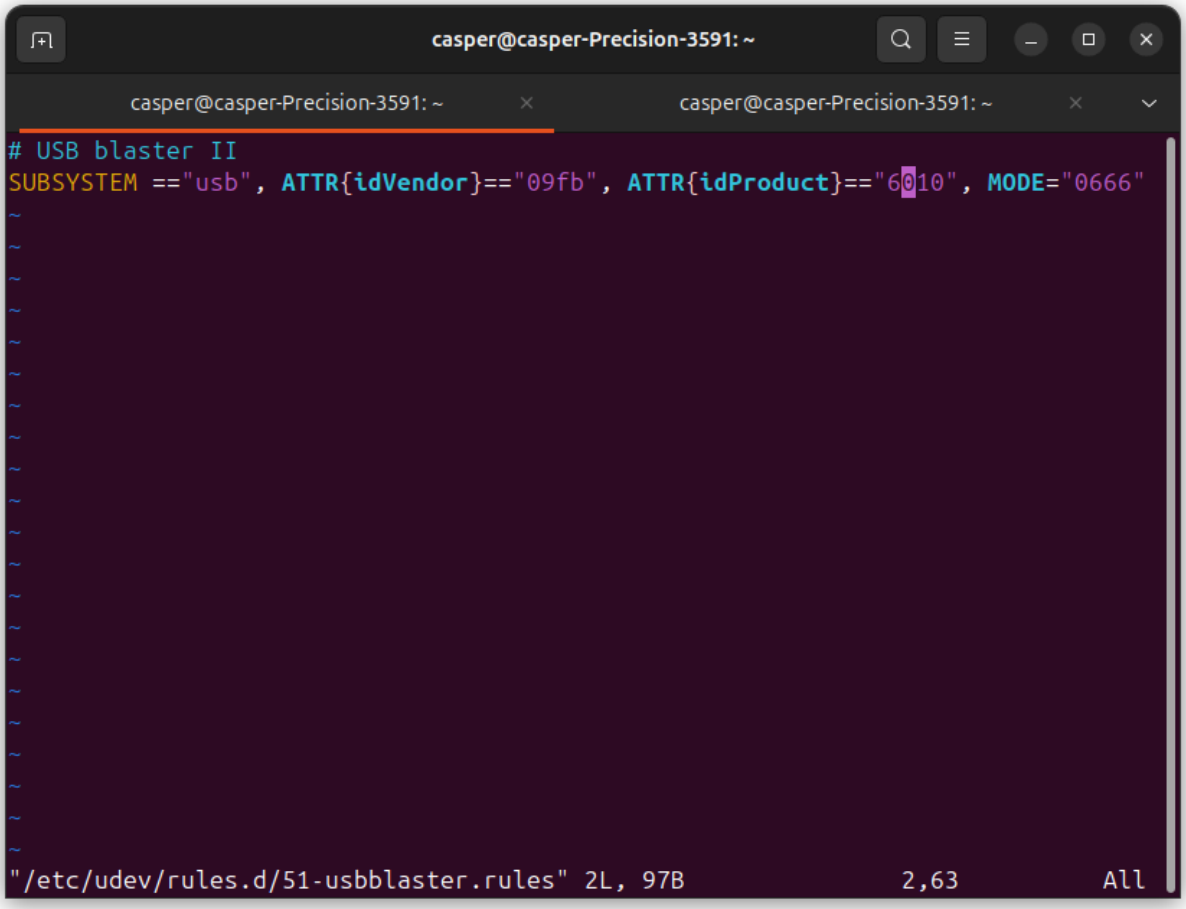
What if your computer doesn’t detect hardware
- in ubuntu, command line

-lsusb to check your connections



- Sometimes there is device compatibility






```
casper@casper-Precision-3591:~$ sudo vi /etc/udev/rules.d/51-usbblaster.rules
```

```
casper@casper-Precision-3591:~$ sudo udevadm control --reload-rules
```

```
casper@casper-Precision-3591:~$ sudo udevadm trigger
```

```
casper@casper-Precision-3591:~$ sudo udevadm control --reload-rules
```

After reload rules, you have to trigger udevadm.

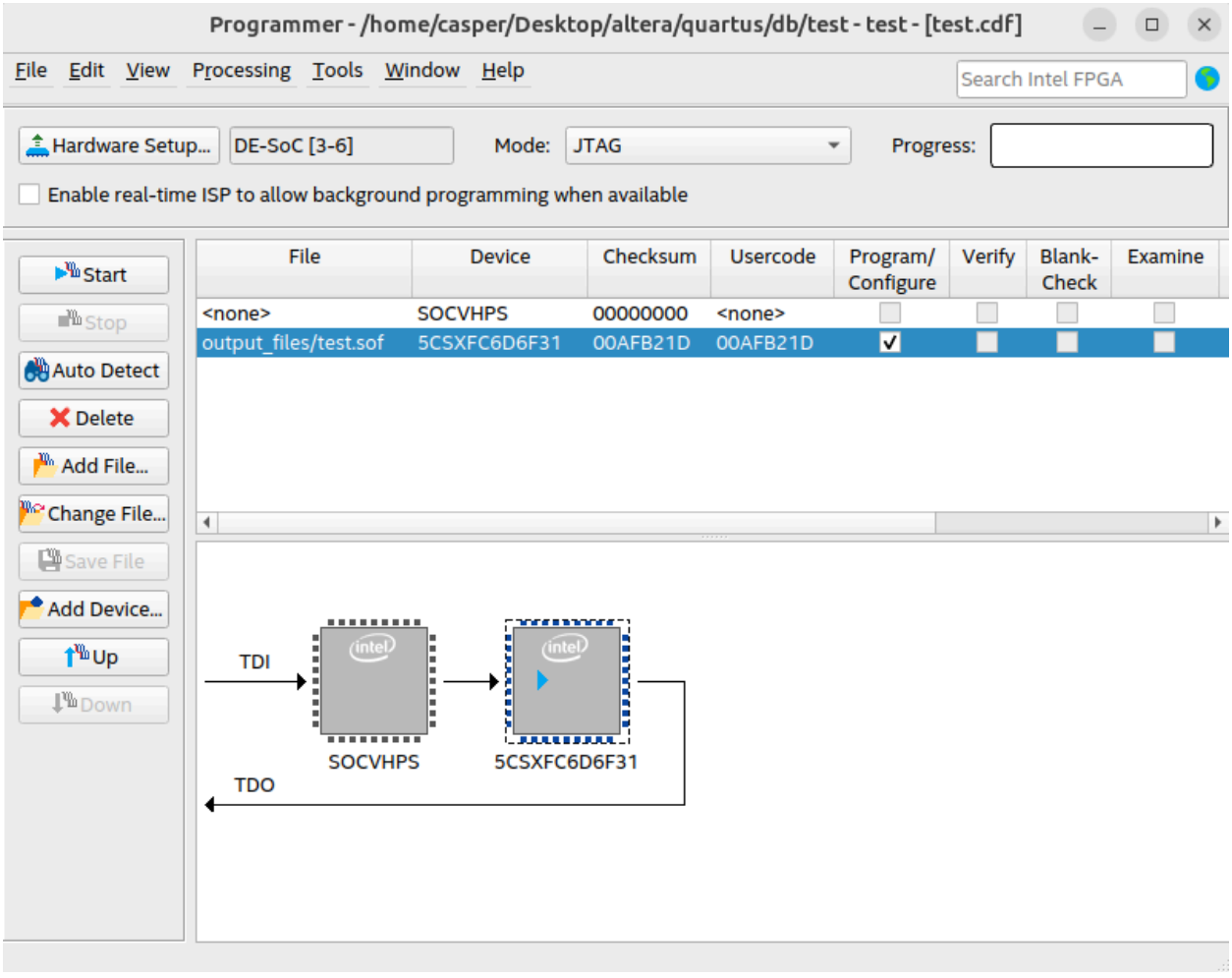
sudo nano /etc/udev/rules.d/51-usbblaster.rules

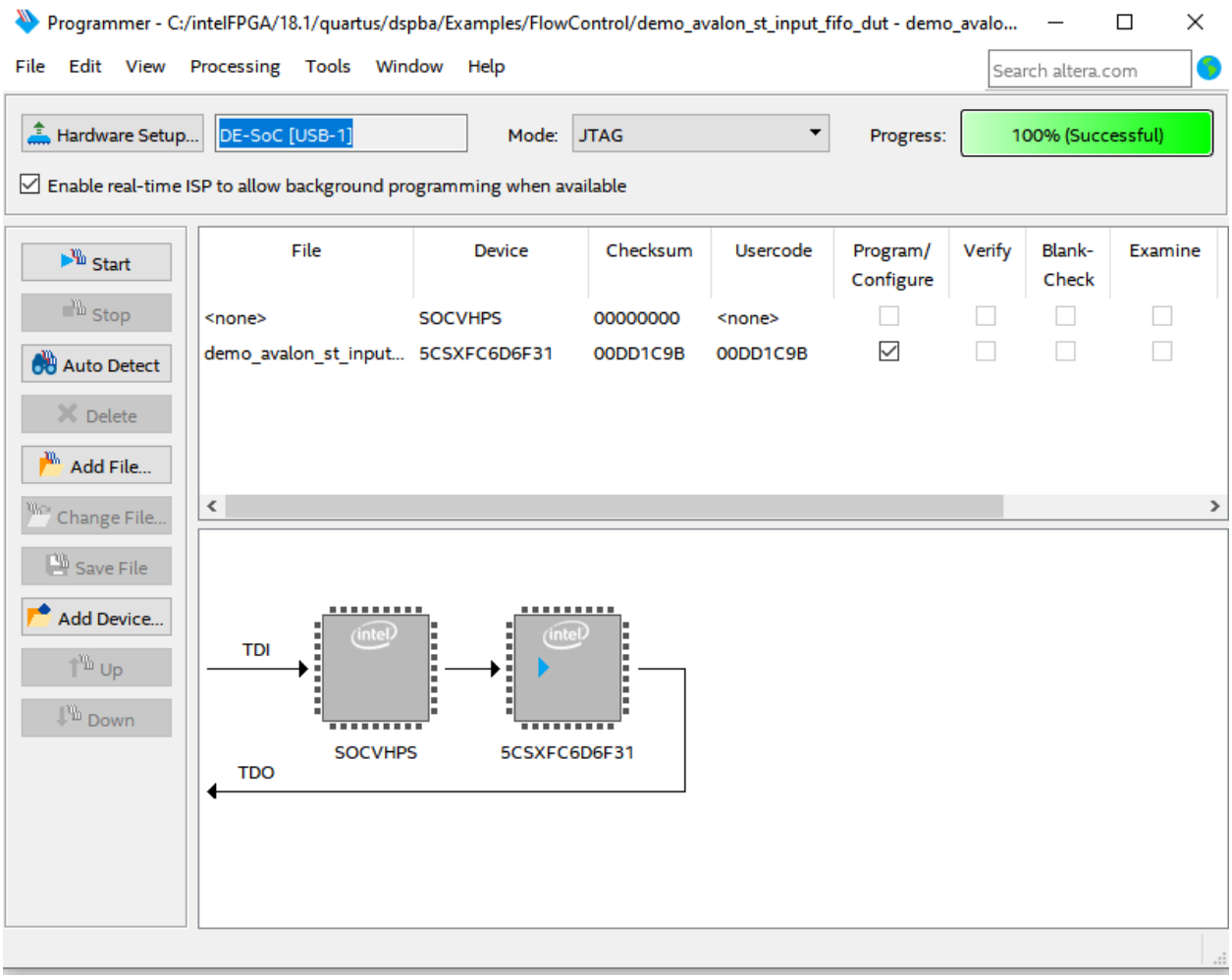
```
# USB-Blaster II
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6810", MOI

# Altera DE-SoC
SUBSYSTEM=="usb", ATTR{idVendor}=="09fb", ATTR{idProduct}=="6010", MOI
```

sudo udevadm control --reload-rules
sudo udevadm trigger

sudo pkill jtagd

Now there is autodetect all the time




Programmer - C:/intelFPGA/18.1/quartus/dspba/Examples/FlowControl/demo_avalon_st_input_fifo_dut - demo_avalo...
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
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Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
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TDI
TDO
SOCVHPS
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