HANDOUT

LOGIC GATES AND LOGIC CIRCUITS

Marking Scheme

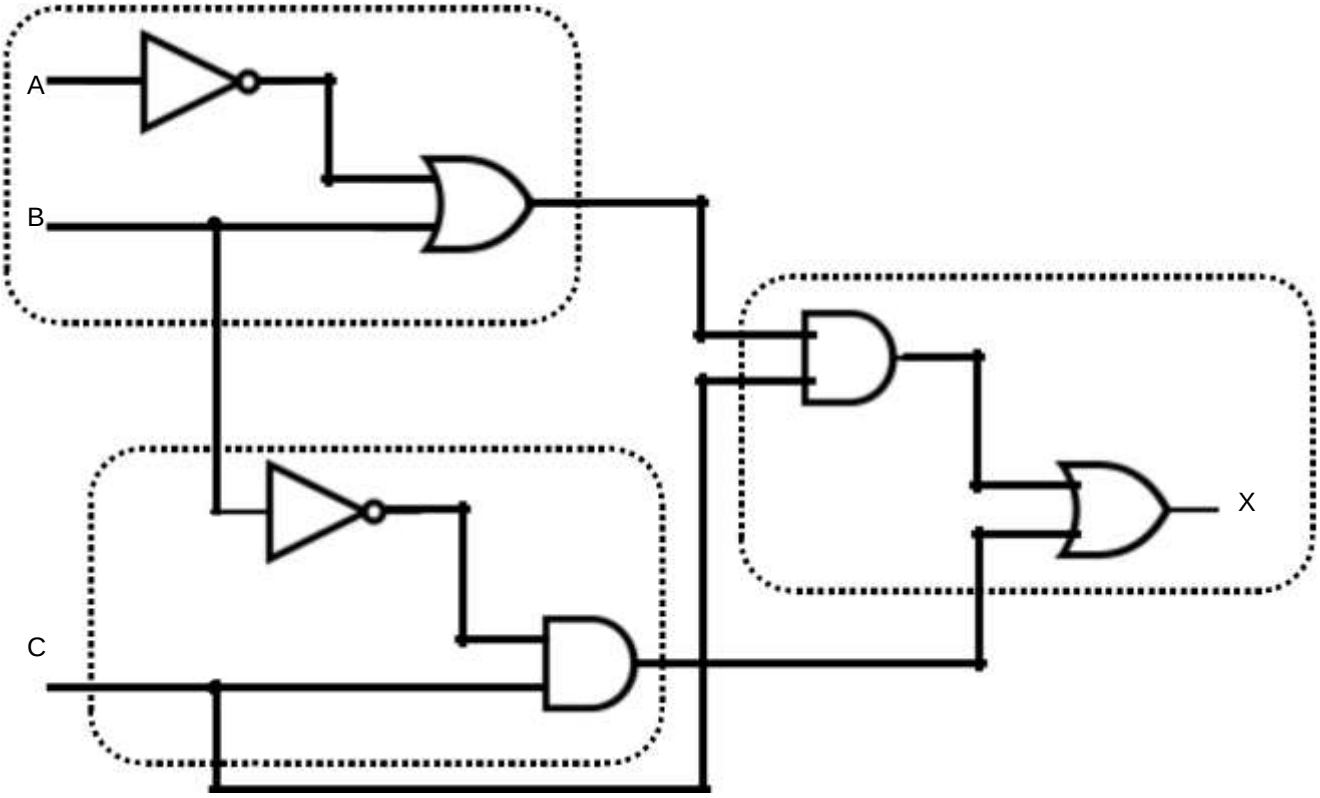
CS Mentor SOORAJ

1 (a)

A	B	C	Working	X	
0	0	0		1	] 1 mark
0	0	1		0	
0	1	0		0	] 1 mark
0	1	1		0	
1	0	0		0	] 1 mark
1	0	1		1	
1	1	0		1	] 1 mark
1	1	1		1	

[4]

(b) 1 mark per dotted section



[3]

(c) X is 1 if:

(A is 1 OR B is 1) (1 mark)

AND (1 mark)

(B is 1 OR C is NOT 1) (1 mark)

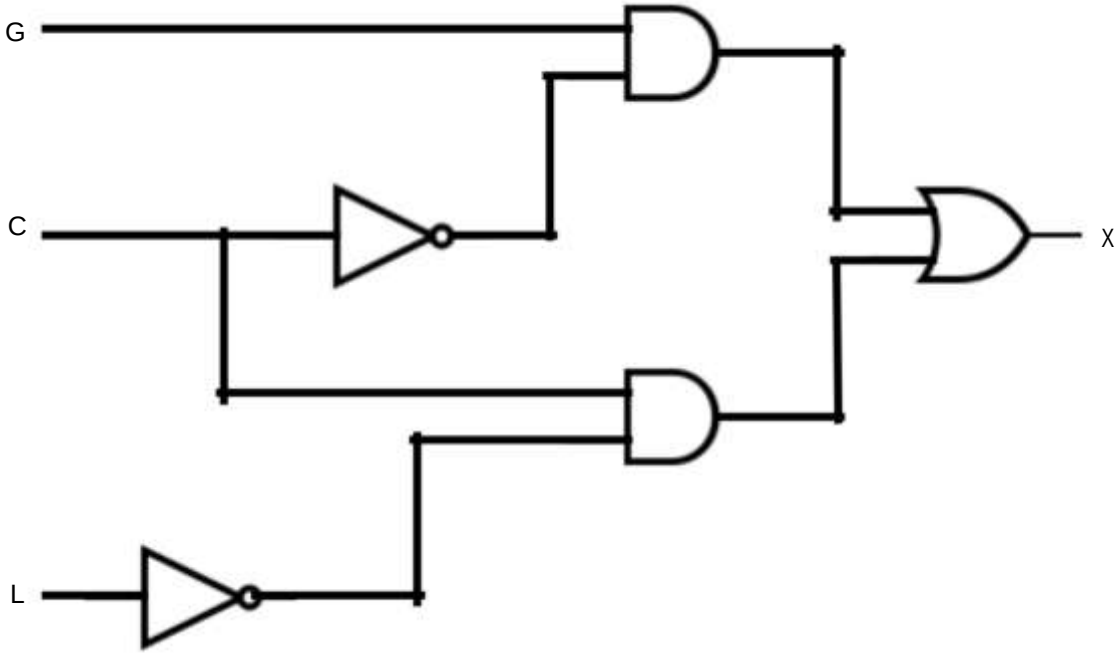
accept equivalent ways of writing this:

e.g. (AORB=1) AND (B OR NOT C = 1)

e.g. (A OR B) AND (B OR NOT C)

e.g. $(A+B)\ (B+C)^{-}$ [3]

2 (a) 1 mark per correct logic gate, correctly connected



[5]

(b)

G	C	L	Workspace	X	
0	0	0		0	1 mark
0	0	1		0	
0	1	0		1	1 mark
0	1	1		0	
1	0	0		1	1 mark
1	0	1		1	
1	1	0		1	1 mark
1	1	1		0	

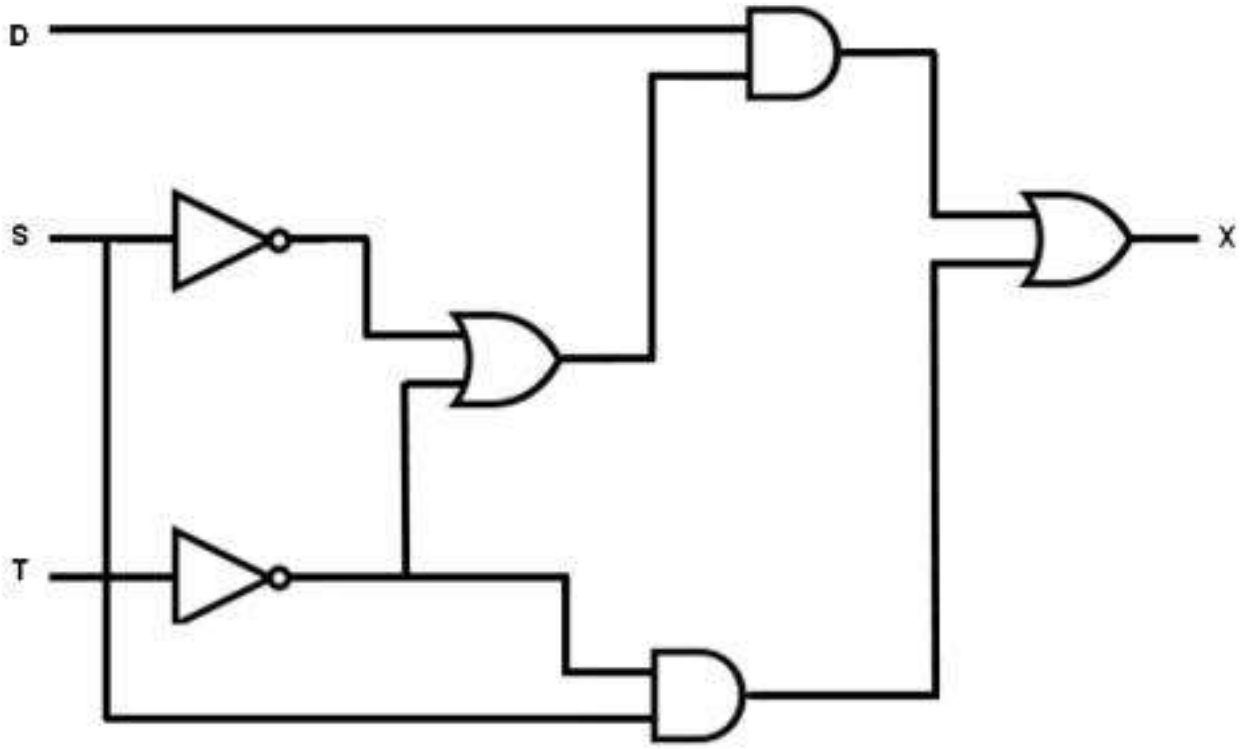
[4]

(c) 1 mark for correctly completed truth table

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

[1]

3 (a) 1 mark for each correct gate, with correct source of input(s)



[6]

(b)

D	S	T	Working Space	X
0	0	0		0
0	0	1		0
0	1	0		1
0	1	1		0
1	0	0		1
1	0	1		1
1	1	0		1
1	1	1		0

4 marks for 8 correct X bits
3 marks for 6 correct X bits
2 marks for 4 correct X bits
1 mark for 2 correct X bits

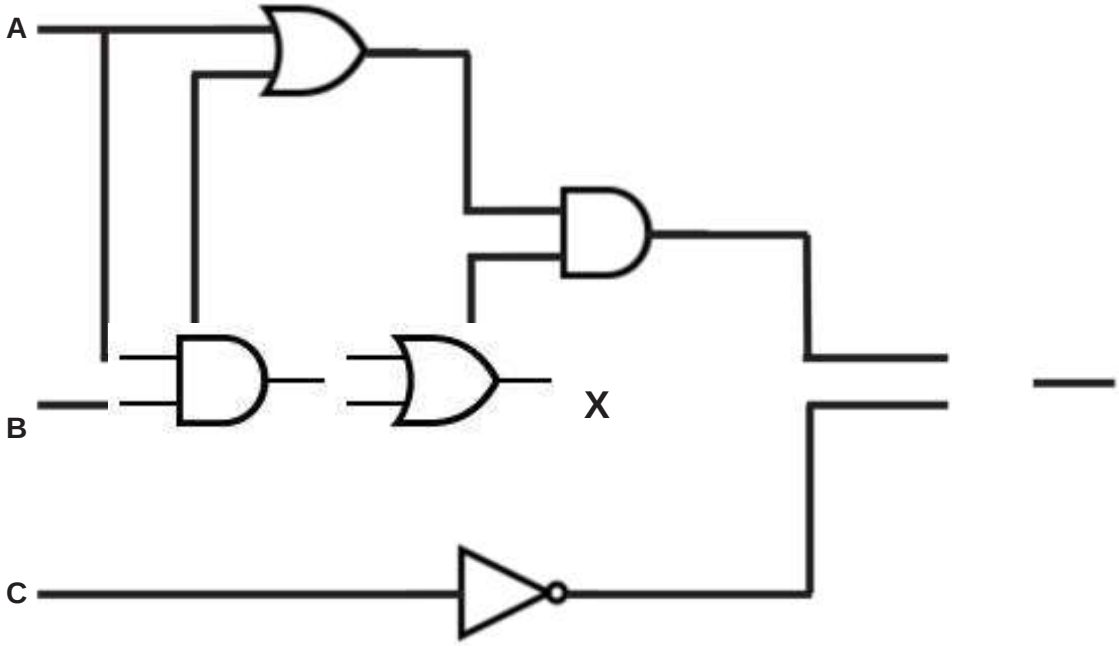
[4]

4 (a)

A	B	C	Working space	X
0	0	0		0
0	0	1		1
0	1	0		0
0	1	1		1
1	0	0		0
1	0	1		1
1	1	0		1
1	1	1		0

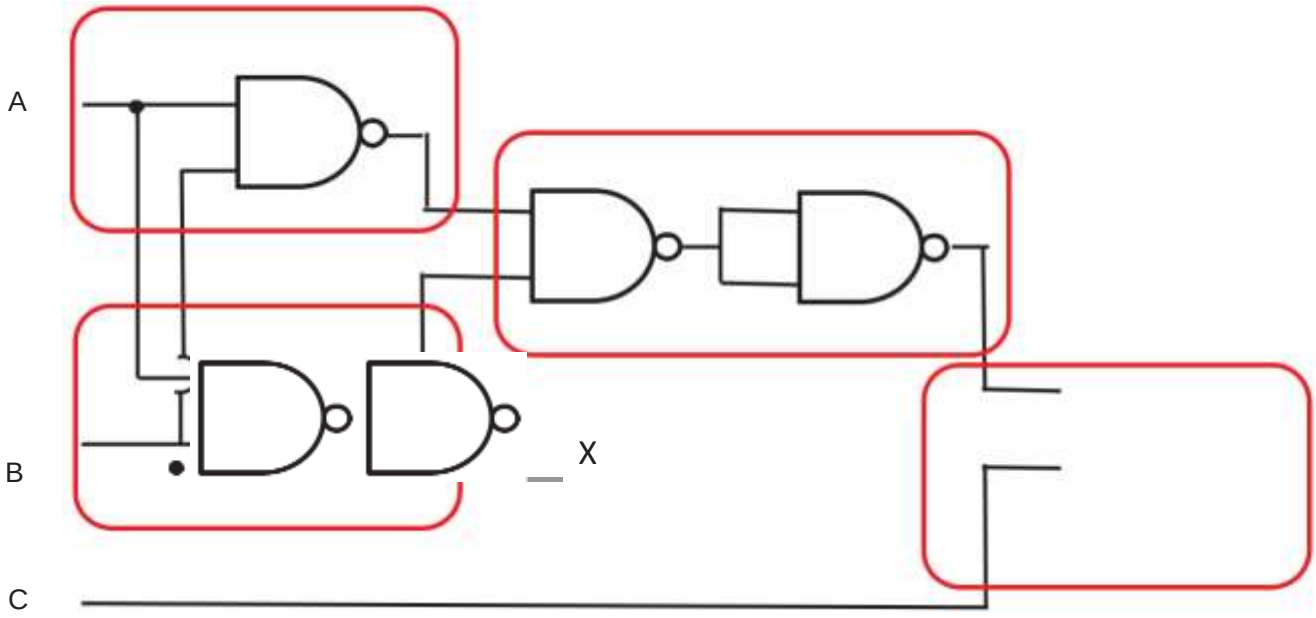
4 marks for 8 correct X bits
3 marks for 6 correct X bits
2 marks for 4 correct X bits
1 mark for 2 correct X bits [4]

(b) 1 mark for each correct gate with correct source of input



[5]

(c) Each dotted area is 1 mark

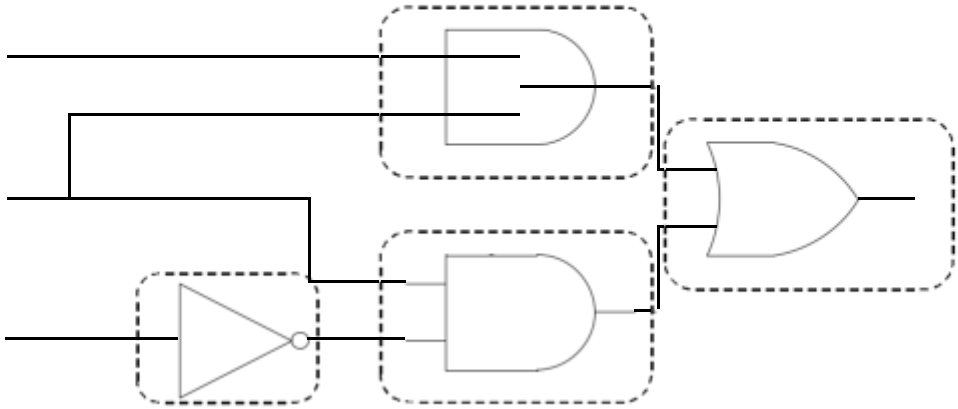


[4]

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>5(a)</td><td>1 mark for four correct outputs only

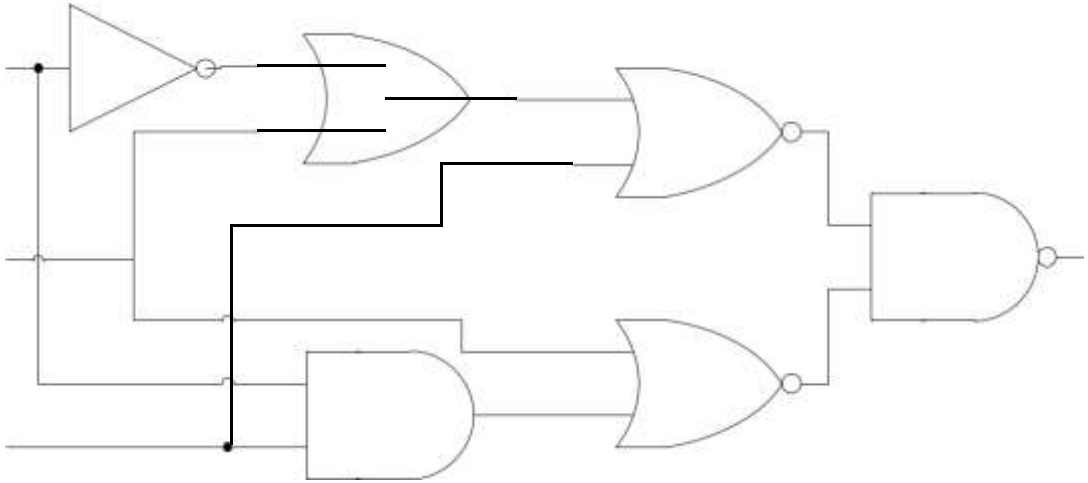
<table><tr><th>A</th><th>B</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table></td><td>1</td></tr>
<tr><td>5(b)</td><td>1 mark for each correct section of the statement

□ (A AND B)
□ AND
□ (C OR NOT B)</td><td>3</td></tr>
</table>

Question	Answer	Marks
6(a)	1 mark for each correct gate, with the correct input(s) 	**4**
6(b)		**4**

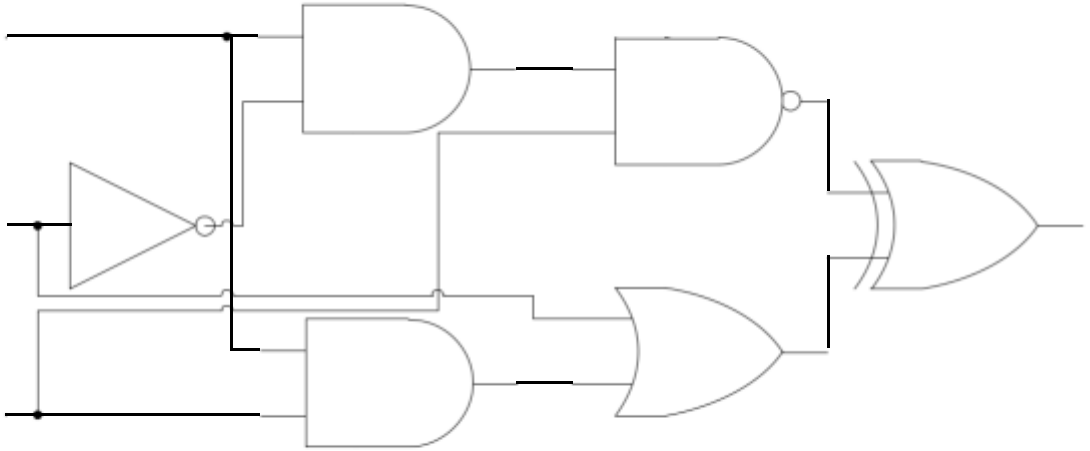
A	B	C	X
0	*0*	*0*	**0**
0	*0*	*1*	**0**
0	*1*	*0*	**1**
0	*1*	*1*	**0**
1	*0*	*0*	**0**
1	*0*	*1*	**0**
1	*1*	*0*	**1**
1	*1*	*1*	**1**

4 marks for 8 correct outputs
3 marks for 6 or 7 correct outputs
2 marks for 4 or 5 correct outputs
1 mark for 2 or 3 correct outputs

Question	Answer	Marks
7(a)	1 mark for each correct logic gate (with the correct direction of input(s)) 	**6**

Question	Answer	Marks
7(b)	4 marks for 8 correct outputs 3 marks for 6 or 7 correct outputs 2 marks for 4 or 5 correct outputs 1 mark for 2 or 3 correct outputs	**4**

A	B	C	Working space	X
0	0	0		**1**
0	0	1		**1**
0	1	0		**1**
0	1	1		**1**
1	0	0		**0**
1	0	1		**1**
1	1	0		**1**
1	1	1		**1**

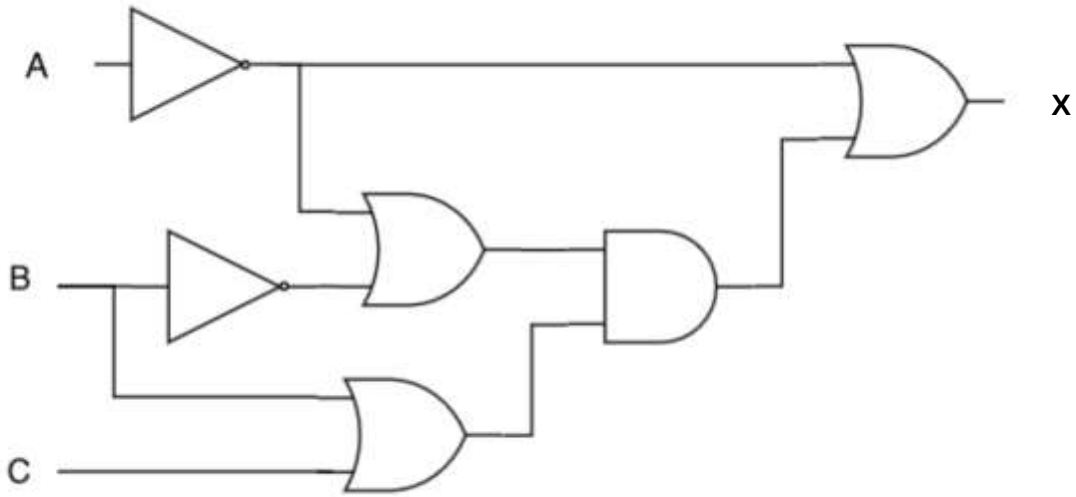
<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>8(a)</td><td>1 mark for each correct logic gate with correct direct of input(s):
  </td><td>6</td></tr>
<tr><td>8(b)</td><td>4 marks for 8 correct outputs
3 marks for 6 or 7 correct outputs
2 marks for 4 or 5 correct outputs
1 mark for 2 or 3 correct outputs

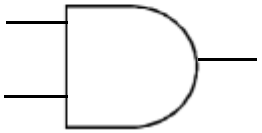
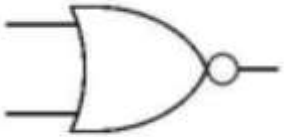
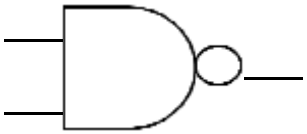
<table>
<tr><th>A</th><th>B</th><th>C</th><th>Working space</th><th>X</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td></td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td></td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td></td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td></td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td></td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td></td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td></td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td></td><td>0</td></tr>
</table></td><td>4</td></tr>
</table>

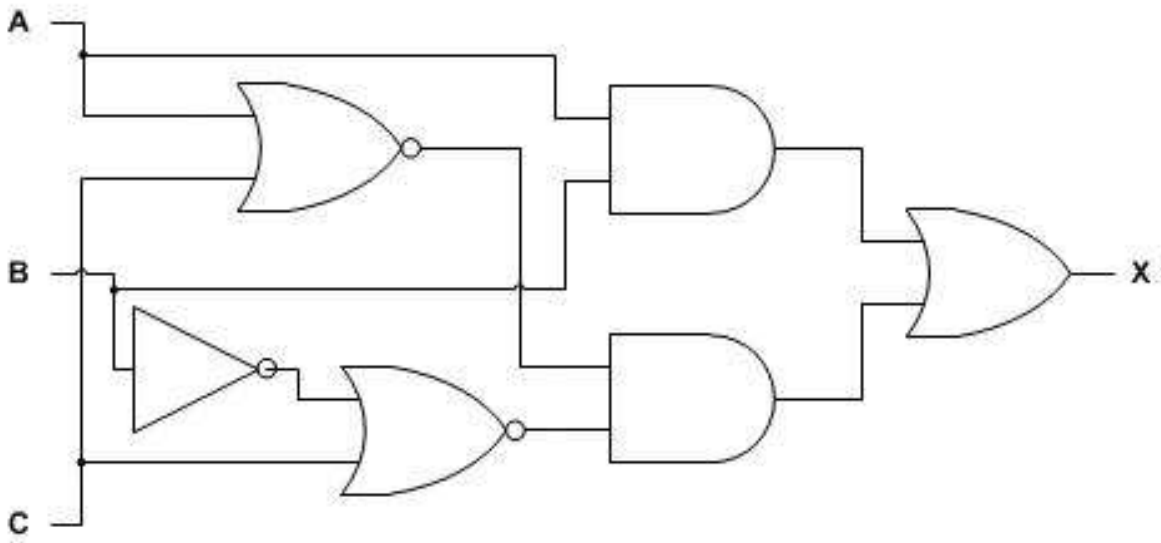
Question	Answer	Marks
9(a)		**4**

A	B	C	X
0	0	0	**1**
0	0	1	**1**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

All 8 for 4 marks
6 or 7 for 3 marks
4 or 5 for 2 marks
2 or 3 for 1 mark

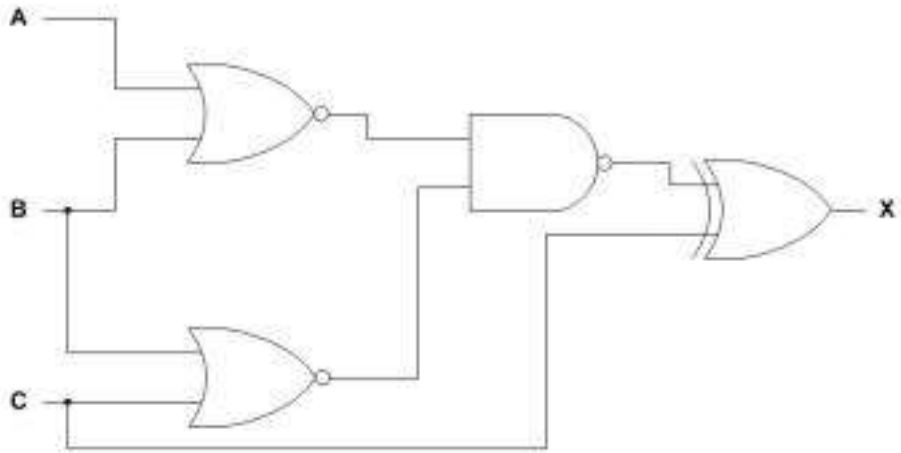
Question	Answer	Marks
9(b)	 1 mark per gate with correct inputs	**6**

Question	Answer	Marks
10(a)	1 mark for correct name, 1 mark for correct gate symbol – AND 	**2**
10(b)	1 mark for correct name, 1 mark for correct gate symbol – NOR 	**2**
10(c)	1 mark for correct name, 1 mark for correct gate symbol – NAND 	**2**

Question	Answer	Marks
11(a)	1 mark per each correct logic gate, with correct input(s) 	**6**

Question	Answer	Marks
11(b)	4 marks for 8 correct outputs 3 marks for 6/7 correct outputs 2 marks for 4/5 correct outputs 1 mark for 2/3 correct outputs	**4**

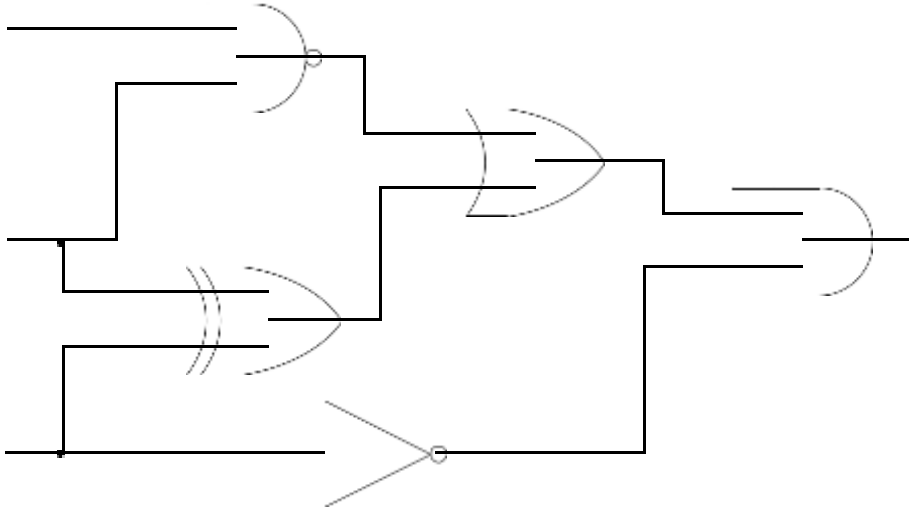
A	B	C	Working space	X
0	0	0		**0**
0	0	1		**0**
0	1	0		**1**
0	1	1		**0**
1	0	0		**0**
1	0	1		**0**
1	1	0		**1**
1	1	1		**1**

Question	Answer	Marks
12(a)	1 mark for each correct logic gate, with correct inputs: 	**4**

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>12(b)</td><td>4 marks for 8 correct outputs
3 marks for 6/7 correct outputs
2 marks for 4/5 correct outputs
1 mark for 2/3 correct outputs

<table>
<tr><th>A</th><th>B</th><th>C</th><th>Working space</th><th>X</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td></td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td></td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td></td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td></td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td></td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td></td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td></td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td></td><td>0</td></tr>
</table>
</td><td>4</td></tr>
<tr><td>12(c)</td><td>Two from:

− To carry out a logical operation
− To control the flow of electricity through a logic circuit
− An input is given and the logic of the gate is applied to give an output // to alter the output from given inputs</td><td>2</td></tr>
</table>

Question	Answer	Marks
13(a)	 1 mark for each correct gate.	**5**

Question	Answer	Marks
13(b)		3

A	B	C	Working space	X
0	0	0		**1**
0	0	1		**0**
0	1	0		**1**
0	1	1		**0**
1	0	0		**1**
1	0	1		**0**
1	1	0		**1**
1	1	1		**0**

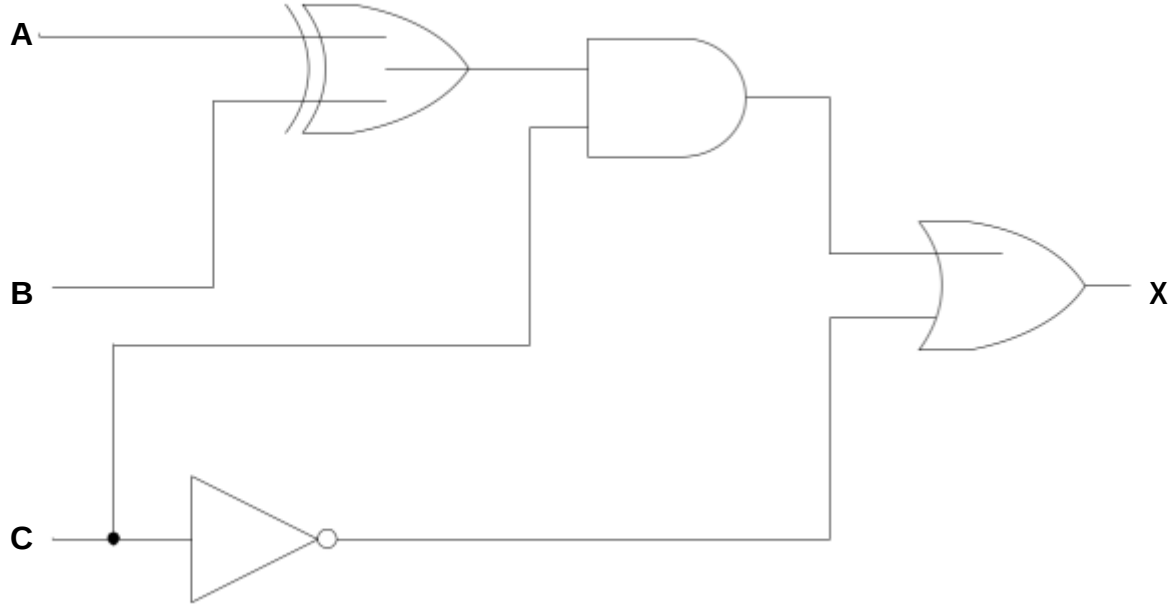
4 marks for 8 correct outputs
3 marks for 6 or 7 correct outputs
2 marks for 4 or 5 correct outputs
1 mark for 2 or 3 correct outputs

Question	Answer	Marks
14(a)(i)	− NAND 	**2**
14(a)(ii)	−NOR 	**2**

Question	Answer	Marks
14(b)		**4**

A	**B**	**C**	Working space	**X**
0	0	0		**0**
0	0	1		**0**
0	1	0		**1**
0	1	1		**1**
1	0	0		**0**
1	0	1		**0**
1	1	0		**1**
1	1	1		**1**

4 marks for 8 correct outputs
3 marks for 6 or 7 correct outputs
2 marks for 4 or 5 correct outputs
1 mark for 2 or 3 correct outputs

Question	Answer	Marks
15(a)	 One mark for each correct gate.	4

Question	Answer	Marks
15(b)		4

A	B	C	Working space	X
0	0	0		**1**
0	0	1		**0**
0	1	0		**1**
0	1	1		**1**
1	0	0		**1**
1	0	1		**1**
1	1	0		**1**
1	1	1		**0**