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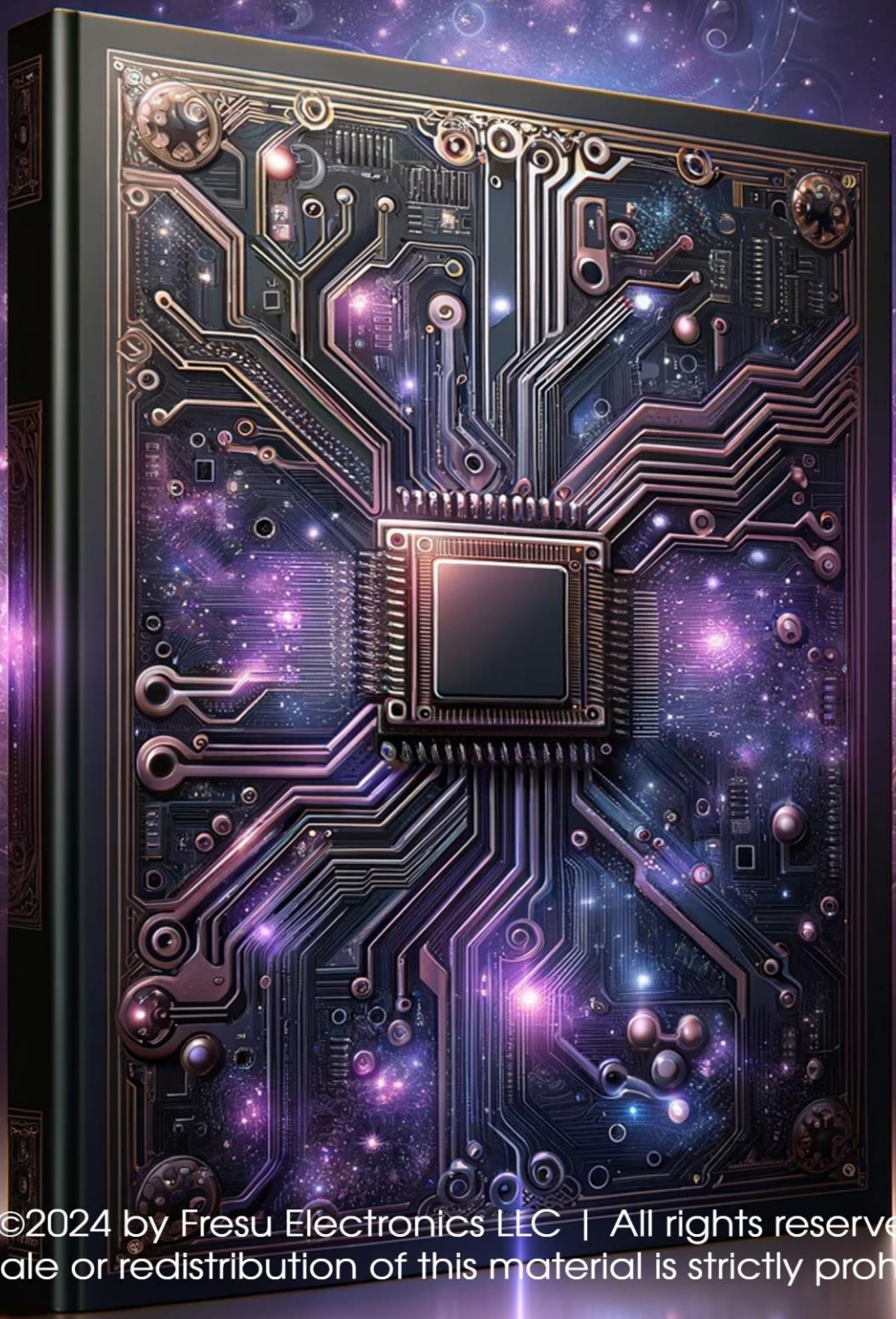
PRE-LAYOUT REVIEW CHECKLIST



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PRE-LAYOUT REVIEW CHECKLIST

Welcome to the Pre-Layout Review Checklist!

This handy checklist is here to assist you in getting started with your PCB layout design smoothly.

It ensures that your schematics are all set and ready for the layout phase.
Using this checklist is simple and easy to understand.

Just go through the items listed on the following pages and mark them as done when you've completed each step.

I've noticed that as I gained more experience, I sometimes overlooked the basics while focusing on the more critical aspects. This checklist is designed to help you avoid such common mistakes.

As you become more experienced, you'll probably develop your unique style and create a personalized checklist.

Now, let's begin the review process.
Dario

PROJECT IDENTIFICATION AND OVERVIEW:

☐ My Overview Page has a clear title that illustrates the name of the project.

☐ I have added a revision number to identify the project version I am working with.

☐ Other Project details are updated, including the Title, revision, and version number, file name.

☐ My contact details are displayed on each page, including at least:

- ✓ Name and surname of the designer
- ✓ Email address
- ✓ Logo / Company name

SCHEMATIC ORGANIZATION AND CLARITY:

☐ I confirm that I have included a block diagram of the connections between components and systems.

☐ I confirm the title is displayed on each page and is descriptive of the functional block.

☐ The pages of the schematics are numbered for easy block location.

☐ Each block has an intuitive name and a page number for easy identification.

☐ The status of the schematic is clearly reported.

☐ The date of the last update is clearly visible on each page.

DESIGN DETAILS AND ANNOTATIONS:

☐ I confirm that each module of my schematic is subdivided into clear blocks.

☐ I confirm that each net has a net label assigned for easy identification.

☐ I confirm that each symbol has consistent directionality to avoid confusion.

☐ I confirm that sensitive traces are labeled for attention during the layout phase.

PROTECTION AND DEBUGGING FEATURES:

☐ I confirm that each input and output connector has appropriate protections and/or filters.

☐ I confirm that I added testing points and other tools for easy debugging and bring-up where necessary.

☐ I confirm that each IC has bypass capacitors.

☐ I confirm that all unused pins are terminated.

☐ I confirm that polarized components are placed correctly according to their polarity.

☐ I confirm that the design includes necessary safety features such as overvoltage, overcurrent, and thermal protection.

☐ I confirm that the design adheres to relevant industry standards and regulatory requirements (such as IEC standards for electronic equipment).

☐ I confirm that all necessary power decoupling and filtering strategies are incorporated in the design.

☐ I confirm that user interface elements, if any (like LEDs, switches, and display interfaces), have been correctly implemented and documented.

☐ I confirm that ESD protection measures are in place for all sensitive components and interfaces.

☐ I confirm that RF components and circuits (if any) have been reviewed for frequency, impedance matching, and interference issues.

☐ I confirm that provisions for calibration, if required, are incorporated into the design.

POWER AND SIGNAL INTEGRITY:

☐ I confirm that each power net has its voltage value and polarity clearly indicated.

☐ I confirm that signal traces with high harmonic content have a series Zero-ohm resistor from promt replacement if necessary.

☐ I confirm that I added terminations where necessary for impedance matching.

☐ I confirm that power components have the correct power ratings.

☐ I confirm that there are no crossing nets or wires on the schematics.

☐ I confirm that all external interfaces (connectors, ports) have been correctly defined and meet the requirements for signal, power, and mechanical robustness.

☐ I confirm that inter-board or intra-board communication protocols and connections are correctly implemented.

☐ I confirm that any identified issues from previous design reviews have been addressed.

☐ I confirm that each subsystem (e.g., power supply, microcontroller unit, communication interfaces) has been individually verified for its functionality.

COMPONENT AND CONNECTION VERIFICATION:

☐ I confirm that all components used in the design are readily available or have identified substitutes to avoid supply chain issues.

☐ I confirm that all components used in the design are sourced from reliable suppliers and are not at risk of becoming obsolete in the near future.

☐ I confirm that I double-checked each pin of major components for correct connections.

☐ I confirm that RX and TX pins are connected to the correct pins.

☐ I confirm that I added net ties for tracks with the same voltages but different roles.

☐ I confirm that each block is interconnected to the right block on the block diagram.

☐ I confirm that the design has been checked for interoperability with other systems or modules it will interface with.

LAYOUT AND MECHANICAL CONSIDERATIONS:

☐ I confirm that the input and output ports are designed according to the left-to-right convention.

☐ I confirm that I added extra footprint between mounting holes and board return Ground.

☐ I confirm that I added fiducials and mounting holes to the mechanical page.

☐ I confirm that a component represents the PCB in the Bill of Material.

COMPLIANCE AND DOCUMENTATION:

☐ I confirm that I added symbols for labels like CE mark, ESD, Hot surface, High-Voltage, UL certification, RoHS compliance etc.

☐ I confirm that differential nets are labeled and annotated accordingly.

☐ I confirm that the schematic looks clean and orderly.

☐ I have confirmed that I studied the datasheet of each IC and checked the errata files.

☐ I confirm that all critical signal paths (like clock lines, high-speed data) are optimized for minimal interference and delay.

☐ I confirm that key components such as microcontrollers, memory, and power regulators have been correctly implemented as per their datasheets.

☐ I confirm that a basic FMEA has been performed to identify potential failure modes and their impact on the circuit's performance.

FINAL CHECKS:

☐ I confirm that I added notes for quick understanding or debugging where necessary.

☐ I confirm that modifications of previous versions are reported with special notes included.

☐ I confirm that I followed all signals and checked the entire connection path.

☐ I confirm that the ERC rules are set according to the project and manufacturing requirements.

☐ I confirm that I have reserved a special place for either the model of the PCB or real photos post-completion.

☐ I confirm that a detailed bill of materials (BOM) is prepared and includes specifications for all components.

☐ I confirm that the Electrical Rule Checker complies without errors and warnings.

NEXT STEP:

The schematic is now ready to be reviewed by another engineer or team member for a second opinion and to catch potential oversights.

NAME AND SURNAME

EMAIL

DATE

SIGNATURE