1. A positive OR gate is also a negative
    a. NAND gate
    b. OR gate
    **c. NOR gate**
    d. AND gate
2. The inverter is ……
    a. OR gate
    **b. NOT gate**
    c. AND gate
    d. Both a and b
3. Minterms are also called
    **a. standard product**
    b. standard sum
    c. Both A & B
    d. standard division
4. The NAND gate is AND gate followed by ……
    a. OR gate
    **b. NOT gate**
    c. AND gate
    d. Both a and b
5. The device which changes from serial data to parallel data is
    a. **Demultiplexe**r
    b. Multiplexer
    c. Flip-Flop
    d. Counter
6. In Boolean algebra, (A.A')+A=?
    **a. A**
    b. 0
    c. A'
    d. 1
7. Which condition in J-K flip-flop as no changes next state from the present state?
    **a. J=0,k=0**
    b. J=0,k=1
    c. J=1,k=0
    d. J=1,k=1
8. T flip flop can be made from a j-k flip flop by making
    **a. J=k**
    b. J=k=1
    c. J=0,k=1
    d. J=K'
9. 16-bit 2's complement representation, the decimal number -28 is:
    a. 1111 1111 0001 1100
    b. 0000 0000 1110 0100
    c. 1111 1111 1110 0100

d. 1000 0000 1110 1000

10. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
    a. Two 2 input AND gates
    b. Two 3 input AND gates
    c. Two 2 input OR gates
    d. Two 3 input OR gates
11. What will be the output from a D flip – flop if the clock is low and D = 0?
    a. 0
    b. 1
    c. No change
    d. Toggle between 0 and 1
12. What input should be given to "S" when SR flip – flop is converted to JK flip – flop?
    a) K.Q
    b) K.Q'
    c) J.Q
    d) J.Q' R=KQ



13. What value is to be considered for a "don't care condition"?
    a) 0
    b) 1
    c) Either 0 or 1
    d) Any number except 0 and 1

14. What will be the frequency of the output from a JK flip – flop, when J = 1, K = 1, and a clock with pulse waveform is given?
    a) Half the frequency of clock input
    b) Equal to the frequency of clock input
    c) Twice the frequency of clock input
    d) Independent of the frequency of clock input

15. What must be the input given to "R" when SR flip – flop is converted to JK flip – flop?
    a) K.Q
    b) K.Q'
    c) J.Q
    d) J.Q'

16. Which of these flip – flops cannot be used to construct a serial shift register?
    a) D – flip flop
    b) SR flip – flop

c) T flip – flop when input is 1 it gives 0 and when o it gives 1 so
d) JK flip – flop

17. What kind of operation occurs in a J – K flip flop when both inputs J and K are equal to 1?
a) Preset operation
b) Reset operation
c) Clear operation
d) Toggle operation

18. The result "X + XY = X" follows which of these laws? X(1+Y)=X
a) Consensus law
b) Distributive law
c) Duality law
d) Absorption law

19. What frequency division of the pulsed clock signal can be obtained by connecting 4 flip – flops in cascade?
a) 2
b) 4
c) 8
d) 16 2n



20. A priority encoder has four inputs $I_0$, $I_1$, $I_2$, and $I_3$ where $I_3$ has the highest priority and $I_0$ has the least priority. If $I_2$ = 1, what will be the output?
a) 00
b) 01
c) 10
d) 11

i3 is highest means four input case it is 11, so io is least mean io is 00
i1 is 01, i2 is 10 so

21. Which of the following options are correct for a 4×1 multiplexer?
a) It has four 3 – input AND gates 2 select line and one input so
b) It has four 2 – input AND gates
c) It has one 3 – input AND gate
d) It has one 3 – input AND gate

22. Which of these pins will allow to activate and deactivate a multiplexer?
a) Enable pin
b) Selection pin
c) Logic pin
d) Preset pin

23. A digital circuit that can store only one bit is a

    a. Register
    b. NOR gate
    c. Flip flop
    d. XOR gate

24. DeMorgan's Law states that
    a. (A+B)'= A'.B
    b. (A.B)'= (A+B)'
    c. (A+B)'=A'.B'
    d. (A'+B')=A.B'

25. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
    a) Two 2 input AND gates
    b) Two 3 input AND gates
    c) Two 2 input OR gates
    d) Two 3 input OR gate

26. Which of the following options represent the synchronous control inputs in an S – R flip flop?
    a) S
    b) R
    c) Clock
    d) Both S and R

27. What must be used along with synchronous control inputs to trigger a change in the flip flop?
    a) 0
    b) 1
    c) Clock
    d) Previous output

28. What will be the output from a D flip – flop if the clock is low and D = 0?
    a) 0
    b) 1
    c) No change
    d) Toggle between 0 and 1

29. What will be the output from a D flip-flop if D = 1 and the clock is low?
    a) No change
    b) Toggle between 0 and 1



Type text here

if clock is low(0) , no change but
if clock is high(1), input=0, output=0
if clock is high(1), input=1, output=1

c) 0
d) 1

30. What input should be given to "S" when SR flip – flop is converted to JK flip – flop?
a) K.Q
b) K.Q'
c) J.Q
d) J.Q'

31. What must be the input given to "R" when SR flip – flop is converted to JK flip – flop?
a) K.Q
b) K.Q
c) J.Q
d) J.Q

32. Which of the following gives the correct number of multiplexers required to build a 32 x 1 multiplexer?
a) Two 16 x 1 mux
b) Three 8 x 1 mux
c) Two 8 x 1 mux
d) Three 16 x 1 mux

33. Which of these flip – flops cannot be used to construct a serial shift register?
a) D – flip flop
b) SR flip – flop
c) T flip – flop
d) JK flip – flop

34. What kind of operation occurs in a J – K flip flop when both inputs J and K are equal to 1?
a) Preset operation
b) Reset operation
c) Clear operation
d) Toggle operation

35. What determines the output from the combinational logic circuit in Digital Electronics?
a) Input signals from the past condition
b) Input signals at the present moment
c) Input signals from both past and present
d) Input signals expected in future

36. Which of the following is a type of microprocessor?
    a) CISC
    b) RISC
    c) EPIC
    d) All of the mentioned
37. The microprocessor of a computer can operate on any information if it is present in _____ only.
    a) Program Counter
    b) Flag
    c) Main Memory
    d) Secondary Memory
38. Which of the following technology was used by Intel to design its first 8-bit microprocessor?
    a) NMOS
    b) HMOS
    c) PMOS
    d) TTL
39. Which of the following addressing method does the instruction, MOV AX,[BX] represent?
    a) register indirect addressing mode
    b) direct addressing mode
    c) register addressing mode
    d) register relative addressing mode
40. Which of the following is not true about the address bus?
    a) It consists of control PIN 21 to 28
    b) It is a bidirectional bus
    c) It is 16 bits in length
    d) Lower address bus lines ($AD_0$ – $AD_7$) are called “Line number”
41. Which of the following is true about microprocessors?
    a) It has an internal memory
    b) It has interfacing circuits
    c) It contains ALU, CU, and registers
    d) It uses Harvard architecture

42. Which of the following is the correct sequence of operations in a microprocessor?
    a) Opcode fetch, memory read, memory write, I/O read, I/O write
    b) Opcode fetch, memory write, memory read, I/O read, I/O write
    c) I/O read, opcode fetch, memory read, memory write, I/O write
    d) I/O read, opcode fetch, memory write, memory read, I/O write
43. Which of the following is not a property of TRAP interrupt in microprocessor?
    a) It is a non-maskable interrupt
    b) It is of highest priority
    c) It uses edge-triggered signal
    d) It is a vectored interrupt
44. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?
    a) Parallel-in Parallel-out
    b) Parallel-in Serial-out
    c) Serial-in Serial-out
    d) Serial-in Parallel-out
45. In a 4-bit Johnson counter sequence, there are a total of how many states or bit patterns?
    a) 1
    b) 3
    c) 4
    d) 8
46. If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?
    a) 1101000000
    b) 0011010000 after shifting 2 bit we get output this as 2 zeros are fist and second postion
    c) 1100000000
    d) 0000000000
47. Ring shift and Johnson counters are _____
    a) Synchronous counters
    b) Asynchronous counters
    c) True binary counters
    d) Synchronous and true binary counters
48. What is the preset condition for a ring shift counter?
    a) All FFs set to 1
    b) All FFs cleared to 0

c) A single 0, the rest 1
d) A single 1, the rest 0.

49. A flip flop stores _____
    a) 10 bit of information
    b) 1 bit of information
    c) 2 bit of information
    d) 3-bit information
50. A register is able to hold _____
    a) Data
    b) Word 16 bit or 2 byte =1 word
    c) Nibble
    d) Both data and word
51. In a computer, registers are present _____
    a) Within control unit
    b) Within RAM
    c) Within ROM
    d) Within CPU
52. PLDs with programmable AND and fixed OR arrays are called _____
    a) PAL
    b) PLA
    c) APL
    d) PPL
53. When both the AND and OR are programmable, such PLDs are known as _____
    a) PAL
    b) PPL
    c) PLA
    d) APL
54. A set of register which contain are:
    a. Data
    b. memory addresses
    c. result
    d. all of these
55. Suppose registers 'A' and 'B' contain 50H and 40H respectively. After instruction MOV A, B, what will be the contents of registers A and B?
    a) 40H, 40H
    b) 50H, 40H

c) 50H, 50H
d) 60H, 40H

56. Conditional instructions are independent of which of the following flag?
    a) Z
    b) AC
    c) CY
    d) P
57. Which of the following is not correct about HLT instruction?
    a) It is a machine control instruction
    b) It is used to start the execution of the program
    c) PC is disconnected from the address bus
    d) A reset interrupt is required to come out of halt state
58. A machine language instruction format consists of
    a) Operand field
    b) Operation code field
    c) Operation code field & operand field
    d) none of the mentioned
59. The instruction "JUMP" belongs to
    a) sequential control flow instructions
    b) control transfer instructions
    c) branch instructions
    d) control transfer & branch instructions
60. The disadvantage of machine level programming is
    a) time consuming
    b) chances of error are more
    c) debugging is difficult
    d) all of the mentioned
61. Port C of 8255 can function independently as
    a) input port
    b) output port
    c) either input or output ports
    d) both input and output ports
62. If A1=0, A0=1 then the input read cycle is performed from
    a) port A to data bus
    b) port B to data bus
    c) port C to data bus
    d) CWR to data bus

63. How many address and input-output data lines are needed for the 64K* 8 memory unit?
    a. 16 address line, 3 data line
    b. 6 address line, 3 data line
    c. 10 address line, 8 data lines
    **d. 16 address line, 8 data lines**
64. Microprogram is
    a. The name of source program in micro computers
    **b. Set of instructions that defines the individual operations in response to a machine language instruction**
    c. A primitive form of macros used in assembly language programming
    d. A very small segment of machine code
65. A sequence of control words corresponding to a control sequence is called
    **a. Micro routine**
    b. Micro function
    c. Micro procedure
    d. None of the above
66. The part of a processor which contains hardware necessary to perform all the operations required by a computer:
    a) Data path
    b**) Controller**
    c) Registers
    d) Cache
67. If the control signals are generated by combinational logic, then they are generated by a type of _____ controlled unit.
    a) Micro programmed
    b) Software
    c) Logic
    d**) Hardwired**
68. A set of microinstructions for a single machine instruction is called _____
    a) Program
    b) Command
    c) Micro program
    d) Micro command
69. Micro-program consists of a set of microinstructions which are strings of 0s and 1s.
    a**) True**
    b) False
70. In the case of, Zero-address instruction method the operands are stored in _____
    a) Registers
    b) Accumulators
    c) **Push down stack**
    d) Cache

71. The addressing mode/s, which uses the PC instead of a general purpose register is _____
    a) Indexed with offset
    **b)** Relative
    c) Direct
    d) Both Indexed with offset and direct
72. The addressing mode, where you directly specify the operand value is _____
    a) Immediate
    b) Direct
    c) Definite
    d) Relative
73. The status bit is also called as-
    a. Unsigned bit
    b. Signed bit
    **c. Flag bit**
    d. None of the above
74. In micro-programmed approach, the signals are generated by _____
    a**) Machine instructions**
    b) System programs
    c) Utility tools
    d) None of the mentioned
75. A word whose individual bits represent a control signal is _____
    a) Command word
    b) **Control word**
    c) Co-ordination word
    d) Generation word
76. Individual control words of the micro routine are called as _____
    a) Micro task
    b) Micro operation
    c) **Micro instruction**
    d) Micro command
77. The directly mapped cache no replacement algorithm is required.
    a) **True**
    b) False
78. The surroundings of the recently accessed block is called as _____
    a) Neighborhood
    b) Neighbour
    c**) Locality of reference**
    d) None of the mentioned

79. The algorithm which replaces the block which has not been referenced for a while is called _____
    a) **LRU**
    b) ORF
    c) Direct
    d) Both LRU and ORF
80. The main purpose of having memory hierarchy is to _____
    a) Reduce access time
    b) Provide large capacity
    c) Reduce propagation time
    **d) Reduce access time & Provide large capacity**
81. Which one of the following facilitates transfer of bulk data from hard disk to main memory with the highest throughput?
    a. **DMA based I/O transfer**
    b. Interrupt driven I/O transfer
    c. Polling based I/O transfer
    d. Programmed I/O transfer
82. Which of the following is a type of architecture used in the computers nowadays?
    a) Microarchitecture
    b) Harvard Architecture
    c) **Von-Neumann Architecture**
    d) System Design



83. Which of the architecture is power efficient?
    **a) RISC**
    b) ISA
    c) IANA
    d) CISC

84. _____ are the different type/s of generating control signals.
    a) Hardwired
    b) Micro-instruction
    c) Micro-programmed
    **d)** Both Micro-programmed and Hardwired

85. The small extremely fast, RAM's all called as _____
    a) Heaps
    b) Accumulators
    c) Stacks
    d**) Cache**

86. Which of the following is the fullform of CISC?
    a) Complex Instruction Sequential Compilation
    b) Complete Instruction Sequential Compilation
    c) Computer Integrated Sequential Compiler
    d**) Complex Instruction Set Computer**

87. The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____
    a) CMOS
    b) Memory sticks
    c) Blue-ray devices
    d) **Flash memory**

88. During a write operation if the required block is not present in the cache then _____ occurs.
    a) **Write miss**
    b) Write latency
    c) Write hit
    d) Write delay

89. While using the direct mapping technique, in a 16 bit system the higher order 5 bits are used for _____
    a) Id
    b) Word
    c**) Tag**
    d) Block



90. The bit used to indicate whether the block was recently used or not is _____
    a) Reference bit
    b**) Dirty bit**
    c) Control bit
    d) Idol bit

91. The number successful accesses to memory stated as a fraction is called as _____
    a) Access rate
    b) Success rate
    c**) Hit rate**
    d) Miss rate

92. In memory-mapped I/O _____
    **a) The I/O devices and the memory share the same address space**.
    b) The I/O devices have a separate address space
    c) The memory and I/O devices have an associated address space
    d) A part of the memory is specifically set aside for the I/O operation

93. The advantage of I/O mapped devices to memory mapped is _____
    a) **The former offers faster transfer of data**
    b) The devices connected using I/O mapping have a bigger buffer space
    c) The devices have to deal with fewer address lines
    d) No advantage as such

94. The method of accessing the I/O devices by repeatedly checking the status flags is _____
    a) **Program-controlled I/O**
    b) Memory-mapped I/O
    c) I/O mapped
    d) None of the mentioned

95. The method which offers higher speeds of I/O transfers is _____
    a) Interrupts
    b) Memory mapping
    c) Program-controlled I/O
    d**) DM**A

96. The process wherein the processor constantly checks the status flags is called as _____
    **a) Polling**
    b) Inspection
    c) Reviewing
    d) Echoing



97. The signal sent to the device from the processor to the device after receiving an interrupt is _____
    **a)** Interrupt-acknowledge
    b) Return signal
    c) Service signal
    d) Permission signal

98. An interrupt that can be temporarily ignored is _____
    a) Vectored interrupt
    b) Non-maskable interrupt
    **c) Maskable interrupt**
    d) High priority interrupt

99. The interrupt servicing mechanism in which the requesting device identifies itself to the processor to be serviced is _____
    a) Polling
    **b) Vectored interrupts**
    c) Interrupt nesting
    d) Simultaneous requesting

100. _____ method is used to establish priority by serially connecting all devices that request an interrupt.
a) Vectored-interrupting
b) **Daisy chain**
c) Priority
d) Polling

101. In daisy chaining device 0 will pass the signal only if it has _____
a) Interrupt request
**b) No interrupt request**
c) Both No interrupt and Interrupt request
d) None of the mentioned

102. The DMA transfers are performed by a control circuit called as _____
a) Device interface
**b) DMA controller**
c) Data controller
d) Overlooker

103. After the completion of the DMA transfer, the processor is notified by _____
**a) Acknowledge signal**
b) Interrupt signal
c) WMFC signal
d) None of the mentioned

104. The DMA controller has _____ registers.
a) 4
b) 2
**c) 3**
d) 1

105. The technique whereby the DMA controller steals the access cycles of the processor to operate is called _____
a) Fast conning
b) Memory Con
**c) Cycle stealing**
d) Memory stealing

106. The technique where the controller is given complete access to main memory is _____
a) Cycle stealing
b) Memory stealing

c) Memory Con
d**) Burst mode**

107. The DMA transfer is initiated by _____
a) **Processor**
b) The process being executed
c) I/O devices
d) OS

CPU

With DMA, the CPU first initiates the transfer, then it does other operations while the transfer is in progress,

108. When the process requests for a DMA transfer?
a) Then the process is temporarily suspended
b) The process continues execution
c) Another process gets executed
d) process is temporarily suspended & Another process gets executed



109. The fastest data access is provided using _____
a) Caches
b) DRAM's
c) SRAM's
**d) Registers**

110. The effectiveness of the cache memory is based on the property of _____
**a) Locality of reference**
b) Memory localisation
c) Memory size
d) None of the mentioned

111. The temporal aspect of the locality of reference means _____
a) That the recently executed instruction won't be executed soon
b) That the recently executed instruction is temporarily not referenced
**c)** That the recently executed instruction will be executed soon again
d) None of the mentioned

112. The spatial aspect of the locality of reference means _____
a) That the recently executed instruction is executed again next
b) That the recently executed won't be executed again
c) That the instruction executed will be executed at a later time

**d)** That the instruction in close proximity of the instruction executed will be executed in future

113. The correspondence between the main memory blocks and those in the cache is given by _____
a) Hash function
**b) Mapping function**
c) Locale function
d) Assign function

114. The algorithm to remove and place new contents into the cache is called _____
**a) Re**placement algorithm
b) Renewal algorithm
c) Updation
d) None of the mentioned

115. The write-through procedure is used _____
a) To write onto the memory directly
b) To write and read from memory simultaneously
**c)** To write directly on the memory and the cache simultaneously
d) None of the mentioned



116. In associative mapping, in a 16 bit system the tag field has _____ bits.
**a) 12**
b) 8
c) 9
d) 10

117. The technique of searching for a block by going through all the tags is _____
a) Linear search
b) Binary search
**c) Associative search**
d) None of the mentioned

118. What does MAR stand for?
a) Main Address Register
**b) Memory Access Register**
c) Main Accessible Register
d) Memory Address Register

119. A set of microinstructions for a single machine instruction is called _____
a) Program
b) Command

**c) Micro program**
d) Micro command

120. Which of the following holds the last instruction fetched?

a) Program
**b) In**struction Register
c) Micro program
d) Micro command

121. Microprograms are usually stored in _____
**a)** ROM
b) RAM
c) SAN
d) Main memory

122. Which control unit is implemented as combinational circuit in the hardware_
a) Micro Programmed control unit
**b) H**ardwired control unit
c) Macro Programmed control unit
d) Block programmed control unit



123. Among them which are faster control unit_
a) Micro Programmed control unit
**b) H**ardwired control unit
c) Both a and b
d) none of these

124. For CISC architecture _____controllers are better:
**a)** Micro Programmed
b) Hardwired
c) Both a and b
d) none of these

125. Which is a type of microprocessor that is designed with limited number of instructions_
a) CPU
**b) RISC**
c) CISC
d) MUX

126. In the case of, Zero-address instruction method the operands are stored in _____
a) Registers

b) Accumulators
c) Push down stack
d) Cache

127. The addressing mode, where you directly specify the operand value is _____
a) Immediate
b) Direct
c) Definite
d) Relative

128. Which of the following refers to the instructions like MOV or ADD?
a) **OPcode**
b) Oprand
c) Command
d) instructions

129. What is the Von Neumann architecture?
**a) SISD**
b) SIMD
c) MIMD
d) MISD



1. Why do we need concurrent processing for describing digital systems in HDLs?
a) Faster processing than conventional programming languages
b) Concurrent processing is easier than sequential processing
c) It allows taking timing constraints into consideration
**d) Complexity of digital systems needs concurrent processing**

2. Which of the following is the basic building block of a design?
a) Architecture
**b**) Entity
c) Process
d) Package

3. Complete description of the circuit to be designed is given in _____
**a**) **Architecture**
b) Entity
c) Library
d) Configurations

4. Which of the following describes the structure of VHDL code correctly?
**a**) Library Declaration; Entity Declaration; Architecture Declaration; Configurations

b) Entity Declaration; Configuration; Library Declaration; Architecture Declaration
c) Configuration; Library Declaration; Entity Declaration; Architecture Declaration
d) Library Declaration; Configuration; Entity Declaration; Architecture Declaration

5. Which of the following is used at the end of a statement?
**a)** ; (Semicolon)
b) — ( double hyphen)
c) _ (underscore)
d) No sign is used at the end of statement

6. Which of the following is not defined by the entity?
a) Direction of any signal
b) Names of signal
c) Different ports
**d)** Behavior of the signals

7. Which of the following can be the name of an entity?
a) NAND
**b**) Nand_gate
c) Nand gate
d) AND



8. Refer to the VHDL code given below, how many input-output pins are there in MUX entity?

```
ENTITY mux IS
Port ( a,b : IN STD_LOGIC;
Y : OUT STD_LOGIC);
END mux;
```

a) 5
b) 4
c) 3
d) 2

9. What is the difference between OUT and BUFFER?
a) BUFFER can't be used inside the entity for reading the value and OUT can be
b) BUFFER can only be read whereas OUT can only be assigned a value
**c) BUFFER can be read as well as assigned a value but OUT can only be assigned**
d) Both are same

10. What does the architecture of an entity define?
    a) External interface
    **b)** Internal functionality
    c) Ports of the entity
    d) Specifications

11. In real time operating system _____
    a) all processes have the same priority
    **b) a task must be serviced by its deadline period**
    c) process scheduling can be done only once
    d) kernel is not required

12. Hard real time operating system has _____ jitter than a soft real time operating system.
    **a)** less
    b) more
    c) equal
    d) none of the mentioned

13. For real time operating systems, interrupt latency should be _____
    **a)** minimal
    b) maximum
    c) zero
    d) dependent on the scheduling



14. Which one of the following is a real time operating system?
    a) RTLinux
    b) VxWorks
    c) Windows CE
    **d)** All of the mentioned

15. In a real time system the computer results _____
    **a**) must be produced within a specific deadline period
    b) may be produced at any time
    c) may be correct
    d) all of the mentioned

16. To schedule the processes, they are considered _____
    a) infinitely long
    **b**) periodic
    c) heavy weight
    d) light weight

17. How an embedded system communicate with the outside world?
    a) Memory
    b) Output
    c) **Peripherals**
    d) Input

18. . Which of the following statements are true for von Neumann architecture?
    a) separate bus between the program memory and data memory
    b) external bus for program memory and data memory
    c) external bus for data memory only
    **d) shared bus between the program memory and data memory**

19. What is approximate data access time of SRAM?
    a) 2ns
    b) 10ns
    c) 60ns
    **d) 4ns**