Study of ADC and DAC circuits using Sample and Hold

Biswaranjan Meher
Integrated M.Sc.
Roll No.-2011050
School of Physical Sciences
National Institute of Science Education and Research, Bhubaneswar
(Dated: February 13, 2023)

In the previous experiment, we constructed ADC and DAC circuits using an R-2R ladder with various ICs and verified their working. In this experiment, we use a dedicated 8-bit ADC IC for analog-to-digital conversion and similarly an 8-bit DAC IC for digital-to-analog conversion. We use sample and hold in this experiment before the ADC circuit which is an integral part of an ADC circuit. We verified all the parts of the circuit and then try to recreate the input signal as output. We then checked the output for various input frequencies keeping the clock rate constant (but the sampling rate with respect to the input signal was varying).

I. OBJECTIVES

- To observe the sample and hold output and learn the importance of sample and sampling frequency which is provided by the clock
- To reproduce the input signal which is input to the ADC with the complete ADC-DAC circuit at the output of the trans-impedance amplifier.
- Determine the minimum ratio of sampling frequency to the frequency of the input sine wave signal for reproducing chosen frequency of the input sine wave signal.

II. THEORY

A. Sampling

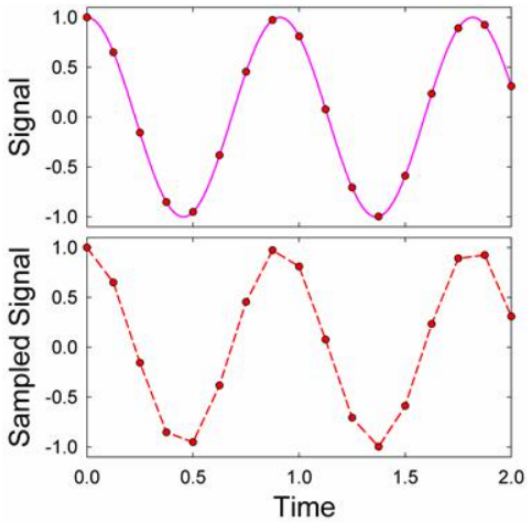


FIG. 1. Sampling of an input signal
https://instrumentationlab.berkeley.edu/Lab10

Let, the curve in the upper plot of the graph in FIG.1. represents a signal to be sampled. The dots represent the samples. If we then use the samples to represent the signal, we get an approximate signal in the lower plot, where the points are joined by the dashed line.
Sampling always approximates the signal. The accuracy of the sampled signal is limited by resolution (number of bits) and sampling rate.

B. Components used in the circuit

1. *Sample and Hold circuit*

This circuit is constructed using the LF398 IC. It is used to sample the input signal and hold it until it is converted to digital format. It works in the following manner:

- Sample mode captures the signal at a given instant of time.
- Hold mode holds the signal captured.

Every sample and hold circuit has a sampling rate associated with it. In this case, this sampling rate is given by a clock provided to the circuit using the function generator. The output signal depends primarily on this sampling rate.

2. *ADC circuit*

It is constructed with ADC0804 IC, which is an 8-bit successive approximation ADC converter. It also has an internal clock to give a clock pulse to the sample and hold circuit but we do not use it in this experiment due to noise in the clock pulse signal.

3. DAC circuit

It is constructed using DAC0808 IC, it is an 8 bit DAC chip with R-2R ladder. It comes in two different packages and we use DIP (dual in-line package) for this experiment. The output of this IC is given by the equation:

$$Io = K\left(\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{128}+\frac{A_8}{256}\right) \quad (1)$$

where K = $\frac{V_{ref}}{R}$
In our experimental observation,
V_{ref}= 5.04 V and $R = 4.7k\Omega$

4. Transimpedance amplifier

It is constructed using 741 IC. Its main purpose is to convert the current coming from DAC output to voltage output.
All the components are connected as shown in FIG.2 and 3.

III. EXPERIMENTAL SETUP

A. Circuit

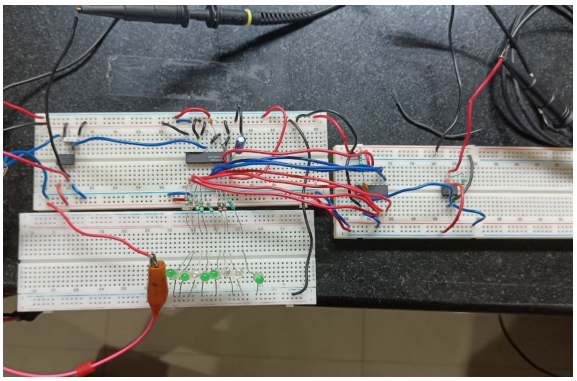


FIG. 3. Circuit to perform the experiment

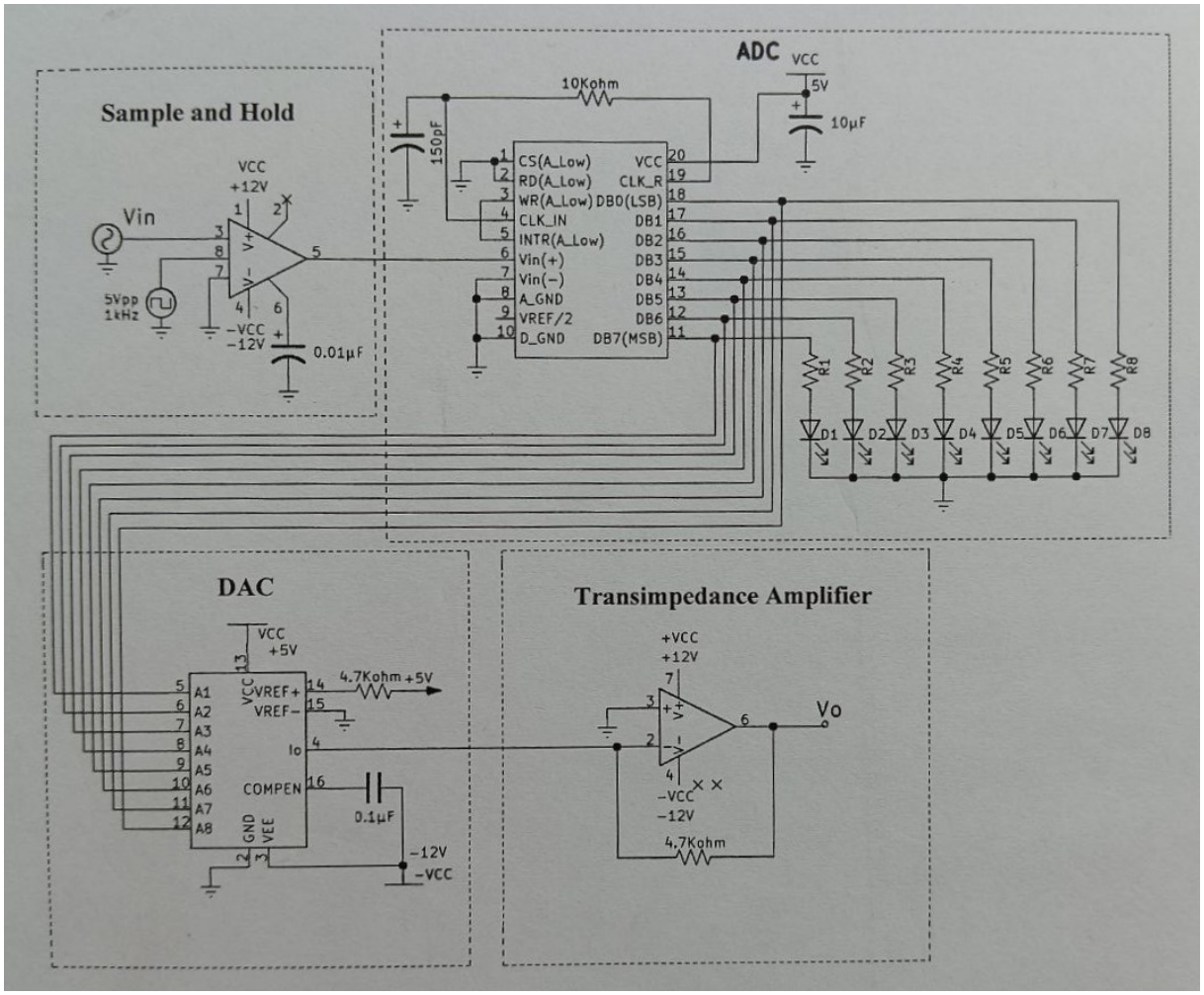


FIG. 2. Circuit diagram

Components required :

- LF398 IC (for sample and hold)
- ADC0804 IC (for converting analog signal to digital signal)
- DAC0808 IC (converting digital signal to analog signal in the form of current output)
- IC 741 (trans-impedance amplifier to convert current to voltage output)
- Resistors, capacitors, LEDs, cables, breadboards, connecting wires, etc.

Instruments required : DC power supply, Function generators, and Oscilloscope.

IV. OBSERVATIONS AND DATA

A. Sample and hold

Here we choose the sampling frequency as 5 Volt V_{p-p} 1 kHz square wave and signal frequency as 100 Hz sine wave. We observe the following output via an oscilloscope.

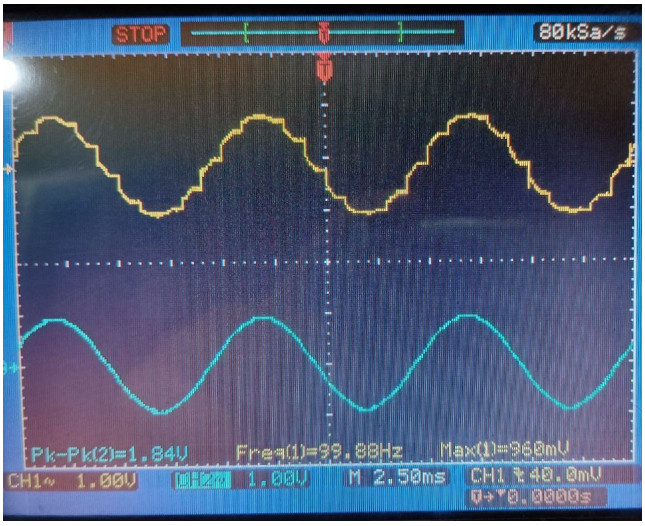


FIG. 4. Output of the sample and hold circuit for a given input sign signal

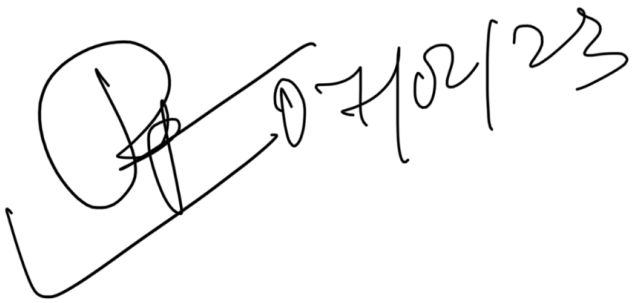
Here, the lower signal represents the input sine wave signal and the upper signal represents the sampled signal.

B. ADC and DAC circuits

Table 1: Data for verification of ADC and DAC circuits

ADC Verification									
Input Voltage	D1	D2	D3	D4	D5	D6	D7	D8	Theoretical
1	0	0	1	1	0	0	0	0	0.9375
2	0	1	1	0	0	0	1	0	1.875
3	1	0	0	1	0	0	0	0	2.8125
4	1	1	0	0	0	1	0	1	3.85
5	1	1	1	1	1	1	1	1	5

DAC Verification		
Digital Input	Analog output(calculated)	Analog Output(observed)
10000000	2.52	2.536
11000000	3.78	3.803
11100000	4.41	4.43
11110000	4.725	4.74
11111000	4.88	4.9
11111100	4.96	4.98
11111110	5	5.02
11111111	5.02	5.04
1	0.01968	0.0198



Following the observation in table 1, we can observe that the observed values of the analog input in the ADC circuit suffice the theoretically calculated values. Also, the observed values of the analog output in the DAC circuit suffice the theoretically calculated values.

C. Final output

After all the verification was done, we assembled all the circuit components and studied the various outputs by varying the frequency of the input signal with the clock pulse remaining constant.
Please refer to the next page for the observation.

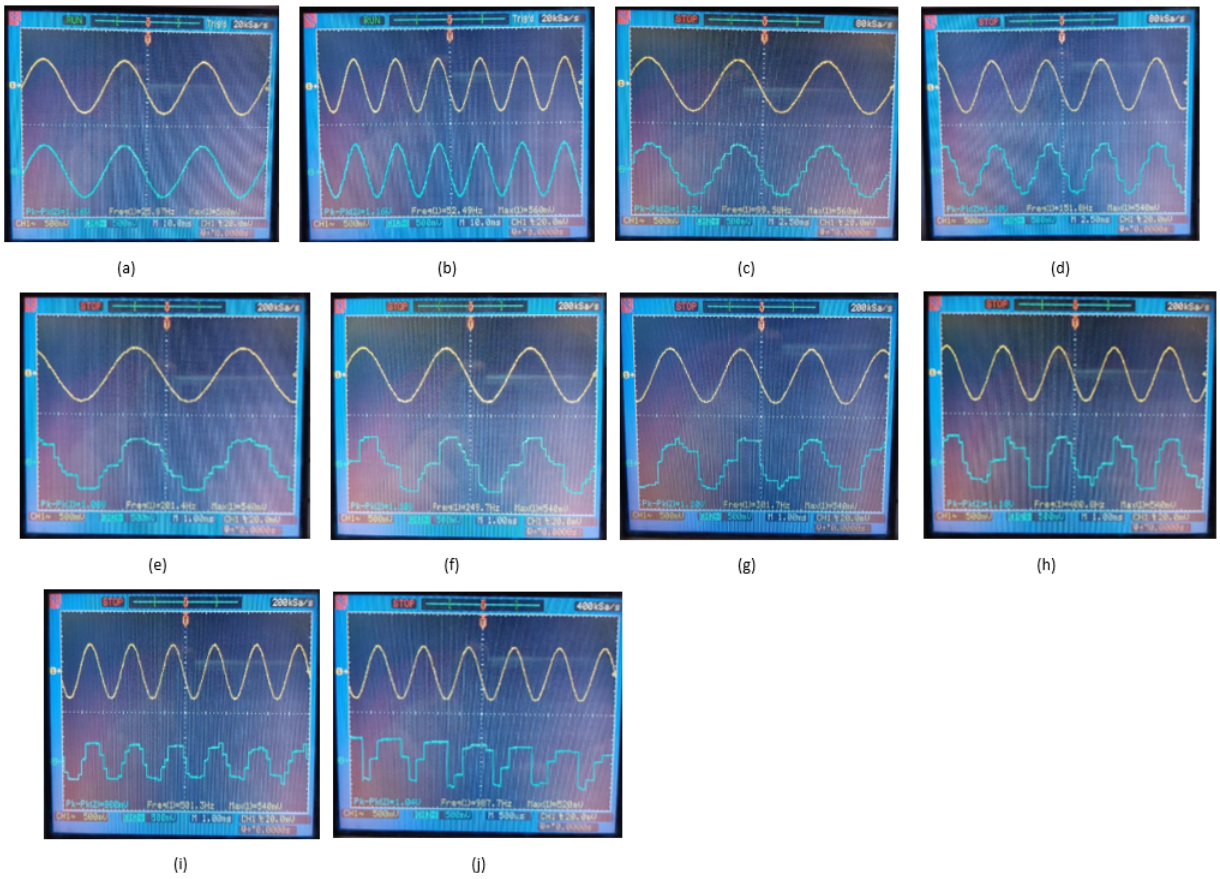


FIG. 5. The sampled signal (lower signal) vs the input signal (upper signal) for the following frequencies of the input signal. (a) f= 25.97Hz, (b) f= 52.49Hz, (c) f= 99.5Hz, (d) f= 151.8Hz, (e) f= 201.4Hz, (f) f= 249.7Hz, (g) f= 301.7Hz, (h) f= 400Hz, (i) f= 501.5Hz, (j) f= 1kHz

V. CONCLUSIONS

- We verified the individual circuit components and studied how the sampling rate impacts the output of the circuit. Then, we obtained the whole output by assembling all the circuit components and tried recreating the output the same as the input.

- While verifying the DAC circuit, the maximum voltage was 5 V and the minimum voltage we got was 19.8 mV which matches the theoretical expectation (the value of one bit was approximately 19.6 mV.

- After assembling all the components we gave an input sinusoidal signal with different frequencies and obtained the corresponding outputs. We get better sampling when $\frac{fclock}{fsig} \geq 3$, which we refer to as "SAMPLING IS GOOD". Otherwise, at higher input frequencies, the output gets heavily distorted and hence we call it here as "SAMPLING IS BAD".

VI. SOURCES OF ERRORS AND PRECAUTIONS

- Always use good quality capacitors such as mica, polystyrene, or polypropylene dielectric in the sample and hold circuit. Avoid using ceramic capacitors.

- Loose connections should be avoided.

- Analog values of the voltages have an error bar corresponding to the least count of the Digital multimeter, which is negligible to consider.

VII. REFERENCES

- NISER Lab Manual

- `https://electronicscoach.com/sample-and-hold-circuit.html`

- `https://electronicsdesk.com/sample-and-hold-circuit.html`