Atmel SMART SAM L21
Product Highlights

Ultra Low Power
Cortex-M0+ based Microcontroller

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Outline

- Introduction
- System Architecture
- Power Supply
- Clocks
- Low Power Features
- New and Enhanced Peripherals
- Ecosystem

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Introduction

SAM L21 Product Positioning

- Targeted for Battery powered applications
- Industries first Ultra Low Power Large Flash and SRAM Cortex-M0+
- Designed with emphasis on
  - Low active mode power consumption
  - Smart Low power peripherals
  - Industry leading RAM retention numbers
- Leveraging two decades of Atmel Ultra Low power ARM, AVR and AVR32 know how
- Pin compatible to existing SAM D families

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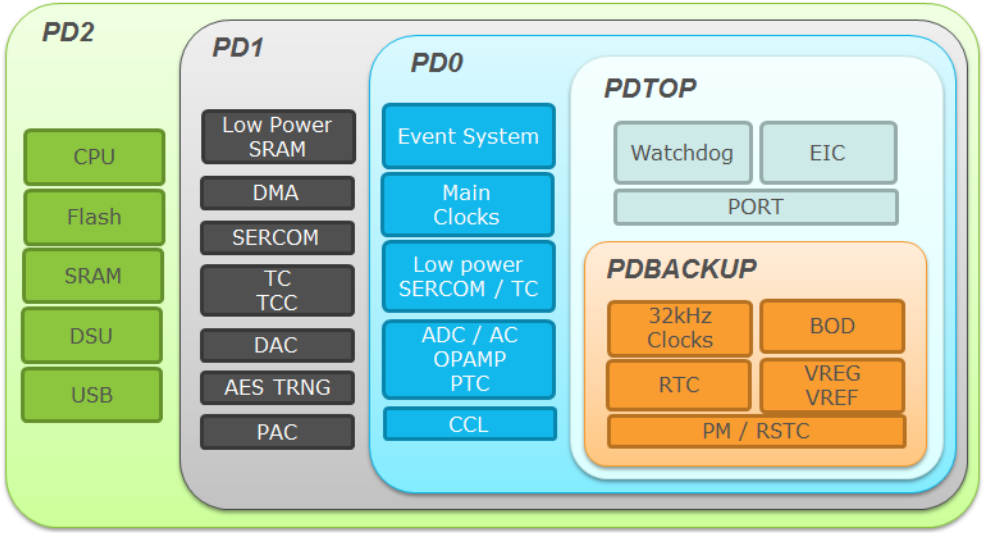
Introduction

SAM L21 Design Methodology for picoPower Devices

- Regulators & Oscillators
  - Multiple power sources and clocking options
- Multiple Domains
  - Power & Clock gating
- picoPower peripherals
- Low Power Analog
- Flexible Sleep Modes
  - Scale performance vs. power consumption
- Event System and Sleepwalking
- Ultra Low Power Process

Overview of SAM L21 Power Domains



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Introduction

SAM L21 Series

Flash / SRAM / LP SRAM	Sub-Series		
256KB / 32KB / 8KB	SAM L21E 3x 16b T/C 4x SERCOM 10-ch ADC 2-ch DAC 2x An.comp	SAM L21G 3x 16b T/C 6x SERCOM 14-ch ADC 2-ch DAC 2x An.comp	SAM L21J 5x 16b T/C 6x SERCOM 20-ch ADC 2-ch DAC 2x An.comp
128KB / 16KB / 8KB			
64KB / 8KB / 4KB			
32KB / 4KB / 2KB			
Package	32-pin QFN and TQFP	48-pin QFN and TQFP	64-pin QFN, TQFP and WLCSP

Main Features and Functions in all devices:

ARM Cortex M0+ CPU at 48 MHz, 1.62-3.6V operation, -40°C – 85°C temp grade
Ultra low power analog: 12-bit 1 Msps ADC, 12-bit DAC, 2 analog comparators, **3x op-amp**
Peripheral Touch Controller, 32-bit RTC with calendar mode, **AES, TRNG**
12-ch Event system, and 16-ch DMA controller with **next generation SleepWalking**
USB host/device, SERCOM supports USART, UART with autobaud,
SPI, I^2C up to 3.4MHz, PM/SMBus, IrDA
3 Timer/Counters for Control applications, **Ultra low power SERCOM and Timer/Counter**

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Introduction

SAM L21 / SAM D21 Products Comparison

Feature	SAM D20	SAM D21	SAM L21
CPU	48MHz CM0+	48MHz CM0+ with MTB	48MHz CM0+ with MTB
Memory	16-256KB Flash 4-32KB SRAM	32-256KB Flash 4-32KB SRAM	32-256KB Flash 4-32KB SRAM **2-8KB Low Power SRAM** **1-8KB Flash RWW**
Pin range	32 – 64 26 – 52 GPIO	32 – 64 **26 – 52 GPIO**	32 – 64 25 – 51 GPIO
Operating range	1.62 – 3.63V	1.62 – 3.63V	1.62 – 3.63V
Event System	8-ch	12-ch	12-ch
DMA	-	12-ch	**16-ch**
CRC	32-bit for memory	32-bit for memory 32-bit for peripherals 16-bit for peripherals	32-bit for memory 32-bit for peripherals 16-bit for peripherals
Analog	350ksps 12-bit ADC (20-ch) 350ksps 10-bit DAC (1-ch) 2x AC inputs	350ksps 12-bit ADC (20-ch) 350ksps 10-bit DAC (1-ch) 2x AC inputs	**1Msps 12-bit ADC** (20-ch) **1Msps 12-bit DAC (2-ch)** 4x AC inputs
Timer/counters	Up to 8x TC - 1x RTC	Up to 5x TC 3x TCC 1x RTC	Up to 5x TC 3x TCC 1x RTC
Communication	Up to 6x SERCOM	Up to 6x SERCOM 1x USB **1x I2S**	Up to 6x SERCOM 1x USB
Cryptography	-	-	**AES / TRNG**
PTC	Up to **256** channels	Up to **256** channels	Up to 169 channels
CCL	-	-	**Yes**

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Introduction

SAM L21 Cortex-M0+ Implementation

Features	Configurable Options	SAM L21 Implementation
Data endianness	Little-endian or big-endian	Little-endian
SysTick timer	Present or Absent	Present
Nb of Watchpoints	0,1, 2	2
Nb of Breakpoints	0,1, 2, 3, 4	4
Micro Trace Buffer (MTB)	Present or Absent	Present
Halting Debug Support	Present or Absent	Present
Multiplier	Fast or Small	Fast (Single cycle)
Single-cycle I/O port	Present or Absent	Present
Vector Table Offset Register	Present or Absent	Present
Unprivileged/Privileged support	Present or Absent	Absent (All SW run in Privileged mode only)
MPU	Not present or 8-region	Not present
NMI support	Present or Absent	Present

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System Architecture

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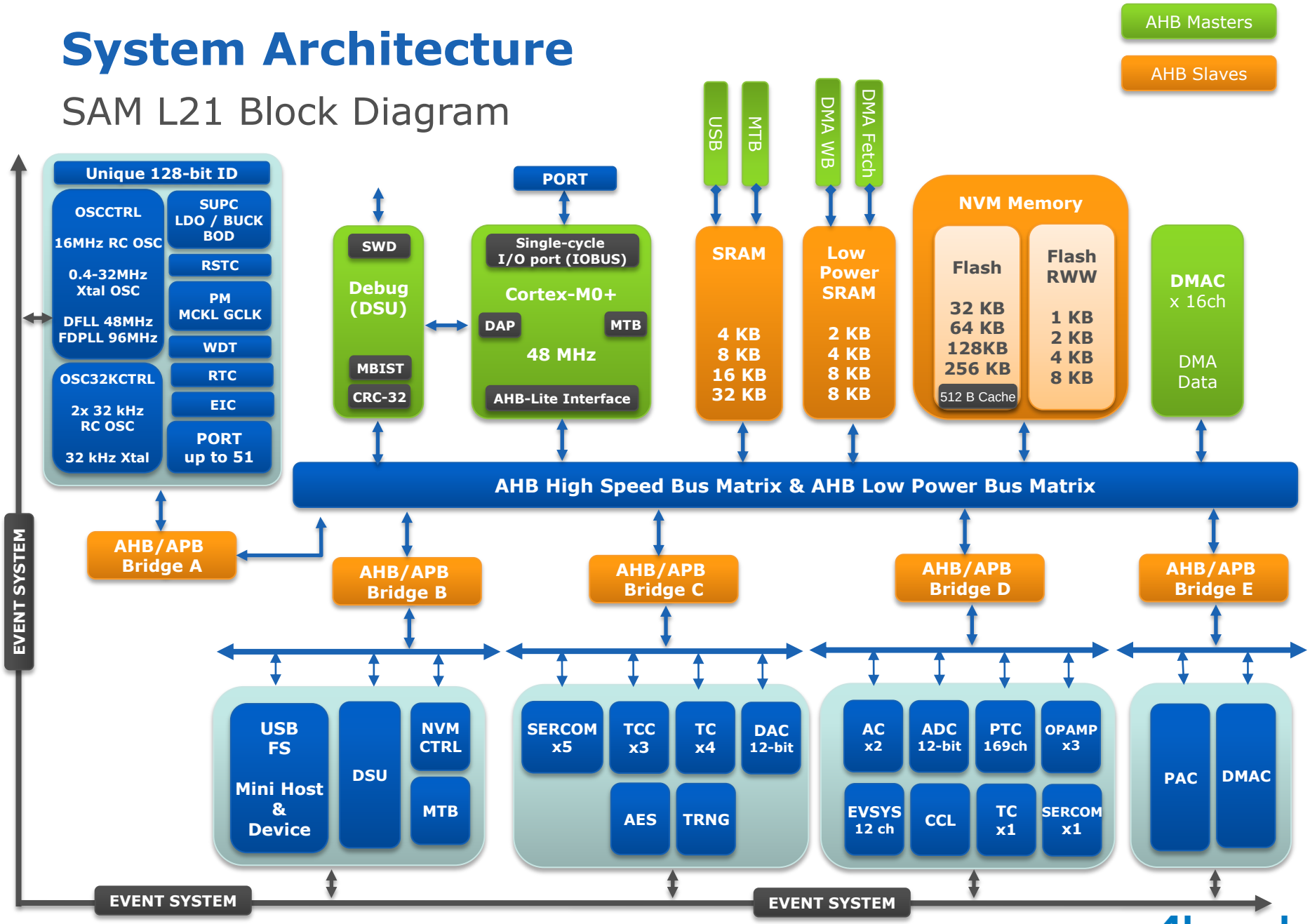
System Architecture

SAM L21 Block Diagram



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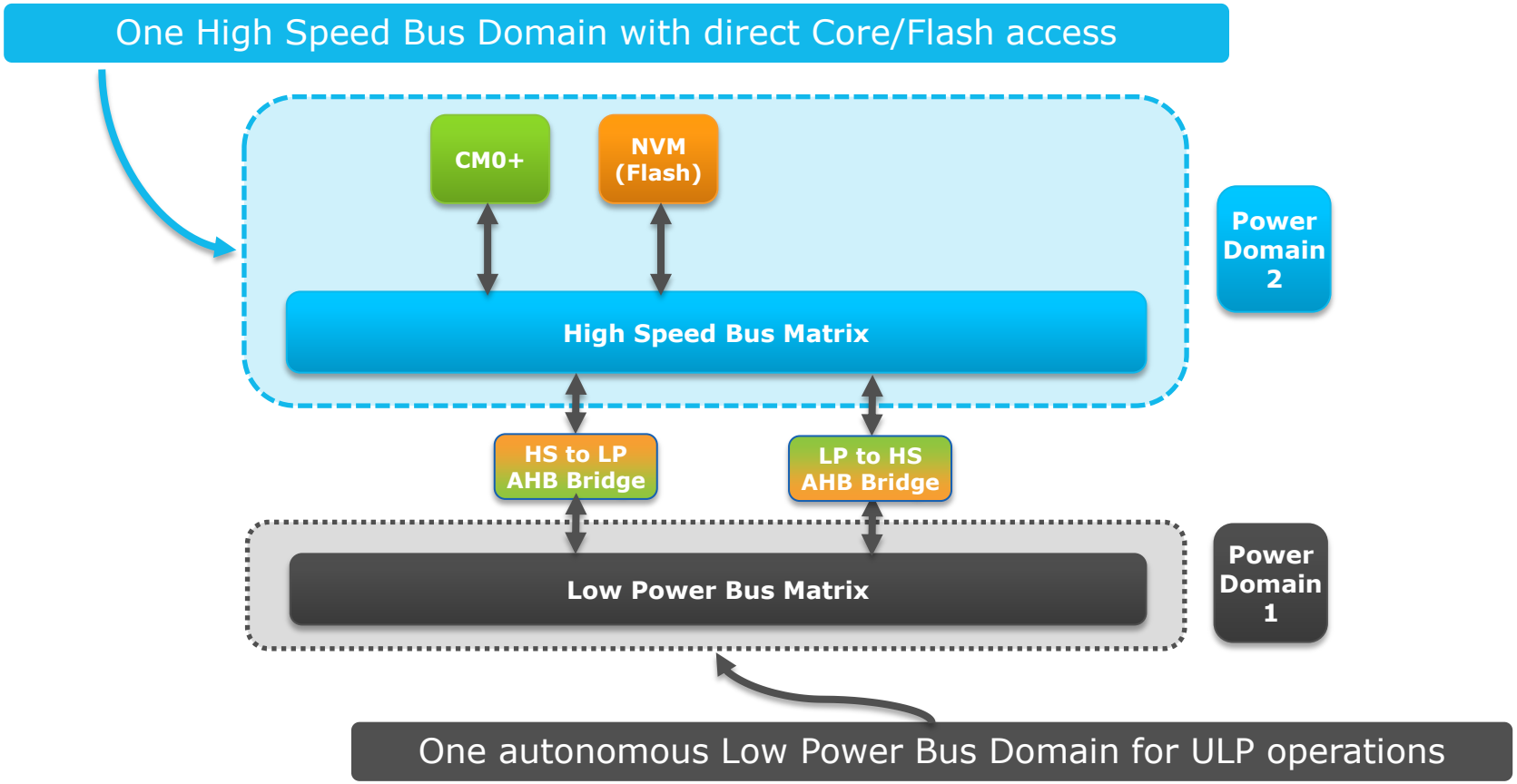
System Architecture

Bus Matrix Architecture

- Two Bus Matrix on different power domains to optimize power consumption



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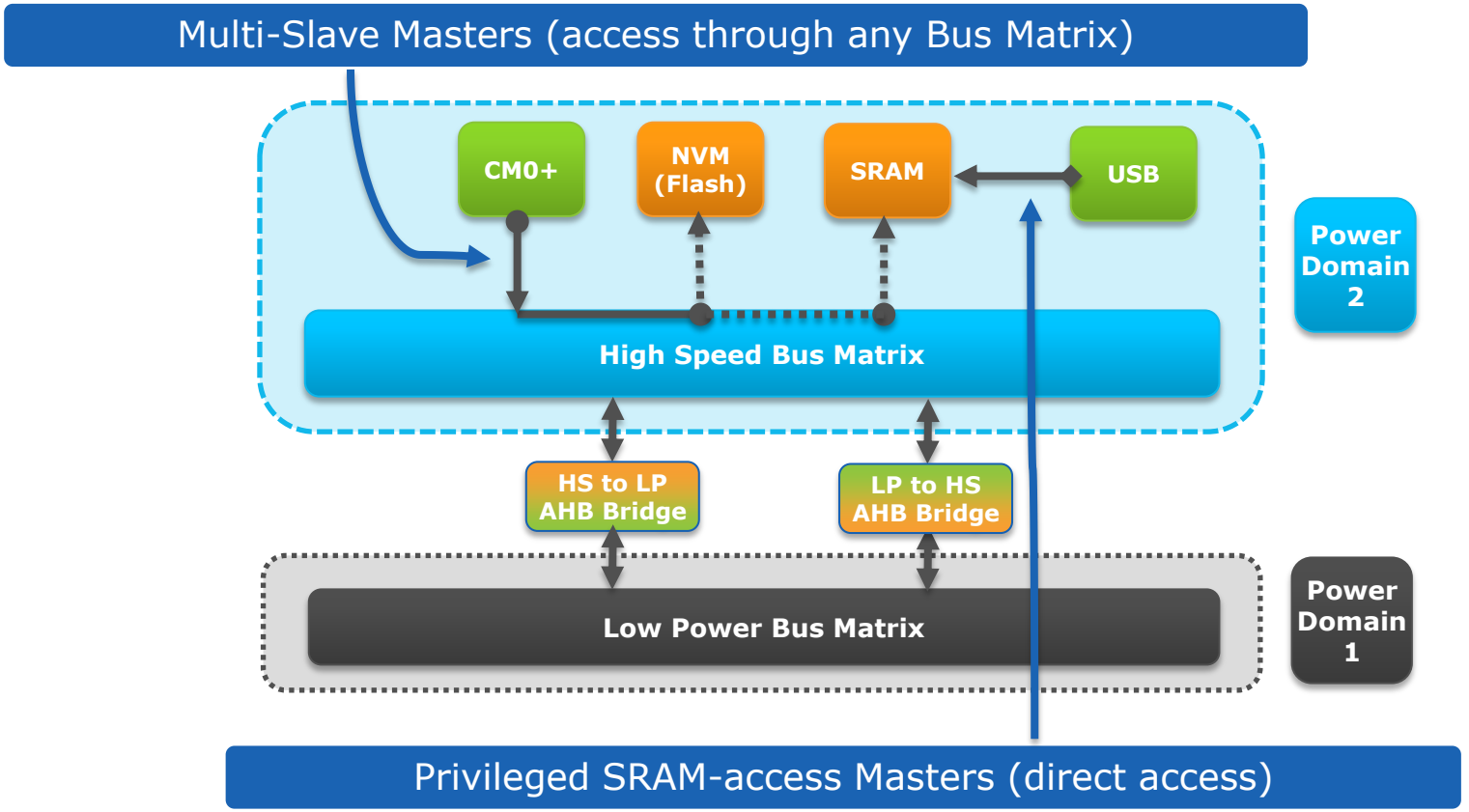
System Architecture

Masters/Slaves Connections

- Two different Master to Slave connections to optimize system bandwidth
  - Reduced latency using direct Master <-> SRAM access



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System Architecture

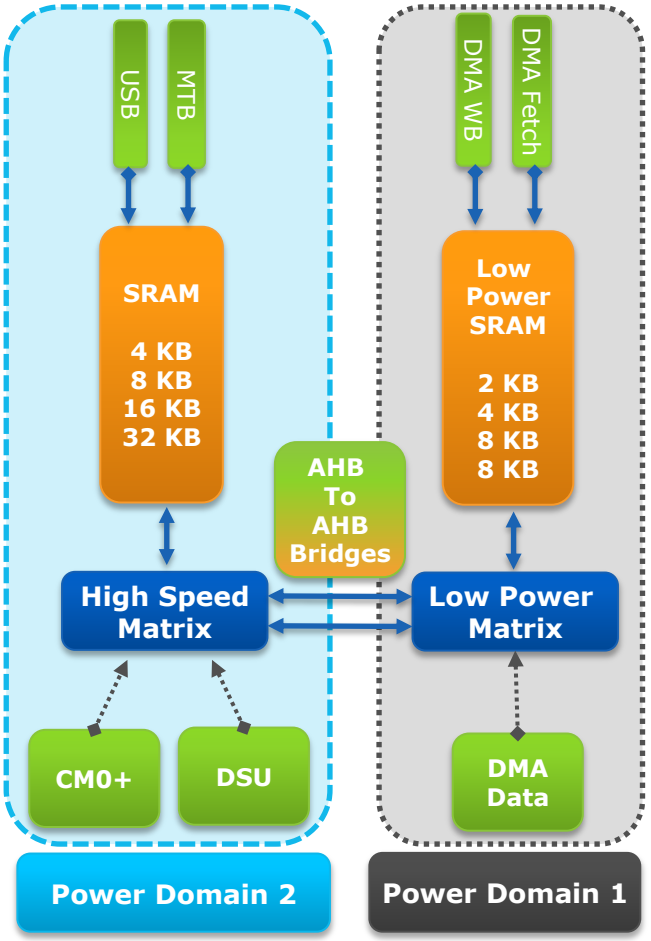
SRAM Memories

Memory	Start address
Embedded high-speed SRAM	0x20000000
Embedded low power SRAM	0x30000000

- Two distinct multi-port SRAM to optimize power consumption
  - System SRAM on High Speed Matrix
  - Low Power SRAM on Low Power Matrix
- SRAM port connection types

SRAM Port Connection	Connection Type	SRAM Type
Micro Trace Buffer (MTB)	Direct	SRAM
USB (Configuration & Data)	Direct	SRAM
DMAC Write Back access	Direct	Low Power SRAM
DMAC Fetch access	Direct	Low Power SRAM
Cortex M0+ Processor	Bus Matrix	Both(*)
DMAC Data access	Bus Matrix	Both(*)
Device Service Unit (DSU)	Bus Matrix	Both(*)

(*) Accesses may be done through the AHB to AHB bridges



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System Architecture

SRAM Quality of Service (QoS)

- SRAM QoS for each master accessing SRAM to manage priorities
  - Four levels for each configurable master

Value	Name	Description
00	DISABLE	Background (no sensitive operation)
01	LOW	Sensitive Bandwidth
10	MEDIUM	Sensitive Latency
11	HIGH	Critical Latency

  - SRAM port connection ID used in case two masters have same QoS level
    - The lowest ID, the highest priority

System SRAM Port Connection	Port ID	QoS Default Level	QoS Level Setting
Cortex M0+	0	3 - HIGH	Configurable
Device Service Unit (DSU)	1	2 - MEDIUM	Configurable
LP to HS AHB Bridge	2	2 - MEDIUM	Configurable
USB (Config, Data)	3	3 - HIGH	Configurable
Micro Trace Buffer (MTB)	4	3 - HIGH	Fixed

Low Power SRAM Port Connection	Port ID	QoS Default Level	QoS Level Setting
DMAC Data access	1	2 - MEDIUM	Configurable
HS to LP AHB Bridge	2	2 - MEDIUM	Configurable
DMAC Fetch access	3,4	2 - MEDIUM	Configurable
DMAC Write Back access	5,6	2 - MEDIUM	Configurable

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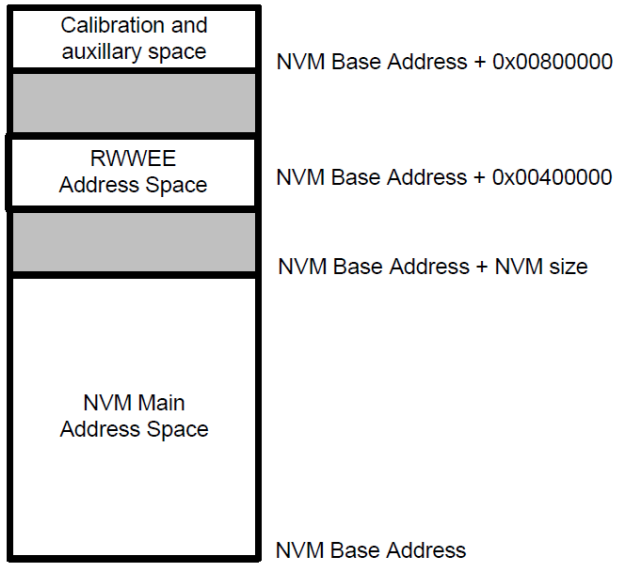
System Architecture

NVM Memory

Memory	Start address
Embedded Flash	0x00000000
Embedded WWR section	0x00400000

- Up to 256kB of Flash Memory (NVM main array)
  - Organized into 256-byte rows: one row ⇔ four pages
  - 512 bytes of direct-mapped cache
  - 16 Region Lock bits
  - Endurance: 25kcycles
- Up to 8kB of Flash RWW Memory (EEPROM emulation)
  - Can be programmed while reading the main array
  - Not cached / No lock bits
  - Endurance: 100kcycles
- Speed Characteristics
  - 0 WS @7,5MHz / 1 WS @12MHz (PL0)
  - 0 WS @25MHz / 1 WS @48MHz (PL2)
- Calibration & Auxiliary space
  - NVM SW Calibration Area (Read only)
  - NVM User Row (Read / Write)
- Security bit
  - Cleared by Chip Erase command (including Main array as Flash RWW)



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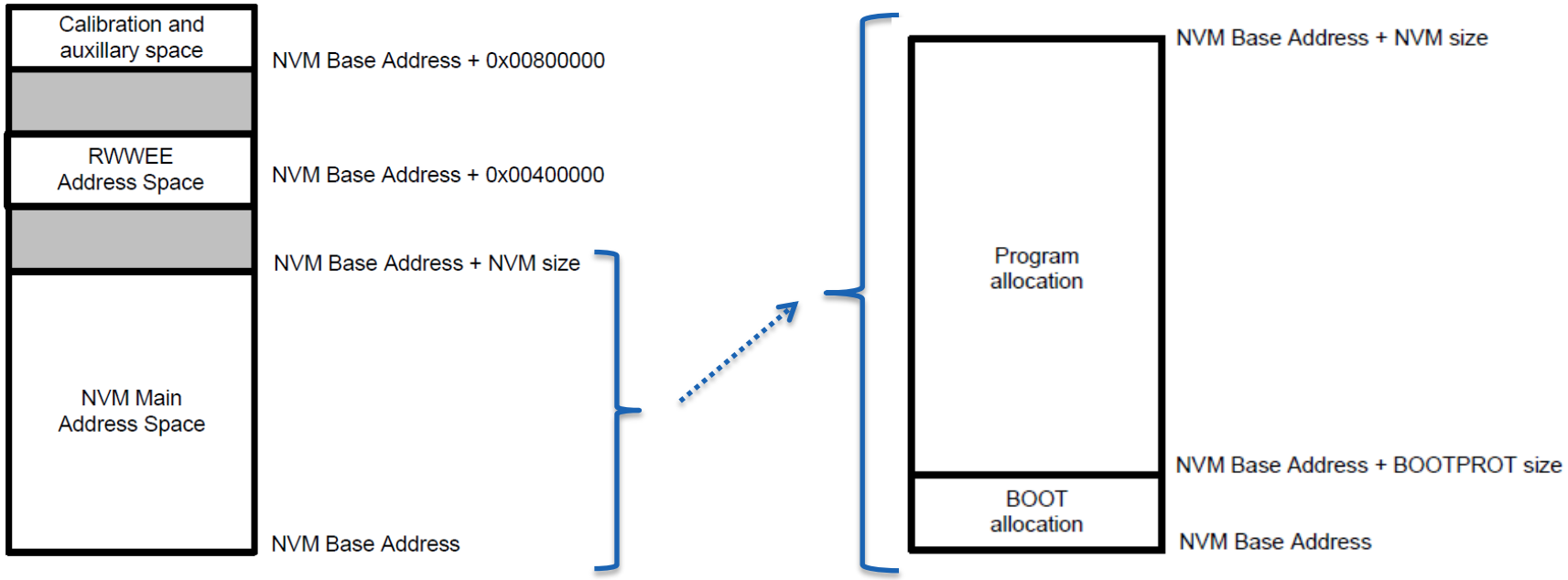
System Architecture

NVM Memory Organization

- For compatibility reasons with Atmel SAM D Series, a boot loader section can be allocated in the main array
  - BOOTPROT bit field from NVM User Row area



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Power Supply

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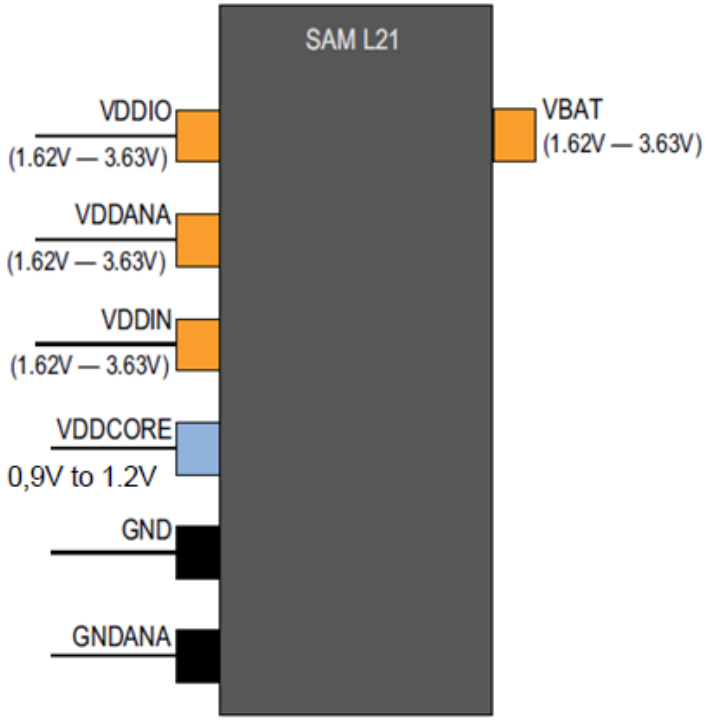
Power Supply

Power Supplies Pins

Power Supply	Voltage Range	Description
VDDIN	1.62V – 3.63V	Powers I/O lines, OSC16M and the Voltage Regulator
VDDIO	1.62V – 3.63V	Powers I/O lines and XOSC
VDDANA	1.62V – 3.63V	Powers I/O lines and analog peripherals
VDDCORE	0,9V – 1.2V	Voltage REG Output (Linear mode) Voltage REG Input (Switching mode) Powers the core, memories, peripherals and DFLL48M/FDPLL96M
VBAT	1.62V – 3.63V	External battery supply Input



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Power Supply

Power Supply Considerations

- VDDIN and VDDANA must have:
  - The same voltage
  - The same supply sequence
- VDDIO:
  - Independant from VDDIN/VDDANA supply sequence
  - Must be equal to VDDIN/VDDANA if PTC is used
    - Can be lower/equal if PTC is not used
  - Must be present before the application enables the 0.4-32 MHz oscillator (XOSC)
- No constraints on VBAT
  - Must be present when the application uses Battery Backup mode
- Check product datasheet for Min/Max rise time

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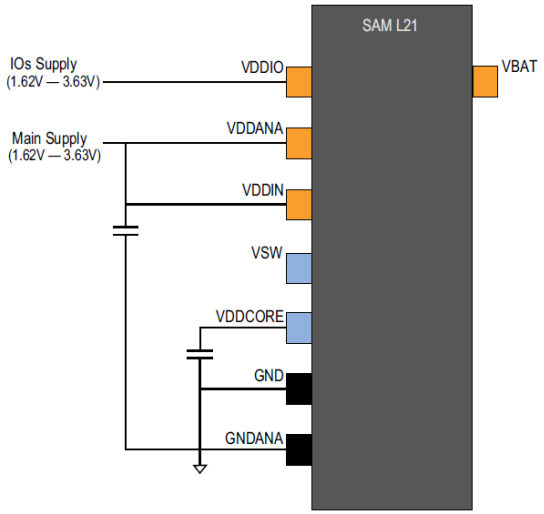
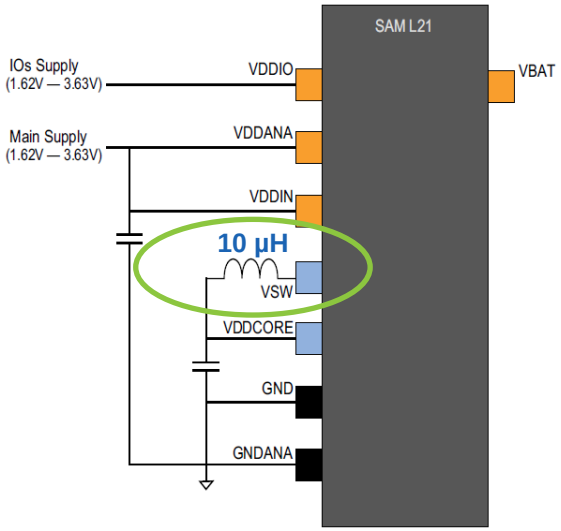
Power Supply

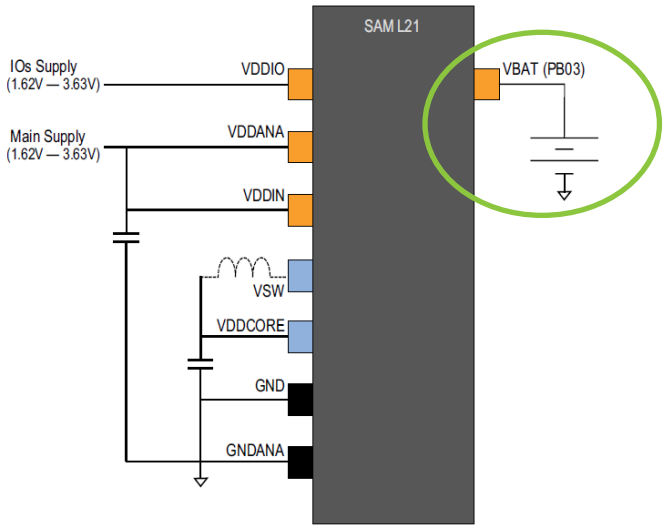
Power Supply Connection Schemes



Linear Mode Only



Switching / Linear Mode



Battery Backup Mode

- Switching/Linear Mode
  - Embedded Buck/LDO regulator supporting software on-the-fly selection
  - LDO selected by default after reset
- Battery Backup Mode support using VBAT power pin
  - Backup domain supplied by VDDIN after power up

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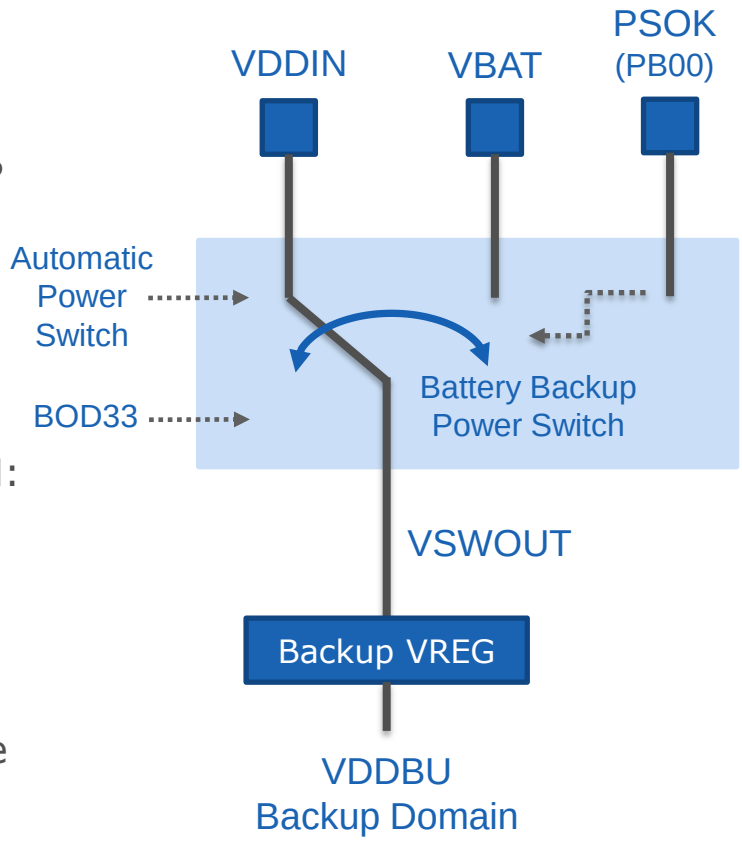
Power Supply

Battery Backup Power Switch (BBPS)

- Automatic switching between battery (VBAT) and main power (VDDIN) to increase battery lifetime
  - Backup domain can also be forced to VBAT
- Switch Backup domain to VBAT then enter BACKUP mode when VDDIN:
  - < 1,75 V (Automatic Power Switch event)
  - < BOD33 threshold (BOD33 event)
- Switch Backup domain to main power when VDDIN:
  - > 1,84 V (Automatic Power Switch event)
  - Is restored and if a low to high transition occurs on PSOK pin (Main Power Supply OK)
- Possibility to exit automatically from BACKUP mode once switched back on main power



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Clocks

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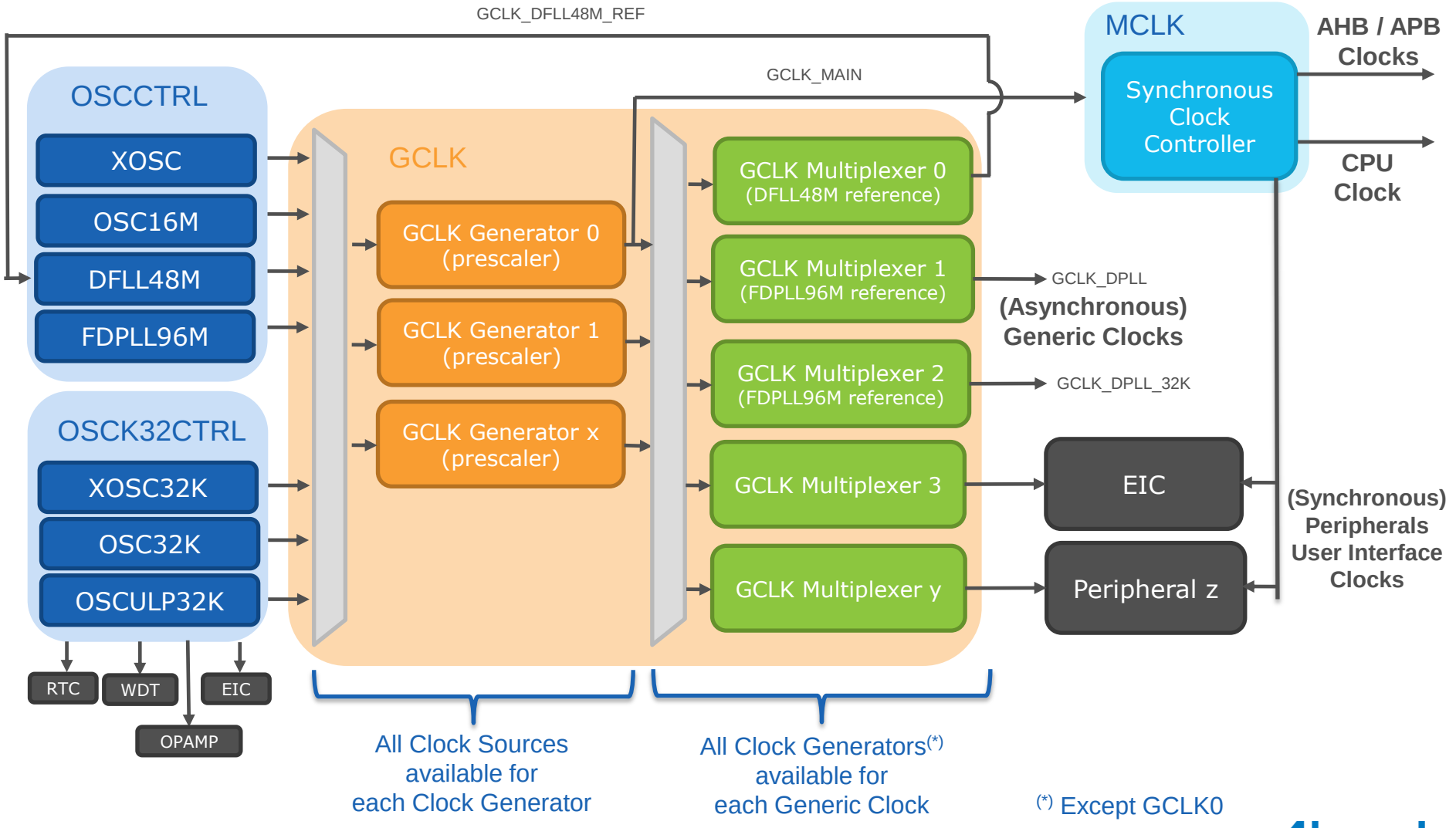
Clocks

Clocks Distribution



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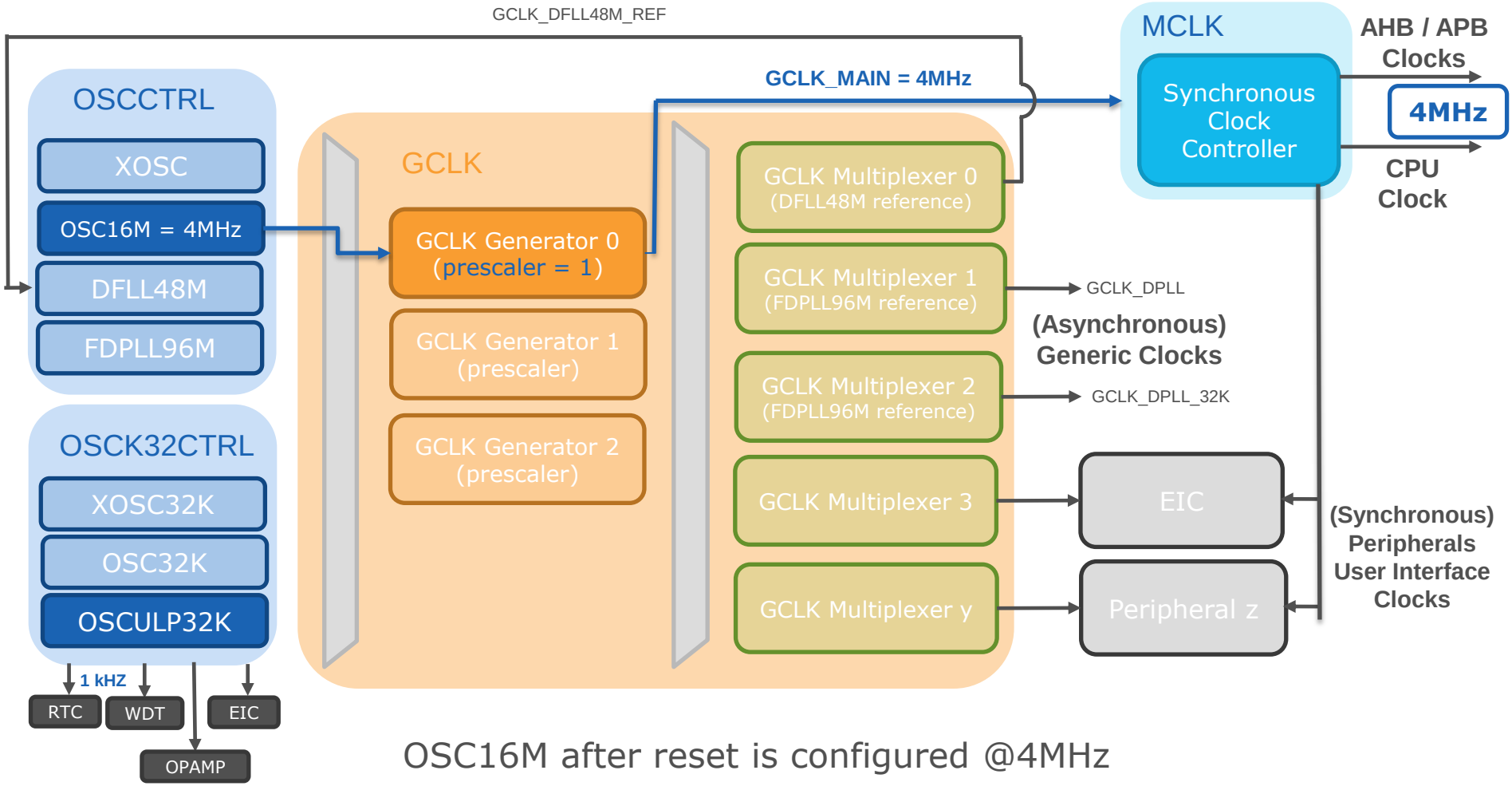
Clocks

Clocks after Power Reset



OSC16M after reset is configured @4MHz

OSCULP32K clocks RTC, WDT @1kHz

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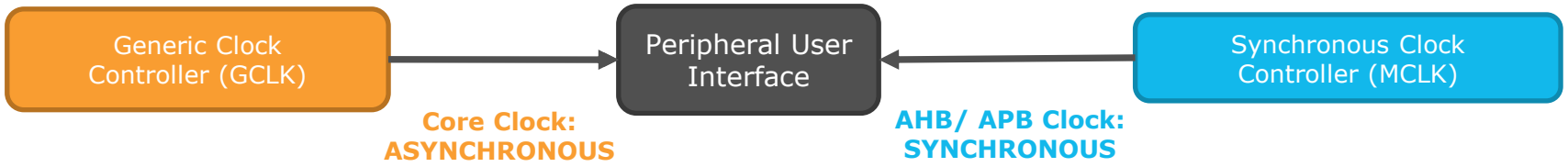
Clocks

Peripherals Synchronization

- Each peripheral has two clock domains
  - Synchronous clock for peripheral control
  - Asynchronous clock for peripheral core logic (can be kept active in sleep modes)



- One common synchronization scheme for all peripherals
  - Peripheral SYNCBUSY flag to check when required
  - Read/Write synchronization feature can be enabled for each concerned peripheral

- General Write Synchronization
  - SYNCBUSY bit will be cleared when write-synchronization is complete
  - A write to the same core register while synchronization is on going will be discarded and an error reported

- General Read Synchronization
  - Read value is reliable only when SYNCBUSY is cleared

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Low Power Techniques

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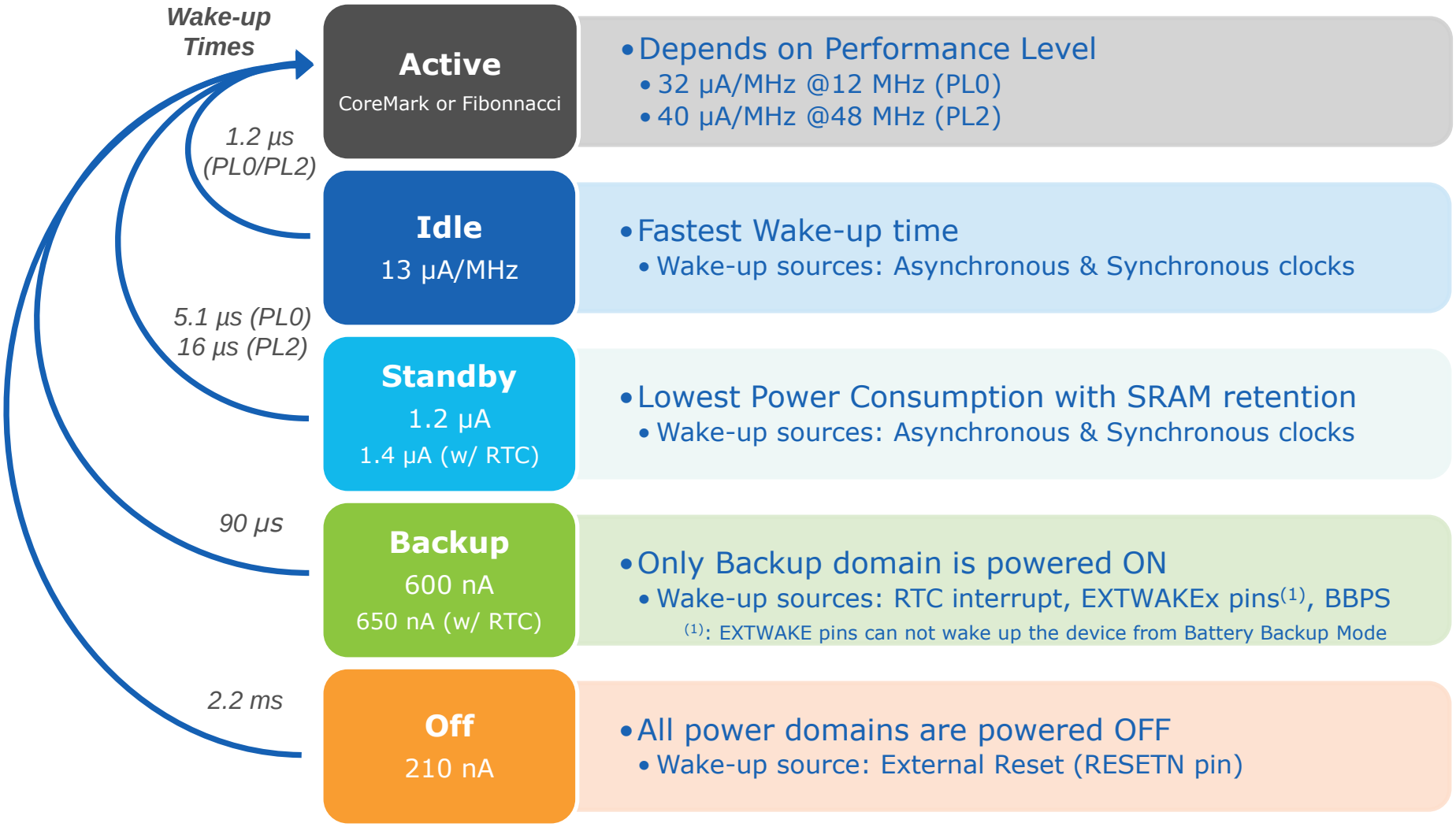
Low Power Techniques

SAM L21 Key Numbers (VDDIN=3,3V, T=25°C, BUCK mode)



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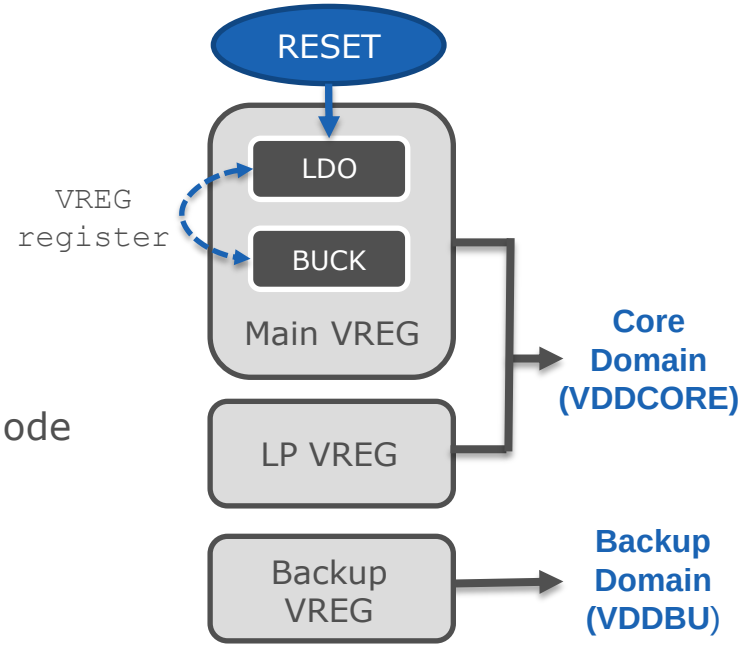
Low Power Techniques

Voltage Regulators

- SAM L21 embeds three voltage regulators
  - Main Regulator (VREG)
    - Powers Core domain by default
    - Two modes (LDO, Buck Converter)
  - Low Power Regulator (LP VREG)
    - Powers Core domain in STANDBY sleep mode
  - Backup Regulator (Backup VREG)
    - Powers Backup domain
    - Unique regulator in BACKUP sleep mode



- Main Regulator (VREG) modes can be selected on the fly by software
  - Linear mode (LDO)
    - Default mode after power up
  - Switching mode (BUCK)
    - The most efficient mode when the CPU and peripherals are running

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Low Power Techniques

Sleep Modes

- SAM L21 supports four sleep modes
  - IDLE
  - STANDBY: Main Regulator is OFF but may be automatically selected if required
  - BACKUP: only Backup domain is powered
  - OFF: all power domains are OFF except PORs and wake-up logic

	Clocks			Voltage Regulators			I/O Retention
Mode	**CPU clock**	**AHB/APB Clocks** (Synchronous)	**GCLK Clocks** (Asynchronous)	**Main Regulator Mode** (VREG)	**Low Power Regulator Mode** (LP VREG)	**Backup Regulator** (Backup VREG)	-
Active	Run	Run	Run	ON	ON	ON	Yes
Idle	Stopped	Stopped (1)	Run	ON	ON	ON	Yes
Standby	Stopped	Stopped (1)	Stopped (1)	OFF (2)	ON	ON	Yes
Backup	Stopped	Stopped	Stopped	OFF	OFF	ON	Yes (3)
Off	Stopped	Stopped	Stopped	OFF	OFF	OFF	No

(1): **Run** if requested by the peripheral in case of SleepWalking
(2): **ON** if requested in case of SleepWalking on GCLK or AHB/APB clocks
(3): I/Os configuration can be either released or stretched when exiting BACKUP mode

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Low Power Techniques

Performance Levels

- Two software-selectable performance levels to optimize active power consumption
  - PL0 is the mode by default after reset
  - PL0 has peripherals/clocks limitations
    - Listed in Power Level Overview section of product datasheet

- Based on Dynamic Voltage Scaling
  - Technique which adjusts regulator output voltage against operating frequency

Performance Level	VREG Mode	Max CPU Frequency	$I_{VDDIN=3,3V}$ (Coremark or Fibbonacci)
0	**BUCK**	**12 MHz** (1 WS)	**32 µA/MHz**
2		**48 MHz** (2 WS)	**40 µA/MHz**
0	LDO	12 MHz (1 WS)	79 µA/MHz
2		48 MHz (2 WS)	95 µA/MHz

- Voltage Scaling Control capability for smooth transitions when changing performance level
  - VDDCORE voltage can be changed step by step to avoid high peak current

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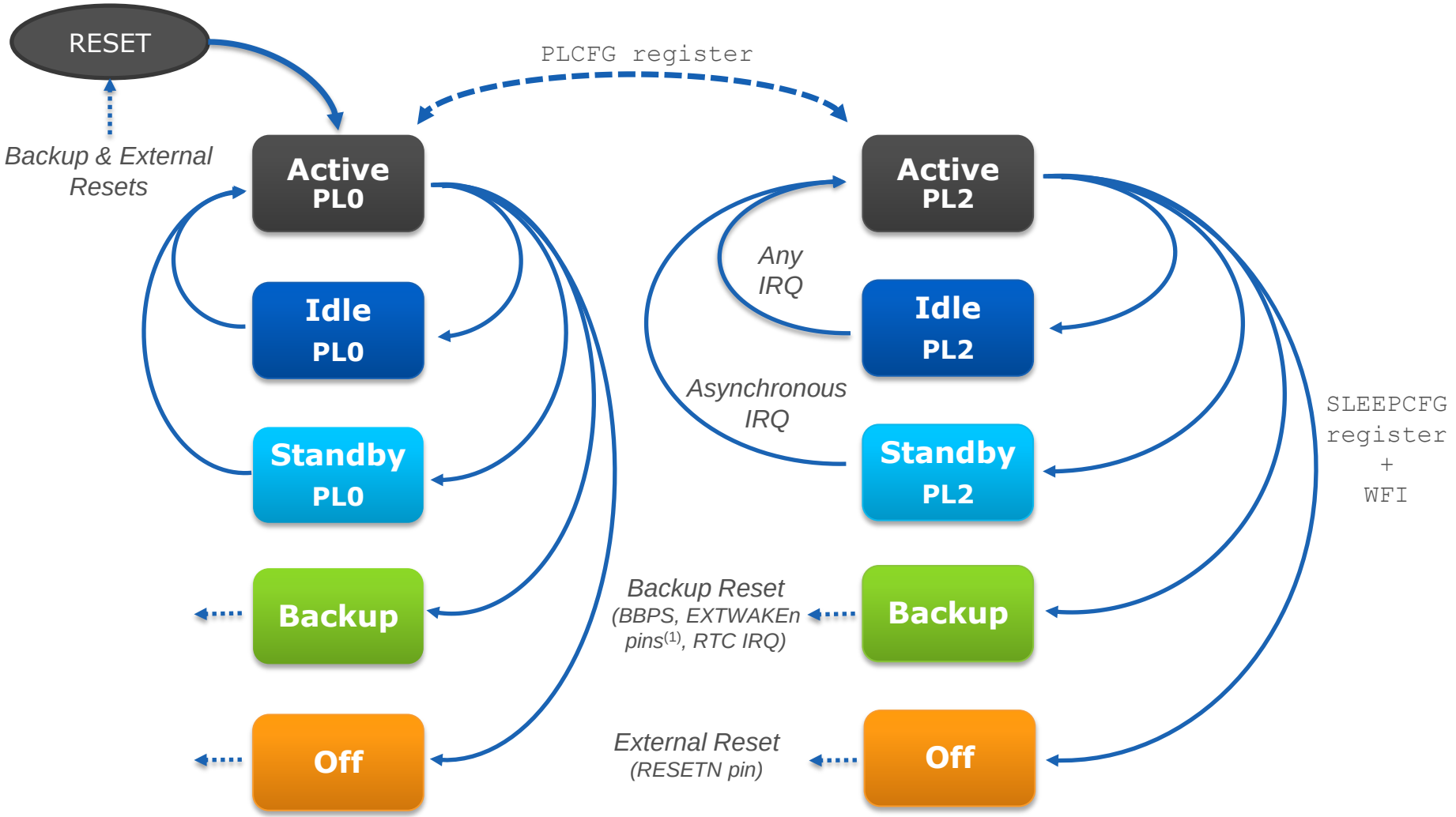
Low Power Techniques

Sleep Modes vs. Performance Levels



(1): EXTWAKE pins can not wake up the device from Battery Backup Mode

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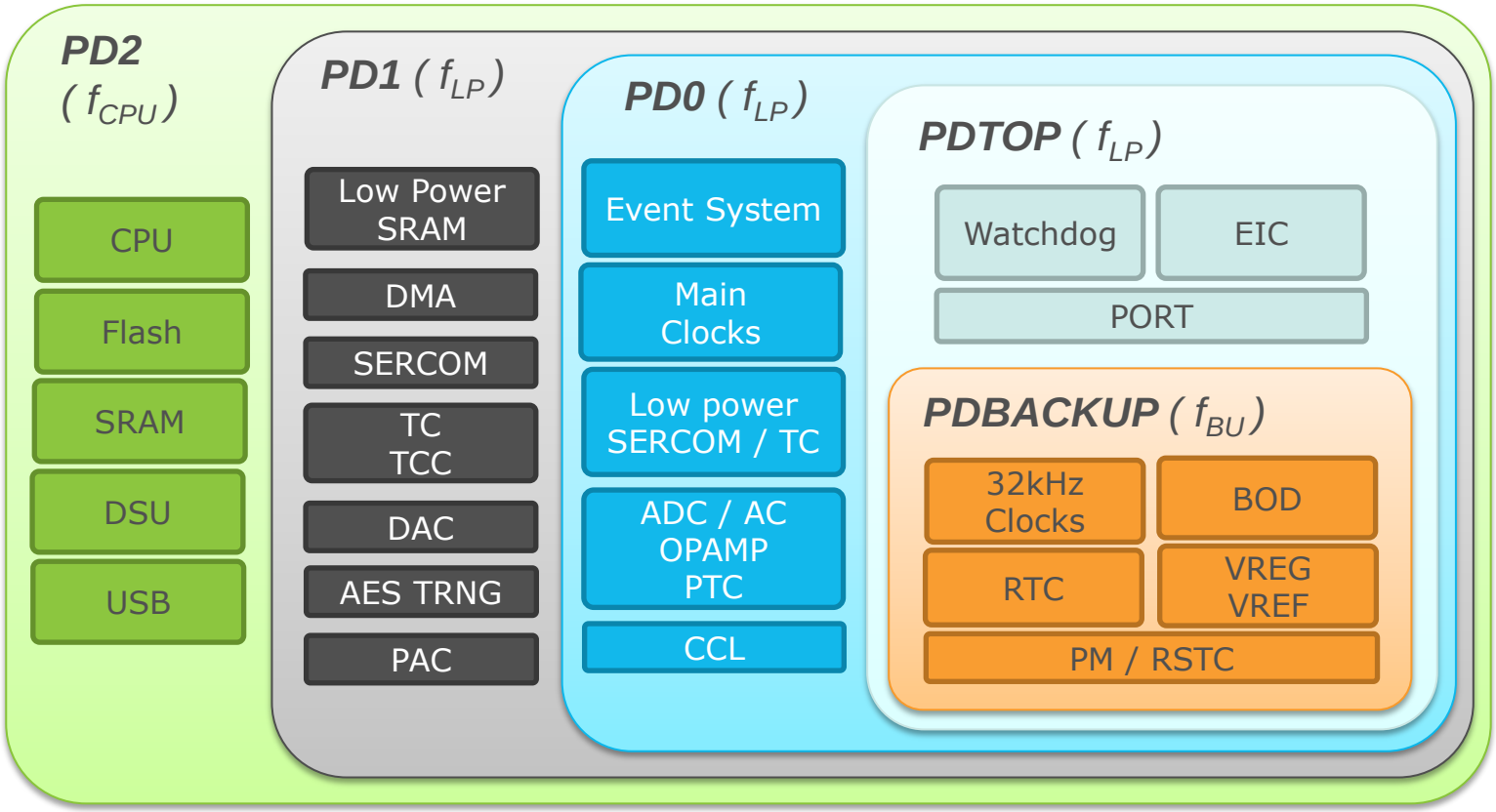
Low Power Techniques

Power Domain Partitioning

- SAM L21 is split into five power domains (PDn)



Clock Domains Constraint: $f_{CPU} \geq f_{LP} \geq f_{BU}$

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Low Power Techniques

Power Domain Gating

STANDBY Mode ONLY

- SAM L21 supports Power Domain Gating
  - Technique which allows to AUTOMATICALLY turn off unused power domain supplies individually while keeping others powered up
  - PD0, PD1 and PD2 can benefit from it

- Power Domains can be in three states
  - Active: power domain is ON
  - Retention: internal state of the power domain logic is retained
  - OFF: power domain is OFF

	Power Domain State				
Mode	**PD0**	**PD1**	**PD2**	**PDTOP**	**PDBACKUP**
Active	Active	Active	Active	Active	Active
Idle	Active	Active	Active	Active	Active
Standby	Active or Retention			Active	Active
Backup	OFF	OFF	OFF	OFF	Active
Off	OFF	OFF	OFF	OFF	OFF

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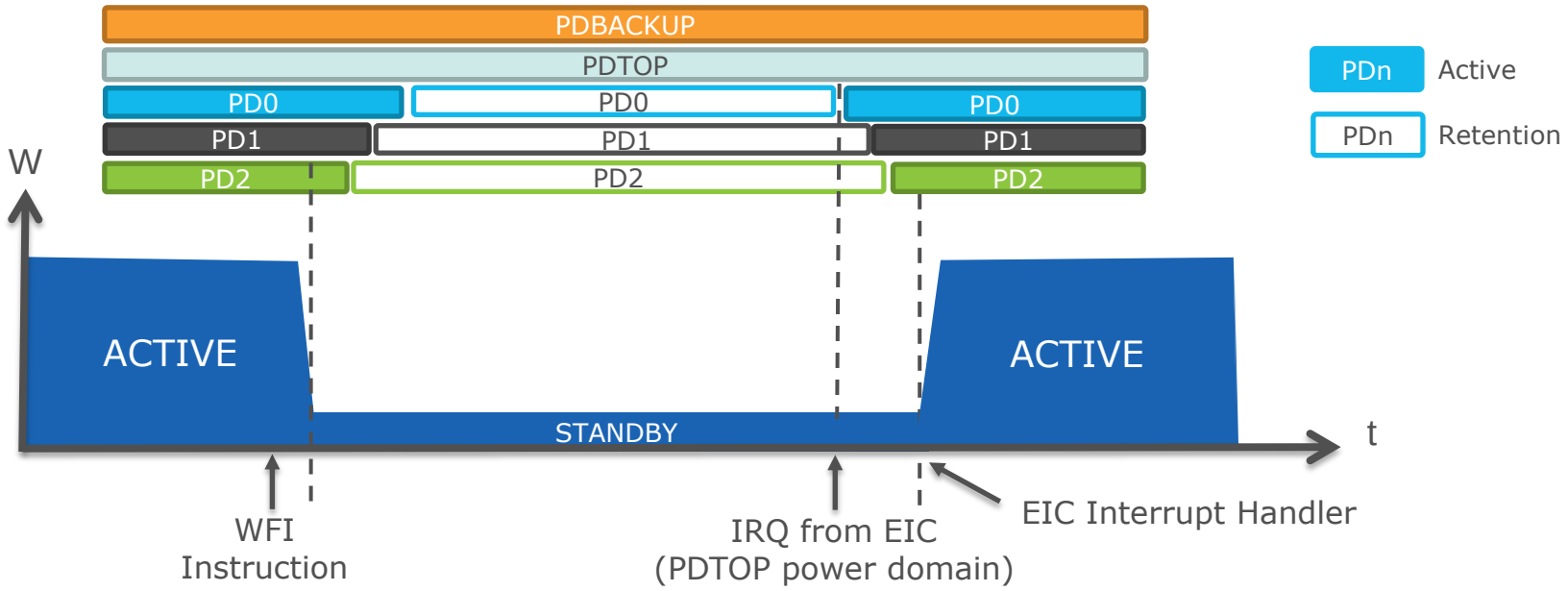
Low Power Techniques

Power Domain Gating (cont.)

STANDBY Mode ONLY

- By default, in STANDBY mode:
  - Each Power Domain (PDn) is set automatically to RETENTION state if no peripheral activity is required on it
  - All Power Domains are returned to Active state when exiting STANDBY mode



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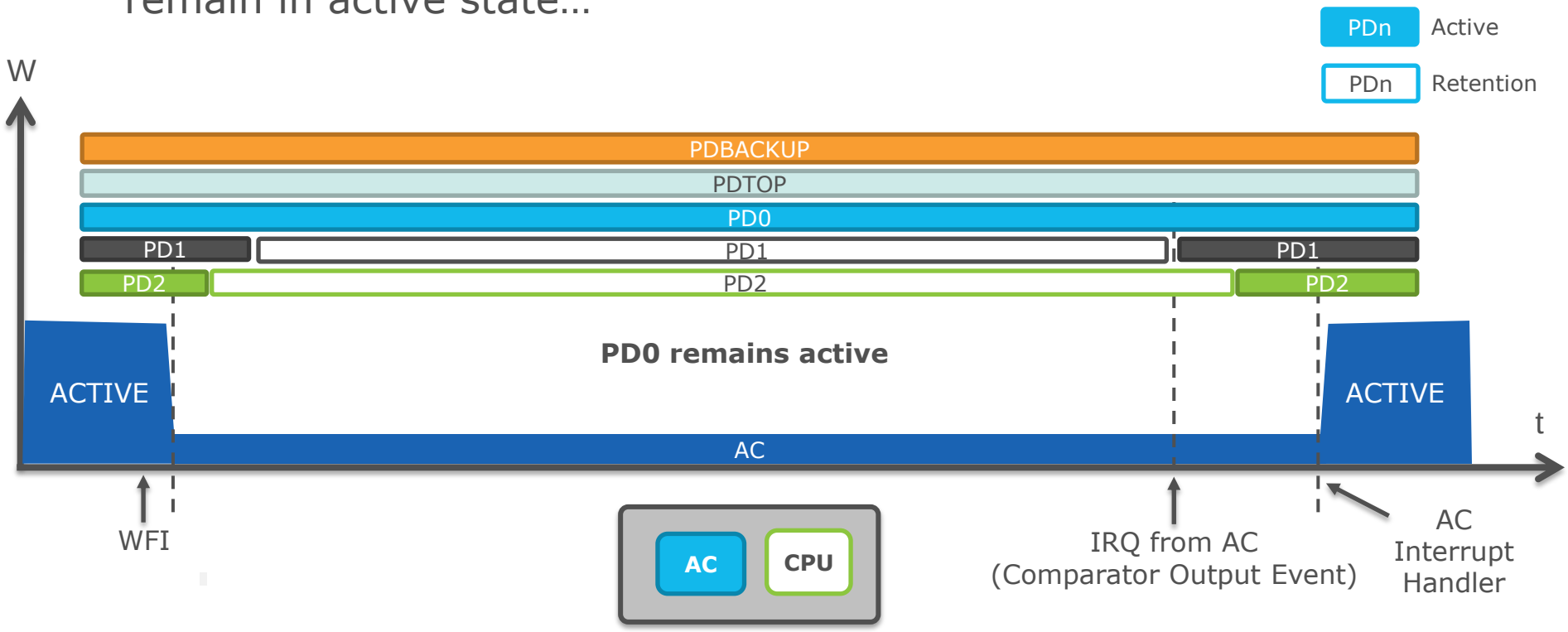
Power Domain Gating (cont.)

STANDBY Mode ONLY

- If a peripheral needs to perform tasks, its power domain (PDn) will remain in active state…



AC in Continuous Measurement mode
monitoring asynchronously comparator output

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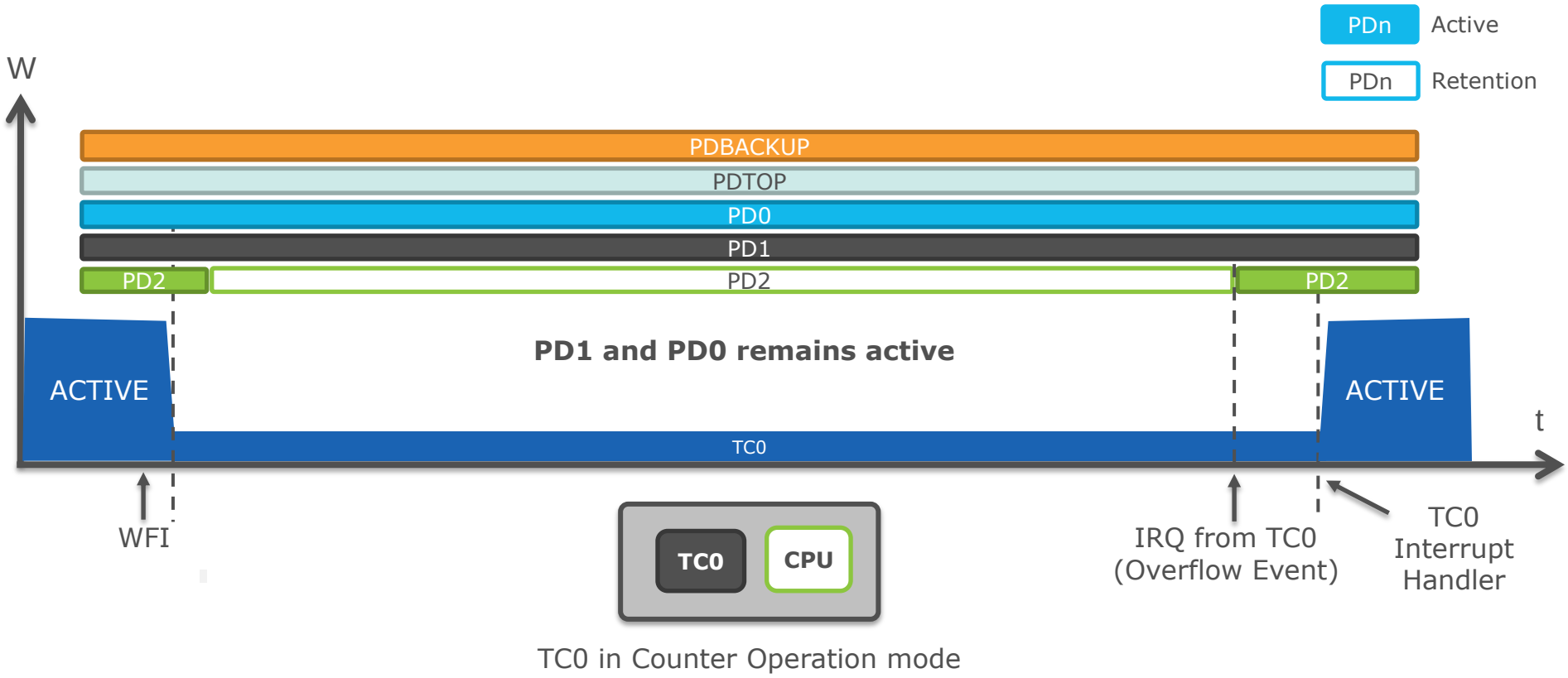
Low Power Techniques

Power Domain Gating (cont.)

STANDBY Mode ONLY

- … as well as the lower power domains (<PDn)



TC0 in Counter Operation mode

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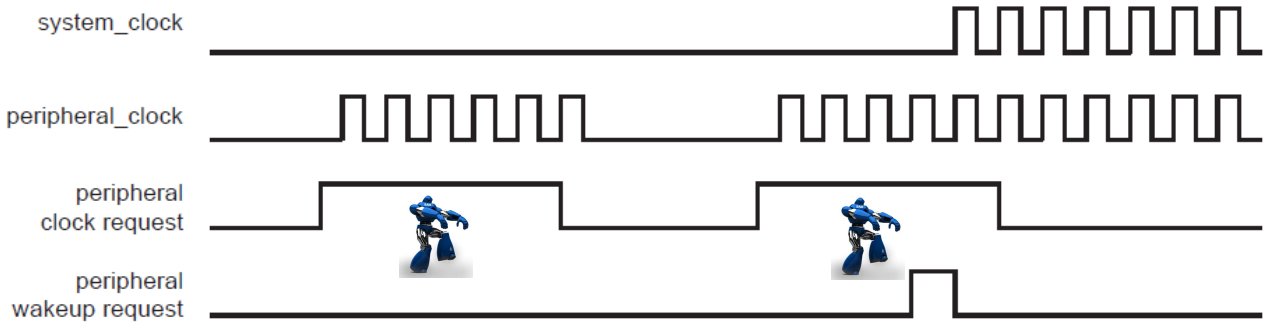
SleepWalking

- Capability for a device in sleep mode, to temporarily wake-up clocks for a peripheral to perform a task without waking-up the CPU
  - Eliminate CPU interrupts
  - Enables intelligent peripherals



- On SAM L21, wake-up clocks can be
  - Asynchronous (GCLK clocks)
  - Synchronous (APB/AHB clocks)

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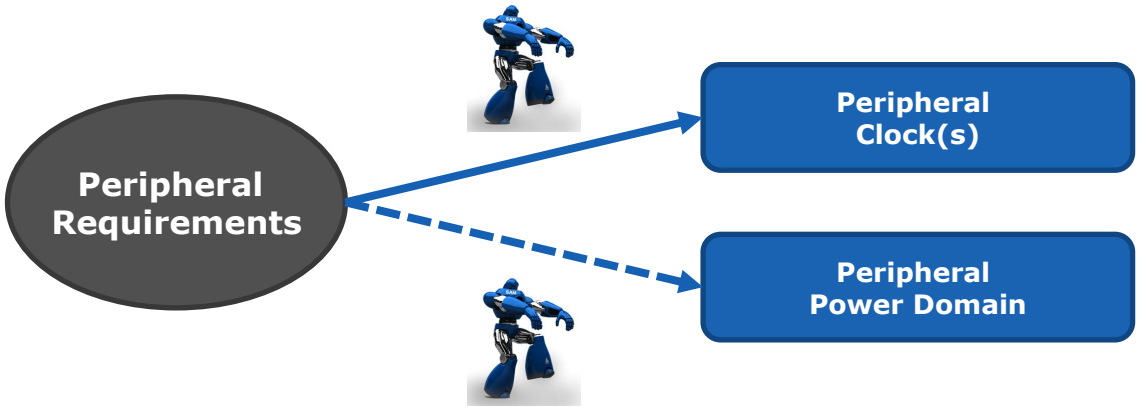
Low Power Techniques

SleepWalking Extension to Power Gating

STANDBY Mode ONLY

- SleepWalking on SAM L21 has been expanded to control power gating in addition to clock gating
- Power domains can be AUTOMATICALLY controlled depending on peripherals' requirements



- That feature is called: SleepWalking with **Dynamic** Power Gating

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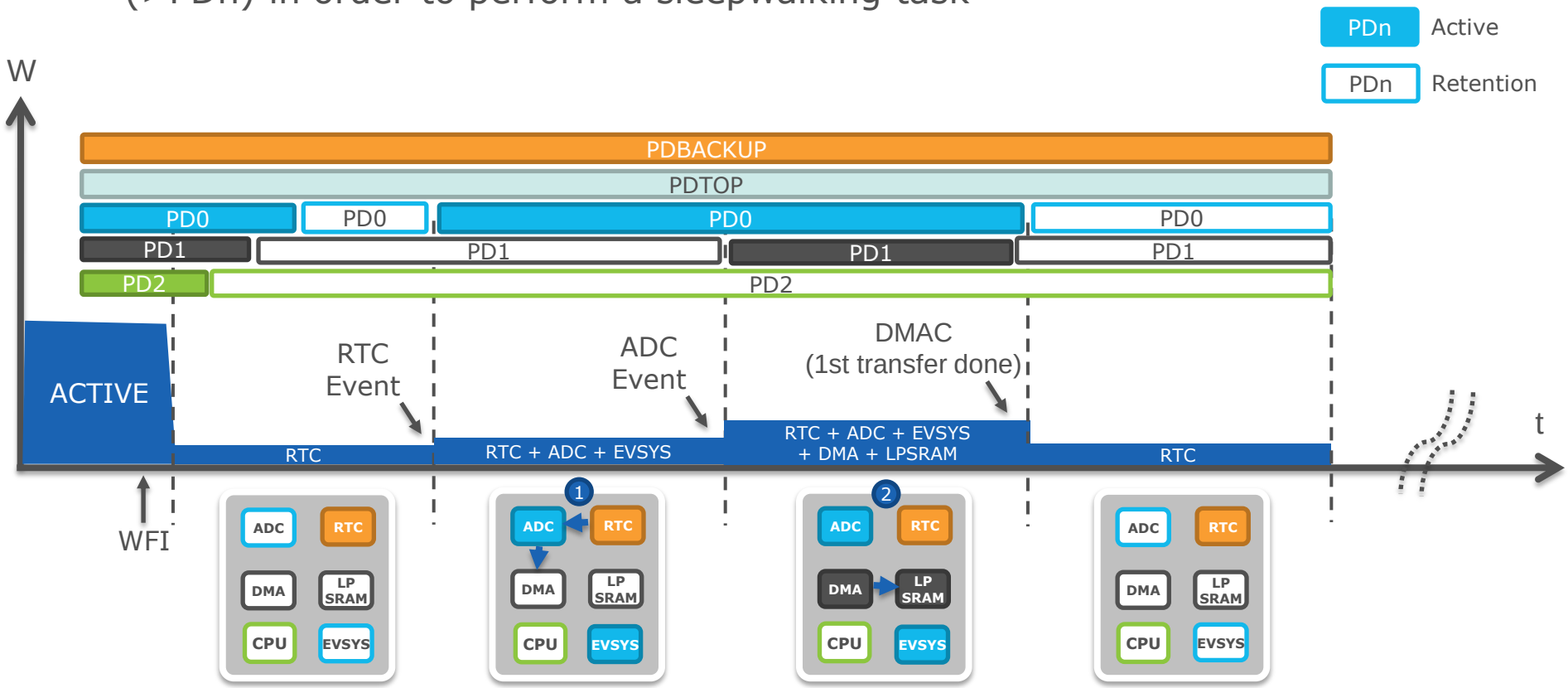
SleepWalking with Dynamic Power Gating

STANDBY Mode ONLY

- A power domain (PDn) in active state, can wakeup a higher power domain (>PDn) in order to perform a sleepwalking task



1. RTC and Event System configured to generate periodic event to the ADC
   ADC in One Shot Measurement mode converting periodically voltage level
2. DMA moves conversion from ADC to Low Power SRAM
3. DMA generates an interrupt after N transfers

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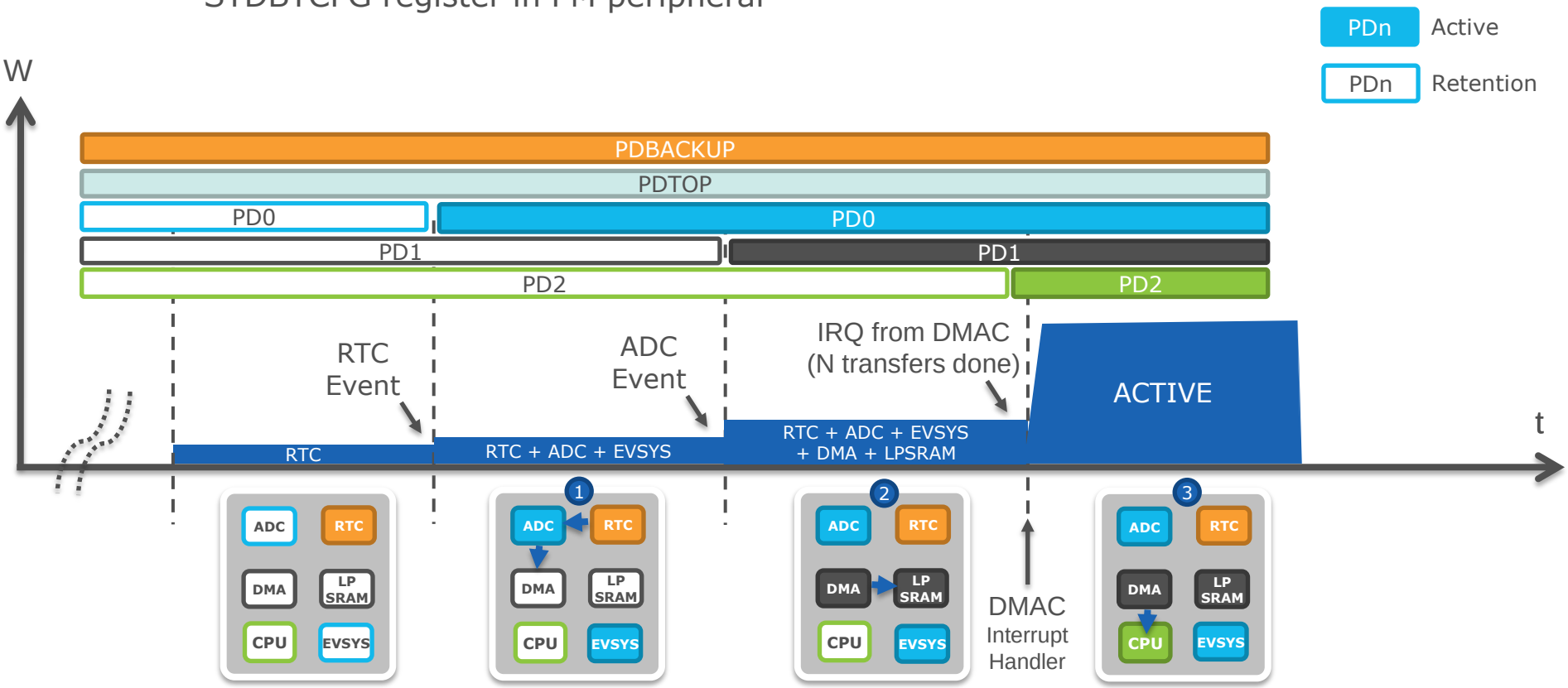
Low Power Techniques

SleepWalking with Dynamic Power Gating (cont.)

STANDBY Mode ONLY

- SleepWalking Extension to Power Gating feature is not enabled by default
  - STDBYCFG register in PM peripheral



1. RTC and Event System configured to generate periodic event to the ADC
   ADC in One Shot Measurement mode converting periodically voltage level
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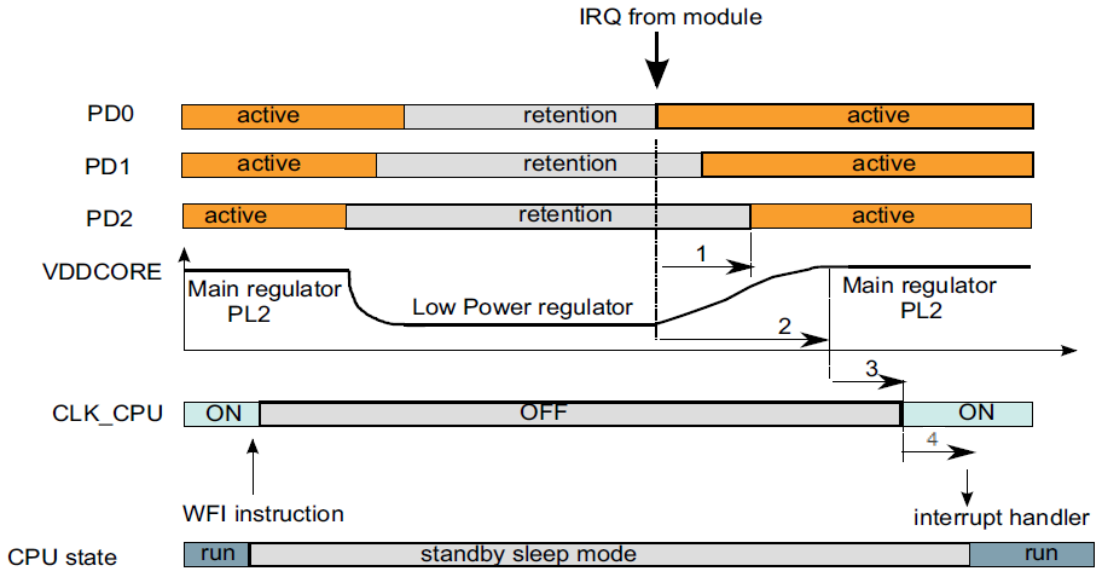
Low Power Techniques

Wake-up Time Considerations in STANDBY

STANDBY Mode ONLY

- Power Domain Gating latency (1)
  - Time to set a power domain from retention to active (~ 2µs)
- Performance Level and regulator latency (2)
  - Time to transition to the regulator voltage level for the concerned Performance Level (~ 12 µs)
- CPU clock source wake-up time (3)
  - Time to start CPU clock (depends on oscillators/ DPLL, DFLL startup times)
- Flash Memory access latency (depends on Wait states) (4)



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Low Power Techniques

SAM L21 Energy Efficiency

- EEMBC ULPBench v1.0 Conditions
  - IAR EWARM 7.30.3.802
  - SAM L21 Active Mode Clock Config
    - f_{CPU} = 12MHz
    - f_{RTC} = 32,768kHz
  - SAM L21 Sleep Mode Name / Conditions
    - STANDBY
    - PD0, PD1, PD2 in RETENTION state

- ULPBench score of 185.8 on SAM L21 rev A
  - The highest publicly-recorded score for any Cortex-M0+ based processor
  - http://www.eembc.org/ulpbench/

ULPBENCH™
An EEMBC Benchmark

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New and Enhanced Peripherals

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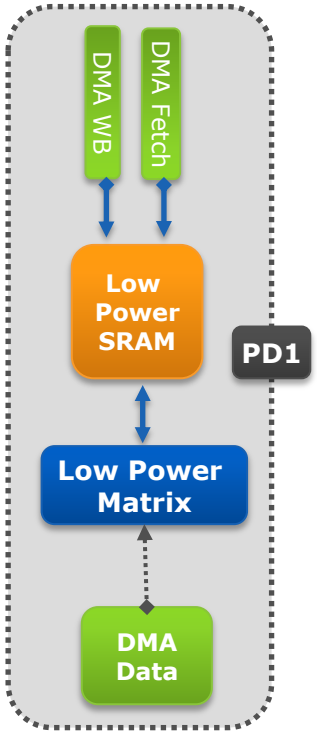
New and Enhanced Peripherals

High Performance DMA with Standby Mode Support

- Tight system RAM interaction allowing a full-featured DMA with Standby mode support
  - Each channel can be configured to operate in sleep modes including STANDBY
  - Event System support for SleepWalking capability
- 16 DMA channels
  - Peripheral-Memory / Memory-Memory transfers
  - Priority levels for each channel
  - SRAM based descriptors support
- SRAM Quality of Service (QoS) support
  - Can give priority to DMAC compared to other masters accessing SRAM
  - Separate priority levels for:
    - Descriptor Fetch priority
    - Descriptor Write-Back priority
    - Data Transfer priority



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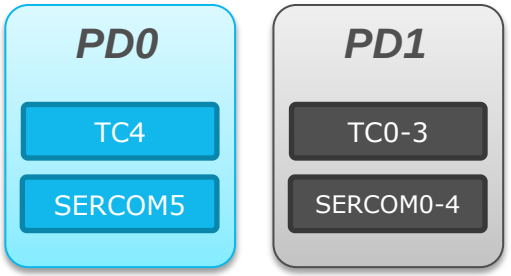
New and Enhanced Peripherals

picoPower Peripherals

- Highly integrated peripherals optimized for Low Power (PD0 domain)
  - Event / Interrupt System
  - STANDBY sleep support with SleepWalking



- picoPower SERCOM (SERCOM5)
  - Differences with SERCOM0-4
    - No DMA capability
    - USART, I2C and SPI specific limitations
      - Listed in SERCOM section of product datasheet

- picoPower Timer Counter (TC4)
  - 32.768 kHz clock source for minimized power consumption
    - Option to be clocked from faster clock source
  - Differences with TC0-3
    - No User events (only Generators events)
    - No 32-bit resolution (need two chained TC)

TC0-3
2.72uA/MHz

TC4
1.45uA/MHz

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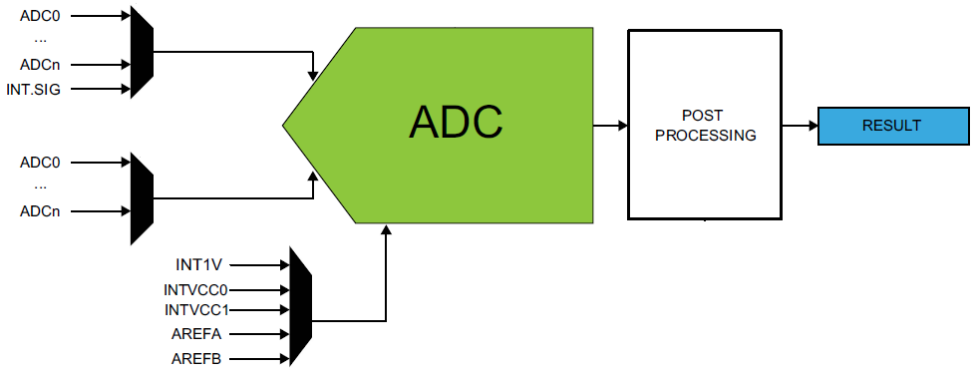
New and Enhanced Peripherals

Up to 1Msps 12-bit ADC optimized for Low Power

- Single-ended or Differential
- No internal gain
  - OPAMP to be used
- Eight internal inputs
  - OPAMP01 (0 or 1) / OPAMP2
  - Scaled VBAT, Core, I/O supply
  - Bandgap voltage
  - DAC
  - Internal temperature sensor



- Large Conversion range
  - 0V to Vref where Vref = [1.0V to VDDANA]
- Automatic Sequencing of a series of conversions
  - Only selected inputs will be scanned from lowest to highest
- Averaging and oversampling with decimation to support up to 16-bit result
- Offset and Gain correction

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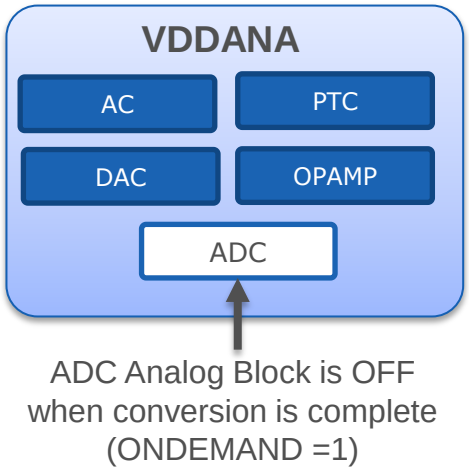
New and Enhanced Peripherals

Up to 1Msps 12-bit ADC optimized for Low Power (cont.)

- Event / Interrupt System
- DMA support
- Sleep Mode Operation
  - Standby sleep support with SleepWalking
  - ADC can request the OPAMP using the OPAMP Analog ONDEMAND functionality
  - ADC Analog block (VDDANA) can be powered off to reduce power consumption



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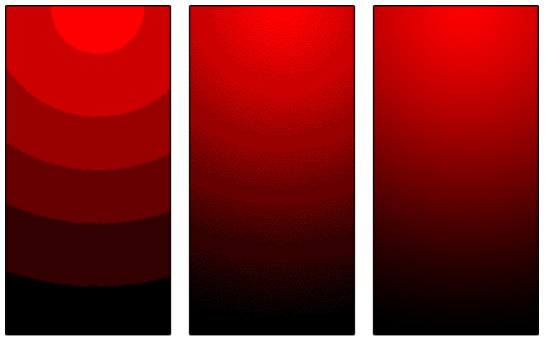
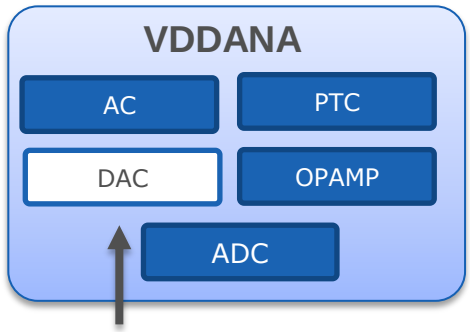
New and Enhanced Peripherals

Up to 1Msps 12-bit DAC optimized for Low Power

- Two DACs or single DAC in differential mode
- Hardware support for 16-bit using Dithering
  - Intentional applied form of noise used to randomize quantization error
  - Can be performed at 1Msps/16 (= 62500 sps)
- Highly integrated / Optimized for Low Power
  - Event / Interrupt System
  - DMA support
  - Standby sleep support with SleepWalking
- (Standby) Sleep Mode Operation
  - Run in Standby feature can be enabled to continue DAC conversions
  - If disabled: DAC Analog block (VDDANA) is powered off to reduce power consumption





DAC Analog Block is OFF
when conversion is stopped in STANDBY

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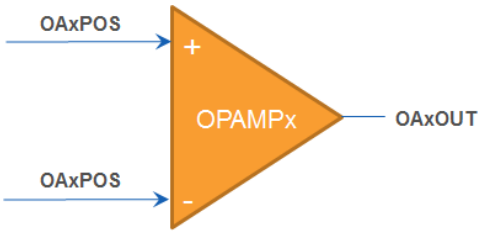
New and Enhanced Peripherals

Low Power Operational Amplifiers (OpAmps)

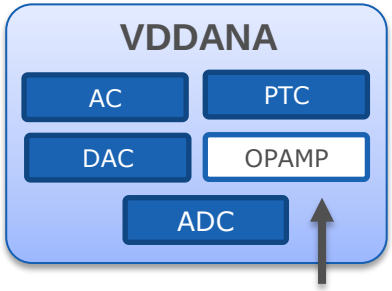
- Three individually configurable Low Power OpAmps with internal feedback resistors to reduce BOM
  - $Gain_{max}$ ~ x15.7
  - OpAmps can be cascaded



- Outputs available
  - On GPIO pins
  - Can be used as Input for AC and ADC

- (Rail-to-rail) Inputs available
  - GPIO pins, DAC or Ground

- Sleep Mode Operation
  - Standby sleep support with SleepWalking



OPAMP Analog Block is OFF until requested by a peripheral

  - Analog ONDEMAND capability
    - Allows other analog peripherals (AC, ADC) to request the OPAMP
    - OPAMP Analog block (VDDANA) can be powered off to reduce power consumption

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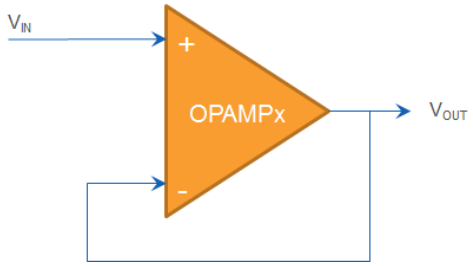
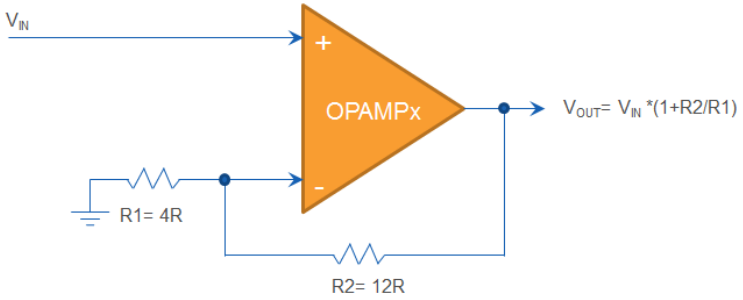
New and Enhanced Peripherals

OpAmp Classical Built-in Amplifiers

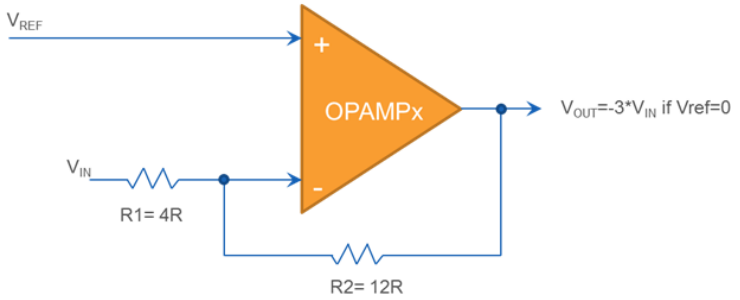
- Standalone mode
- Voltage follower



- Non-Inverting/Inverting Programmable Gain Amplifier (PGA)
  - Non-Inverting/Inverting PGAs can be cascaded



Non-Inverting PGA



Inverting PGA

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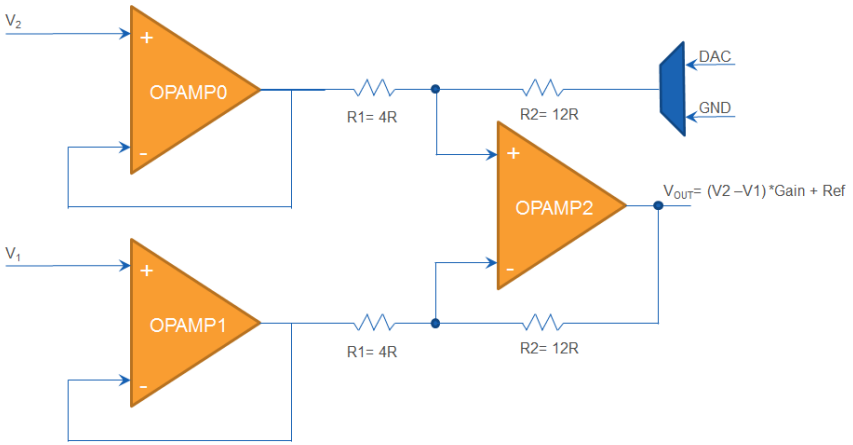
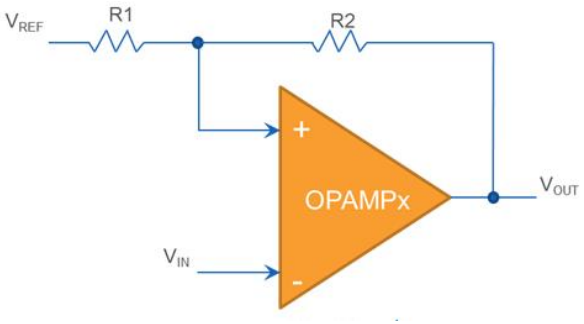
New and Enhanced Peripherals

OpAmp Classical Built-in Amplifiers (cont.)

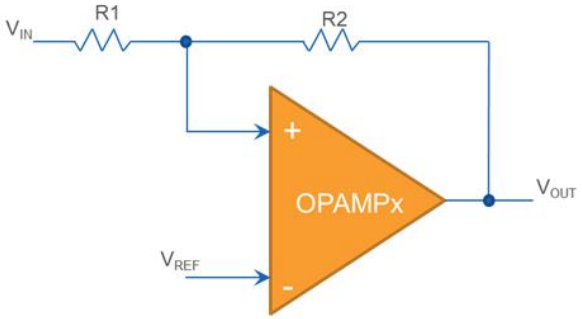
- Instrumentation Amplifier



- Comparator with programmable Hysteresis



Non-Inverting Comparator



Inverting Comparator

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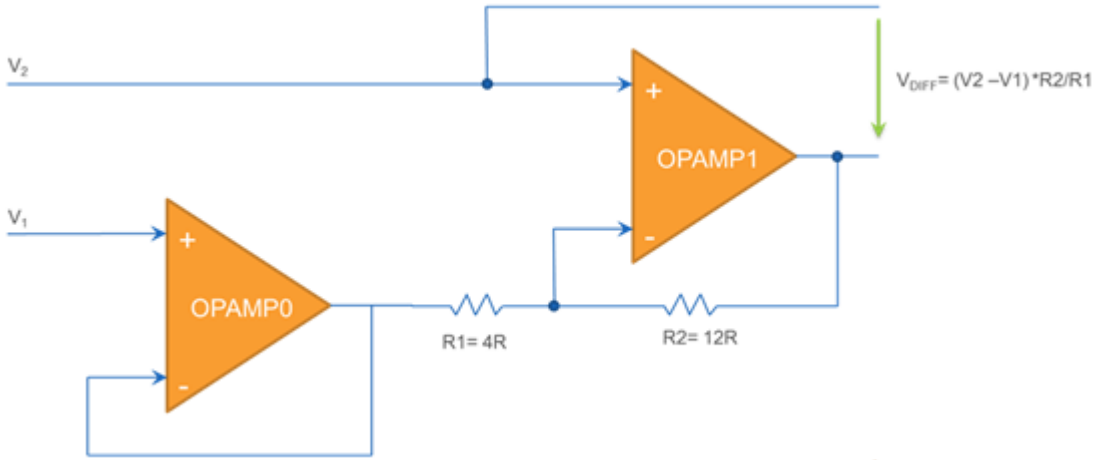
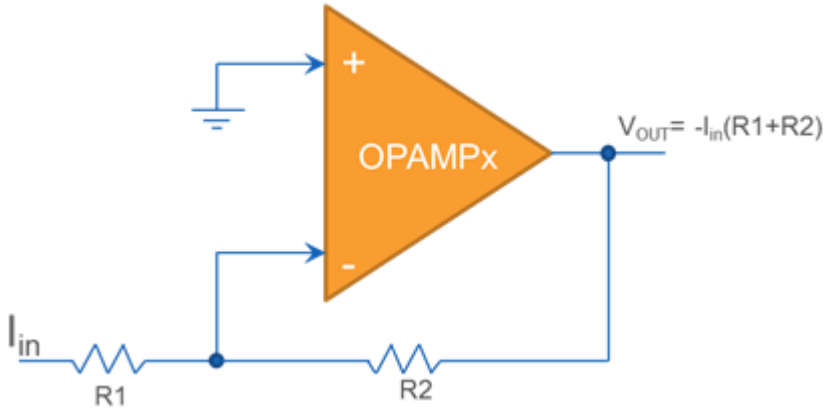
New and Enhanced Peripherals

OpAmp Classical Built-in Amplifiers (cont.)

- Two OpAmps Differential Amplifier



- Transimpedance Amplifier



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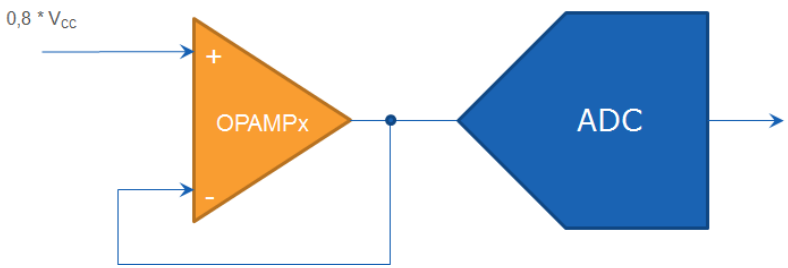
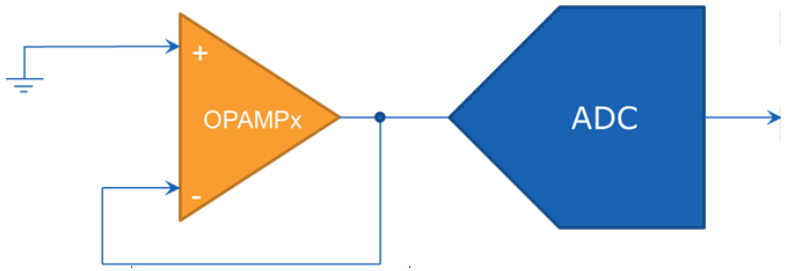
New and Enhanced Peripherals

OpAmp Built-in AC / ADC Driver

- OpAmp can be a buffer or Programmable gain for ADC and AC
  - Can also be cascaded to increase gain
- ADC Offset/Gain Compensation capability
  - Measurement for calibration when used with the ADC



Gain Compensation



Offset Compensation

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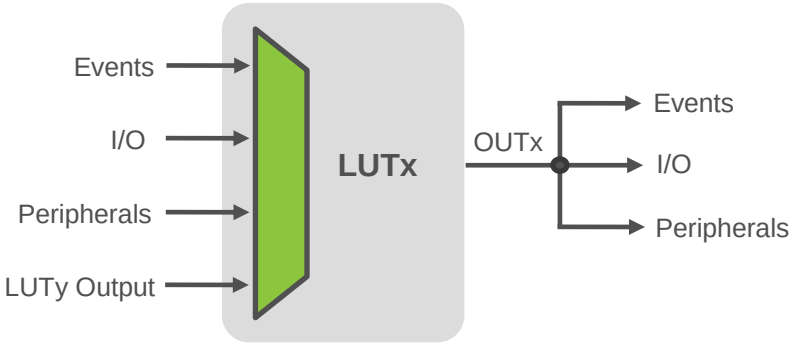
New and Enhanced Peripherals

Configurable Custom Logic (CCL)

- Up to four programmable three-input Look Up Table units (LUT) to provide glue logic for general PCB design
  - BOM cost reduction
  - Real time answer
- Combinatorial Logic Functions
  - AND, NAND, OR, NOR, XOR, XNOR, NOT
- Sequential Logic Functions
  - Gated D Flip-Flop, JK Flip-Flop, gated D Latch, RS Latch



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New and Enhanced Peripherals

Hardware Cryptographic Accelerators

- AES Symmetric-key Encryption Peripheral for Data Confidentiality
  - Compliant with FIPS Publication 197
  - 128 bit block of input data
  - 128-bit/192-bit/256-bit Cryptographic Key
  - ECB, CBC, CFB, OFB, CTR Modes of Operations
  - New Gallois Counter Mode (AES-GCM)
  - Message Authentication Code (MAC) Generation
    - CBC-MAC
  - Countermeasures against DPA attacks (Differential Power Analysis)
    - Can add randomly power consumption / cycles to data processing

- True Random Number Generators (TRNG)
  - Passes NIST Special Publication 800-22 & Diehard Random Tests Suites
  - Provides a 32-bit Random Number Every 84 Clock Cycles
  - Event Generator (each time a new RNG is available)

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New and Enhanced Peripherals

Peripheral Access Controller (PAC) for Software Robustness

- SAM L21 Peripheral Access Controller ensures application robustness (against noise)
  - Provides write protections for registers
  - Reports all violations in a unique flag for each peripheral

- Traditional approach
  - Key protection of critical registers... but which registers are critical?
- SAM L21 Peripheral Access Controller allows the user to decide which peripherals are critical for his application and need SW protection
- Access control can be handled in main code, above driver level to ensure robustness against runaway code

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Ecosystem

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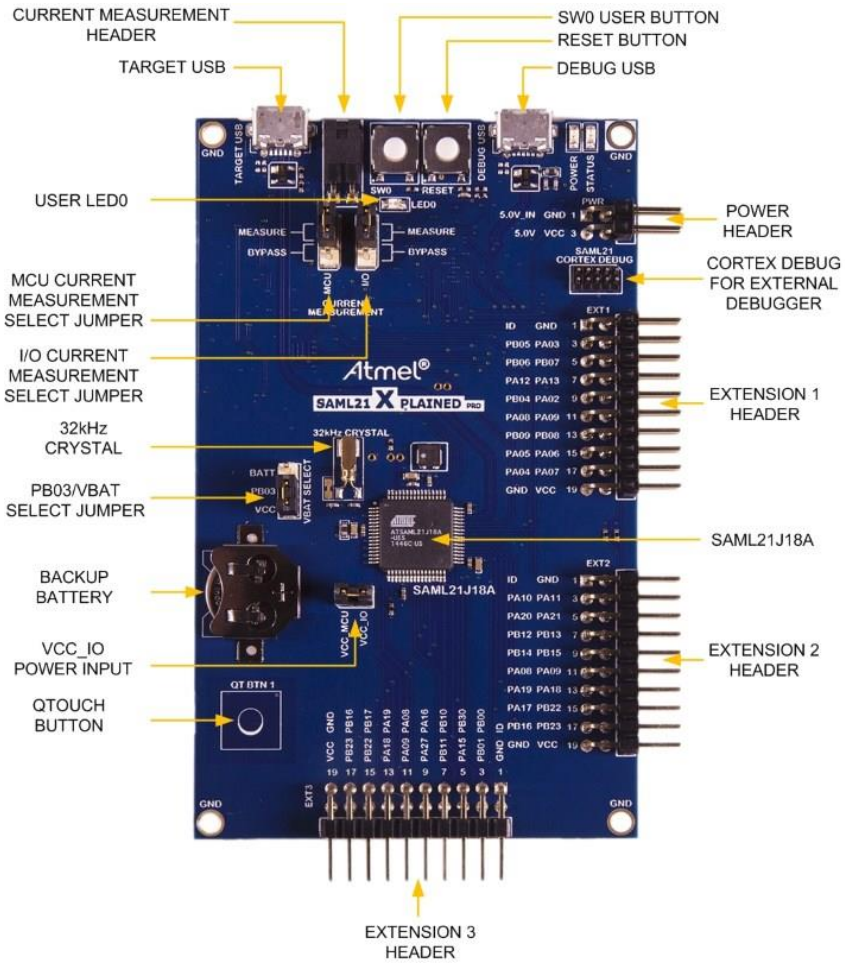
Ecosystem

SAM L21 Xplained Pro

- Embedded Debugger (EDBG)
  - Programming / Debugging
  - Virtual COM port
  - Data Gateway Interface (DGI) for data streaming with the computer
- Xpro Analog Module (XAM)
  - Enables SAM L21 Power Profiling on MCU and/or Board Peripherals
- Support since ASF 3.21.0
- Toolchains
  - Atmel Studio 6.2 SP2 and Studio 7
  - IAR EWARM 7.4 and higher
  - Keil MDK



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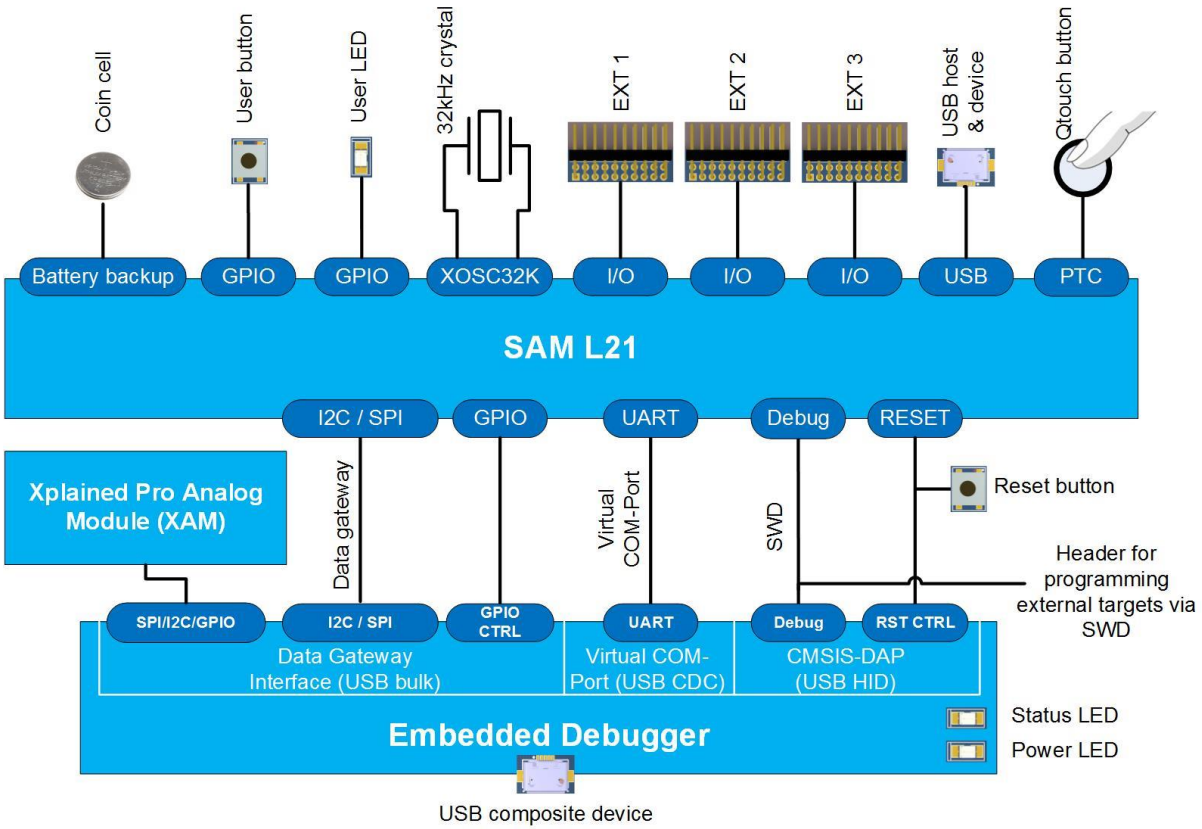
Ecosystem

SAM L21 Xplained Pro (cont.)



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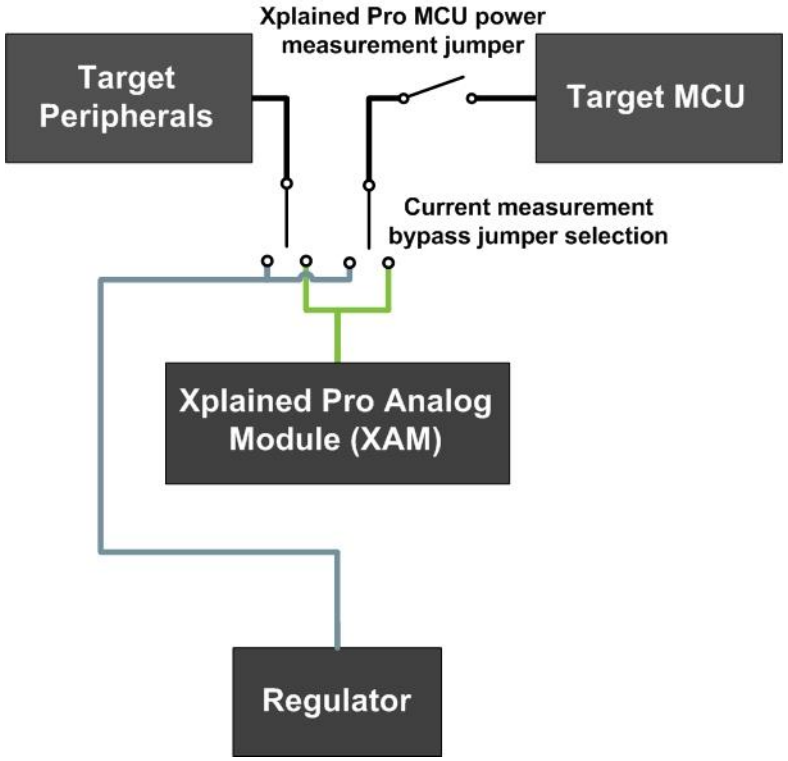
Ecosystem

SAM L21 Xpro Analog Module (XAM)

- Extend EDBG with high dynamic range current measurement
  - 0-400mA
- XAM consists of:
  - Analog frontend with Voltage Reference
  - Control MCU (SAM D20)
- MCU and/or Peripherals (Board extensions) can be measured
- Visualization in Atmel Data Visualizer tool



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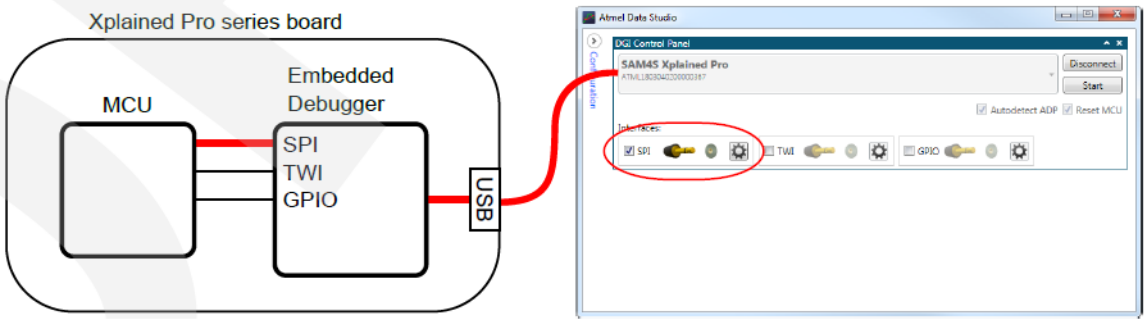
Ecosystem

Atmel Data Visualizer

- Atmel Studio Program used for processing and visualization of data
  - Available on Atmel Gallery

- Uses Atmel EDBG over USB as input for data
  - SPI, TWI or GPIO interfaces supported between Target MCU and EDBG



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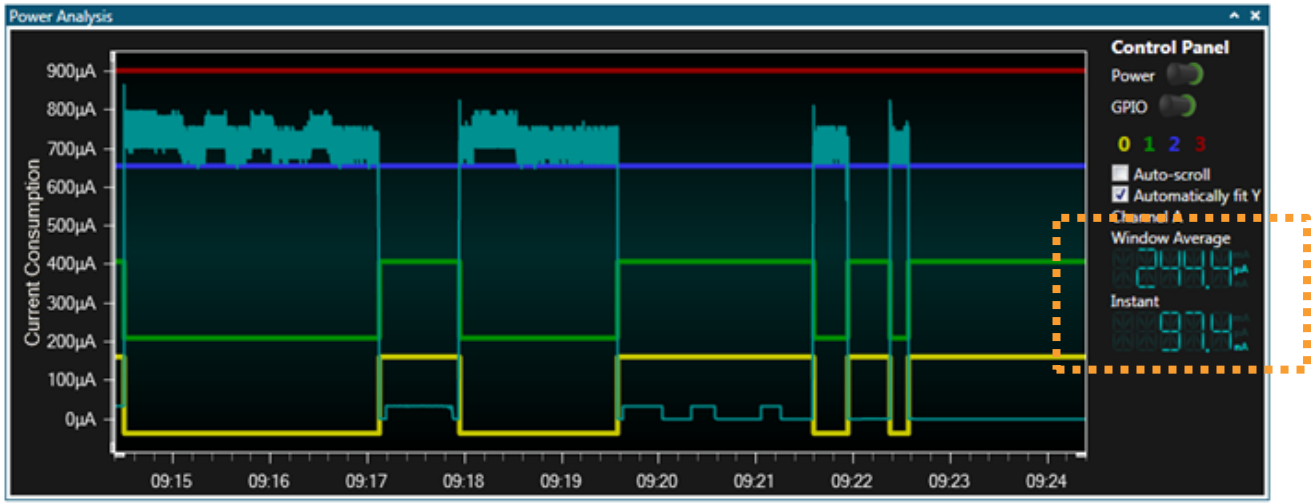
Ecosystem

Atmel Data Visualizer – SAM L21 Xpro Power Analysis

- Power consumption measurement and visualization
  - Support power profiling using SAML21-XPRO
  - Demonstrate SAM L21 low power modes

- Displays two power consumption values
  - Instant current value
  - Averaged current value (graph samples)



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