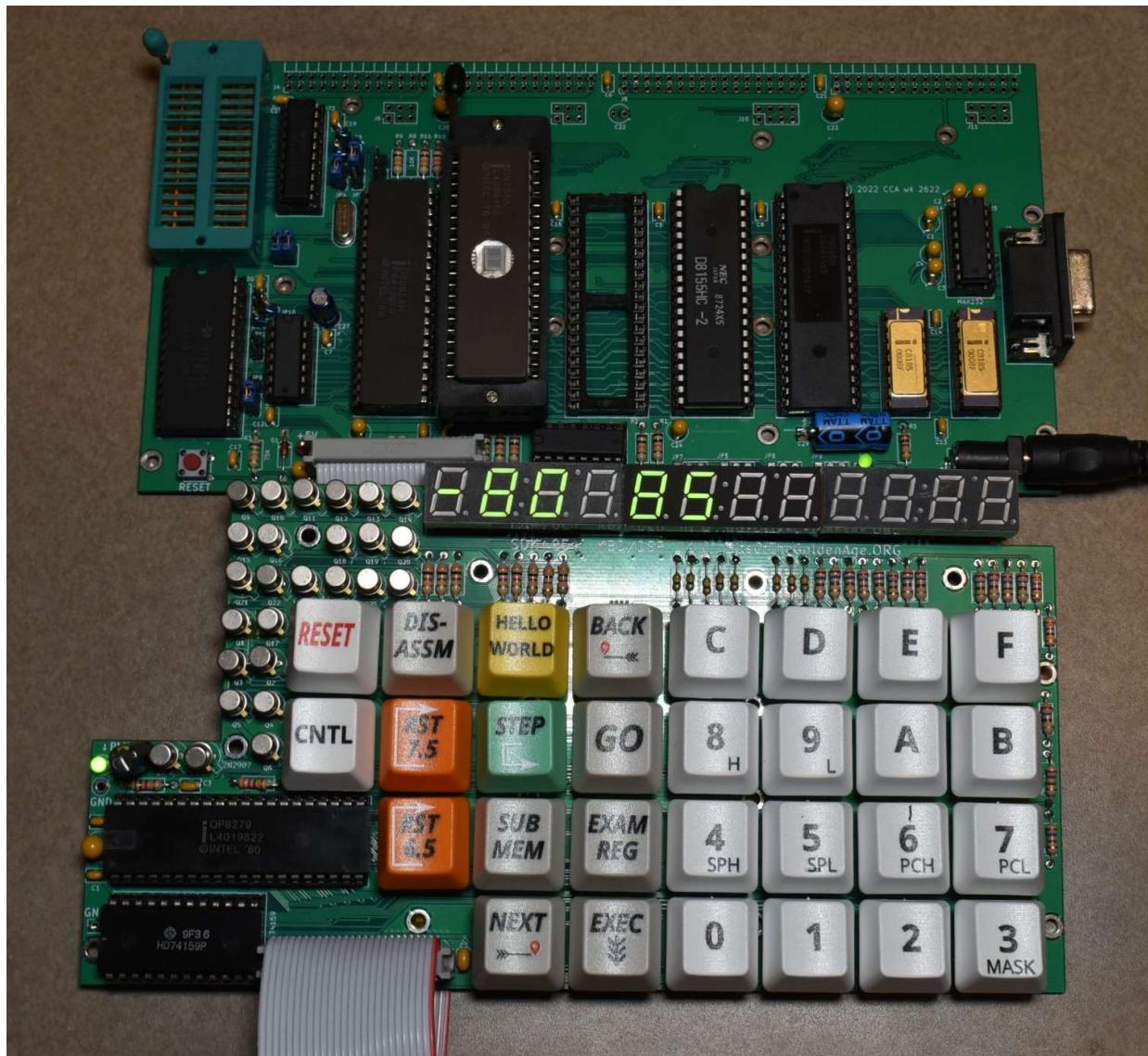


SDK-85+ Single Board Computer

User's guide for the SDK-85+ Single Board Computer

Hardware version 1.1



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Notation:

Pin numbers. Pin numbers are given as **ID.pin**. for example, Pin 5 of connector X3 is given as **X3.5**. IC7 pin 21 is given as **IC7.21**.

Logic Levels. Lines having a signal that is active low is given with either an asterisk or a slash following the signal name. For example, **CS8/** and **CS11*** both refer to signals that are active when at 0V or logic low.

Terminology:

Most abbreviations will be spelled out when they are first used. However, the more commonly used terms are described in the **Definitions of Terms and Notations** at the end of the document.

SDK-85+ DESCRIPTION

The SDK-85+ is a derivative of Intel's SDK-85 (System Development Kit – 8085). It is an 8085 based Single Board Computer and, as such, it contains all elements required for stand-alone operation including the processor, Random Access Memory (RAM) and Read Only Memory (ROM or EPROM) are available through two 8755 ROMs, two 8155 RAMs, two 8185 RAMs and two universal, 28 pin JEDEC sockets (one ZIF). The SDK-85+ also includes an RS232 Serial port with a female DB9 connector for communication with a terminal.

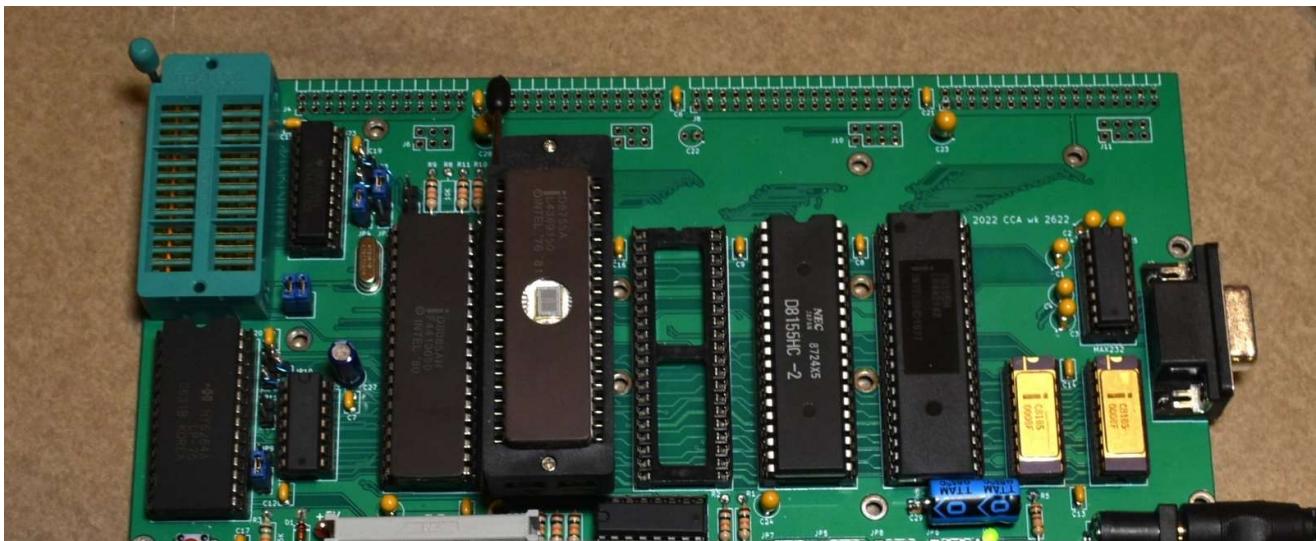
Compared to Intel's original SDK-85, the **plus** features of the SDK-85+ include:

- An additional 2K of RAM provided by the dual 8185 SRAM chips;
- Additional memory provided by the two 28-pin universal sockets;
- Twelve digits of display
- Five additional keys including:
 - Three general use function keys F1, F2, and F3;
 - Dedicated RST 6.5;
 - 8259 SHIFT input.

The SDK-85+ board is *nearly* firmware compatible with Intel's original SDK-85. A version of Intel's SDK-85 Resident Monitor v2.1 has been ported to this board and is on the project website. The primary difference between Intel's SDK-85 and the SDK-85+ is the handling of SID and SOD data. Since the SDK-85+ uses a MAX232 rather than a teletype output, the logic of the SID is inverted from the original SDK and the serial input code needs to account for the difference. Other changes to the resident monitor were minor, such as explicitly setting the 8279 clock divider (rather than accepting the default value), moving the data field one to the right to account for the lack of a physical gap between the first four digits (address field) and the data field.

Note that when code was changed, each code change takes the exact same number of bytes as Intel's original code. Therefore, all function addresses remain the same between Intel's original SDK-85 monitor and the SDK-85+ resident monitor. Critically important from a software application perspective, the ported SDK-85+ monitor operates the same as Intel's original SDK monitor, and any program that runs on the original SDK using original function calls should run on the SDK-85+. If you find any exceptions to this, please let me know.

SDK-85+ CPU BOARD



CPU BOARD CIRCUIT DESCRIPTION

CPU Board Primary Components	
ID	Description
U1	8085 Microprocessor operating at 3MHz
U2	Base 8755 2K ROM, I/O
U3	Base 8155 256 bytes of RAM, plus I/O, Timer
U4	Expansion 8755 2K ROM, I/O
U5	Expansion 8155 256 bytes of RAM, plus I/O, Timer
U6	74LS138 1-of-8 Memory Map Decoders
U7	74LS573 low address byte latch (for U9 and U12)
U8	Base 8185 1K static RAM
U9	JEDEC 28-pin Memory ZIF Socket
U11	Expansion 8185 1K static RAM
U12	JEDEC 28-pin Memory Socket
U14	MAX232 TTL / RS232 Driver - Receiver Level Shifter
U13	74LS00 Quad 2 input NAND. Address decoding, logical NOT

8085

The 8085 microprocessor needs only +5VDC and an oscillator input to operate. On the SDK-85+, the oscillator input is provided by Q1 which is a 6.144MHz crystal. The 8085 immediately begins fetching instructions from address 0x0000 upon power up, however the power up must be somewhat controlled to allow the 8085's internal charge pump to build sufficient charge before the CPU fetches its first instruction. Because of this, the 8085 needs a slight delay in the release of its *ResetIN** after power up. This is accomplished by the RC circuit which is a 75K (R2) bleed into a 1uF (C5) capacitor. After power is applied, this RC circuit takes around 80 uS to reach a logic high on *RESETIN**, and releasing the CPU from reset.

Once out of reset, the CPUs operation is controlled by its *READY*, and *HOLD* inputs. The *READY* is primarily intended as a means of an external circuit pausing the CPUs operation so it can "catch-up", e.g., so slow memory or a slow I/O port can stop the CPU until it can complete a requested action. Therefore, for the CPU to operate the *READY* must be TRUE, or logic one. This is accomplished by (10K) pull-up resistor R4. *HOLD* must be at logic zero and is pulled down to ground by the 10K resistor R10.

Finally, the 8085's operation can be interrupted by hardware inputs, namely *INTR*, *TRAP*, *RST7.5*, *RST6.5*, and *RST5.5*. Of these, all are disabled when the processor first starts except for the *TRAP* which cannot be masked or turned off. If these are not controlled by another device they must be pulled low. *HOLD* is pulled low by R10, *INTR* is pulled by R11. When not used by the keypad / display board, *RST 6.5* and *RST 7.5* are pulled low by U13C and

U13D as the inputs to U13C, U13D are pulled high by R6 and R7. When the keypad/display board is used, the RST 6.5 and RST 7.5 keys take these inputs to ground, and U13 subsequently drives the interrupt to logic one. J3 can be used to reconfigure the restarts, but is normally jumpered straight across with four shorting plugs, i.e., 1-2, 3-4, 5-6, 7-8.

CPU Interrupt Allocation		
Input	Function	Note
RST 5.5 (lowest)	Dedicated to 8279 keyboard / display controller	High Level Until Sampled
RST 6.5	Keypad RST 6.5 input	High Level Until Sampled
RST 7.5	Keypad RST 7.5 Input	Rising Edge
TRAP (highest)	8155 U3 Timer Interrupt	Non Maskable, Used for Single Step
INTR	Unused	

ADDRESS LATCH

The 8085 has 16 address lines and can therefore access 2^{16} locations or 65536 address (a.k.a. 64KB) of memory. During each memory access the 8085 first puts all 16 addresses onto the output bus, but the lower 8-bits (AD0-AD7) are only held for a short period before those eight lines are used to transfer the data byte. While the lower address byte is transient, most components require that the lower 8 address bits be continuously available throughout the machine instruction. This is accomplished by U7 which is an 8-bit (octal) latch which takes the transient input of AD0-AD7 and creates a sustained A0-A7. AD0-AD7 are latched on the falling edge of the 8085's Address Latch Enable (ALE) signal. In operation, the 8085 puts the lower address byte on AD0-AD7 and raises the ALE signal and the AD0-AD7 logic levels exit the latch on Q0-Q7 onto the A0-A7 address lines. After enough time is given for these signals to propagate and stabilize, the 8085 lowers the ALE signal and the values are latched onto the A0-A7 signals. When combined with the A8-A15 signals, which the 8085 is still holding, the universal memory sites U9 and U12 now have a sustained A0-A15 address.

ADDRESS DECODING

As the 8085 microprocessor outputs addresses for memory locations or I/O ports, a portion of the circuit known as an *address decoder* determines which addresses are in which component. As its name implies, the address decoder uses the address output from the 8085 onto the A0-A15 address bus and compares this address to the system *address map*. As the result of the comparison, while there may be several components connected to the same data bus, only a single device will be selected to communicate with the CPU.

U6 is a one-of-eight decoder (a.k.a. three-to-eight decoder) whose output is controlled by the high three address bits, i.e., A13, A12, and A11 and is enabled when A14 AND a15 are both low, i.e., the lower 16K address block from 0x0000 through 0x3FFF. When this low address block is enabled via A14 and A15, U6 breaks this address range into eight 2K address blocks as follows:

U6 Memory Map Decoding (Lowest 16K Only)								
A15-A14	A13	A12	A11	Starting Address	Ending Address	Output Select	Output Pin	Selected Device
0	0	0	0	0x0000	0x07FF	CS0	15	U2 8755
0	0	0	1	0x0800	0x0FFF	CS1	14	U4 8755
0	0	1	0	0x1000	0x17FF	CS2	13	Unused
0	0	1	1	0x1800	0x1FFF	CS3	12	J1 (8279)
0	1	0	0	0x2000	0x27FF	CS4	11	U3 8155
0	1	0	1	0x2800	0x2FFF	CS5	10	U5 8155
0	1	1	0	0x3000	0x37FF	CS6	9	U11 8185
0	1	1	1	0x3800	0x3FFF	CS7	7	U8 8185

The memory block above 16K (0x4000 through 0xFFFF) is reserved for the two universal sockets U9 and U12 via active low Chips Selects /CS8 and /CS9. The high memory decode signal is asserted (driven low) for the entire address space where A15 is logic one, i.e., from 0x8000 through 0xFFFF and the middle memory decode signal is asserted for the remaining 16K address space from 0x4000 through 0x7FFF. Jumper JP12 is used to determine which universal site is assigned to which decoded address space. Shorting 1-2 and 3-4 in JP12 (jumpers horizontal) assigns /CS8 (U9 ZIF) to the middle 16K address block and /CS9 (U12) to the high 32K block. Alternatively, shorting 1-3 and 2-4 (jumpers vertical) assigns /CS8 (U9 ZIF) to the high 32K block and /CS9 (U12) to the middle 16K memory block.

MEMORY MAP

Address Range	Device	Note
0x0000 – 0x07FF	Base 8755 U2	
0x0800 – 0x0FFF	Expansion 8755 U4	
0x1000 – 0x17FF	No Connection	
0x1800	8279 Keyboard Controller - Read: Keyboard FIFO; Write: Display Data	
0x1900	8279 Keyboard Controller - Read: Status Word; Write: Command Word	
0x2000 – 0x27FF	Base 8155 U5	Foldback 2100-21FF, 2200-22FF, etc.
0x2800 – 0x2FFF	Expansion 8155 U5	Foldback 2900-29FF, 2A00-2AFF, etc.
0x3000 – 0x37FF	Base 8185 U11	Foldback 3400-37FF
0x3800 – 0x3FFF	Expansion 8185 U8	Foldback 3C00-3FFF
0x4000 – 0x7FFF	Middle 16K Memory Block	JP12 1-3:U12, JP12 1-2:U9 (ZIF)
0x8000 – 0xFFFF	Top 32K Memory Block	JP12 2-4:U9 (ZIF), JP12 3-4:U12

PORT MAP

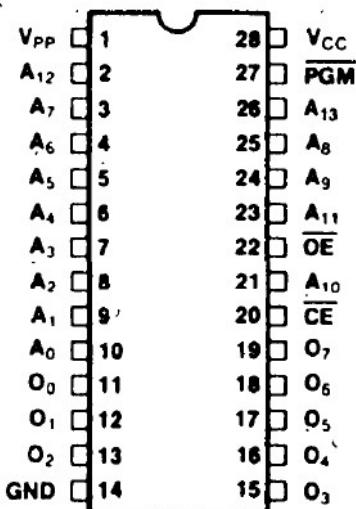
Port Address	Function	Note
0x00	Base Monitor ROM PORT A	
0x01	Base Monitor ROM PORT B	
0x02	Base Monitor ROM PORT A Data Direction Register	
0x03	Base Monitor ROM PORT B Data Direction Register	
0x08	Expansion ROM PORT A	
0x09	Expansion ROM PORT B	
0x0A	Expansion ROM PORT A Data Direction Register	
0x0B	Expansion ROM PORT B Data Direction Register	
0x20	Base RAM Command / Status Register	
0x21	Base RAM Port A	
0x22	Base RAM Port B	
0x23	Base RAM Port C	
0x24	Base RAM Low Order Byte of Counter Value	
0x25	Base RAM High Order Byte of Counter Value	
0x28	Expansion RAM Command / Status Register	
0x29	Expansion RAM Port A	
0x2A	Expansion RAM Port B	
0x2B	Expansion RAM Port C	
0x2C	Expansion RAM Low Order Byte of Counter Value	
0x2D	Expansion RAM High Order Byte of Counter Value	

UNIVERSAL MEMORY SOCKETS

Nearly from the very beginning, the industry recognized that the ever-increasing availability of larger and larger ROM devices was going to be problematic if a standard was not adopted. The design scheme resulted in the “Universal Site” Socket concept in-which all future ROMs, PROMs, and EPROMs would have pin mapping such that, with minor adjustments, the different sizes of EPROMS were compatible if bottom justified in the socket. The following graphic (lifted from the 1984 Intel Memory Components Handbook) is a typical example. The 27128 is shown in the center and the function of each pin on the left and the right is shown in the corresponding table on each side. This concept was eventually standardized by the Joint Electron Device Engineering Council (JEDEC) and the socket referred to as the JEDEC 28-Pin Universal Memory Socket.

27128A

27256	2764A	2732A	2716
V _{PP}	V _{PP}		
A ₁₂	A ₁₂		
A ₇	A ₇	A ₇	A ₇
A ₆	A ₆	A ₆	A ₆
A ₅	A ₅	A ₅	A ₅
A ₄	A ₄	A ₄	A ₄
A ₃	A ₃	A ₃	A ₃
A ₂	A ₂	A ₂	A ₂
A ₁	A ₁	A ₁	A ₁
A ₀	A ₀	A ₀	A ₀
O ₀	O ₀	O ₀	O ₀
O ₁	O ₁	O ₁	O ₁
O ₂	O ₂	O ₂	O ₂
Gnd	Gnd	Gnd	Gnd



2716	2732A	2764A	27256
V _{CC}	V _{CC}	V _{CC}	V _{CC}
PGM	N.C.	A ₁₄	A ₁₃
A ₈	A ₈	A ₈	A ₈
A ₉	A ₉	A ₉	A ₉
V _{PP}	A ₁₁	A ₁₁	A ₁₁
OE	OE/V _{PP}	OE	OE
A ₁₀	A ₁₀	A ₁₀	A ₁₀
CE	CE	CE	CE
O ₇	O ₇	O ₇	O ₇
O ₆	O ₆	O ₆	O ₆
O ₅	O ₅	O ₅	O ₅
O ₄	O ₄	O ₄	O ₄
O ₃	O ₃	O ₃	O ₃

NOTE: INTEL "UNIVERSAL SITE"-COMPATIBLE EPROM PIN CONFIGURATIONS ARE SHOWN IN THE BLOCKS ADJACENT TO THE 27128A PINS.

For example, pin 28 (top right) is not present on the 2716 or 2732, is the power input on the 2764, 27128, and 17256 whereas pin 26 (third from top right) is actually pin 24 on a 2716 or 2732 which it is their power input.

UNIVERSAL SITES ARE BOTTOM JUSTIFIED- When a memory device having fewer pins than the socket, it must be bottom justified, i.e., pin 1 of the EPROM is placed in pin 3 of the socket.

Each of the three memory sockets M1, M2, and M3 are JEDEC 28-pin universal sockets, and each has three configuration jumpers associated with that socket to configure the socket as required for the desired device. For clarity, these jumpers are referred to by the pin number of the socket which they are attached. For example M1.27 is controlled by JP2 which selects one of A14, +5V, or WR*. The same signal on M2 is JP6 and on M3 is JP13.

U9, U12 Jumper Settings

Pin	U9	U12	2732	2764	27128	27256	27512	6264	28C256	62256
Pin 1	JP4.2	JP11.2	Open	1-2	1-2	1-2	---	Open	A14	A14
Pin 26	JP2.2	JP9.2	2-3	Open	1-2	1-2	---	2-3		
Pin 27	JP3.2	JP10.2	Open	2-3	2-3	1-2	2-3	2-4		

U9, U12 Pin 1, Power or No Connection

JP4 and JP11 are installed to connect pin 1 of U9 or U12 respectively to +5V and left open to allow M1, M2, or M3 pin 1 to float. For the 2732 and 6264 this jumper is removed. For 2764s thru 27256 the jumper is installed. On M3 this jumper also provides a connection to A15 (JP7.2 – JP7.3) when a 27512 is installed.

U9 Pin 26 (JP2.2) Power (JP2.3) or A13 (JP2.1)

U12 Pin 26 (JP9.2) Power (JP9.3) or A13 (JP9.1)

JP2 and JP9 are installed in position 2-3 to connect pin 26 to +5V, i.e., to connect pin 24 of the 2732 to power. When using 2764s, pin 26 is unused and the jumper is removed entirely. When using 27128s or a 27257 the jumper is installed between 1-2 to connect address line A13. When using 6264 RAMs, the jumper is installed in position 2-3 to enable CE2

U9 Pin 27 (JP3.2) +5V (JP3.1), WR* (JP3.3), or A14 (JP3.4)

U12 Pin 27 (JP10.2) +5V (JP10.1), WR* (JP10.3), or A14 (JP10.4)

JP3 and JP10 are 1-of-3 jumpers used to determine control of pin 27 (which is connected to JP3.2 and JP10.2). Since pin 27 is not connected in a 2732, the actual position of JP3/JP10 are not applicable for a 2732. For a 2764

and 27128 pin 27 is the Program* pin which must be taken high for normal reads so JP6 is installed 2-1 to connect pins 27 to +5V. When using 27256 in U9 or U12, pin 27 must be controlled by Address line A14 to internally decode the EPROM, so the jumper is installed in position 1-2. For RAMs, pin 27 must be controlled by the system Write signal WR* so the jumper is installed between positions 2-3.

SERIAL INTERFACE

The utility of any single board computer is severely limited if it does not have a means of communication with a terminal or external device. For this reason, Intel included two serial communication lines in the base 8085, eliminating the need for an additional UART or USART component. These are the Serial Output Data (SOD) and Serial Input Data (SID) lines. Depending on the preferred communication standard, code is used in the 8085 to create or “bit-bang” a serial stream. In the case of the SDK-85+, this is RS-232 which is a bipolar serial stream consisting of a starting bit, data bits, stop bit, and parity bit. No other hardware handshaking is used on the SDK-85+. To create the bipolar output, a MAX232 (U14) is used which contains an internal charge pump to create the +/- rails necessary to meet the RS232 standard (+/- 14V typical for the MAX232). The 8085 SID and SOD lines pass through the MAX232 which inverts and level shifts the signals as required by RS232. With rails in the +/-12V range, the RS232 port on the SBC-85 will eat any TTL device connected to J2. If you want to use a TTL signal on J2, then remove U14 access the SID and SOD lines directly at the U14 connector. J2 can also be used to access the remaining unused drivers in U14 (cut the traces at TC1 and/or TC2 before using the respective driver).

The communication settings for the SDK-85+ Resident Monitor v1.1 are 2400, 8, N, 1 (Bit delay 0x51).
The communication settings for the SDK-85+ Resident Monitor v1.2 are 9600, 8, N, 1 (Bit delay 0x10).

8155 Timer Counter

The base 8155 counter tick input is controlled by the system clock and the timer out is used to TRAP the 8085 for use in the SDK-85+ monitor single step function.

The counter in the expansion 8155 can be configured as desired.

The following videos may be helpful in using the 8155 counter:

Programming the 8155 counter: https://youtu.be/kagzY65Z_Yg

Reading the 8155 remaining count: https://youtu.be/9_rI46dmt8

POWER INPUT

The SDK-85+ operates on +5VDC and is fitted with a 2.1mm x 5.5mm barrel connector with the tip positive and a well regulated +5VDC power supply should be used to power the SDK-85+. Vcc specifications on the 8085 are +5VDC +/- 10%. Depending on how much current is going out the I/O port and onto the bus, the SBC-85 will take about 3A of current. +5V power is provided to the keyboard / display board through J1.

CPU BOARD COMPONENT IDs and FUNCTIONS

CPU Board Headers, Jumpers, and Connectors	
ID	Function
J2	RS-232 DB9
J3	RST5.5, RST6.5, RST7.5, TRAP Patch Header or Jumper. Default: 1-2 (TRAP), 3-4 (RST7.5), 5-6 (RST6.5), 7-8 (RST5.5).
J4	26 position header for the 8755 U2 I/O
J5	26 position header for the 8755 U4 I/O
J6	Allow onboard signals to be wirewrapped to the offboard header J4
J7	Allow onboard signals to be wirewrapped to the offboard header J5
J8	8155 U3 I/O pins and J10 onboard wirewrap patch pins to take onboard signals off board
J9	8155 U5 I/O pins and J11 onboard wirewrap patch pins to take onboard signals off board
J10	allow onboard signals to be wirewrapped to the offboard headers J8
J11	allow onboard signals to be wirewrapped to the offboard headers J9
J12	Power input Barrel Connector: +5VDC, 5.5mm, Tip positive
J13	Uncommitted pull-up (R8, R9) and pull down (R12, R13) resistors
JP1	8755 U2 and 8755 U4 READY tie to 8085 READY. Default is open. Short either 1-2 or 2-3 to use U2 or U4 READY signal
JP2	U9 pin 26 configuration.
JP3	U9 pin 27 configuration. 1-2 to connect U12.1 to +5V
JP3	U12 pin 27 configuration.
JP4	U9 pin 1 configuration

CPU Board Headers, Jumpers, and Connectors

ID	Function
JP5	8755 U5 /Timer Out Jumper / Patch Point. Install to connect /TimerOUT to J11.4, J925
JP6	Provides selection of 8155 U5 TIMER IN signal between system clock and offboard I/O headers
JP9	U12 pin 26 configuration. To use a 6264 in U12, jumper 2-3 to take pin 26 (CE) to +5
JP10	U12 pin 27 configuration.
JP11	U12 pin 1 configuration. 1-2 to connect U12.1 to +5V
JP12	/CS8 and /CS9 mapping. Jumper 1-2 and 3-4 to map U9 (ZIF on /CS8) to 01xx_xxxx and U11 (/CS9) to 1xxx_xxxx. Jumper 1-3 and 2-4 to reverse and map U11 (/CS9) to 01xx_xxxx and U9 (ZIF on /CS8) to 1xxx_xxxx. The default is 1-3, 2-4 (i.e., both jumpers vertical) allowing the entire upper 32K to be mapped to the ZIF socket. The location of the signals in JP12 are shown in Figure 1. For the normal configuration of a 6264 in U12 and a 27256 in U9 (ZIF), jumper 1-3 and 2-4.



Figure 1. JP12 U9 and U11 memory mapping jumper signal location.

CPU Board Test Points

ID	Description
TP1	+5V bus test point Loop
TP2	Ground test point Loop
TP3	Ground test point Dupont
TP4	J1.4 uncommitted pass-through to keypad/display board
TP5	J1.18 uncommitted pass-through to keypad/display board
TP6	Display 8279 /EnableDisplay for override of display enable (addl jumper on display board)

CPU Board Diodes / LEDs

ID	Description
D1	+5V pull-down, accelerates the discharge of reset capacitor C5 if the +5 drops
D2	LED Board +5V power indicator

CPU Board RESISTORS

ID	Description
R1	/RD pull up resistors (4.7K – 10K)
R2	/WR pull up resistors (4.7K – 10K)
R3	charging resistor for reset RC
R4	READY pull up resistors (4.7K – 10K) if 8755 U2 or U4 is unused
R5	current limiting resistor for D1 (~500 ohms to 1K; adjust for desired LED brightness)
R6	Keypad RST6.5 pull down resistors (4.7K – 10K) if keypad not used
R7	Keypad RST7.5 pull down resistors (4.7K – 10K) if keypad not used
R8, R9	Uncommitted pull-up resistors. User specified
R10	HOLD pull down resistors (4.7K – 10K)
R11	INTR pull down resistors (4.7K – 10K)
R14	Uncommitted pull down resistors. User specified
R13	10K pull up resistor for RS232 input when terminal disconnected
R14	Uncommitted pull down resistors. User specified
R15	1K discharge resistor for Reset capacitor C5
R16	10K pull down resistor for SID when SW2 set to keypad mode

CPU Board SWITCHES

ID	Description
SW1	Resets the CPU by taking the RESET IN* to ground

Versions 1.1+ Additional Switches

SW2	SPDT toggle switch to enable / disable serial port in SDK-85 Monitor
-----	--

CPU Board SKIPPED ID NUMBERS

J12, U10, JP7, JP8

CPU Board Trace Cut Points

ID	Description
TC1	Tie the unused input MAX232 U14.11 T1.IN to ground
TC2	Tie the unused input MAX232 U14.13 R1.IN to ground

CPU ASSEMBLY NOTES AND PROCEDURES

– Most of these are important (or useful)

- For most footprints on the PCB, pin 1 is identified as the square pad.
- When buying components, this is my general advice—in almost all cases I design for the 74LS family. If you can find components in the 74LS, great. If not, try the 74ALS family, 74F, or 74HCT which are all TTL compatible with the 74LS. (Note that the 74HC is NOT TTL).
- Tantalum capacitors in KiCAD have pin 1 of the footprint as the positive terminal, however footprints for LEDs are the opposite and have pin 2 as positive. For both LEDs and the polarized capacitors, if one lead is longer than the other that is the positive lead (anode on LEDs).
- Power up the board before inserting any ICs to confirm there are not shorts in the power supply rails. The tantalums can take a good deal of reverse voltage, do not expect them to blow for another hundred hours of operation if any are installed backwards. That will happen totally out of the blue.
- Install the cheap ICs first, then power on and continue in increments.
- CPU – Keyboard / Display connection. Can install vertical or right angle headers and use short ribbon cable between boards. Or can install male and female vertical headers (e.g., male header on CPU board and female vertical receptacle on the solder side of the keyboard / display board).
- CPU Board Assembly Order: Mount components from physically lowest profile to tallest. So that the board can always be flat on the bench to solder, my preference is the following order:
 - Resistors. To reduce the chance of error, install all of one value before going on to the next
 - Small 0.1uF decoupling capacitors. Not polarized
 - Small LEDs, polarity matters
 - Crystal
 - IC sockets—solder two corners of all sockets while laying face down on the bench. Then pick up the board and one at a time gently press on each socket (gentle enough to not push out the pin) and remelt the solder for that corner. Typically there will be a little snap as the socket fully reseats onto the board.
 - Test points
 - 1uF tantalum capacitors. Polarity matters
 - Reset Switch (holes on rectangle, not square but switch is internally symmetric with 180° flip, so will fit at 0° and 180°)
 - Electrolytic capacitors, polarity matters
 - Jumpers & vertical headers EXCEPT J1 TO THE KEYPAD DAUGHTERBOARD. For the 1-of-3 (JP3, JP10), install a jumper when soldering the wing pins to make sure they are aligned.
 - Large LEDs, polarity matters
 - Barrel connector
 - DB9
 - ZIF socket
 - Insert the J1 extended male header but do not solder. Then use whatever standoffs you are going to use between the CPU and display board to mount the display board and **then** solder the J1 header.

DIAGNOSTIC NOTES

Hot or Dead MAX232-

- Check the charge pump capacitors are correctly installed (polarization)

CPU REVISIONS, PATCHES, AND CHANGE REQUESTS

Revisions

v1.0 week 2622

v1.1 week 3223

- Correct pin location on JP3 and JP10. Move Pin 27 needs to be in middle so pins 2&3 were swapped.
- Reconfigured 8085 Restart inputs with J3. Jumper straight across for normal use with keypad or wirewrap
- Remove JP5 and connect CLK directly to U3 8155 Timer In for use with monitor Single Step
- Add 10K pullup from MAX232 pin 14 (unused RS232 output held high) to pin 8 (RS232 RX) so when serial is disconnected the monitor detects terminal is not connected and utilizes keypad.
- On header J1 to keyboard/display board, remove BD, bring pin to wire wrap point.
- On header J1 to key/display bring pin 23 to test point as /ENABLE_DISP
- Add silkscreen to indicate jumper pinouts
- Add bleed resistor to SW1 reset

CPU Future Change Requests

- Add a speaker output on a DIO?

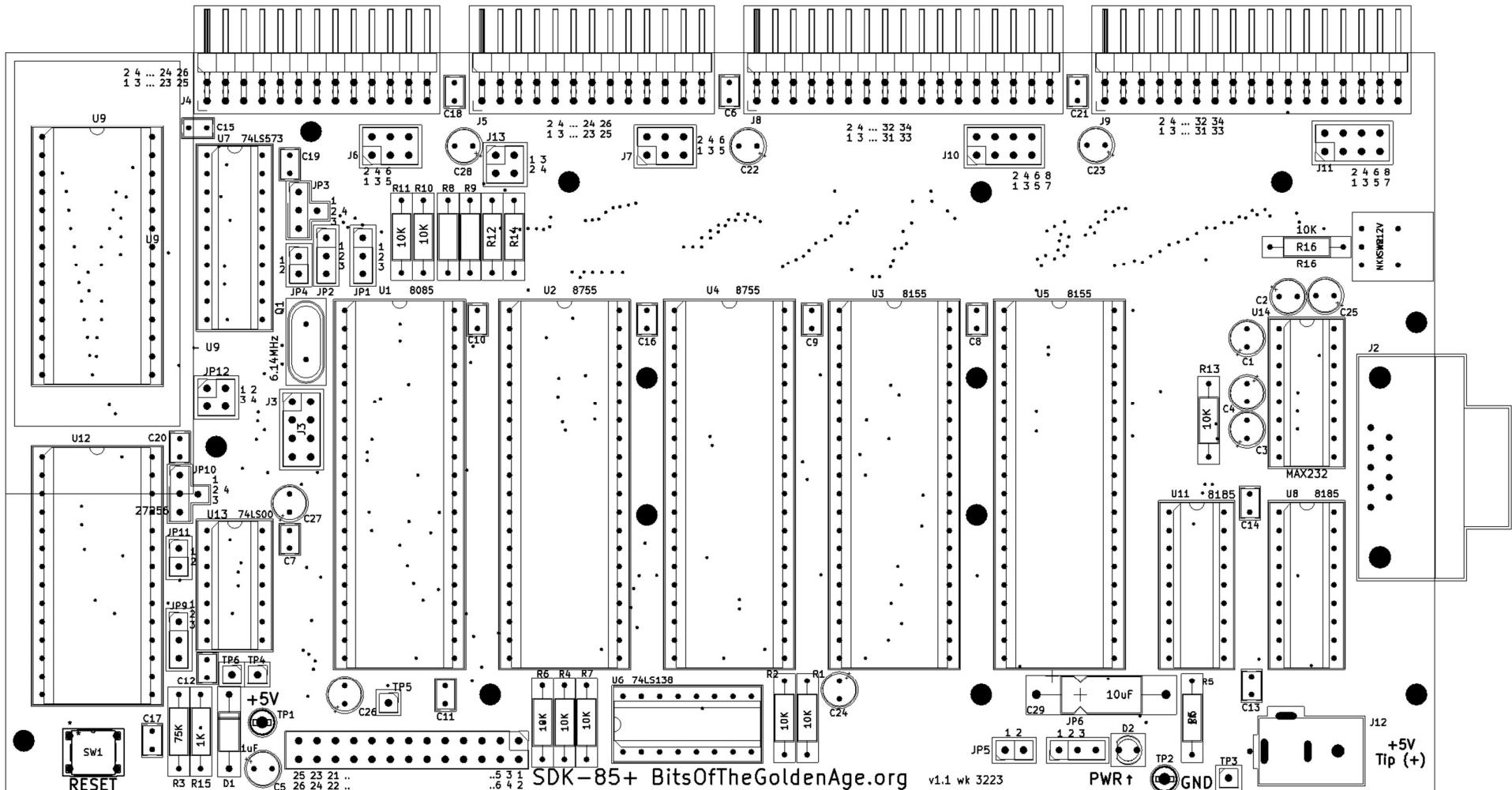
COMPONENT PLACEMENT – SCHEMATICS – BOM

Component placement, schematics, and the bill of materials are on the following pages in reverse chronological order. Higher resolution PDF schematics are available on the BitsOfTheGoldenAge.org project website.

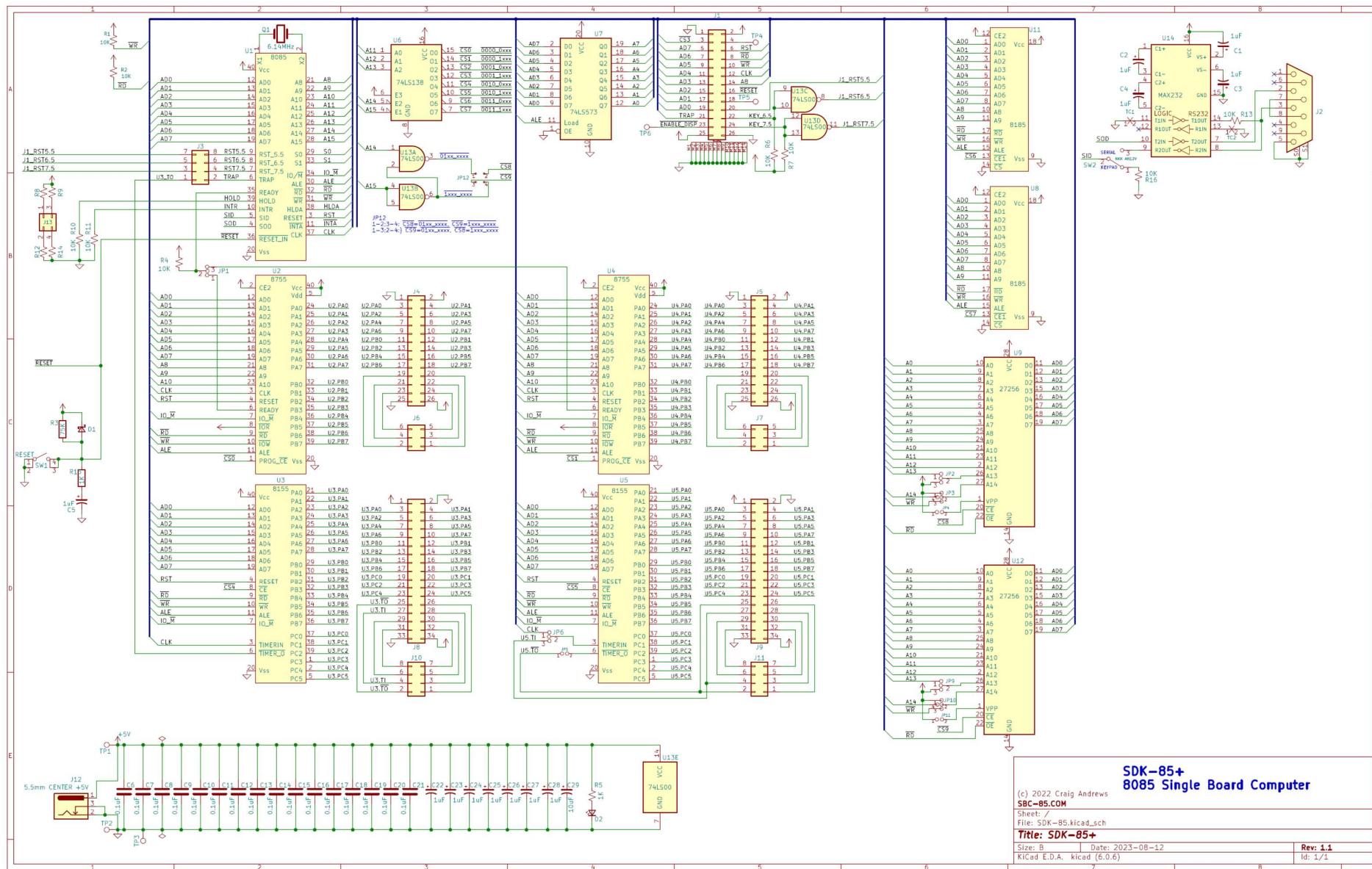
Note that in the CPU board schematics, U9 and U12 are ‘universal sites’ and the actual memory used is bottom justified if the chip has fewer pins than the socket. This means for a 2732, for example, 2732 pin 1 is in pin 3 of the socket, 2732 pin 24 is in pin 26 of the socket. Each pin on the IC is two pins higher when looking at the schematic. The graphic in an earlier section titled Universal EPROM Sockets may be a useful reference.

CPU v1.1 COMPONENT PLACEMENT – SCHEMATICS – BOM

Component Placement v1.1



CPU Schematic v1.1



SDK-85+ v1.x

Sep. 2, 23

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Page 14 of 28

SDK-85+
8085 Single Board Computer

(c) 2022 Craig Andrews
SBC-85.COM

Sheet: / File: SDK-85.kicad_sch

Title: **SDK-85+**

Size: B | Date: 2023-08-12

KiCad E.O.A. kicad (6.0.6)

Rev: 1.1

Id: 1/1

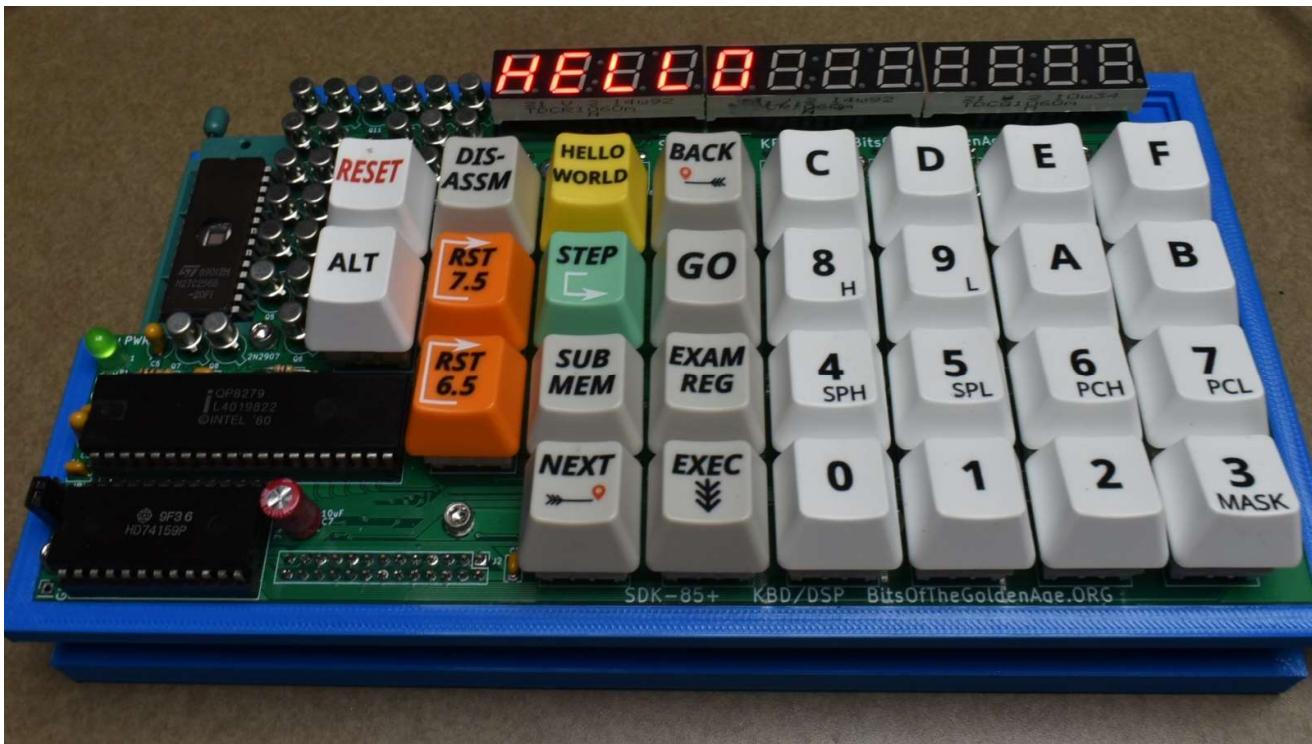
SDK-85+ CPU v1.1 BOM

QTY	Name	Value Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
1	PCB	SDK-85+ CPU v1.1 CARD	BitsOfTheGoldenAge.ORG		
16	C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21	Capacitor, Ceramic, 0.1UF 50V Radial	kemet	C315C104M5U5TA	399-4151-ND
12	C1, C2, C3, C4, C5, C22, C23, C24, C25, C26, C27, C28	1μF Conformal Coated Tantalum Capacitors 35V Radial 8Ohm	avx	TAP105M035SCS	478-5812-ND
1	C29	10μF Electrolytic Capacitor, 16V			
1	D2	Power LED			
1	D1	Schottky (e.g., BAT41 or BAT46 whatever it takes) or germanium (e.g., 1N270), any low V _f diode will do			
3	JP4, JP5, JP11	Connector, 2 position, 1x2, vertical, 0.1"			
4	JP1, JP2, JP6, JP9	Connector, 3 position, 1x3, vertical, 0.1"	Sullins connector Solution	PREC003SAAN-RC	S1012EC-03-ND
2	JP3, JP10	Connector, 4 position, "T" pattern, vertical, 0.1" (1 OF 3 T)			
1	JP12	Connector, 4 position, 2x2, vertical, 0.1"			
1	J1	(top mounted ribbon cable) CONN HEADER VERT or R/A 26 POS 2.54MM	Sullins connector Solution		
		Bottom mounted extended header for board-to-board	Samtec Inc.	TSW-123-15-F-D	SAM15395-ND
1	J2	9 Position D-Sub Receptacle R/A, Female Sockets Connector	Amphenol ICC	D09S13A4GX00LF	609-1484-ND
2	J4, J5	CONN HEADER VERT or R/A 26 POS 2.54MM	Sullins connector Solution		
2	J8, J9	CONN HEADER VERT or R/A 34 POS 2.54MM	Sullins connector Solution		
3	J3, J10*,J11*	Connector, 8 position, 2x4, vertical, 0.1"	Sullins connector Solution		
2	J6*,J7*	Connector, 6 position, 2x3, vertical, 0.1"			
1	J12	Power Barrel Connector Jack 2.10mm ID (0.083"), 5.50mm OD (0.217") Through Hole, Right Angle	CUI	PJ-050AH	CP-050AH-ND
1	J13	Connector, 4 position, 2x2, vertical, 0.1"			
1	TP1*	Loop Test Point .065 RED	keystone electronics	5005	36-5005-ND
1	TP2*	Loop Test Point .065 BLACK	keystone electronics	5006	36-5006-ND
1	TP3*	1-pin dupont connector			
1	Q1	6.144MHz Crystal HC49/US	CTS frequency controls	ATS061B	CTX899-ND
1	R3	Resistor, carbon, 75K 1/4W, 5%	stackpole	CF14JT75K0	CF14JT75K0CT-ND
4	R8, R9, R12, R14	User specified pull up / pull down resistors to J13			
10	R1, R2, R4, R6, R7, R10, R11, R13, R15, R16	Resistor, carbon, 10K 1/4W 5%	stackpole	CF14JT10K00	CF14JT10K00CT-ND
1	R5	Resistor, carbon, 1K 1/4W 5%	stackpole	CF14JT600R	CF14JT600RCT-ND
1	SW1	Tactile Switch SPST-NO Top Actuated Through Hole 0.1A 32V	TE Connectivity	1825910-7	450-1804-ND

SDK-85+ CPU v1.1 BOM

QTY	Name	Value Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
1	SW2	SPDT toggle switch	NKK Switches	A12AH	360-2975-ND
1	U1	74LS273			
1	U1	8085			
2	U2, U4	8755			
2	U3, U5	8155			
2	U8, U11	8185 1K RAM			
1	U6	74LS138			
1	U7	74LS573	Texas Instruments	SN74HCT573N	296-1621-5-ND
1	U13	74LS00	Texas Instruments	SN74LS00N	
1	U14	IC TRANSCEIVER FULL 2/2 16DIP MAX232	Texas Instruments	MAX232N	296-1402-5-ND
2	U9*, U12*	2732-27256, 6264-62256			
1	U13	14-pin DIP Socket			
2	U6, U14	16-pin DIP Socket			
2	U8, U11	18-pin DIP Socket			
1	U7	20-pin DIP Socket 0.3"			
1	U12	28-pin DIP Socket			
1	U9	28-pin ZIF DIP socket			
5	U1, U2, U3, U4, U5	40-pin DIP Socket			
		CONN JUMPER SHORTING .100"		QPC02SXGN-RC	S9337-ND
1	AC/DC DESKTOP ADAPTER 5V 20W*	Power Supply 2.1mm x 5.5mm 5V 20W TIP Positive	Phihong USA	PSAC30U-050L6	993-1343-ND
*Optional Component					

SDK-85+ KEYPAD AND DISPLAY BOARD



KEYPAD / DISPLAY BOARD CIRCUIT DESCRIPTION

Keypad / Display Board Primary Components	
ID	Description
U1	74159 1-of-16 decoder
U2	8279 Keypad and Display Controller
Q1-Q8	Display Segment Anodes
Q9-Q26	Display Digit Cathodes
DS1-DS3	4-digit, 7-segment Common Cathode Displays
SW1-SW24	Scanned Matrix Input Keys
SW25	Configurable Input Key
SW26-SW29	Dedicated function hardwired pull-down keys

8279 Keypad / Display Controller

The 8279 is operated in the “encoded” mode, i.e., the 8279 outputs a binary value on SL0 through SL3 to identify a single row of the keypad to scan and a single display to illuminate. This binary output provided to the 74159 one-of-four decoder / demultiplexer to select one of its sixteen outputs. Scan Lines CS1, CS2, and CS3 are used for the keypad with CS1 selecting hexadecimal keys 0 through 7, CS2 selecting hexadecimal keys 8 through F, and CS3 selecting the function keys EXEC, NEXT, GO, SUBST MEM, EXAM REG, SINGLE STEP, F2, and F3.

The 8279 has two additional hardwired inputs named CONTROL (pin 37) and SHIFT (pin 36). The function of these inputs depends on the operating mode of the keyboard. In scanned keyboard mode, the status of these two inputs creates the two most significant bits of the key closure ID, with CONTROL being the MSBit and SHIFT being the second MSBit. The next three lower bits are the key row and the lowest three bits is the key column.

SW25 Important Note:

While the SDK-85+ keypad uses the SHIFT as a standard input and the CONTROL key as a configurable input, Intel’s SDK monitor (and SDK-85+ monitor through v1.1) uses the MSBit as a character available flag and therefore clears these top two bits before saving the keystroke in the IBUFF memory location (0x20FE). Beginning in v1.2 of the SDK-85+ Resident Monitor, the instruction to clear the top two bits (**ANI 03FH**) has been replaced with an instruction

to flip the top two bits (**XRI 0xC0**). This requires the most significant bit to be set so that when it is moved into IBUFF it is zero to indicate a character is available. If using the resident monitor, SW25 may be used to clear the CNTL bit of the keyboard character byte. However, because that CNTL is flipped and used to fill IBUFF, taking CNTL low will prevent the monitor from recognizing the keystroke.

In matrix mode, these two inputs (CONTROL and SHIFT) are ignored. In Strobed Input mode, the status of the return lines is read into the FIFO on the rising edge of the CONTROL input.

The keypad configuration, key position, display RAM locations, and segment assignment are given in the following tables:

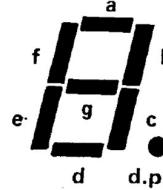
Keypad Configuration								
Scan Line	MSBit							LSBit
	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
1	7	6	5	4	3	2	1	0
2	F	E	D	C	B	A	9	8
3	F3	F2	SINGLE STEP	EXAM REGISTER	SUBSTITUTE MEMORY	GO	NEXT	EXECUTE

Physical Key Location and Decoded Return Code							
RESET	F1 _{1F}	F2 ₁₆	F3 ₁₇	C _{0C}	D _{0D}	E _{0E}	F _{0F}
SHIFT	RST 7.5	SINGLE STEP ₁₅	GO ₁₂	8 ₀₈	9 ₀₉	A _{0A}	B _{0B}
	RST 6.5	SUBST MEM ₁₃	EXAM REG ₁₄	4 ₀₄	5 ₀₅	6 ₀₆	7 ₀₇
		NEXT ₁₁	EXECUTE ₁₀	0 ₀₀	1 ₀₁	2 ₀₂	3 ₀₃

8279 Display RAM Location		
Location	Display	Note
0	Left Most Digit D0	Resident Monitor Address Field D ₃ Left (MSB)
1	Digit D1	Resident Monitor Address Field D ₂
2	Digit D2	Resident Monitor Address Field D ₁
3	Digit D3	Resident Monitor Address Field D ₀ Right (LSB)
4	Digit D4	Resident Monitor Address Field – Data Field Gap
5	Digit D5	Resident Monitor Data Field Left (MSB)
6	Digit D6	Resident Monitor Data Field Right (LSB)
7	Digit D7	
8	Digit D8	
9	Digit D9	
10	Digit D10	
11	Right Most Digit D11	

Segment Display Format. 7-segment display elements are identified as segments **a** through **g** starting at the top segment and going clockwise, ending at the middle segment '**g**'. In the 8279 Display RAM Output Designation, these are mapped as follows:

Segment Assignment								
Bit	MSBit							LSBit
Display Designation	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Segment Assignment	d	c	b	a	d.p.	g	f	e



The hardware is designed so that writing a zero into a bit position turns ON the corresponding LED segment. For example, writing 1001 1001 (0x99) would illuminate segments c,b,g,f and display the number "4".

8279 Keypad / Display Controller Interrupt Mode vs Polling Mode

All versions of the keypad/display board are completely compatible with the 8279 interrupt mode of the SDK-85 monitor. The 8279 IRQ is connected to the 8085 RST5.5 via the CPU (J1) to KeyDisp (J2) board-to-board connection.

KEYPAD / DISPLAY BOARD COMPONENT IDs and FUNCTIONS

Keypad / Display Board Headers, Jumpers, and Connectors	
ID	Description
J1, J3	Optional printed flexible cable connector if display sub-board is separated from main Keypad. If not cut, these traces extend through the connectors to the display sub-board.
J2	26-position header from CPU board
JP2	U1 decoder enable /E1. Jumper 1-2 to control /E1 via the 26 pin header to the CPU board. Normally jumper 2-3 to leave enabled
JP4	Switch 25 (F1) output select. Connect pin 1 (SW25) to one of the following outputs. Default is 1-2 to include SW25 in matrix scan. <ul style="list-style-type: none"> • 2 = Keypad scan row 3, Return Line 7 • 3 = TRAP • 4 = J2.4 • 5 = J2.18 • 6 = CNTL input to 8279 (U2.37)
JP5	Switch 25 (F1) input select. Connect pin 1 (SW25) to one of the following outputs. Default is 1-2 to include SW25 in matrix scan. <ul style="list-style-type: none"> • 2 = 8279 Return Line 7 • 3 = Pull up via R36 (user determined value) • 4 = Pull down via R37 (user determined value)

Keypad / Display Board Test Points

ID	Description
TP1, TP3	Ground test point

Keypad / Display Board Diodes / LEDs

ID	Description
D1	Board +5V power indicator
D2-D9	Keypad Scan Logical AND diodes. Any low Vf diode such as BAT41

Keypad / Display Board RESISTORS

ID	Description
R1-R8	Display segment anode transistor Base-- 3K
R9-R16	Display segment anode transistor Collector-- 24 Ohm
R17-R34	Display Cathode transistor Base – 270 Ohm
R35	current limiting resistor for D1 (~500 ohms to 1K; adjust for desired LED brightness)
R36, R37	User determined pull up / pull down resistors for SW35

Keypad / Display Board SWITCHES

ID	Description
SW1-SW8	8279 Scan Row 0
SW9-SW16	8279 Scan Row 1
SW17-SW24	8279 Scan Row 2
SW25	Function (F1) key configured via JP4 and JP5. If include in matrix scan it is Row 4, bit 7
SW26	Resets the CPU by taking the <i>RESET IN*</i> to ground via J2.16
SW27	8279 SHIFT input (U2.36)
SW28	Vector Interrupt 7.5 via J2.24
SW29	Vector Interrupt 6.5 via J2.22

Keypad / Display Board TRANSISTORS

ID	Description
Q1-Q8	Display Segment Anode transistor 2907A
Q9-Q26	Display Cathode transistors 2907A

SWITCH 25 CONFIGURATION

Switch SW25 is user configured via JP4 and JP5. It can be made a normal member of the scanned keypad matrix, it can be used to initiate a TRAP interrupt, it can be used to set the CNTL bit of the character byte, or it can be patched back through to the CPU board via either of two pins in the board-to-board header.

- Matrix Scan – Default Configuration
 - On keypad/display board as SCAN 3 RETURN 7 (0x1F)
 - Jumper JP4.1 to JP4.2
 - Jumper JP5.1 to JP5.2
- Character CNTL (MSBit)--- NOTICE: See *SW25 Important Note*: on page 17.
 - On keypad/display board
 - Jumper JP4.1 to JP4.6
 - Jumper JP5.1 to JP5.4
 - Insert 0-Ohm pull-down resistor in R27
- TRAP input--J1.21 directly connects TRAP on the Keypad/Display board to the 8085 TRAP. To use SW25 to trigger a TRAP interrupt:
 - On CPU board
 - Remove any jumper from J3.1 to J3.2.
 - Wirewrap from J3.2 to J13.2 and insert a 10K pull-down resistor as R12
 - On keypad/display board
 - Jumper JP4.1 to JP4.3
 - Jumper JP5.1 to JP5.4
 - Insert 0-Ohm pull-down resistor in R27

KEYPAD / DISPLAY ASSEMBLY NOTES AND PROCEDURES

– Most of these are important (or useful)

- For most footprints on the PCB, pin 1 is identified as the square pad.
- Tantalum capacitors in KiCAD have pin 1 of the footprint as the positive terminal, however footprints for LEDs are the opposite and have pin 2 as positive. For both LEDs and the polarized capacitors, if one lead is longer than the other that is the positive lead (anode on LEDs).
- Power up the board before inserting any ICs to confirm there are not shorts in the power supply rails. The tantalums can take a good deal of reverse voltage, do not expect them to blow for another hundred hours of operation if any are installed backwards. That will happen totally out of the blue.
- Install the cheap ICs first, then power on and continue in increments.
- CPU – Keypad / Display connection. Can install vertical or right angle headers and use short ribbon cable between boards. Or can install male and female vertical headers (e.g., male header on CPU board and female vertical receptacle on the solder side of the Keypad / display board).
- Keypad / Display Board Assembly Order: Mount components from physically lowest profile to tallest. So that the board can always be flat on the bench to solder, my preference is the following order:
 - (if used) Flat Printed Display Cable Connectors on Solder Side
 - Resistors. To reduce the chance of error, install all of one value before going on to the next
 - Diodes
 - Small 0.1uF decoupling capacitors. Not polarized
 - IC sockets—solder two corners of all sockets while laying face down on the bench. Then pick up the board and one at a time gently press on each socket (gentle enough to not push out the pin) and remelt the solder for that corner. Typically there will be a little snap as the socket fully reseats onto the board.
 - Display Sockets – I install a display when soldering to make sure sockets are straight and aligned
 - Test points
 - Jumper JP2 (or strap)
 - Transistors (A 3D printed transistor jig is extremely useful and can be downloaded from project site)
 - 1uF tantalum capacitors. Polarity matters
 - Power LED

- Key Switches. If using Kailh switches, an alignment jig is extremely useful and can be downloaded from the project site. If using Cherry Keys with alignment pins, they will self align and the jig is not needed.
- Electrolytic capacitors, polarity matters
- JP4 and JP5 (install header & wirewrap or (default) strap 1-2 on solder side of board)
- Solder Side 26-Position Female Header
- Displays and Keycaps (and JP2 shorting plug if not directly strapped)

KEYPAD / DISPLAY REVISIONS, PATCHES, AND CHANGE REQUESTS

Revisions

V1.0 week 2622 In-House Prototype

v1.0a week 2823

- Expanded F1 key jumper configuration to allow F1 to be included in scan matrix
- Added additional bulk capacitance C7
- Added signal diodes to keypad cathode select lines.
- Added /RESET and /ENABLE select jumper to 74159

V1.1 week 3223

- /E0 on U1 (74159 1-of-16 decoder) changed from /RESET to RST

Required Patches

- None Identified

Keypad / Display Future Change Requests

- None Identified

DIAGNOSTIC NOTES

Shift Key Not Recognized (key directly below RESET)

As it was ported over from Intel's original SDK-85 Resident Monitor, the default SDK-85+ Resident Monitor leaves in place the clearing of the two most significant bits of the key character. See the note under 8279 Keypad / Display Controller on page 17.

Keypad / Display Test Utility

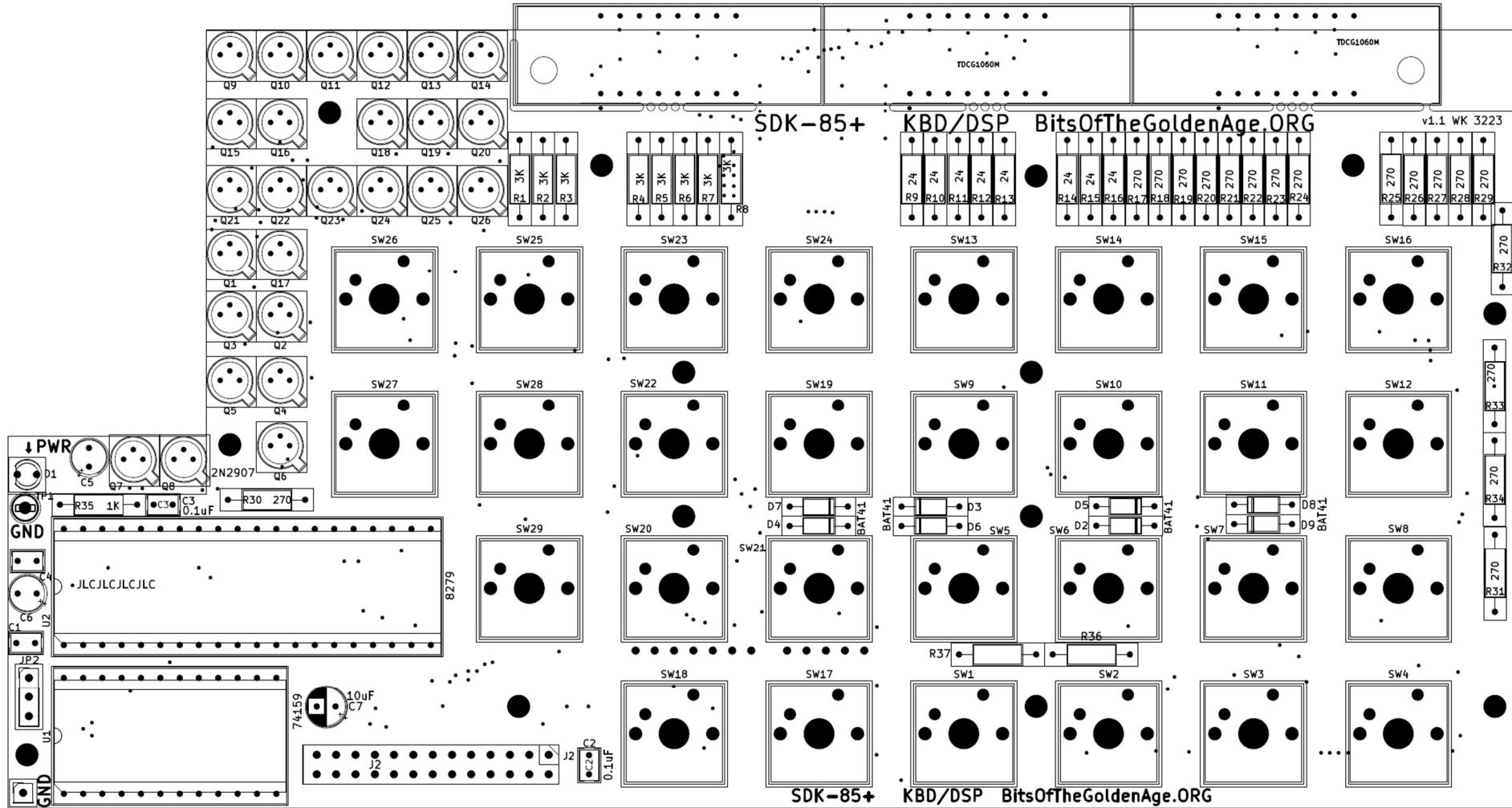
A test utility program for the keypad / display is on the project site (<https://bitsofthegoldenage.org/download/sdk-85-displaykeytest/>). This utility is programmed located at 0x8000 and is programmed into an EPROM in the ZIF socket (with default address mapping). The program operates under the SDK-85+ Resident Monitor and steps the word **HELLO** across the display from left to right. If a key is pressed (or a sequence of keys), the key row/column is displayed as they keys were entered into the 8279 FIFO.

KEYPAD / DISPLAY COMPONENT PLACEMENT – SCHEMATICs – BOM v1.1

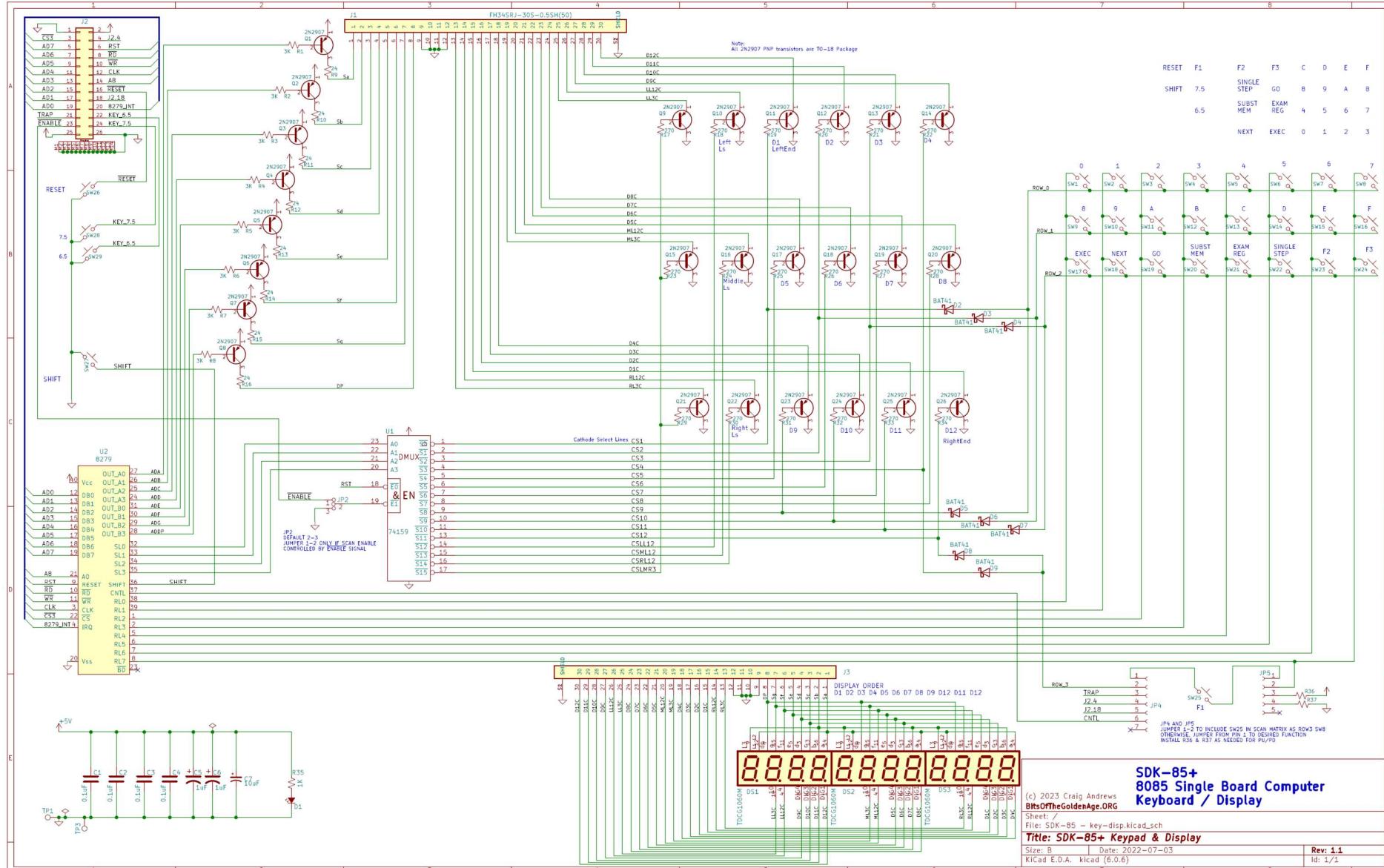
Component placement, schematics, and the bill of materials are on the following pages in reverse chronological order. Higher resolution PDF schematics are available on the BitsOfTheGoldenAge.org project website.

KEYPAD / DISPLAY v1.1 COMPONENT PLACEMENT – SCHEMATICS – BOM

KEYPAD / DISPLAY COMPONENT PLACEMENT v1.1



KEYPAD / DISPLAY SCHEMATIC v1.1



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KEYPAD / DISPLAY BOM v1.1

SDK-85+ Keypad / Display v1.1 BOM

QTY	Name	Value Package/description	Manufacturer	Manufacturer PN	DIGI KEY PN
1	PCB	SDK-85+ Keypad and Display v1.0a CARD	BitsOfTheGoldenAge.ORG		
4	C1, C2, C3, C4	100nF CAP CER 0.1UF 50V Z5U RADIAL KEMET	kemet	C315C104M5U5TA	399-4151-ND
2	C5, C6	1μF Conformal Coated Tantalum Capacitors 35V Radial 8Ohm	avx	TAP105M035SCS	478-5812-ND
1	C7	10μF Electrolytic Capacitor, 16V			
1	D1	LED, your preferred color for power			
3	DS1, DS2, DS3	Four character 7-segment clock display	Vishay	TDCG1060M (green)	TDCG1060M-ND
				TDCR1060M (red)	TDCR1060M-ND
8	D2-D9	Schottky (e.g., BAT41 or BAT46 whatever it takes) or germanium (e.g., 1N270), any low V _f diode will do			
2*	J1*, J3*	FH34SRJ-30S-0.5SH(50) printed flexible cable connector	Hirose Electric Co Ltd	FH34SRJ-30S-0.5SH(50)	HFT430CT-ND
1*	Display Cable*	CABLE FFC 30POS 0.50MM 2" long	Molex	0151660317	WM11310-ND
1	J2	26-position dual row 0.1" pitch female (solder side for direct connection) or male (component side + ribbon cable) header			
1	JP2	CONN HEADER VERT 3POS 2.54MM (or just solder a strap)	Sullins connector Solution	PREC003SAAN-RC	S1012EC-03-ND
1	TP1	PC TEST POINT .065 HOLE COMPACT BLACK	keystone electronics	5006	36-5006-ND
26	Q1-Q26	2N2907A Transistor TO-18	Purchase from Anchor Electronics		
8	R1-R8	RES 3K OHM 1/4W 5% AXIAL	stackpole	CF14JT3K0	CF14JT3K0CT-ND
8	R9-R16	RES 24 OHM 1/4W 5% AXIAL	stackpole	CF14JT24R	CF14JT24RCT-ND
1	R35	RES 1K OHM 1/4W 5% AXIAL Or adjust value for brightness	stackpole	CF14JT1K0	CF14JT1K0CT-ND
16	R17-R34	RES 270 OHM 1/4W 5% AXIAL	stackpole	CF14JT270R	CF14JT270RCT-ND
29	SW1-SW29	Cherry MX Type Key Switch			
		Kailh Box Switch White (I prefer Clicky)			
1	Keycap set	WASD Keyboards Custom Art Cherry MX Keycaps - WASD Keyboards Or Tindie SDK-85+ Keycap set from Bits Of The Golden Age on Tindie Keycap Design File Download: https://bitsofthegoldenage.org/download/wasd-keyboards-keycap-design-file/			
1	U1	74159 1-of-16 decoder			
1	U2	8279 Keypad / display Controller			
1	U1	24-pin DIP Socket			
1	U2	40-pin DIP Socket			
1		CONN JUMPER SHORTING .100"		QPC02SXGN-RC	S9337-ND
2*	Hinges*	TorqMaster, Inc. SB-188-SB-115 &116 (short) or SB-188-SB-108&109 (long)	Torqmaster.com		

*Optional Component

DEFINITIONS OF TERMS AND NOTATION

0xF

Hex Interpretation of 4 binary bits (nibble), in this example HEX F which is 1111 in binary

0xFF

Hex Interpretation of 8 binary bits (byte), in this example HEX FF which is 1111 1111 in binary

0xFFFF

Hex Interpretation of 16 binary bits or Word (two bytes). In this example HEX FFFF is the interpretation of the binary value 1111 1111 1111 1111

Address Decoding

The process (decoding) or part of the circuit (decoder) that determines which addresses are assigned to which memory or I/O device and, typically, results in the enabling of one specific memory or I/O device on the board or system.

A_n

Individual Address Line where n is 0-15

AD_n

Individual Multiplexed Address / Data line where n is 0-8

BOM

Bill of Materials

Buffer (also driver)

A device that ‘re-drives’ or buffers a signal to unload (or separate from) the original signal.
One direction (see also transceiver)

Byte

8-bits

Component Side

The ‘top’ of the PC board where the components are mounted. On the SBC-85 this is the side with the bulk of the silkscreen and the component numbers and footprints.

Contention (e.g., bus contention or signal contention)

A condition where two or more devices are simultaneously attempting to drive the same signal or bus. Technically, I suppose ‘contention’ only occurs when they disagree as to what the status of the signal or bus should be, e.g., one is pulling high while the other is pulling low but neither is enjoying the situation.

CS/ or CS*

Chip Select (reverse, a.k.a., negative logic) where a logic LOW (0v) is active

Decoding (Memory or I/O)

The process of determining which specific device should be enabled given any memory or I/O address.

EPROM

Erasable Programmable, Read Only Memory. A non-volatile memory device that can repeatedly be erased (generally by exposing to a UV light source) and field programmed. Compare to ROM, PROM, and EEPROM

EEPROM

Electrically Erasable Programmable, Read Only Memory. A non-volatile memory device that can repeatedly be erased and programmed, typically in-circuit. Compare to ROM, PROM, and EPROM

JEDEC Socket

Joint Electron Device Engineering Council standardized memory socket that can be configured to accept any JEDEC compliant memory chip within the design range of the socket.

I/O

Input / Output

I/O Mapped I/O

An address decoding scheme where the I/O ports are mapped using the address lines AND requiring that the *IO/M* signal be at logic LOW*. In this configuration, a port instruction such as OUT 23H would write only to the I/O port that decodes to address 23H. The instruction LDA 2323H will only read from the memory location at 2323H. See also *Memory Mapped I/O*.

LSB

Least Significant Byte. On a multibyte word this is the byte with the least weight, i.e., the furthest towards the right. E.g., the '34' in the word 0x1234

LSBit

Least Significant Bit. The bit with the least weight, i.e., the furthest towards the right. E.g., in the byte 11111110 the least significant bit is the '0'

Memory Mapped I/O

An address decoding scheme where the I/O ports are intermixed and use the same addresses as memory and the *IO/M* signal is not used*. In this configuration, there is no differentiation between memory and I/O. As an example, a port instruction such as OUT 23H will write not only to the I/O port that decodes to address 23H but it would write to the memory location at 2323H. Likewise, the instruction LDA 2323H will read the contents of Port 23H. The advantage of memory mapped I/O is that any memory instructions can be used to access I/O ports. The disadvantage is that I/O port addresses must be set to not overlap with any memory locations. See also *I/O Mapped I/O*.

MSB

Most Significant Byte. On a multibyte word this is the byte with the highest weight, i.e., the furthest towards the left. E.g., the 'AB' in the word 0A12 Be careful not to confuse a leading zero as the MSB such as in the byte 0A3H where the leading zero is required for many assemblers

MSBit

Most Significant Bit. The bit with the most weight, i.e., the furthest towards the left. E.g., in the byte 10000000 the most significant bit is the '1'.

Nibble

4-bits, half a byte.

OBP

On Board Port.

On

Logic TRUE or active. May be HIGH (+5V) or LOW (0V)

Off

Logic FALSE or inactive. May be HIGH (+5V) or LOW (0V)

o.c. (Open Collector or Open Drain)

A form of device output where the driving device can only pull the logic level low (e.g., to 0V in TTL). Since no output can drive the circuit, multiple open collector outputs can be tied together. Typically a pull-up resistor takes the circuit to logic one (+5V) if none of the open collector outputs are actively pulling the circuit low.

PROM

Programmable Read Only Memory. A non-volatile memory device that can be field programmed, and is typically One Time Programmable (OTP). Compare to ROM, EPROM, and EEPROM

ROM

Read Only Memory. A non-volatile memory device that is (typically) factory masked to create its internal bit pattern. Compare to PROM, EPROM, and EEPROM

Sandbox

An expansion or prototype area for free-range creators to play and express themselves.

SBC

Single Board Computer, i.e., a system which contains the processor and any memory (RAM & ROM) required to fully operate.

STD Bus

Standard Bus. A backplane based bus created by Pro-Log and Mostek, primarily for process control.

SW_n

Switch where n is the switch identifier

SID

Serial Input Data (8085 pin 5)

SOD

Serial Output Data (8085 pin 4)

Solder Side

The 'bottom' of the PC board

Transceiver

A bi-directional buffer, i.e., a device that ‘re-drives’ or buffers a signal to unload (or separate from) the original signal. The transceiver can either drive the signal from A to B or from B to A depending upon the state of the direction input (usually labelled something obvious like *D/R* or *A->B*). See also *buffer*.

Tri-State (or 3-state)

A form of device output where the output can be released into the high-impedance state where it is not driven high or low by the output device. When an output is in the tri-state mode, that device output is no longer controlling the output circuit which then allows another device to control the circuit.

Un

Integrated Circuit ID n. *Un.m* would be pin m on IC n.

UART

Universal Asynchronous Receiver Transmitter. A serial port controller that autonomously handles asynchronous serial communication e.g., RS232

Universal Site

A term used to reference a socket (usually memory) that can be used with multiple devices.

USART

Universal Synchronous Asynchronous Receiver Transmitter. A serial port controller that autonomously handles either synchronous or asynchronous serial communication e.g., RS232