Getting Started

with QuickUSB®

Evaluation Board

FIFO Demo

Bitwise™ systems

Getting started with QuickUSB
Evaluation Board FIFO Demo

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Version 1.00.2
October 1, 2009

Introduction

The FIFO Demo instantiates two FIFO's in the FPGA, an Output FIFO that the QuickUSB Module writes data to, and an Input FIFO that the QuickUSB Module reads data from over the QuickUSB High Speed Parallel Port.

This demo can provide the base for further development since the demo already handles the interface between the QuickUSB Module and the FIFO's in the FPGA.

System Requirements

- QuickUSB Library v2.11 or greater.
- QuickUSB Module QUSB2 with FIFO Handshake I/O model firmware v2.11 or greater.
- QuickUSB Diagnostics Application v2.11 or greater.
- QuickUSB Evaluation Board Library CD.
- Altera's Quartus II software.

Attach the QuickUSB Module

Please attach the QuickUSB Module to the QuickUSB Evaluation Board as shown in Figure 1. The QuickUSB Module will lock into place with the Keystone metric lock-in supports.

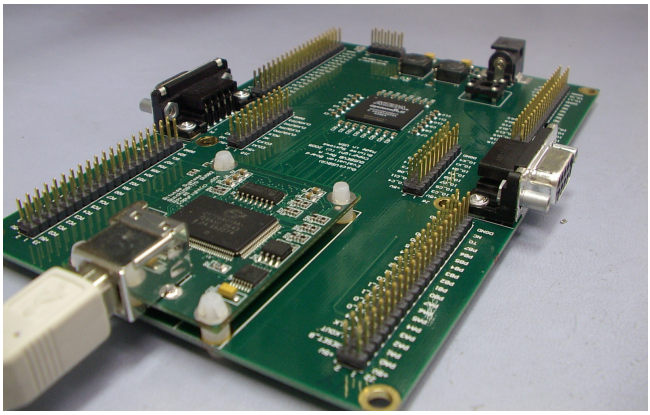

Figure 1 – Proper Attachment of the QuickUSB Module

Configuring the FPGA

1. Apply Power
    a. Run the QuickUSB Diagnostics application.
    b. Click on the “Ports” tab.
    c. Under “Port A”, check Bit 7 in the “Dir” Bit Check Box Field to set PA7 as an Output (see Figure 2).
    d. Under “Port A”, check Bit 7 in the “Value” Bit Check Box Field to Drive PA7 High. This will enable power to the board (see Figure 2).
2. Configure the FPGA
    a. Click on the “General” tab of the QuickUSB Diagnostics application.
    b. In the “FPGA” section, click the “Browse” button and select the “QUSBEVB_REVA_EP2C20_FIFO.rbf” file in the “Evaluation Board\Samples\Rev A\Verilog\ QUSBEVB_REVA_EP2C20_FIFO” directory.
    c. Ensure that the “FPGA Type” is set to “Altera Passive Serial”.
    d. Configure the FPGA by clicking the “Upload” button.
    e. Click “Start” and the QuickUSB Diagnostics application will program the FPGA. The QuickUSB Diagnostics application will display “FPGA was successfully configured” at the bottom of the form if the FPGA was successfully configured.

Modes of Operation

The Santa Cruz Adapter FIFO Demo can operate in two different modes, Loop Back Test and Read/Write Test.

Loop Back Test mode will read data out of the Output FIFO and write data back to the Input FIFO when data is available. This will allow you to write data to the FPGA and read back what you just wrote.

Read/Write Test mode will pull data out of the Output FIFO when data is available, and will write an incrementing count to the Input FIFO when space is available. This will allow you to read and write large blocks of data from or to the FPGA to measure the average data rate.

The modes are controlled by the Command Register at Address “0x00” as shown in Table 1.

Command Register Address	Value
0x00	0x00: Loop Back Test 0x01: Read/Write Test

Table 1 – FIFO Demo Command Registers

Running the Loop Back Test

1. Reset the FPGA Logic. PA0 is the active low reset for the logic in the FPGA. Asserting PA0 will reset the FIFO and Control Registers in the FPGA.
    a. Click on the “Ports” tab.
    b. Under “Port A”, check Bit 0 in the “Dir” Bit Check Box Field to turn PA0 into an output as shown in Figure 2.
    c. Under “Port A”, uncheck Bit 0 in the “Value” Bit Check Box Field to drive PA0 low and reset the logic in the FPGA. Then check Bit 0 in the “Value” Bit Check Box Field again to drive PA0 high.

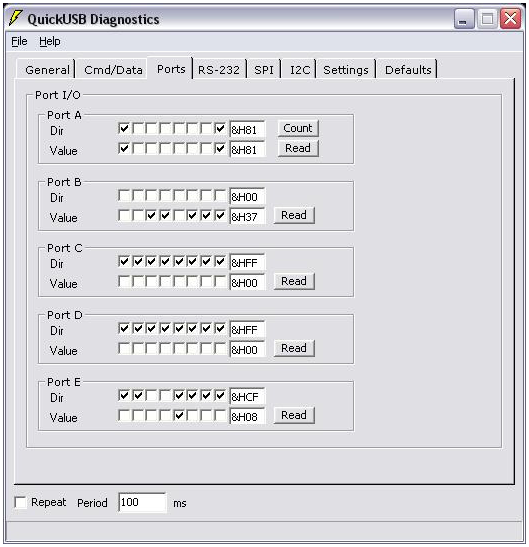

Figure 2 – Reset the FIFO Demo with the QuickUSB Diagnostics Program

2. Put FPGA in Loop Back Test mode:
    a. Click on the “Cmd/Data” tab as shown in Figure 3.
    b. Under the “Command” section, in the “Address” text box, type “0” as shown in Figure 3.
    c. In the “Length” text box, type “1” as shown in Figure 3.
    d. In the “Command Editor”, Type “0” as shown in Figure 3.
    e. Click the “Write” button. This will write the value in the Command Editor to the FPGA at Control Register “0”.

3. Write Data to the Output FIFO in the FPGA:
    a. Click on the “Cmd/Data” tab.
    b. Under the “Data” section, in the “Data Length” text box, enter a value of “512” as shown in Figure 3. This will set the number of words to write to the Output FIFO in the FPGA.
    c. Under the “Data” section, click “Count”. This will write an incrementing count to the Output FIFO in the FPGA. In Loop Back Test mode, the data will be read out of the Output FIFO and written to the Input FIFO automatically.

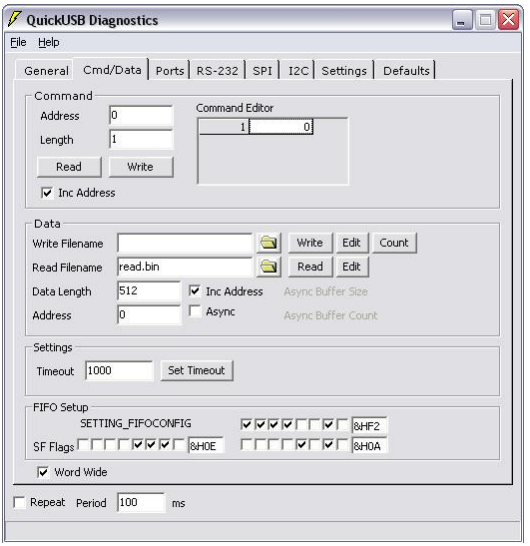

Figure 3 – QuickUSB Diagnostics Cmd/Data Tab for Loop Back Test

4. Read Data from the Input FIFO in the FPGA:
    a. Under the “Data” section, click “Read”
    b. The QuickUSB Diagnostics program will look for a file to write the data. Type “read.bin” for the File Name and click “Open”.
    c. The QuickUSB Module will read the data from the Input FIFO and write it to the “read.bin” file.
    d. Under the “Data” section, click “Edit”. This will open the file in the hex editor program included with QuickUSB. The hex editor will display the binary file “read.bin” that the QuickUSB Diagnostics program wrote the count to after reading it from the FPGA. Verify that there is an incrementing count as shown in Figure 4.

Figure 4 – Hex Editor with Incrementing Count

Running the Read/Write Test

1. Reset the FPGA Logic. PA0 is the active low reset for the logic in the FPGA. Asserting PA0 will reset the FIFO and Control Registers in the FPGA.
    a. Click on the “Ports” tab.
    b. Under “Port A”, check Bit 0 in the “Dir” Bit Check Box Field to turn PA0 into an output as shown in Figure 2.
    c. Under “Port A”, uncheck Bit 0 in the “Value” Bit Check Box Field to drive PA0 low and reset the logic in the FPGA. Then check Bit 0 in the “Value” Bit Check Box Field again to drive PA0 high as shown in Figure 2.
2. Put FPGA in Read/Write Test mode:
    a. Click on the “Cmd/Data” tab.
    b. Under the “Command” section, in the “Address” text box, type “0” as shown in Figure 5.
    c. In the “Length” text box, type “1” as shown in Figure 5.
    d. In the “Command Editor”, Type “1” as shown in Figure 5.
    e. Click the “Write” button. This will write the value in the Command Editor to the FPGA at address “0”.
3. Write Data to the Output FIFO in the FPGA:
    a. Click on the “Cmd/Data” tab.
    b. Under the “Data” section, in the “Data Lenth” text box, enter a value of “1024000” as shown in Figure 5.
    c. Under the “Data” section, click “Count”. This will write an incrementing count to the Output FIFO in the FPGA. The transfer rate can be seen at the bottom of the QuickUSB Diagnostics window when you click the “Count” button as shown in Figure 5.

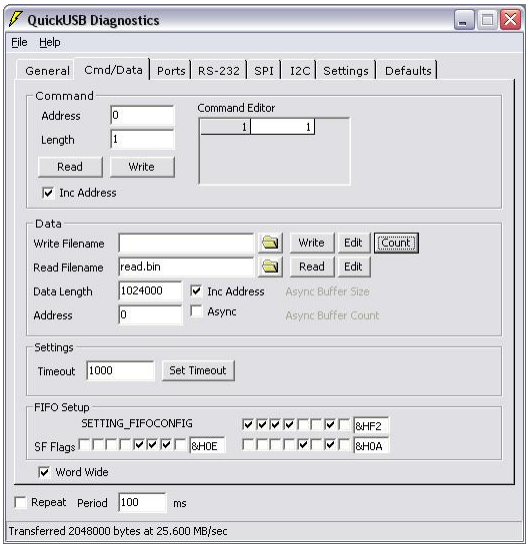

Figure 5 – QuickUSB Diagnostics Cmd/Data Tab for Read/Write Test

4. Read Data from the Input FIFO in the FPGA:
    a. Click on the “Cmd/Data” tab.
    b. Under the “Data” section, click “Read”.
    c. The QuickUSB Diagnostics program will look for a file to write the data. Type “read.bin” for the File Name and click “Open”.
    d. The QuickUSB Module will read the data from the Input FIFO. The transfer rate can be seen at the bottom of the QuickUSB Diagnostics window when you click the “Count” button as shown in Figure 5.
    e. Under the “Data” section, click “Edit”. This will open the file in the hex editor program included with QuickUSB. The hex editor will display the binary file “read.bin” that the QuickUSB Diagnostics program wrote the count to after reading it from the FPGA. Verify that there is an incrementing count as shown in Figure 4.

Appendix A

Updating the QuickUSB Module Firmware

For proper operation, the Evaluation Board FIFO Demo requires the QuickUSB Module to have the FIFO I/O model firmware loaded.

You can tell which version of firmware your module has by starting the QuickUSB Programmer and reading the 'Description' box. If the box has the words 'Simple I/O' displayed, its running the simple I/O firmware.

If the QuickUSB Module does not have the FIFO I/O Model Firmware loaded, perform the following steps in load the firmware:

1. Start the QuickUSB Programmer v2.11 included with the QuickUSB Library.

   NOTE: Do not use a QuickUSB Programmer version earlier than v2.11.0 to program the QuickUSB Module with a *.qusb file, or permanent damage to the QuickUSB Module will occur.

   You can verify which version of the QuickUSB Programmer is running by selecting "Help" -> "About".

2. Select "File" -> "Program EEPROM" and browse to "quickusb-fifo v2.11.qusb".

3. After the Firmware has been updated, disconnect and reconnect the QuickUSB Module from the USB cable to load the firmware. See Figure 6.

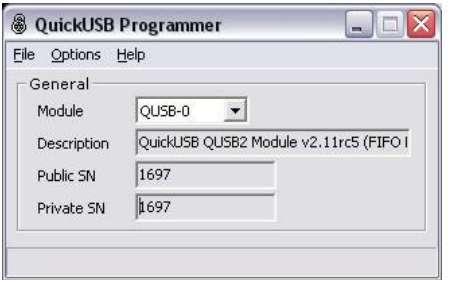

Figure 6 – QuickUSB Programmer