QuickUSB Adapter Board Pinout

Rev 1.33 Date 5/28/2003





Con	ector	J2					
Pin	Name	Dir	Description	Pin	Name	Dir	Description
	+5V	N/A	Unregulated +5V from the USB bus (300mA total)	2	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
	PA0	I/O	FX2 Port A, Bit 0 / nSS2	4	RESET_B	OD	FX2 Reset, Active low.
	PA1	I/O	FX2 Port A, Bit 1 / nSS3	6	CLKOUT	Output	FX2 48MHz CPU clock
,	PA2	I/O	FX2 Port A, Bit 2 / nSS4 / SLOE	8	IFCLK	Output	FX2 48MHz GPIO clock
)	PA3	I/O	FX2 Port A, Bit 3 / nSS5	10	INT4	Input	FX2 INT4 IRQ. Active high, edge sensitive
1	PA4	I/O	FX2 Port A, Bit 4 / nSS6 / FIFOADR0	12	RXD_0	Input	FX2 Serial Port 0 RS-232 RxD
3	PA5	I/O	FX2 Port A, Bit 5 / nSS7 / FIFOADR1	14	TXD_0	Output	FX2 Serial Port 0 RS-232 TxD
5	PA6	I/O	FX2 Port A, Bit 6 / nSS8 / PKTEND	16	TXD_1	Output	FX2 Serial Port 1 RS-232 TxD
7	PA7	I/O	FX2 Port A, Bit 7 / nSS9 / FLAGD (SLCS)	18	RXD_1	Input	FX2 Serial Port 1 RS-232 RxD
9	PB0	I/O	FX2 Port B, Bit 0 / FD0	20	CTL0	Output	FX2 GPIF CTL 0 / CMD_DATA / FLAGA (PF)
1	PB1	I/O	FX2 Port B, Bit 1 / FD1	22	CTL1	Output	FX2 GPIF CTL 1 / REN / FLAGB (FULL)
23	PB2	I/O	FX2 Port B, Bit 2 / FD2	24	CTL2	Output	FX2 GPIF CTL 2 / WEN / FLAGC (EMPTY)
5	PB3	I/O	FX2 Port B, Bit 3 / FD3	26	CTL3	Output	FX2 GPIF CTL 3 / nREN
7	PB4	I/O	FX2 Port B, Bit 4 / FD4	28	CTL4	Output	FX2 GPIF CTL 4 / nWEN
29	PB5	I/O	FX2 Port B, Bit 5 / FD5	30	CTL5	Output	FX2 GPIF CTL 5 / AEN
31	PB6	I/O	FX2 Port B, Bit 6 / FD6	32	RXD0	Input	FX2 Serial Port 0 TTL RxD (Do not use if U1 is populated
33	PB7	I/O	FX2 Port B, Bit 7 / FD7	34	TXD0	Output	FX2 Serial Port 0 TTL RxD (Do not use if U1 is populated
5	T0	Input	FX2 Input for Timer0	36	T1	Input	FX2 Input for Timer1
-	NC	N/A	No Connect	38	NC	N/A	No Connect
37 39	GND	N/A	Ground	40	GND	N/A	Ground
39		N/A J3	Ground	40	GND	N/A	Ground
39 Coni	GND		Ground Description	40 Pin	GND Name	N/A Dir	Ground Description
9 Soni Pin	GND nector	J3			Name +5V		Description Unregulated +5V from the USB bus (300mA total)
9 Coni Pin	GND nector Name	J3 Dir	Description	Pin	Name	Dir	Description
9 Coni Pin	GND nector Name +5V	J3 Dir N/A	Description Unregulated +5V from the USB bus (300mA total)	Pin 2	Name +5V	Dir N/A	Description Unregulated +5V from the USB bus (300mA total)
oni Pin	GND nector Name +5V PC0	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0	Pin 2 4	Name +5V RDY0	Dir N/A Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD
9 Con i Pin	GND nector Name +5V PC0 PC1	J3 Dir N/A I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1	Pin 2 4 6	Name +5V RDY0 RDY1	Dir N/A Input Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR
9 Oni Pin	GND nector Name +5V PC0 PC1 PC2	J3 Dir N/A I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2	Pin 2 4 6 8	Name +5V RDY0 RDY1 RDY2	Dir N/A Input Input Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4
9 Coni Pin 1	Hector Name +5V PC0 PC1 PC2 PC3	J3 Dir N/A I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3	Pin 2 4 6 8 10	Name +5V RDY0 RDY1 RDY2 RDY3	Dir N/A Input Input Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3
2000 Pin 3 5 7 9 11	Hector Name +5V PC0 PC1 PC2 PC3 PC4	J3 Dir N/A I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4	Pin 2 4 6 8 10 12	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4	Dir N/A Input Input Input Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5
Soni Pin 3 5 1 3 5	Hector Name +5V PC0 PC1 PC2 PC3 PC4 PC5	J3 Dir N/A I/O I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5	Pin 2 4 6 8 10 12 14	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5	Dir N/A Input Input Input Input Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated
39 Coni Pin 3 5 7	Hector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6	J3 Dir N/A I/O I/O I/O I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6	Pin 2 4 6 8 10 12 14 16	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1	Dir N/A Input Input Input Input Input Input Input Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated
39 Coni 3 5 7 9	Hector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7	J3 Dir N/A I/O I/O I/O I/O I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7	Pin 2 4 6 8 10 12 14 16 18	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1	Dir N/A Input Input Input Input Input Input Input Input Input Output	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populat
99 Conin 3 5 7 9 21	Hector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0	J3 Dir N/A I/O I/O I/O I/O I/O I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8	Pin 2 4 6 8 10 12 14 16 18 20	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0	Dir N/A Input	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI
9 Conin 1 3 5 7 9 1 1 3	Hector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9	Pin 2 4 6 8 10 12 14 16 18 20 22	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1	Dir N/A Input I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK
9 Coni 1 3 5 7 9 1 3 5	Hector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10	Pin 2 4 6 8 10 12 14 16 18 20 22 24	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2	Dir N/A Input I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE
9 Coni Pin 1 3 5 7 9 11 3 5 7 7 9 11 3 5 7 7 9 17 17 17 17 17 17 17 17 17 17 17 17 17	PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11	Pin 2 4 6 8 10 12 14 16 18 20 22 24 26	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3	Dir N/A Input I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG
39 Coni 3 5 7 9 21 23 25 27 29	ector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12	Pin 2 4 6 8 10 12 14 16 18 20 22 24 26 28	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4	Dir N/A Input I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS
9 Coni 20 1 3 5 7 9 1 1 3 5 7 9 1 1 3 1 5 1 7 9 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4 PD5	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 5 / FD13 FX2 Port D, Bit 6 / FD14	Pin 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4 PE5	Dir N/A Input I/O I/O I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0
39 Coni Pin 3 5 5 7 9 21 23 25 27 29 31 33	PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 5 / FD13 FX2 Port D, Bit 6 / FD14 FX2 Port D, Bit 7 / FD15	Pin 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4 PE5 PE6	Dir N/A Input I/O I/O I/O I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0 FX2 Port E, Bit 7 / GPIFADR8 / nSS1
39	ector Name +5V PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4 PD5 PD6	J3 Dir N/A I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 Port C, Bit 0 / GPIFADR0 FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 5 / FD13 FX2 Port D, Bit 6 / FD14	Pin 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34	Name +5V RDY0 RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4 PE5 PE6 PE7	Dir N/A Input I/O I/O I/O I/O I/O I/O I/O	Description Unregulated +5V from the USB bus (300mA total) FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0

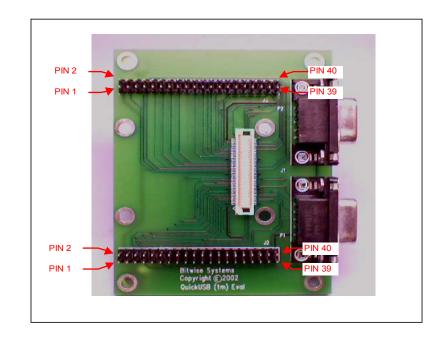
QuickUSB Adapter Board Pinout

Rev 1.33 Date 5/28/2003





Conr	nector	P1	
Pin	Name	Dir	Description
1	NC	N/A	Not Connected
2	TXD_0	Output	FX2 RXD_0 Pin 51 (NULL Modem incorporated into board)
3	RXD_0	Input	FX2 TXD_0 Pin 50 (NULL Modem incorporated into board)
4	NC	N/A	Not Connected
5	GND	N/A	Ground
6	NC	N/A	Not Connected
7	NC	N/A	Not Connected
8	NC	N/A	Not Connected
9	NC	N/A	Not Connected
Conr	nector	P2	
Conr Pin	nector Name	P2 Dir	Description
			Description Not Connected
Pin	Name	Dir	Not Connected
Pin 1	Name NC	Dir N/A	Not Connected
Pin 1 2	Name NC TXD_1	Dir N/A Output	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board)
Pin 1 2 3	Name NC TXD_1 RXD_1	Dir N/A Output Input	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board)
Pin 1 2 3 4	Name NC TXD_1 RXD_1 NC	Dir N/A Output Input N/A	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected
Pin 1 2 3 4 5	Name NC TXD_1 RXD_1 NC GND	Dir N/A Output Input N/A N/A	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected Ground
Pin 1 2 3 4 5 6	Name NC TXD_1 RXD_1 NC GND NC	Dir N/A Output Input N/A N/A	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected Ground Not Connected



Notes:

- 1) +5V is the USB bus power. Do not exceed 300mA current drain. USB bus supplies 500mA and QuickUSB consumes 200mA.
- 2) RXD0, TXD0, RXD1 & TXD1 are TTL serial lines from the FX2. These signals are only usable when U1 is not populated (Only usable on the QUSB2T board).