## **QuickUSB Adapter Board Pinout**

Rev 1.32 Date 5/15/2003





٠.	nector	J2	B	ъ.		Б.	<b>D</b> 1.0
Pin	Name	Dir	Description	Pin	Name	Dir	Description
1	+5V	N/A	Unregulated +5V from the USB bus (300mA total)	2	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
}	PA0	I/O	FX2 Port A, Bit 0 / nSS2	4	RESET_B	OD	FX2 Reset, Active low.
5	PA1	I/O	FX2 Port A, Bit 1 / nSS3	6	CLKOUT	Output	FX2 48MHz CPU clock
,	PA2	I/O	FX2 Port A, Bit 2 / nSS4 / SLOE	8	IFCLK	Output	FX2 48MHz GPIO clock
)	PA3	I/O	FX2 Port A, Bit 3 / nSS5	10	INT4	Input	FX2 INT4 IRQ. Active high, edge sensitive
11	PA4	I/O	FX2 Port A, Bit 4 / nSS6 / FIFOADR0	12	RXD_0	Input	FX2 Serial Port 0 RS-232 RxD
3	PA5	I/O	FX2 Port A, Bit 5 / nSS7 / FIFOADR1	14	TXD_0	Output	FX2 Serial Port 0 RS-232 TxD
5	PA6	I/O	FX2 Port A, Bit 6 / nSS8 / PKTEND	16	TXD_1	Output	FX2 Serial Port 1 RS-232 TxD
7	PA7	I/O	FX2 Port A, Bit 7 / nSS9 / FLAGD	18	RXD_1	Input	FX2 Serial Port 1 RS-232 RxD
9	PB0	I/O	FX2 Port B, Bit 0 / FD0	20	CTL0	Output	GPIF CTL 0 / CMD_DATA / FLAGA (PF)
1	PB1	I/O	FX2 Port B, Bit 1 / FD1	22	CTL1	Output	GPIF CTL 1 / REN / FLAGB (FULL)
23	PB2	I/O	FX2 Port B, Bit 2 / FD2	24	CTL2	Output	GPIF CTL 2 / WEN / FLAGC (EMPTY)
25	PB3	I/O	FX2 Port B, Bit 3 / FD3	26	CTL3	Output	GPIF ctl out 3 / nREN
7	PB4	I/O	FX2 Port B, Bit 4 / FD4	28	CTL4	Output	GPIF ctl out 4 / nWEN
9	PB5	I/O	FX2 Port B, Bit 5 / FD5	30	CTL5	Output	GPIF ctl out 5 / AEN
81	PB6	I/O	FX2 Port B, Bit 6 / FD6	32	RXD0	Input	Serial Port 0 TTL RxD (Do not use if U1 is populated)
33	PB7	I/O	FX2 Port B, Bit 7 / FD7	34	TXD0	Output	Serial Port 0 TTL RxD (Do not use if U1 is populated)
5	T0	Input	FX2 Input for Timer0	36	T1	Input	Input for Timer1
37	NC	N/A	No Connect	38	NC	N/A	No Connect
9	GND	N/A	Ground	40	GND	N/A	Ground
Conr	nector	J3					
Pin	Name	Dir	Description	Pin	Name	Dir	Description
	+5V	N/A	Unregulated +5V from the USB bus (300mA total)	2	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
	٠.						
1	PC0	I/O	Port C, Bit 0 / GPIFADR0	4	RDY0	Input	FX2 GPIF input signal 0 / SLRD
		I/O I/O	Port C, Bit 0 / GPIFADR0 Port C, Bit 1 / GPIFADR1	4 6	RDY0 RDY1	Input Input	FX2 GPIF input signal 1 / SLWR
	PC0					•	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2
	PC0 PC1	I/O	Port C, Bit 1 / GPIFADR1	6	RDY1	Input	FX2 GPIF input signal 1 / SLWR
	PC0 PC1 PC2	I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2	6 8	RDY1 RDY2	Input Input	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2
i · · 1	PC0 PC1 PC2 PC3	I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3	6 8 10	RDY1 RDY2 RDY3	Input Input Input	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5
1 3	PC0 PC1 PC2 PC3 PC4	I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4	6 8 10 12	RDY1 RDY2 RDY3 RDY4	Input Input Input Input	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5
1 3 5	PC0 PC1 PC2 PC3 PC4 PC5	I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5	6 8 10 12 14	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1	Input Input Input Input Input Input Input Output	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated
1 3 5 7	PC0 PC1 PC2 PC3 PC4 PC5 PC6	I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6	6 8 10 12 14 16 18 20	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0	Input Input Input Input Input Input Input Output I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated
3 5 7 9 11 13 15 17 19	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7	I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7	6 8 10 12 14 16 18 20 22	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1	Input Input Input Input Input Input Output I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use
5 7 9 11 13 15 17	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7	I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8	6 8 10 12 14 16 18 20	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0	Input Input Input Input Input Input Input Output I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI
1 3 5 7 9	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1	I/O I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8 Port D, Bit 1 / FD9	6 8 10 12 14 16 18 20 22	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1	Input Input Input Input Input Input Output I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK
1 3 5 7 9 21	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2	I/O I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8 Port D, Bit 1 / FD9 Port D, Bit 2 / FD10	6 8 10 12 14 16 18 20 22 24	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2	Input Input Input Input Input Input Output I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE
5 7 9 11 13 15 17 19	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3	I/O I/O I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8 Port D, Bit 1 / FD9 Port D, Bit 2 / FD10 Port D, Bit 3 / FD11	6 8 10 12 14 16 18 20 22 24 26	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3	Input Input Input Input Input Input Output I/O I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG
5 7 9 11 13 15 17 19 21 23 25 27	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4	I/O I/O I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8 Port D, Bit 1 / FD9 Port D, Bit 2 / FD10 Port D, Bit 3 / FD11 Port D, Bit 4 / FD12	6 8 10 12 14 16 18 20 22 24 26 28	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4	Input I/O I/O I/O I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO
5 1 1 3 5 7 9 2 2 2 3 2 5 7 9 2 7 2 7 8 7 9 2 7 7 9 8 7 7 9 9 9 9 9 9 9 9 9 9 9 9 9 9	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4 PD5	I/O I/O I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8 Port D, Bit 1 / FD9 Port D, Bit 2 / FD10 Port D, Bit 3 / FD11 Port D, Bit 4 / FD12 Port D, Bit 5 / FD13 Port D, Bit 6 / FD14	6 8 10 12 14 16 18 20 22 24 26 28 30	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4 PE5	Input Output I/O I/O I/O I/O I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0
5 7 9 11 13 15 17 19 21 23 25	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4 PD5 PD6	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8 Port D, Bit 1 / FD9 Port D, Bit 2 / FD10 Port D, Bit 3 / FD11 Port D, Bit 4 / FD12 Port D, Bit 6 / FD13 Port D, Bit 6 / FD14 Port D, Bit 7 / FD15	6 8 10 12 14 16 18 20 22 24 26 28 30 32	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4 PE5 PE6 PE7	Input I/O I/O I/O I/O I/O I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATAO / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0 FX2 Port E, Bit 7 / GPIFADR8 / nSS1
5 7 9 11 13 5 5 7 9 9 21 22 25 27 29 31	PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Port C, Bit 1 / GPIFADR1 Port C, Bit 2 / GPIFADR2 Port C, Bit 3 / GPIFADR3 Port C, Bit 4 / GPIFADR4 Port C, Bit 5 / GPIFADR5 Port C, Bit 6 / GPIFADR6 Port C, Bit 7 / GPIFADR7 Port D, Bit 0 / FD8 Port D, Bit 1 / FD9 Port D, Bit 2 / FD10 Port D, Bit 3 / FD11 Port D, Bit 4 / FD12 Port D, Bit 5 / FD13 Port D, Bit 6 / FD14	6 8 10 12 14 16 18 20 22 24 26 28 30 32 34	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 PE0 PE1 PE2 PE3 PE4 PE5 PE6	Input I/O I/O I/O I/O I/O I/O I/O	FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0

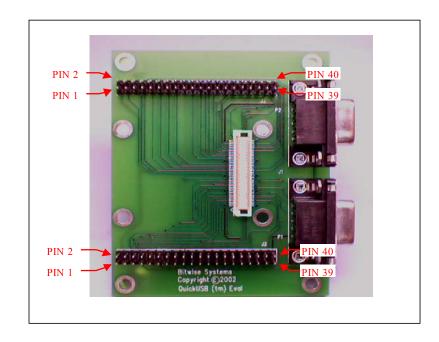
## **QuickUSB Adapter Board Pinout**

Rev 1.32 Date 5/15/2003





Conr	nector	P1	
Pin	Name	Dir	Description
1	NC	N/A	Not Connected
2	TXD_0	Output	FX2 RXD_0 Pin 51 (NULL Modem incorporated into board)
3	RXD_0	Input	FX2 TXD_0 Pin 50 (NULL Modem incorporated into board)
4	NC	N/A	Not Connected
5	GND	N/A	Ground
6	NC	N/A	Not Connected
7	NC	N/A	Not Connected
8	NC	N/A	Not Connected
9	NC	N/A	Not Connected
Conr	nector	P2	
<b>Conr</b> Pin	nector Name	<b>P2</b> Dir	Description
			Description Not Connected
Pin	Name	Dir	Not Connected
Pin 1	Name NC	Dir N/A	Not Connected
Pin 1 2	Name NC TXD_1	Dir N/A Output	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board)
Pin 1 2 3	Name NC TXD_1 RXD_1	Dir N/A Output Input	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board)
Pin 1 2 3 4	Name NC TXD_1 RXD_1 NC	Dir N/A Output Input N/A	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected
Pin 1 2 3 4 5	Name NC TXD_1 RXD_1 NC GND	Dir N/A Output Input N/A N/A	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected Ground
Pin 1 2 3 4 5 6	Name NC TXD_1 RXD_1 NC GND NC	Dir N/A Output Input N/A N/A	Not Connected FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected Ground Not Connected



## Notes:

- 1) +5V is the USB bus power. Do not exceed 300mA current drain. USB bus supplies 500mA and QuickUSB consumes 200mA.
- 2) RXD0, TXD0, RXD1 & TXD1 are TTL serial lines from the FX2. These signals are only usable when U1 is not populated (Only usable on the QUSB2T board).