

## Product Overview

The Universal Serial Bus is a popular computer interface that has become the de-facto standard interface for PC peripherals. Now, Hi-Speed USB 2.0 is the new standard in PC peripheral connectivity. With a speed of 480 Mbps, USB 2.0 is up to 40 times faster than the 12 Mbps USB 1.1. USB 2.0 uses the exact same cabling as USB 1.1 and is fully backward compatible.

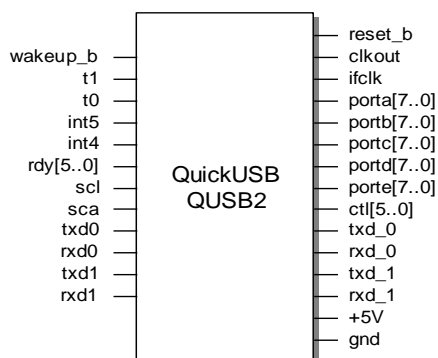
Implementing a USB peripheral typically requires in-depth knowledge of the USB protocol, a considerable amount of firmware and software development effort, and rigorous compliance testing. But now there's an alternative.

The QuickUSB® QUSB2 module makes adding Hi-Speed USB 2.0 to new or existing products quick and easy by integrating all the hardware, firmware, and software needed to implement a general-purpose USB endpoint into a simple plug-in module and development library. The module may simply be used as a development station when combined with the QuickUSB Adapter Board or QuickUSB Evaluation Board, designed as a plug-in module for new products, or designed directly into new products and licensed using the QuickUSB iChipPack or QuickUSB EEPROMs.

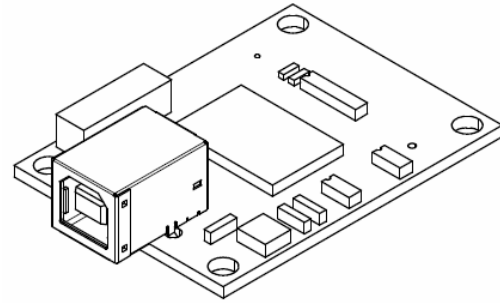
If you need your product to enumerate as a custom device instead of as a QuickUSB module you may use the QuickUSB Customizer. No one would ever know that you used QuickUSB in your design. With the customizer you get your own unique PID, a unique serial number for each module/license to uniquely identify each device, and the ability to change the QuickUSB string descriptors.

The QuickUSB module contains hardware parallel and serial ports that are connected to circuitry within the peripheral. The QuickUSB library provides user-callable software functions that transfer data to and from the hardware ports over the USB. The designer gets multiple ports of flexible, high-speed USB connectivity and no prior knowledge of USB is required.

## Schematic Symbol



## The QuickUSB Module



### Functional Description

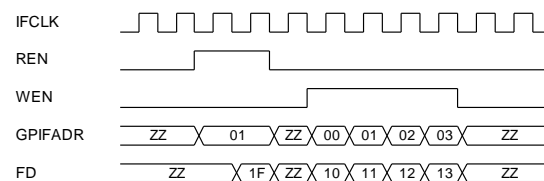
The QuickUSB QUSB2 module is a 2" x 1 1/2" circuit board that implements a bus-powered Hi-Speed USB 2.0 endpoint terminating in a single 80-pin target interface connector.

The target interface consists of:

- One 8- or 16-bit high-speed parallel port.
- Up to three general-purpose 8-bit parallel I/O ports.
- Two RS-232 ports.
- One I<sup>2</sup>C port.
- One soft SPI port/FPGA configuration port.
- 2 KB of user available, non-volatile memory.

### High-Speed Parallel Port

The high-speed parallel port is configurable as an 8- or 16-bit synchronous parallel port. It delivers a sustained data rate of up to 12 MB/s and a burst rate of up to 48MB/s for packets up to 512 bytes long. The high-speed interface consists of the data port FD[15:0], control lines CMD\_DATA, REN, WEN and GPIFADR [8:0]. The port can be used as a multiplexed command/data bus by decoding CMD\_DATA (CMD = 0, DATA = 1) in the target logic. Reads are indicated by REN = 1 and writes are indicated by WEN = 1. If the address bus is configured to be active, then the GPIFADR bus contains the address of each data element read from or written to FD [15:0].



### General Purpose I/O

General purpose I/O pins must be configured to indicate whether they are being used as input or output pins. This is accomplished using library calls documented in the QuickUSB User Guide.

The parallel ports have multiple functions and may not be available if alternate functions are enabled. The

general-purpose I/O ports are ports A, C, and E. Ports B and D are reserved for the high-speed parallel port. Port E has an alternate function for FPGA configuration and soft SPI. If these alternate functions are used, Port E is reserved and may not be used for general-purpose I/O.

### **RS-232**

The module contains two full-duplex, asynchronous RS-232 ports with a configurable baud rate between 4.8 and 230 Kbaud (Both ports use the same baud rate). These interrupt-driven ports are internally buffered to a depth of 32 bytes per port.

### **I<sup>2</sup>C**

An I<sup>2</sup>C compatible port is included on the QuickUSB module. The port is a bus master only and operates at a programmable rate of 100 kHz or 400 kHz. The QuickUSB library provides functions to write and read blocks of data to and from I<sup>2</sup>C peripherals.

### **SPI**

The module supports SPI peripherals through a 'soft' SPI port which uses pins on Port E. The pins MOSI, SCK, MISO and nSS are shared with the FPGA configuration function and will not interfere with each other *if* the SPI peripherals only drive the MISO when nSS is asserted (nSS=0).

### **FPGA Configuration**

The QuickUSB module can program SRAM-based Altera (and Xilinx) programmable logic devices using five pins of Port E. When designing your peripheral to use this feature, consult the 'PS Configuration with a Microprocessor' section of Altera Application Note 116, 'Configuring SRAM-Based LUT Devices'. This document specifies the circuitry needed to configure an Altera device with a microcontroller.

The QuickUSB module provides the DCLK, DATA0, nCE, nCONFIG, nSTATUS and CONF\_DONE signals required to configure Altera devices in passive-serial mode. If more than one Altera device must be configured over the interface, the devices should be daisy-chained and the programming files combined into a single RBF file. Consult AN116 for details on this configuration or contact Bitwise Systems.

## **The QuickUSB Library**

The QuickUSB Library included with QuickUSB provides Windows DLL and Linux library files with library interfaces to so that you may develop QuickUSB in nearly any language, including C, C++, VB6, Delphi, and many others. The QuickUSB Library hides the complexity of USB 2.0 behind an easy-to-use application programming interface. A complete description of each library function is provided in the QuickUSB User Guide.

The library also includes numerous sample applications written in many programming languages which demonstrate how easy and quick it is to truly integrate USB 2.0 connectivity in your hardware.

## **Contact**

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