Getting Started

with

QuickUSB®

Evaluation Board

FIFO Demo

Bitwise™ systems

Getting started with QuickUSB
Evaluation Board FIFO Demo

Bitwise Systems
6489 Calle Real, Suite E
Goleta, CA 93117

Voice	(805) 683-6469
Fax	(805) 683-4833
Toll Free	(800) 224-1633
Web Site	www.bitwisesys.com
Information	info@bitwisesys.com
Technical Support	support@bitwisesys.com

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Introduction

The FIFO Demo FPGA sample demonstrates how to create a data interface to FIFO's instantiated inside an FPGA, as well as how to read and write registers inside the FPGA using the command data interface.

The FIFO Demo may be used as a simple test to verify connectivity of the QuickUSB data bus to an FPGA using the FIFO HS IO Model, as well as a way for a designer to test a new software application developed for QuickUSB. The FIFO Demo should be used as a base design from which to build from when using the FIFOHS IO Model with an FPGA.

While the FIFO Demo sample and documentation are intended for use with the QuickUSB Starter Kit, the HDL concepts covered in the sample, as well as the process for testing the sample, are applicable to any FPGA design using QuickUSB.

System Requirements

- QuickUSB Library v2.15.1 (or later)
- QuickUSB Starter Kit v2.15.1 (or later)
- QuickUSB Starter Kit containing a QuickUSB Evaluation Board and QuickUSB Module programmed with the FIFO HS I/O Model firmware (v2.15.1 or later)

Hardware Setup

Attach the QuickUSB Module to the QuickUSB Evaluation Board as shown in Figure 1. The QuickUSB Module will lock into place with the four plastic lock-in supports.

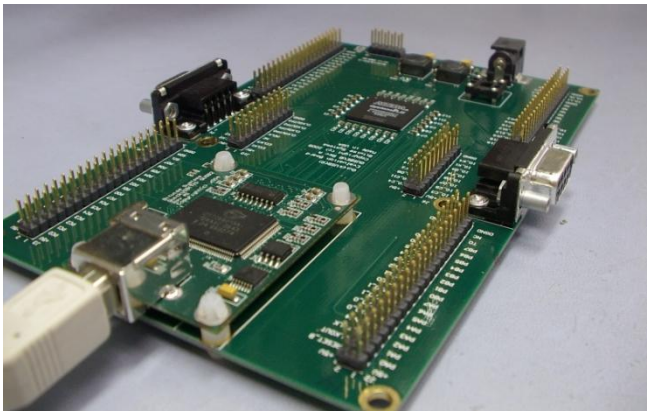

Figure 1 – Proper Attachment of the QuickUSB Module

Updating the QuickUSB Module Firmware

For proper operation, the FIFO Demo requires the QuickUSB Module to have the FIFO HS I/O Model firmware loaded. You can tell which version of firmware your module has either with the QuickUSB Diagnostics software or by starting the QuickUSB Programmer and reading the "Description" field. If description of the QuickUSB firmware does not contain "FIFO Handshake" or reports a version older than v2.15.1, then you need to change the firmware.

Perform the following steps to change the QuickUSB firmware:

1. Start the QuickUSB Programmer that is installed with the QuickUSB Library
2. Select "File->Program EEPROM" and browse to the "quickusb-fifohs v2.15.1.qusb" firmware file.
3. The programming process should take only a few seconds and its progress is indicated with a progress bar near the status bar. After the firmware has been updated, you will be prompted to disconnect and reconnect the QuickUSB Module from the USB cable to load the firmware. If you have external power connected to the QuickUSB Evaluation Board, please remove it as well (See Figure 2).

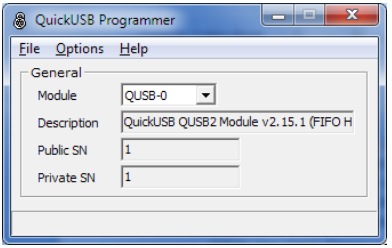

Figure 2 – QuickUSB Programmer

Configuring the FPGA

1. Apply Power
   a. Run the QuickUSB Diagnostics application that is installed with the QuickUSB Library
   b. Navigate to the "Ports" tab. Under "Port A", check Bit 7 in the "Dir" bit checkbox field to set PA7 as an output (see Figure 4)
   c. Under "Port A", check Bit 7 in the "Value" bit checkbox field to drive PA7 high. This will enable power to the FPGA (see Figure 4).
2. Configure the FPGA
   a. Navigate to the "General" tab of the QuickUSB Diagnostics application (see Figure 3)
   b. In the "FPGA" section, click the "Browse" button and select the "counter.rbf" file. The RBF file is installed with the QuickUSB Starter Kit Library, typically under "C:\Program Files\Bitwise Systems\Evaluation Board\Samples\Verilog\QUSBEVB_FIFO" directory.
   c. Ensure that the "FPGA Type" is set to "Altera Passive Serial"
   d. Configure the FPGA by clicking the "Upload" button. Once the

configuration has completed, a message will be displayed in the status bar indicating success or failure. You may also query if the FPGA is configured by clicking the "Is Configured?" button. If the programming process fails, ensure that power in applied to the FPGA (see Step 1).

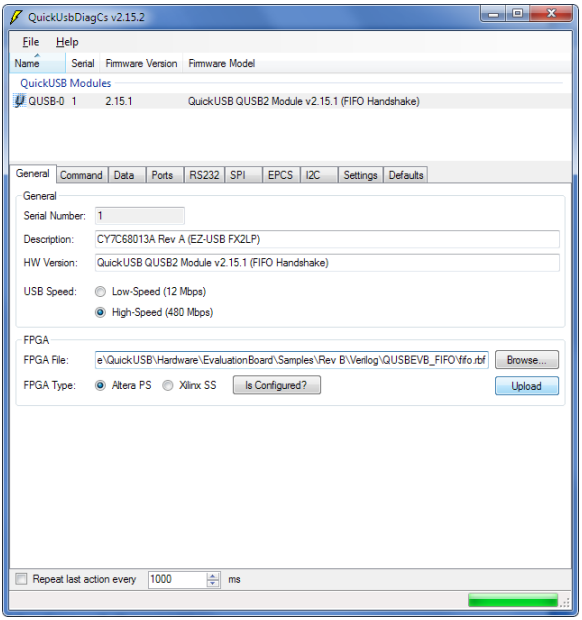

Figure 3 – QuickUSB Diagnostics "General" Tab

Modes of Operation

The FIFO Demo can operate in two different modes: Loopback Test mode and Read/Write Test mode.

The Loopback Test mode will read data out of the Output FIFO and write data back to the Input FIFO when data is available. This will allow you to write data to the FPGA and read back the same data.

Read/Write Test mode will pull data out of the Output FIFO when data is available, and will write an incrementing count to the Input FIFO when space is available. This will allow you to read and write large blocks of data from or to the FPGA to measure maximum data rate when the FIFOs never report themselves as being full or empty.

The modes are controlled by a register inside the FPGA that may be accessed using the Command Bus. The Command bus shares the same physical connection between QuickUSB and the FPGA, but uses the CMD_DATA line to determine which kind of transaction is being performed. With FPGAs, the Command bus is very useful in allowing R/W access to registers to control FPGA operation. The FIFO Demo allows you to R/W the registers in Table 1.

Command Register Address	Value
0x0000	0x0000: Loopback Test 0x0001: Read/Write Test

Table 1 – FIFO Demo Command Registers

Running the Loop Back Test

1. PA0 is the active low reset for the logic in the FPGA. Driving PA0 then high will reset the Counter in the FPGA.
   a. Navigate to the "Ports" tab
   b. Under "Port A", check Bit 0 in the "Dir" bit checkbox field to configure PA0 as an output, as shown in Figure 4
   c. Under "Port A", uncheck Bit 0 in the "Value" bit checkbox field to drive PA0 low and reset the logic in the FPGA. Then, check Bit 0 in the "Value" bit checkbox field again to drive PA0 high.

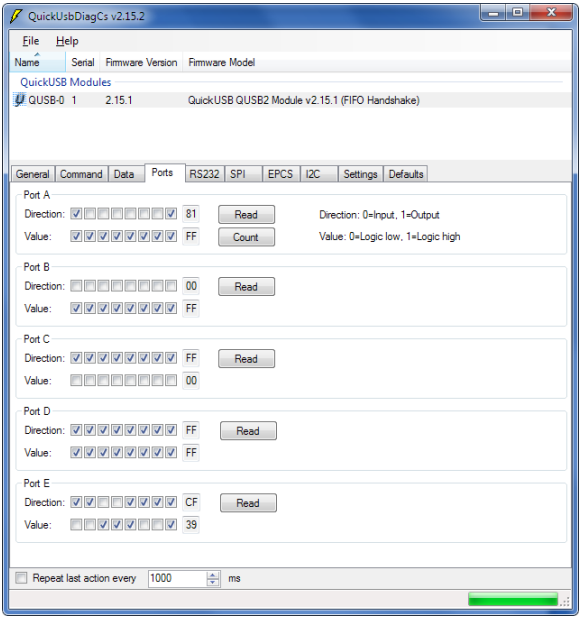

Figure 4 – Reset the FIFO Demo with the QuickUSB Diagnostics Program

1. Put FPGA in Loop Back Test mode:
   a. Click on the "Command" tab (see Figure 5)
   b. Under the "Write" section, in the "Address" textbox enter "0x0000" to select the FPGA control register and in the "Length" textbox enter "2"
   c. In the multiline textbox in the "Write" section, enter the data "0x00 0x00"
   d. Click the "Write" button to write the control register

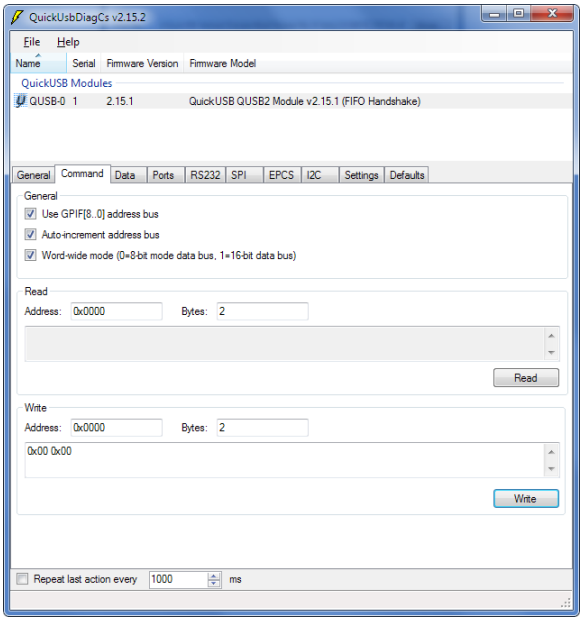

Figure 5 – QuickUSB Diagnostics Command Tab for Loop Back Test

2. Write Data to the Output FIFO in the FPGA:
   a. Navigate to the "Data" tab. Check the "Word-wide mode" checkbox if it is not already checked (see Figure 6). This will enable the QuickUSB Module to be in Word-Wide mode and use a 16-bit data bus.
   b. Under the "Write" section, in the "Data Length" text box, enter a value of "512. This will set the number of bytes to write to the Output FIFO in the FPGA.
   c. Under the "Data" section, click "Count". This will write an incrementing count to the Output FIFO in the FPGA. In Loop Back Test mode, the data will be read out of the Output FIFO and written to the Input FIFO automatically.

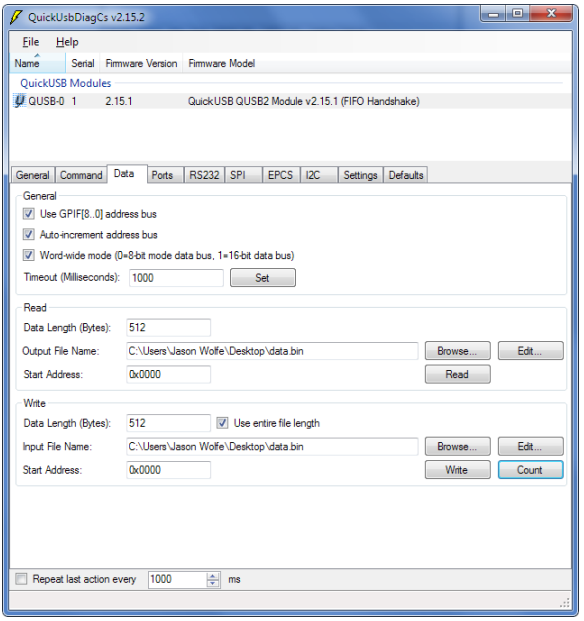

Figure 6 – QuickUSB Diagnostics Data Tab for Loop Back Test

3. Read Data from the Input FIFO in the FPGA:
   a. Navigate to the "Data" tab. Under the "Read" section, enter "512" into the Data Length textbox. This value sets the number of bytes for the QuickUSB Module to read.
   b. Specify a file for the read data to be written to by clicking the "Browse" button next to the "Output File Name" textbox. If the file already exists, it will be overwritten.
   c. Click the "Read" button to begin reading data from the FPGA. The QuickUSB Module will then read the requested amount of data from the Input FIFO in the FPGA and write it to the specified file.
   d. To verify that the data read correctly, click the "Edit" button in the "Read" section. This will launch a hex editor that will display the contents of the file. Verify that there is an incrementing count as shown in Figure 7. Note that depending on the endianness of your system, the MSB and LSB of the read data may be reversed from that shown in Figure 7.

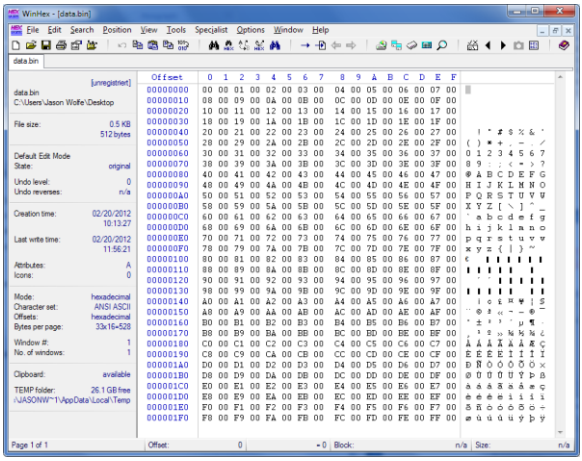

Figure 7 – Hex Editor with Incrementing Count

Running the Read/Write Test

1. PA0 is the active low reset for the logic in the FPGA. Driving PA0 then high will reset the Counter in the FPGA.
   a. Navigate to the "Ports" tab
   b. Under "Port A", check Bit 0 in the "Dir" bit checkbox field to configure PA0 as an output, as shown in Figure 4
   c. Under "Port A", uncheck Bit 0 in the "Value" bit checkbox field to drive PA0 low and reset the logic in the FPGA. Then, check Bit 0 in the "Value" bit checkbox field again to drive PA0 high.
2. Put FPGA in Read/Write Test mode:
   a. Click on the "Command" tab
   b. Under the "Write" section, in the "Address" textbox enter "0x0000" to select the FPGA control register and in the "Length" textbox enter "2"
   c. In the multiline textbox in the "Write" section, enter the data "0x01 0x00"
   d. Click the "Write" button to write the control register
3. Write Data to the Output FIFO in the FPGA:
   a. Navigate to the "Data" tab. Check the "Word-wide mode" checkbox if it is not already checked. This will enable the QuickUSB Module to be in Word-Wide mode and use a 16-bit data bus.
   b. Under the "Write" section, in the "Data Length" text box, enter a value of "16384". This will set the number of bytes to write to the Output FIFO in the FPGA.
   c. Under the "Data" section, click "Count". This will write an incrementing count to the Output FIFO in the FPGA. In the Read/Write Test mode, the data will be immediately drained from the Output FIFO and discarded.
4. Read Data from the Input FIFO in the FPGA:
   a. Navigate to the "Data" tab. Under the "Read" section, enter "32768"

into the Data Length textbox. This value sets the number of bytes for the QuickUSB Module to read.

b. Specify a file for the read data to be written to by clicking the "Browse" button next to the "Output File Name" textbox. If the file already exists, it will be overwritten.

c. Click the "Read" button to begin reading data from the FPGA. The QuickUSB Module will then read the requested amount of data from the Input FIFO in the FPGA and write it to the specified file.

d. To verify that the data read correctly, click the "Edit" button in the "Read" section. In Read/Write Test mode, an incrementing count is always written on the Input FIFO is there is room. You should verify that the read data is an incrementing counting pattern. If you perform successive reads, the count will pick up from where it left off.