Getting Started

with

QuickUSB®

Evaluation Board

Asynchronous
Slave FIFO Demo

Bitwise™ systems

Getting started with QuickUSB
Evaluation Board Asynchronous Slave FIFO Demo

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Introduction

The Asynchronous Slave FIFO Demo FPGA sample demonstrates how to create a data interface between the QuickUSB endpoint FIFO's and a FIFO instantiated inside an FPGA using the Asynchronous Slave FIFO IO Model.

The Asynchronous Slave FIFO Demo may be used as a simple test to verify connectivity of the QuickUSB data bus to an FPGA using the Asynchronous Slave FIFO HS IO Model, as well as a way for a designer to test a new software application developed for QuickUSB. The Asynchronous Slave FIFO Demo should be used as a base design from which to build from when using the Asynchronous Slave FIFOHS IO Model with an FPGA.

While the Asynchronous Slave FIFO Demo sample and documentation are intended for use with the QuickUSB Starter Kit, the HDL concepts covered in the sample, as well as the process for testing the sample, are applicable to any FPGA design using QuickUSB.

System Requirements

- QuickUSB Library v2.15.1 (or later)
- QuickUSB Starter Kit v2.15.1 (or later)
- QuickUSB Starter Kit containing a QuickUSB Evaluation Board and QuickUSB Module programmed with the Simple I/O Model firmware (v2.15.1 or later)

Design Overview

Figure 1 – Slave FIFO Sample Design Block Diagram

The Asynchronous Slave FIFO sample demonstrates how to use the Asynchronous Slave FIFO IO Model to allow an FIFO to directly access the endpoint (EP) FIFO's inside a QuickUSB device. The FPGA acts are the FIFO master, monitoring the nEMPTY and nFULL lines of the IN and OUT endpoints in the QuickUSB device and controlling when to move data. The QuickUSB device acts as the FIFO slave with data transactions asynchronous to read and write strobe lines, hence the name Asynchronous Slave FIFO IO Model.

The FPGA instantiates an 8 KWord (16 KB) FIFO to act as a data loopback buffer to allow for both reads and writes in the design. The FPGA continually monitors the status of both the IN and OUT endpoints by continually switching the currently addressed FIFO buffer. As data becomes present in the OUT EP FIFO, it is read out by the FPGA into the FPGA's FIFO as long as the FIFO is not full. If data is present in the FPGA FIFO and the IN EP FIFO is not full, data is written to the IN EP FIFO by the FPGA. This behavior creates a data loopback that may be used to verify correct operation of the Slave FIFO design.

This design currently only allows for data transfers in multiples of 512 bytes. This is because data written from the FPGA to the IN EP is automatically committed for transfer over USB by QuickUSB in 512-byte chunks. You may alter

the design to toggle the nPKTEND signal to manually commit data packets of any size, but such behavior is design specific and omitted for clarity.

Hardware Setup

Attach the QuickUSB Module to the QuickUSB Evaluation Board as shown in Figure 2. The QuickUSB Module will lock into place with the four plastic lock-in supports.

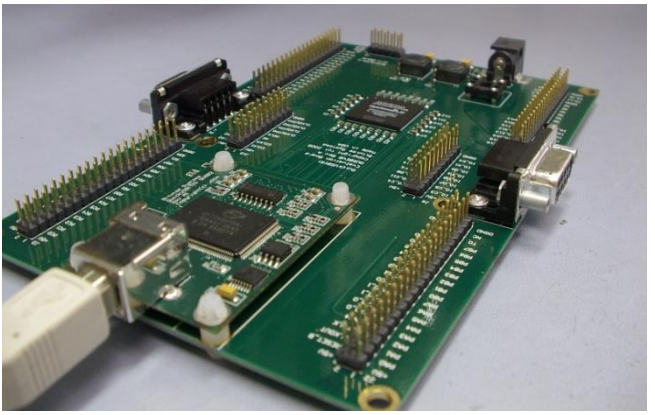

Figure 2 – Proper Attachment of the QuickUSB Module

Updating the QuickUSB Module Firmware

For proper operation, the Asynchronous Slave FIFO Demo requires the QuickUSB Module to have the Simple I/O Model firmware loaded. You can tell which version of firmware your module has either with the QuickUSB Diagnostics software or by starting the QuickUSB Programmer and reading the "Description" field. If description of the QuickUSB firmware does not contain "Simple I/O" or reports a version older than v2.15.1, then you need to change the firmware.

Perform the following steps to change the QuickUSB firmware:

1. Start the QuickUSB Programmer that is installed with the QuickUSB Library
2. Select "File->Program EEPROM" and browse to the "quickusb-simple v2.15.1.qusb" firmware file.
3. The programming process should take only a few seconds and its progress is indicated with a progress bar near the status bar. After the firmware has been updated, you will be prompted to disconnect and reconnect the QuickUSB Module from the USB cable to load the firmware. If you have external power connected to the QuickUSB Evaluation Board, please remove it as well (See Figure 3).

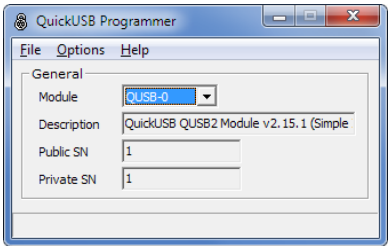

Figure 3 – QuickUSB Programmer

Configuring the FPGA

1. Apply Power
   a. Run the QuickUSB Diagnostics application that is installed with the QuickUSB Library
   b. Navigate to the "Ports" tab. Under "Port A", check Bit 7 in the "Dir" bit checkbox field to set PA7 as an output (see Figure 6)
   c. Under "Port A", check Bit 7 in the "Value" bit checkbox field to drive PA7 high. This will enable power to the FPGA (see Figure 6).
2. Configure the FPGA
   a. Navigate to the "General" tab of the QuickUSB Diagnostics application (see Figure 4)
   b. In the "FPGA" section, click the "Browse" button and select the "counter.rbf" file. The RBF file is installed with the QuickUSB Starter Kit Library, typically under "C:\Program Files\Bitwise Systems\Evaluation Board\Samples\Verilog\QUSBEVB_AsyncSlaveFIFO" directory.
   c. Ensure that the "FPGA Type" is set to "Altera Passive Serial"
   d. Configure the FPGA by clicking the "Upload" button. Once the configuration has completed, a message will be displayed in the status bar indicating success or failure. You may also query if the FPGA is configured by clicking the "Is Configured?" button. If the programming process fails, ensure that power in applied to the FPGA (see Step 1).

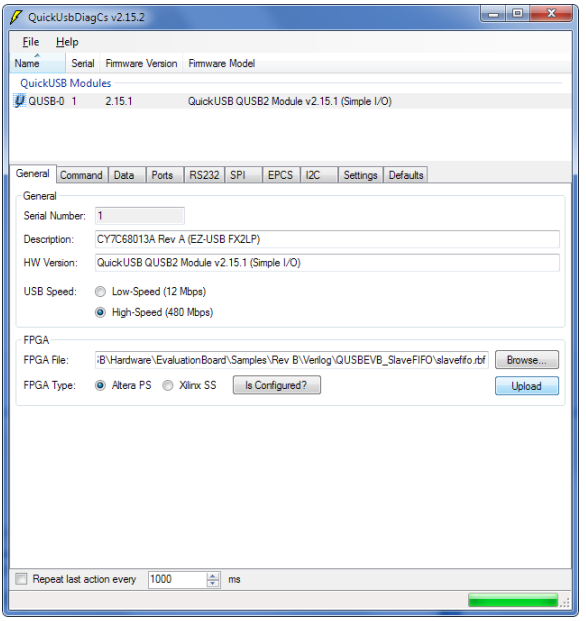

Figure 4 – QuickUSB Diagnostics "General" Tab

Setup Async Slave FIFO Mode

1. Asynchronous Slave FIFO mode is enabled when a QuickUSB device is programmed with the Simple IO Model firmware and the appropriate settings are set.
   a. Navigate to the "Settings" tag
   b. Under the "FIFOPolar/IFCONFIG" setting, which corresponds to the SETTING_FIFO_CONFIG, check bits 0 and 1 (if they are not already checked) to enter Slave FIFO mode (See Figure 5)
   c. Under the "FIFOPolar/IFCONFIG" setting, which corresponds to the SETTING_FIFO_CONFIG, ensure that bit 3 is checked to enabled Asynchronous Slave FIFO mode (as opposed to Synchronous Slave FIFO) and that bit 4 is unchecked to use normal IFCLK polarity (See Figure 5)

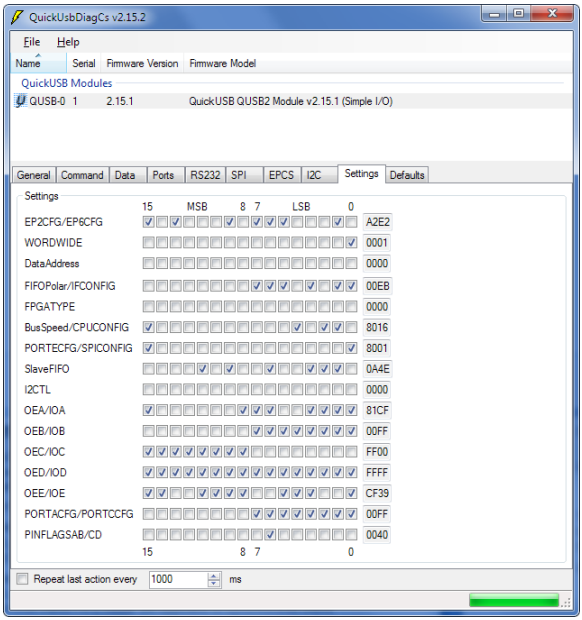

Figure 5 – QuickUSB Diagnostics "Settings" Tab

Running the Async Slave FIFO Loopback Test

1. PA0 is the active low reset for the logic in the FPGA. Driving PA0 then high will reset the Counter in the FPGA.
   a. Navigate to the "Ports" tab
   b. Under "Port A", check Bit 0 in the "Dir" bit checkbox field to configure PA0 as an output, as shown in Figure 6
   c. Under "Port A", uncheck Bit 0 in the "Value" bit checkbox field to drive PA0 low and reset the logic in the FPGA. Then, check Bit 0 in the "Value" bit checkbox field again to drive PA0 high.
2. The endpoint FIFOs in the QuickUSB Module are reset by writing any value to the SETTING_FIFO_CONFIG setting, labeled as "FIFOPolar/IFCONFIG" in the "Settings" tab.
   a. Reset the endpoint FIFOs by unchecking and checking bit 0 of the "FIFOPolar/IFCONFIG" setting (See Figure 5)

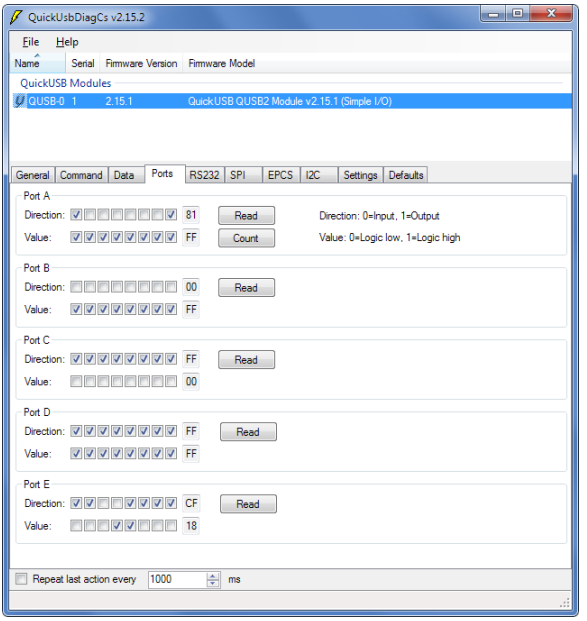

Figure 6 – Reset the FIFO Demo with the QuickUSB Diagnostics Program

3. Write Data to the FPGA:
   a. Navigate to the "Data" tab. Check the "Word-wide mode" checkbox if it is not already checked (see Figure 7). This will enable the QuickUSB Module to be in Word-Wide mode and use a 16-bit data bus. Note that the GPIF address bus is not used in Asynchronous Slave FIFO mode.
   b. Under the "Write" section, in the "Data Length" text box, enter a value of "4096". This will set the number of bytes to write to the Output FIFO in the FPGA.
   c. Under the "Data" section, click "Count". This will write an incrementing count to the OUT EP FIFO in the QuickUSB Module. The FPGA will then see that the OUT EP FIFO is not empty and read out the data into the FIFO inside the FPGA. Once data is present in the FIFO in the FPGA, the FPGA transfers the data to the IN EP FIFO as long as there is room (the QuickUSB IN EP FIFO is not full).

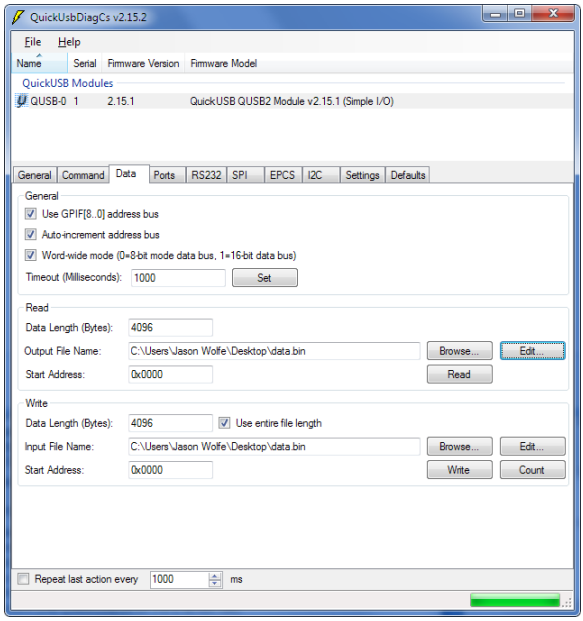

Figure 7 – QuickUSB Diagnostics Data Tab for Loop Back Test

4. Read Data from the FPGA:
   a. Navigate to the "Data" tab. Under the "Read" section, enter "4096" into the Data Length textbox. This value sets the number of bytes for the QuickUSB Module to read.
   b. Specify a file for the read data to be written to by clicking the "Browse" button next to the "Output File Name" textbox. If the file already exists, it will be overwritten.
   c. Click the "Read" button to begin reading data from the FPGA. The QuickUSB Module will then read the requested amount of data from the IN EP FIFO and write it to the specified file. As data is read out of the QuickUSB IN EP FIFO, the FPGA will transfer more data to the IN EP FIFO if there is any data present in the FPGA FIFO.
   d. To verify that the data read correctly, click the "Edit" button in the "Read" section. This will launch a hex editor that will display the contents of the file. Verify that there is an incrementing count as shown in Figure 8. Note that depending on the endianness of your system, the MSB and LSB of the read data may be reversed from that shown in Figure 8.

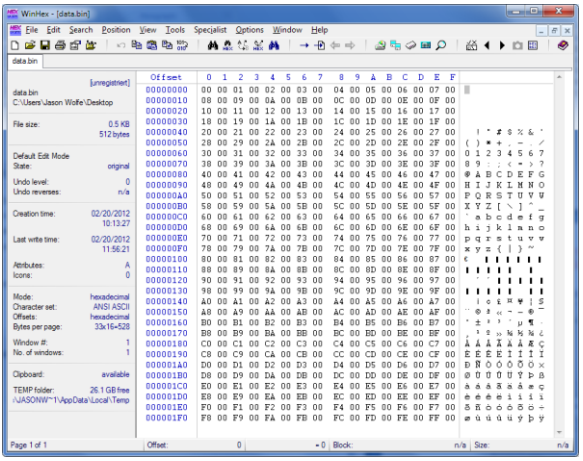

Figure 8 – Hex Editor with Incrementing Count