Getting Started

with

QuickUSB®

Evaluation Board

Memory Demo

Bitwise™ systems

Getting started with QuickUSB
Evaluation Board Memory Demo

Bitwise Systems
6489 Calle Real, Suite E
Goleta, CA 93117
Voice (805) 683-6469
Fax (805) 683-4833
Toll Free (800) 224-1633
Web Site www.bitwisesys.com
Information info@bitwisesys.com
Technical Support support@bitwisesys.com

Version 2.15.1
February 21, 2012

Introduction

The Memory Demo FPGA sample demonstrates how to create a simple interface to memory blocks inside an FPGA. This sample shows how to perform data and command reads and writes to FPGA RAM memory without needing to write any software or even having to build the Quartus II FPGA project.

The Memory Demo may be used as a simple test to verify connectivity of the QuickUSB data bus to an FPGA using the Simple IO Model, as well as a way for a designer to test a new software application developed for QuickUSB.

While the Memory Demo sample and documentation are intended for use with the QuickUSB Starter Kit, the HDL concepts covered in the sample, as well as the process for testing the sample, are applicable to any FPGA design using QuickUSB.

System Requirements

- QuickUSB Library v2.15.1 (or later)
- QuickUSB Starter Kit v2.15.1 (or later)
- QuickUSB Starter Kit containing a QuickUSB Evaluation Board and QuickUSB Module programmed with the Simple I/O Model firmware (v2.15.1 or later)

Hardware Setup

Attach the QuickUSB Module to the QuickUSB Evaluation Board as shown in Figure 1. The QuickUSB Module will lock into place with the four plastic lock-in supports.

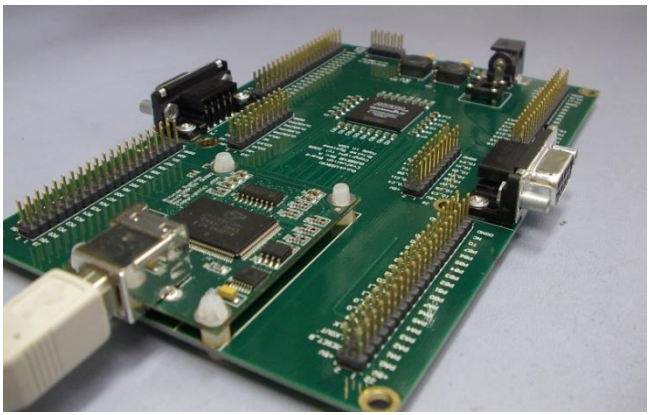

Figure 1 – Proper Attachment of the QuickUSB Module

Updating the QuickUSB Module Firmware

For proper operation, the Memory Demo requires the QuickUSB Module to have the Simple I/O Model firmware loaded. You can tell which version of firmware your module has either with the QuickUSB Diagnostics software or by starting the QuickUSB Programmer and reading the "Description" field. If description of the QuickUSB firmware does not contain "Simple I/O" or reports a version older than v2.15.1, then you need to change the firmware.

Perform the following steps to change the QuickUSB firmware:

1. Start the QuickUSB Programmer that is installed with the QuickUSB Library
2. Select "File->Program EEPROM" and browse to the "quickusb-simple v2.15.1.qusb" firmware file.
3. The programming process should take only a few seconds and its progress is indicated with a progress bar near the status bar. After the Firmware has been updated, you will be prompted to disconnect and reconnect the QuickUSB Module from the USB cable to load the firmware. If you have external power connected to the QuickUSB Evaluation Board, please remove it as well (See Figure 2).

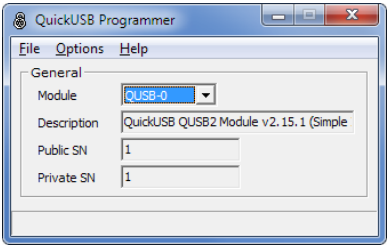

Figure 2 – QuickUSB Programmer

Configuring the FPGA

1. Apply Power
   a. Run the QuickUSB Diagnostics application that is installed with the QuickUSB Library
   b. Navigate to the "Ports" tab. Under "Port A", check Bit 7 in the "Dir" bit checkbox field to set PA7 as an output (see Figure 4)
   c. Under "Port A", check Bit 7 in the "Value" bit checkbox field to drive PA7 high. This will enable power to the FPGA (see Figure 4).
2. Configure the FPGA
   a. Navigate to the "General" tab of the QuickUSB Diagnostics application (see Figure 3)
   b. In the "FPGA" section, click the "Browse" button and select the "counter.rbf" file. The RBF file is installed with the QuickUSB Starter Kit Library, typically under "C:\Program Files\Bitwise Systems\Evaluation Board\Samples\Verilog\QUSBEVB_Memory" directory.
   c. Ensure that the "FPGA Type" is set to "Altera Passive Serial"
   d. Configure the FPGA by clicking the "Upload" button. Once the

configuration has completed, a message will be displayed in the status bar indicating success or failure. You may also query if the FPGA is configured by clicking the “Is Configured?” button. If the programming process fails, ensure that power in applied to the FPGA (see Step 1).

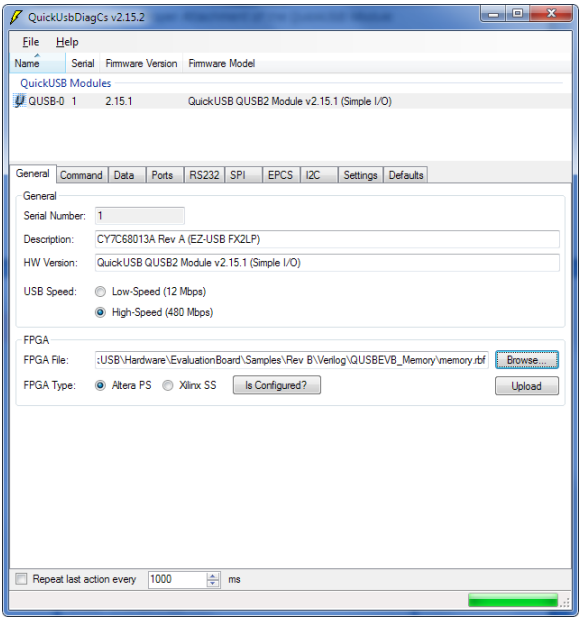

Figure 3 – QuickUSB Diagnostics ”General” Tab

Running the Memory Test

1. Run the QuickUSB Diagnostics application that is installed with the QuickUSB Library.
2. PA0 is the active low reset for the logic in the FPGA. Driving PA0 then high will reset the Counter in the FPGA.
   a. Navigate to the “Ports” tab
   b. Under “Port A”, check Bit 0 in the “Dir” bit checkbox field to configure PA0 as an output, as shown in Figure 4
   c. Under “Port A”, uncheck Bit 0 in the “Value” bit checkbox field to drive PA0 low and reset the logic in the FPGA. Then, check Bit 0 in the “Value” bit checkbox field again to drive PA0 high.

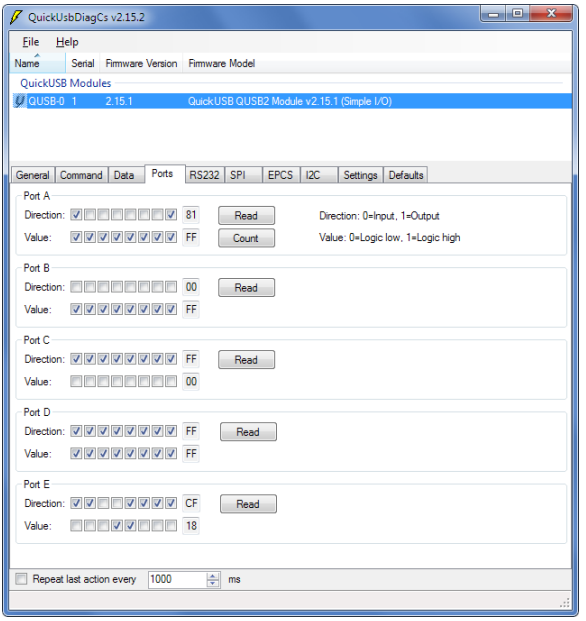

Figure 4 – Reset the Counter Demo with the QuickUSB Diagnostics Program

3. Write Data to the Data RAM.
   a. Click on the "Data" tab as shown in Figure 5
   b. Ensure that the "Use GPIF address bus", "Auto-increment address bus", and "Word-wide mode" checkbox are all checked under the "General" section. The address bus is used to as the RAM address and we are using a 16-byte data bus. Each RAM (the Data RAM and Command RAM) are 512 words wide (1024 bytes).
   c. In the "Write" section, enter "1024" in the "Data Length" textbox and "0x0000" in the "Start Address" textbox, then click the "Count" button. This will write an incrementing count of 512 words to the Data RAM in the FPGA.
4. Read Data from RAM
   a. Click on the "Data" tab (see Figure 5)
   b. Specify a file for the read data to be written to by clicking the "Browse" button next to the "Output File Name" textbox. If the file already exists, it will be overwritten.
   c. In the "Read" section, enter "1024" in the "Data Length" textbox and "0x0000" in the "Start Address" textbox, then click "Read". The QuickUSB Module will read the data from the memory in the FPGA.
   d. To verify that counting data was written and read correctly, click the "Edit" button in the "Read" section. This will launch a hex editor that will display the contents of the file. Verify that there is an incrementing count as shown in Figure 6. Note that depending on the endianness of your system, the MSB and LSB of the read data may be reversed from that shown in Figure 6.

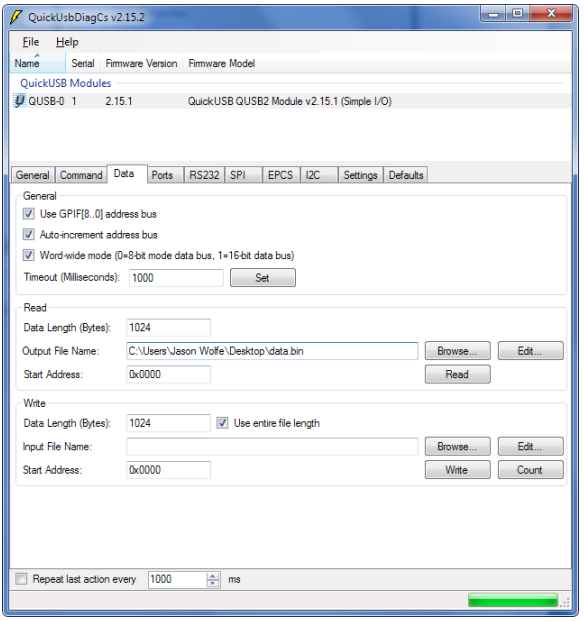

Figure 5 – QuickUSB Diagnostics "Data" Tab

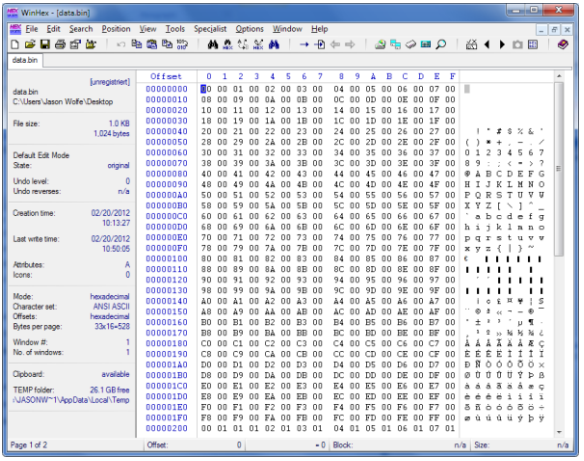

Figure 6 – Hex Editor with Incrementing Count

5. Write Commands to RAM
   a. Click on the "Command" tab (see Figure 7)
   b. Under the "Write" section, enter "0x0100" in the address textbox to set the memory address to 256. Enter "8" in the "Bytes" textboxes to indicate that we will write 8 bytes of data.
   c. In The "Write" section, in the multiline text box enter the space-separated byte data "0xab 0xcd 0xef 0x01 0x23 0x45 0x67 0x89"

d. Click “Write” to write the commands to the Command RAM in the FPGA

6. Read Commands from RAM

a. Click on the “Command” tab (see Figure 7)

b. Under the “Read” section, enter “0x00FF” in the address textbox to set the word memory address to 255. Enter “12” in the “Bytes” textboxes to indicate that we will read 12 bytes of data.

c. Click the “Read” button to read the Command RAM. Because we indicated a read address one word before our write, and because we are reading two extra words, you will read the words both before and after the data written earlier (See Figure 7), which will be zero as the FPGA memory blocks initialize to zero.

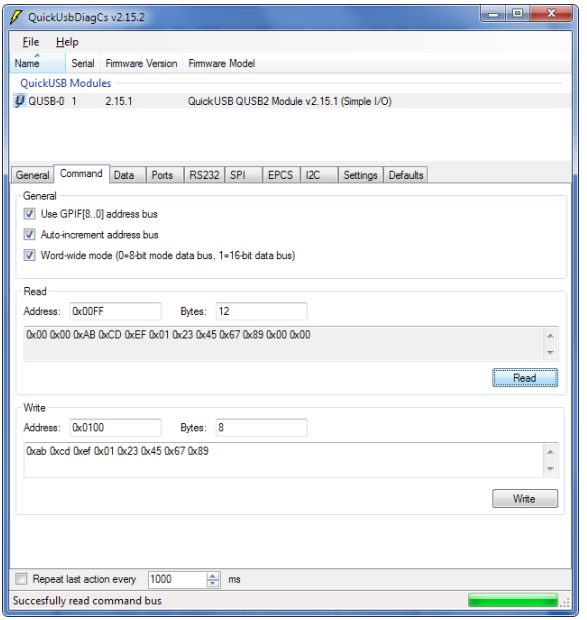

Figure 7 – QuickUSB Diagnostics “Command” Tab