

*Getting Started*  
*with*  
**QuickUSB<sup>®</sup>**

*Evaluation Board*  
*Counter Demo*

**Bitwise<sup>™</sup>**  
..... **systems**

Getting started with QuickUSB  
Evaluation Board Counter Demo

Bitwise Systems  
6489 Calle Real, Suite E  
Goleta, CA 93117

Voice	(805) 683-6469
Fax	(805) 683-4833
Toll Free	(800) 224-1633
Web Site	<a href="http://www.bitwisesys.com">www.bitwisesys.com</a>
Information	<a href="mailto:info@bitwisesys.com">info@bitwisesys.com</a>
Technical Support	<a href="mailto:support@bitwisesys.com">support@bitwisesys.com</a>

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## Overview

The Counter Demo FPGA sample demonstrates how to create a basic data interface between a computer and an FPGA using QuickUSB. This sample shows how to perform and verify data reads using an incrementing counter register without needing to write any software or even having to build the Quartus II FPGA project.

The Counter Demo may be used as a simple test to verify connectivity of the QuickUSB data bus to an FPGA using the Simple IO Model, as well as a way for a designer to test a new software application developed for QuickUSB.

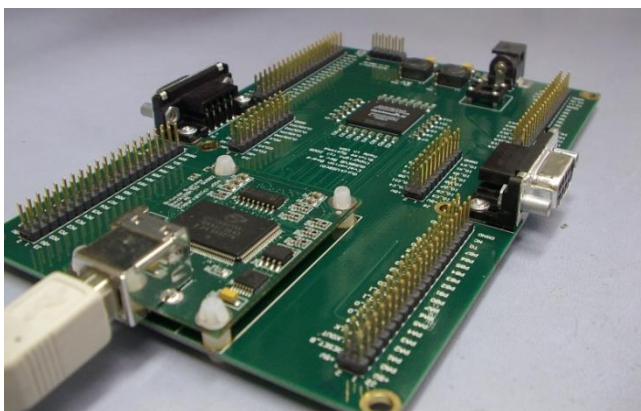
While the Counter Demo sample and documentation are intended for use with the QuickUSB Starter Kit, the HDL concepts covered in the sample, as well as the process for testing the sample, are applicable to any FPGA design using QuickUSB.

## System Requirements

- QuickUSB Library v2.15.1 (or later)
- QuickUSB Starter Kit v2.15.1 (or later)
- QuickUSB Starter Kit containing a QuickUSB Evaluation Board and QuickUSB Module programmed with the Simple I/O Model firmware (v2.15.1 or later)

## Hardware Setup

Attach the QuickUSB Module to the QuickUSB Evaluation Board as shown in Figure 1. The QuickUSB Module will lock into place with the four plastic lock-in supports.



*Figure 1 – Proper Attachment of the QuickUSB Module*

### Updating the QuickUSB Module Firmware

For proper operation, the Counter Demo requires the QuickUSB Module to have the Simple I/O Model firmware loaded. You can tell which version of firmware your module has either with the QuickUSB Diagnostics software or by starting the QuickUSB Programmer and reading the “Description” field. If description of the QuickUSB firmware does not contain “Simple I/O” or reports a version older than v2.15.1, then you need to change the firmware.

Perform the following steps to change the QuickUSB firmware:

1. Start the QuickUSB Programmer that is installed with the QuickUSB Library
2. Select “File->Program EEPROM” and browse to the “quickusb-simple v2.15.1.qusb” firmware file.
3. The programming process should take only a few seconds and its progress is indicated with a progress bar near the status bar. After the Firmware has been updated, you will be prompted to disconnect and reconnect the QuickUSB Module from the USB cable to load the firmware. If you have external power connected to the QuickUSB Evaluation Board, please remove it as well (See Figure 2).

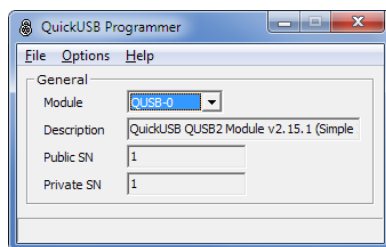


Figure 2 – QuickUSB Programmer

### Configuring the FPGA

1. Apply Power
  - a. Run the QuickUSB Diagnostics application that is installed with the QuickUSB Library
  - b. Navigate to the “Ports” tab. Under “Port A”, check Bit 7 in the “Dir” bit checkbox field to set PA7 as an output (see Figure 4)
  - c. Under “Port A”, check Bit 7 in the “Value” bit checkbox field to drive PA7 high. This will enable power to the FPGA (see Figure 4).
2. Configure the FPGA
  - a. Navigate to the “General” tab of the QuickUSB Diagnostics application (see Figure 3)
  - b. In the “FPGA” section, click the “Browse” button and select the “counter.rbf” file. The RBF file is installed with the QuickUSB Starter Kit Library, typically under “C:\Program Files\Bitwise Systems\Evaluation Board\Samples\Verilog\QUSBEVB\_Counter” directory.
  - c. Ensure that the “FPGA Type” is set to “Altera Passive Serial”
  - d. Configure the FPGA by clicking the “Upload” button. Once the

configuration has completed, a message will be displayed in the status bar indicating success or failure. You may also query if the FPGA is configured by clicking the “Is Configured?” button. If the programming process fails, ensure that power is applied to the FPGA (see Step 1).

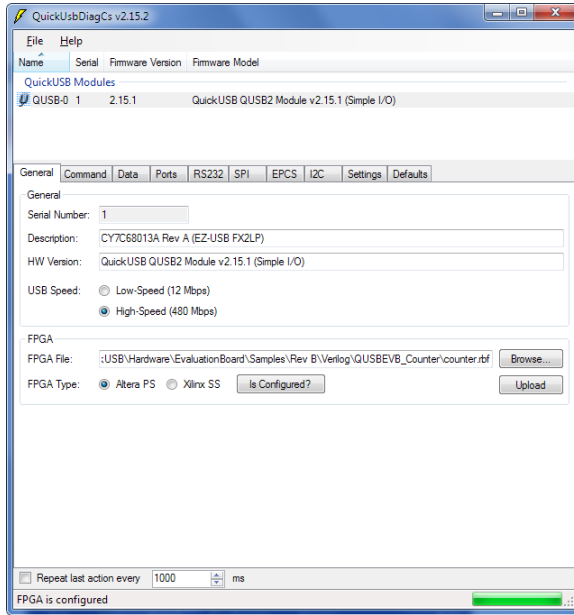


Figure 3 – QuickUSB Diagnostics “General” Tab

## Running the Counter Test

1. Run the QuickUSB Diagnostics application that is installed with the QuickUSB Library.
2. PA0 is the active low reset for the logic in the FPGA. Driving PA0 then high will reset the Counter in the FPGA.
  - a. Navigate to the “Ports” tab
  - b. Under “Port A”, check Bit 0 in the “Dir” bit checkbox field to configure PA0 as an output, as shown in Figure 4
  - c. Under “Port A”, uncheck Bit 0 in the “Value” bit checkbox field to drive PA0 low and reset the logic in the FPGA. Then, check Bit 0 in the “Value” bit checkbox field again to drive PA0 high.

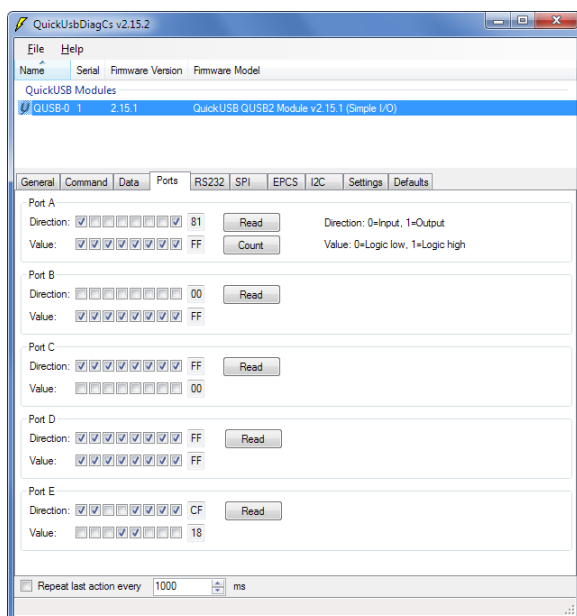


Figure 4 – Reset the Counter Demo with the QuickUSB Diagnostics Program

3. Read Data from the Counter in the FPGA.
  - a. Navigate to the “Data” tab. Check the “Word-wide mode” checkbox if it is not already checked (see Figure 5). This will enable the QuickUSB Module to be in Word-Wide mode and use a 16-bit data bus.
  - b. Under the “Read” section, enter “512” into the Data Length textbox. This value sets the number of bytes for the QuickUSB Module to read.
  - c. Specify a file for the read data to be written to by clicking the “Browse” button next to the “Output File Name” textbox. If the file already exists, it will be overwritten.
  - d. Click the “Read” button to begin reading data from the FPGA. The QuickUSB Module will then read the requested amount of data from the Counter in the FPGA and write it to the specified file.
  - e. To verify that the data read correctly, click the “Edit” button in the “Read” section. This will launch a hex editor that will display the contents of the file. Verify that there is an incrementing count as shown in Figure 6. Note that depending on the endianness of your system, the MSB and LSB of the read data may be reversed from that shown in Figure 6.

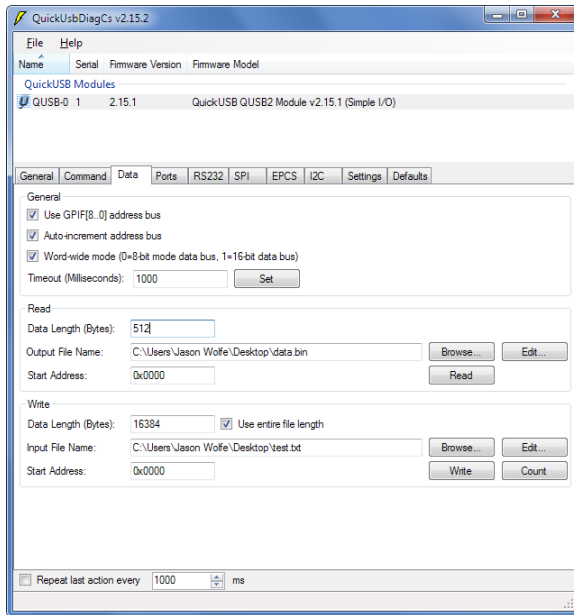


Figure 5 – QuickUSB Diagnostics "Data" Tab

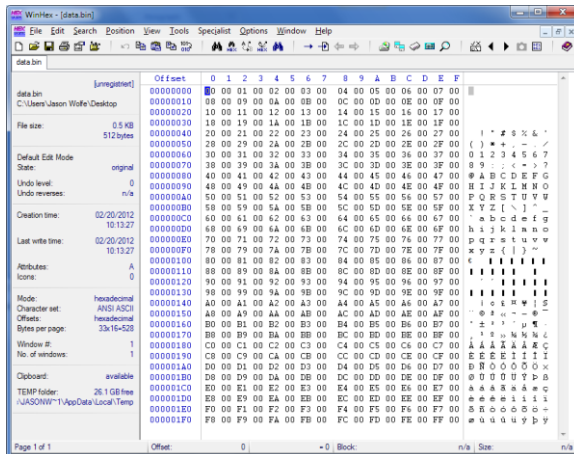


Figure 6 – Hex Editor with Incrementing Count