Rev 1.32 Date 5/16/2003





Connector J1 See Target Interface Document

Conr	nector	J2					
Pin	Name	Dir	Description	Pin	Name	Dir	Description
1	GND	N/A	Ground	2	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
3	PA0	I/O	FX2 Port A, Bit 0 / U1 Pin 7 / nSS2	4	RESET B	OD	FX2 Reset, Active low.
5	PA1	I/O	FX2 Port A, Bit 1 / U1 Pin 8 / nSS3	6	CLKOUT	Output	FX2 48MHz CPU clock
7	PA2	I/O	FX2 Port A, Bit 2 / U1 Pin 9 / nSS4 / SLOE	8	IFCLK	Output	FX2 48MHz GPIO clock
9	PA3	I/O	FX2 Port A, Bit 3 / U1 Pin 10 / nSS5	10	INT4	Input	FX2 INT4 IRQ. Active high, edge sensitive
11	PA4	I/O	FX2 Port A, Bit 4 / U1 Pin 11 / nSS6 / FIFOADR0	12	RXD 0	Input	FX2 Serial Port 0 RS-232 RxD
13	PA5	I/O	FX2 Port A, Bit 5 / U1 Pin 12 / nSS7 / FIFOADR1	14	TXD 0	Output	FX2 Serial Port 0 RS-232 TxD
15	PA6	I/O	FX2 Port A, Bit 6 / U1 Pin 13 / nSS8 / PKTEND	16	TXD 1	Output	FX2 Serial Port 1 RS-232 TxD
17	PA7	I/O	FX2 Port A, Bit 7 / U1 Pin 14 / nSS9 / FLAGD	18	RXD_1	Input	FX2 Serial Port 1 RS-232 RxD
19	GND	N/A	Ground	20	+5V _	N/A	Unregulated +5V from the USB bus (300mA total)
21	PB0	I/O	FX2 Port B, Bit 0 / FD0	22	CTL0	Output	FX2 GPIF CTL 0 / CMD DATA / FLAGA (PF)
23	PB1	I/O	FX2 Port B, Bit 1 / FD1	24	CTL1	Output	FX2 GPIF CTL 1 / REN / FLAGB (FULL)
25	PB2	I/O	FX2 Port B, Bit 2 / FD2	26	CTL2	Output	FX2 GPIF CTL 2 / WEN / FLAGC (EMPTY)
27	PB3	I/O	FX2 Port B, Bit 3 / FD3	28	CTL3	Output	FX2 GPIF CTL 3 / nREN
29	PB4	I/O	FX2 Port B, Bit 4 / FD4	30	CTL4	Output	FX2 GPIF CTL 4 / nWEN
31	PB5	I/O	FX2 Port B, Bit 5 / FD5	32	CTL5	Output	FX2 GPIF CTL 5 / AEN
33	PB6	I/O	FX2 Port B, Bit 6 / FD6	34	RXD0	Input	FX2 Serial Port 0 TTL RxD (Do not use if U1 is populated)
35	PB7	I/O	FX2 Port B, Bit 7 / FD7	36	TXD0	Output	FX2 Serial Port 0 TTL RxD (Do not use if U1 is populated)
37	T0	Input	FX2 Input for Timer0	38	T1	Input	FX2 Input for Timer1
39	GND	N/A	Ground	40	+5V	N/A	Unregulated +5V from the USB bus (300mA total)
•	4						
Conr Pin	nector Name	J3 Dir	Description	Pin	Name	Dir	Description
1 <u>.</u>	PC0	I/O				ווט	
3	PC1		FX2 Port C. Bit 0 / GPIFADR0	2	RDY0	Innut	
			FX2 Port C, Bit 0 / GPIFADR0 EX2 Port C, Bit 1 / GPIFADR1	2 4	RDY0 RDY1	Input Input	FX2 GPIF input signal 0 / SLRD
5		I/O	FX2 Port C, Bit 1 / GPIFADR1	4	RDY1	Input	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR
	PC2	I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2	4 6	RDY1 RDY2	Input Input	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2
7	PC2 PC3	I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3	4 6 8	RDY1 RDY2 RDY3	Input Input Input	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3
7 9	PC2 PC3 PC4	I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4	4 6 8 10	RDY1 RDY2 RDY3 RDY4	Input Input Input Input	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4
7 9 11	PC2 PC3 PC4 PC5	I/O I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5	4 6 8 10 12	RDY1 RDY2 RDY3 RDY4 RDY5	Input Input Input Input Input	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5
7 9 11 13	PC2 PC3 PC4 PC5 PC6	I/O I/O I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6	4 6 8 10 12 14	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1	Input Input Input Input Input Input Input	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated)
7 9 11 13 15	PC2 PC3 PC4 PC5 PC6 PC7	I/O I/O I/O I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7	4 6 8 10 12 14 16	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1	Input Input Input Input Input Input Input Output	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated)
7 9 11 13 15	PC2 PC3 PC4 PC5 PC6 PC7 GND	I/O I/O I/O I/O I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground	4 6 8 10 12 14 16 18	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V	Input Input Input Input Input Input Input Output N/A	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total)
7 9 11 13 15 17	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0	I/O I/O I/O I/O I/O I/O N/A I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8	4 6 8 10 12 14 16 18 20	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0	Input Input Input Input Input Input Output N/A I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI
7 9 11 13 15 17 19	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1	I/O I/O I/O I/O I/O I/O N/A I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9	4 6 8 10 12 14 16 18 20 22	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1	Input Input Input Input Input Input Output N/A I/O I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK
7 9 11 13 15 17 19 21	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2	I/O I/O I/O I/O I/O I/O I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10	4 6 8 10 12 14 16 18 20 22 24	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2	Input Output N/A I/O I/O I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE
7 9 11 13 15 17 19 21 23	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2 PD3	I/O I/O I/O I/O I/O I/O I/O I/O I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11	4 6 8 10 12 14 16 18 20 22 24 26	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2 PE3	Input Output N/A I/O I/O I/O I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG
7 9 11 13 15 17 19 21 23 25 27	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2 PD3 PD4	I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12	4 6 8 10 12 14 16 18 20 22 24 26 28	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2 PE3 PE4	Input Output N/A I/O I/O I/O I/O I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS
7 9 11 13 15 17 19 21 23 25 27	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2 PD3 PD4 PD5	I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 5 / FD13	4 6 8 10 12 14 16 18 20 22 24 26 28 30	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2 PE3 PE4 PE5	Input Output N/A I/O I/O I/O I/O I/O I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO
7 9 111 13 15 17 19 21 23 25 27 29	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2 PD3 PD4 PD5 PD6	I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 5 / FD13 FX2 Port D, Bit 6 / FD14	4 6 8 10 12 14 16 18 20 22 24 26 28 30 32	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2 PE3 PE4 PE5 PE6	Input I/O I/O I/O I/O I/O I/O I/O I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATAO / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0
7 9 11 13 15 17 19 21 23 25 27 29 31	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7	I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 6 / FD14 FX2 Port D, Bit 6 / FD14 FX2 Port D, Bit 7 / FD15	4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2 PE3 PE4 PE5 PE6 PE7	Input I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 6 / nSS0 FX2 Port E, Bit 6 / nSS0 FX2 Port E, Bit 7 / GPIFADR8 / nSS1
7 9 11 13 15 17 19 21 23 25 27 29 31 33 35	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7 SCL	I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 3 / FD11 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 6 / FD14 FX2 Port D, Bit 6 / FD14 FX2 Port D, Bit 7 / FD15 Clock for I2C interface (Termination supplied on-board)	4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2 PE3 PE4 PE5 PE6 PE7 WAKEUP_B	Input I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 5 / CONF_DONE / MISO FX2 Port E, Bit 6 / nSS0 FX2 Port E, Bit 7 / GPIFADR8 / nSS1 FX2 USB Wakeup. Active low.
5 7 9 11 13 15 17 19 21 22 27 29 31 33 35 37 39	PC2 PC3 PC4 PC5 PC6 PC7 GND PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7	I/O	FX2 Port C, Bit 1 / GPIFADR1 FX2 Port C, Bit 2 / GPIFADR2 FX2 Port C, Bit 3 / GPIFADR3 FX2 Port C, Bit 4 / GPIFADR4 FX2 Port C, Bit 5 / GPIFADR5 FX2 Port C, Bit 6 / GPIFADR6 FX2 Port C, Bit 7 / GPIFADR7 Ground FX2 Port D, Bit 0 / FD8 FX2 Port D, Bit 1 / FD9 FX2 Port D, Bit 2 / FD10 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 4 / FD12 FX2 Port D, Bit 6 / FD14 FX2 Port D, Bit 6 / FD14 FX2 Port D, Bit 7 / FD15	4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34	RDY1 RDY2 RDY3 RDY4 RDY5 RXD1 TXD1 +5V PE0 PE1 PE2 PE3 PE4 PE5 PE6 PE7	Input I/O I/O I/O I/O I/O I/O I/O I/O I/O	FX2 GPIF input signal 0 / SLRD FX2 GPIF input signal 1 / SLWR FX2 GPIF input signal 2 FX2 GPIF input signal 3 FX2 GPIF input signal 4 FX2 GPIF input signal 4 FX2 GPIF input signal 5 FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) FX2 Serial Port 1 TTL RxD (Do not use if U1 is populated) Unregulated +5V from the USB bus (300mA total) FX2 Port E, Bit 0 / DATA0 / MOSI FX2 Port E, Bit 1 / DCLK / SCK FX2 Port E, Bit 2 / nCE FX2 Port E, Bit 3 / nCONFIG FX2 Port E, Bit 4 / nSTATUS FX2 Port E, Bit 6 / nSS0 FX2 Port E, Bit 6 / nSS0 FX2 Port E, Bit 7 / GPIFADR8 / nSS1

Rev 1.32 Date 5/16/2003





Connector J4 Pin Name Dir Description Pin Name Dir Description Regulated +3.3V from evaluation board regulator +3VD N/A Regulated +3.3V from evaluation board regulator +3VD N/A USERIO7 USERIO8 3 I/O U1. Pin 7 / Port A. Bit 0 I/O U1. Pin 8 / Port A. Bit 1 USERIO9 I/O U1. Pin 9 / Port A. Bit 2 6 USERIO10 I/O U1. Pin 10 / Port A. Bit 3 5 7 USERIO11 I/O U1, Pin 11 / Port A, Bit 4 8 USERIO12 I/O U1, Pin 12 / Port A, Bit 5 USERIO13 I/O U1. Pin 13 / Port A. Bit 6 USERIO14 I/O U1, Pin 14 / Port A, Bit 7 USERIO15 U1. Pin 15 / Port B. Bit 0 12 USERIO16 I/O U1. Pin 16 / Port B. Bit 1 11 I/O 13 USERIO17 I/O U1. Pin 17 / Port B. Bit 2 14 USERIO18 I/O U1. Pin 18 / Port B. Bit 3 15 USERIO19 I/O U1, Pin 19 / Port B, Bit 4 16 USERIO24 I/O U1. Pin 24 / Port B. Bit 5 17 USERIO25 I/O U1, Pin 25 / Port B, Bit 6 18 USERIO26 I/O U1, Pin 26 / Port B, Bit 7 19 USERIO27 I/O U1, Pin 27 / Port C, Bit 0 20 USERIO28 I/O U1, Pin 28 / Port C, Bit 1 USERIO29 U1, Pin 29 / Port C, Bit 2 USERIO30 U1. Pin 30 / Port C. Bit 3 21 I/O 22 I/O 23 USERIO31 I/O U1. Pin 31 / Port C. Bit 4 24 USERIO36 I/O U1. Pin 36 / Port C. Bit 5 USERIO38 25 USERIO37 I/O U1. Pin 37 / Port C. Bit 6 26 I/O U1. Pin 38 / Port C. Bit 7 27 USERIO39 I/O U1, Pin 39 / Port D, Bit 0 28 USERIO40 I/O U1, Pin 40 / Port D, Bit 1 29 USERIO41 I/O U1, Pin 41 / Port D, Bit 2 30 USERIO44 I/O U1, Pin 44 / Port D, Bit 3 31 USERIO45 I/O U1. Pin 45 / Port D. Bit 4 32 USERIO46 I/O U1. Pin 46 / Port D. Bit 5 U1, Pin 53 / Port D, Bit 7 33 USERIO47 I/O U1, Pin 47 / Port D, Bit 6 34 USERIO53 I/O 35 USERIO54 I/O U1. Pin 54 / FX2 SCL 36 USERIO55 I/O U1. Pin 55 / FX2 SDA 37 USERIO56 I/O U1, Pin 56 / FX2 T0 38 USERIO57 I/O U1, Pin 57 / FX2 INT4 39 N/A N/A Ground **GND** Ground **GND** Connector J5 Name Dir Description Pin Name Dir Description +3VD N/A Regulated +3.3V from evaluation board regulator 2 +3VD N/A Regulated +3.3V from evaluation board regulator 3 USERIO58 I/O U1, Pin 58 / FX2 CTL0 USERIO60 I/O U1. Pin 60 / FX2 CTL1 USERIO61 I/O U1. Pin 61 / FX2 CTL2 6 USERIO62 I/O U1. Pin 62 / FX2 CTL3 5 7 USERIO63 I/O U1, Pin 63 / FX2 CTL4 8 USERIO64 I/O U1, Pin 64 / FX2 CTL5 9 USERIO65 I/O U1, Pin 65 / FX2 RDY0 10 USERIO67 I/O U1, Pin 67 / FX2 RDY0 11 USERIO68 I/O U1, Pin 68 / FX2 RDY2 12 USERIO69 I/O U1, Pin 69 / FX2 RDY3 I/O 13 USERIO70 I/O U1, Pin 70 / FX2 RDY4 14 USERIO71 U1, Pin 71 / FX2 RDY5 15 USERIO73 I/O U1, Pin 73 / Port E, Bit 6 16 USERIO74 I/O U1, Pin 74 / Port E, Bit 7 17 USERIO75 I/O U1, Pin 75 / FX2 USB Wakeup. Active low. 18 INPUT1 Input U1. Pin 78 19 Global Clock 1 See Schematic 20 INPUT2 U1. Pin 80 GLCK1 N/A Input 21 USERIO83 I/O U1, Pin 83 / FX2 T1 22 USERIO85 I/O U1, Pin 85 / FX2 INT5 U1, Pin 86 U1, Pin 87 23 USERIO86 I/O 24 USERIO87 I/O 25 U1. Pin 88 26 USERIO89 I/O U1. Pin 89 USERIO88 I/O 27 USERIO90 I/O U1, Pin 90 28 USERIO92 I/O U1, Pin 92 29 USERIO93 I/O U1. Pin 93 30 USERIO94 I/O U1. Pin 94 31 USERIO95 U1, Pin 95 32 USERIO96 I/O U1, Pin 96 U1, Pin 99 33 USERIO97 I/O U1, Pin 97 34 USERIO99 I/O 35 USERIO100 I/O U1, Pin 100 36 USERIO101 I/O U1, Pin 101 37 USERIO102 I/O U1. Pin 102 USERIO103 I/O U1. Pin 103 39 Ground GND Ground 40 GND N/A

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5385 Hollister Ave, Suite 215 Santa Barbara, CA 93111

Connector		J6					5
Pin	Name	Dir	Description	Pin	Name	Dir	Description
	+3VD	N/A	Regulated +3.3V from evaluation board regulator	2	+3VD	N/A	Regulated +3.3V from evaluation board regulator
	USERIO104	I/O	U1, Pin 104	4	USERIO111	I/O	U1, Pin 111
	USERIO112	I/O	U1, Pin 112	6	USERIO113	I/O	U1, Pin 113
	USERIO114	I/O	U1, Pin 114	8	USERIO115	I/O	U1, Pin 115
	USERIO116	I/O	U1, Pin 116	10	USERIO119	I/O	U1, Pin 119
1	USERIO120	I/O	U1, Pin 120	12	USERIO121	I/O	U1, Pin 121
3	USERIO122	I/O	U1, Pin 122	14	USERIO125	I/O	U1, Pin 125
5	USERIO126	I/O	U1, Pin 126	16	USERIO127	I/O	U1, Pin 127
7	USERIO128	I/O	U1, Pin 128	18	USERIO131	I/O	U1, Pin 131
9	USERIO132	I/O	U1, Pin 132	20	USERIO133	I/O	U1, Pin 133
1	USERIO134	I/O	U1, Pin 134	22	USERIO135	I/O	U1, Pin 135
3	USERIO136	I/O	U1, Pin 136	24	USERIO139	I/O	U1, Pin 139
5	USERIO140	I/O	U1, Pin 140	26	USERIO141	I/O	U1, Pin 141
7	USERIO142	I/O	U1, Pin 142	28	USERIO143	I/O	U1, Pin 143
9	USERIO144	I/O	U1, Pin 144	30	USERIO147		U1, Pin 147
1	USERIO148	I/O	U1, Pin 148	32	USERIO149	I/O	U1, Pin 149
3	USERIO150	I/O	U1, Pin 150	34	USERIO157	I/O	U1, Pin 157
5	USERIO158	I/O	U1, Pin 158	36	USERIO159	I/O	U1, Pin 159
7	USERIO160	I/O	U1, Pin 160	38	USERIO161	I/O	U1, Pin 161
9	GND	N/A	Ground	40	GND	N/A	Ground
on	nector	J7					
in	Name	Dir	Description	Pin	Name	Dir	Description
	+3VD	N/A	Regulated +3.3V from evaluation board regulator	2	+3VD	N/A	Regulated +3.3V from evaluation board regulator
	USERIO162	I/O	U1, Pin 162	4	USERIO163	I/O	U1, Pin 163
	USERIO164	I/O	U1, Pin 164	6	USERIO166	I/O	U1, Pin 166
	USERIO167	I/O	U1, Pin 167	8	USERIO168	I/O	U1, Pin 168
	USERIO169	I/O	U1, Pin 169	10	USERIO170	I/O	U1, Pin 170
1	USERIO172	I/O	U1, Pin 172	12	USERIO173	I/O	U1, Pin 173
3	USERIO174	I/O	U1, Pin 174	14	USERIO175	I/O	U1, Pin 175
5	USERIO176	I/O	U1, Pin 176	16	USERIO177	I/O	U1, Pin 177
	LICEDIO 170	I/O	U1, Pin 179	18	USERIO180	I/O	U1, Pin 180
7	USERIO179	1, 0					EVO 150114 / 114 B1 400
	INPUT3	Input	U1, Pin 182	20	CLK	Input	FX2 IFCLK / U1, Pin 183
9			U1, Pin 182 U1, Pin 184		CLK USERIO186	Input I/O	FX2 IFCLK / U1, Pin 183 U1, Pin 186
9 1	INPUT3	Input	,	20			
9 1 3	INPUT3 INPUT4	Input Input	U1, Pin 184	20 22	USERIO186	I/Ò	U1, Pin 186
9 1 3 5	INPUT3 INPUT4 USERIO187	Input Input I/O	U1, Pin 184 U1, Pin 187 U1, Pin 190	20 22 24	USERIO186 USERIO189 USERIO191	I/O I/O	U1, Pin 186 U1, Pin 189 U1, Pin 191
9 1 3 5 7	INPUT3 INPUT4 USERIO187 USERIO190 USERIO192	Input Input I/O I/O I/O	U1, Pin 184 U1, Pin 187 U1, Pin 190 U1, Pin 192	20 22 24 26 28	USERIO186 USERIO189 USERIO191 USERIO193	I/O I/O I/O I/O	U1, Pin 186 U1, Pin 189 U1, Pin 191 U1, Pin 193
9 1 3 5 7	INPUT3 INPUT4 USERIO187 USERIO190 USERIO192 USERIO195	Input Input I/O I/O I/O I/O	U1, Pin 184 U1, Pin 187 U1, Pin 190 U1, Pin 192 U1, Pin 195	20 22 24 26 28 30	USERIO186 USERIO189 USERIO191 USERIO193 USERIO196	I/O I/O I/O I/O I/O	U1, Pin 186 U1, Pin 189 U1, Pin 191 U1, Pin 193 U1, Pin 196
9 1 3 5 7 9	INPUT3 INPUT4 USERIO187 USERIO190 USERIO192 USERIO195 USERIO197	Input Input I/O I/O I/O I/O	U1, Pin 184 U1, Pin 187 U1, Pin 190 U1, Pin 192 U1, Pin 195 U1, Pin 197	20 22 24 26 28 30 32	USERIO186 USERIO189 USERIO191 USERIO193 USERIO196 USERIO198	I/O I/O I/O I/O I/O I/O	U1, Pin 186 U1, Pin 189 U1, Pin 191 U1, Pin 193 U1, Pin 196 U1, Pin 198
7 9 1 3 5 7 9 1 3 5	INPUT3 INPUT4 USERIO187 USERIO190 USERIO192 USERIO195 USERIO197 USERIO199	Input Input I/O I/O I/O I/O I/O	U1, Pin 184 U1, Pin 187 U1, Pin 190 U1, Pin 192 U1, Pin 195 U1, Pin 197 U1, Pin 199	20 22 24 26 28 30 32 34	USERIO186 USERIO189 USERIO191 USERIO196 USERIO198 USERIO200	I/O I/O I/O I/O I/O I/O	U1, Pin 186 U1, Pin 189 U1, Pin 191 U1, Pin 193 U1, Pin 196 U1, Pin 198 U1, Pin 200
9 1 3 5 7 9 1 3 5	INPUT3 INPUT4 USERIO187 USERIO190 USERIO192 USERIO195 USERIO197 USERIO199 USERIO202	Input Input I/O I/O I/O I/O I/O I/O	U1, Pin 184 U1, Pin 187 U1, Pin 190 U1, Pin 192 U1, Pin 195 U1, Pin 197 U1, Pin 199 U1, Pin 202	20 22 24 26 28 30 32 34	USERIO186 USERIO189 USERIO191 USERIO193 USERIO196 USERIO198 USERIO200 USERIO203	I/O I/O I/O I/O I/O I/O I/O	U1, Pin 186 U1, Pin 189 U1, Pin 191 U1, Pin 193 U1, Pin 196 U1, Pin 198 U1, Pin 200 U1, Pin 203
9 1 3 5 7 9 1	INPUT3 INPUT4 USERIO187 USERIO190 USERIO192 USERIO195 USERIO197 USERIO199	Input Input I/O I/O I/O I/O I/O	U1, Pin 184 U1, Pin 187 U1, Pin 190 U1, Pin 192 U1, Pin 195 U1, Pin 197 U1, Pin 199	20 22 24 26 28 30 32 34	USERIO186 USERIO189 USERIO191 USERIO196 USERIO198 USERIO200	I/O I/O I/O I/O I/O I/O	U1, Pin 186 U1, Pin 189 U1, Pin 191 U1, Pin 193 U1, Pin 196 U1, Pin 198 U1, Pin 200

Rev 1.32 Date 5/16/2003





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Conn	ector	P1	
Pin	Name	Dir	Description
1	NC	N/A	Not Connected
2	TXD_0	Output	FX2 RXD_0 Pin 51 (NULL Modem incorporated into board)
3	RXD_0	Input	FX2 TXD_0 Pin 50 (NULL Modem incorporated into board)
4	NC	N/A	Not Connected
5	GND	N/A	Ground
6	NC	N/A	Not Connected
7	NC	N/A	Not Connected
8	NC	N/A	Not Connected
9	NC	N/A	Not Connected
Conn	ector	P2	
Pin	Name	Dir	Description
1	NC	N/A	Not Connected
2		1 4// 1	
_	TXD_1	Output	FX2 RXD_1 Pin 53 (NULL Modem incorporated into board)
3	TXD_1 RXD_1		
	_	Output	FX2 RXD_1 Pin 53 (NULL Modem incorporated into board)
3	RXD_1	Output Input	FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board)
3 4	RXD_1 NC	Output Input N/A	FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected
3 4 5	RXD_1 NC GND	Output Input N/A N/A	FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected Ground
3 4 5	RXD_1 NC GND NC NC NC	Output Input N/A N/A N/A N/A	FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected Ground Not Connected
3 4 5 6 7	RXD_1 NC GND NC NC	Output Input N/A N/A N/A N/A	FX2 RXD_1 Pin 53 (NULL Modem incorporated into board) FX2 TXD_1 Pin 52 (NULL Modem incorporated into board) Not Connected Ground Not Connected Not Connected

Notes:

- 1) +5V is the USB bus power. Do not exceed 300mA current drain. USB bus supplies 500mA and QuickUSB consumes 200mA.
- 2) RXD0, TXD0, RXD1 & TXD1 are TTL serial lines from the FX2. These signals are only usable when U1 is not populated (Only usable on the QUSB2T board).
- 3) SPI functionality is provided on DATA0 and DCLK