QuickUSB QUSB2 Target Interface Connector
Rev 2.11
Date 3/31/2006

6489 Calle Real, Suite E
Goleta, CA 93117
(805) 683-6469
support@bitwisesys.com

Pin	Name	Alternate Function	Dir	Description
1	GND		N/A	Ground
3	PA0	nSS2 / nINT0	I/O	Port A, Bit 0
5	PA1	nSS3 / nINT1	I/O	Port A, Bit 1
7	PA2	nSS4 / SLOE	I/O	Port A, Bit 2
9	PA3	nSS5	I/O	Port A, Bit 3
11	PA4	nSS6 / FIFOADR0	I/O	Port A, Bit 4
13	PA5	nSS7 / FIFOADR1	I/O	Port A, Bit 5
15	PA6	nSS8 / PKTEND	I/O	Port A, Bit 6
17	PA7	nSS9 / FLAGD / nSLCS	I/O	Port A, Bit 7
19	GND		N/A	Ground
21	PB0	FD0	I/O	Port B, Bit 0
23	PB1	FD1	I/O	Port B, Bit 1
25	PB2	FD2	I/O	Port B, Bit 2
27	PB3	FD3	I/O	Port B, Bit 3
29	PB4	FD4	I/O	Port B, Bit 4
31	PB5	FD5	I/O	Port B, Bit 5
33	PB6	FD6	I/O	Port B, Bit 6
35	PB7	FD7	I/O	Port B, Bit 7
37	GND		N/A	Ground
39	PC0	GPIFADR0	I/O	Port C, Bit 0
41	PC1	GPIFADR1	I/O	Port C, Bit 1
43	PC2	GPIFADR2	I/O	Port C, Bit 2
45	PC3	GPIFADR3	I/O	Port C, Bit 3
47	PC4	GPIFADR4	I/O	Port C, Bit 4
49	PC5	GPIFADR5	I/O	Port C, Bit 5
51	PC6	GPIFADR6	I/O	Port C, Bit 6
53	PC7	GPIFADR7	I/O	Port C, Bit 7
55	GND		N/A	Ground
57	PD0	FD8	I/O	Port D, Bit 0
59	PD1	FD9	I/O	Port D, Bit 1
61	PD2	FD10	I/O	Port D, Bit 2
63	PD3	FD11	I/O	Port D, Bit 3
65	PD4	FD12	I/O	Port D, Bit 4
67	PD5	FD13	I/O	Port D, Bit 5
69	PD6	FD14	I/O	Port D, Bit 6
71	PD7	FD15	I/O	Port D, Bit 7
73	SCL		OD	Clock for I2C interface
75	SDA		OD	Data for I2C interface
77	T0		Input	Input for Timer0
79	GND		N/A	Ground

Pin	Name	Alternate Function	Dir	Description
2	+5V		N/A	Unregulated +5V from the USB bus (250mA total)
4	RESET_B		OD	FX2 reset, Active low.
6	CLKOUT		Output	48MHz CPU clock
8	IFCLK		Output	48MHz GPIO clock
10	INT4		Input	8051 INT4 IRQ. Active high, edge sensitive
12	RXD_0		Input	Serial Port 0 EIA/TIA 564 RxD
14	TXD_0		Output	Serial Port 0 EIA/TIA 564 TxD
16	TXD_1		Output	Serial Port 1 EIA/TIA 564 TxD
18	RXD_1		Input	Serial Port 1 EIA/TIA 564 RxD
20	+5V		N/A	Unregulated +5V from the USB bus (250mA total)
22	CTL0	CMD_DATA / FLAGA	Output	GPIF control output 0
24	CTL1	REN / FLAGB	Output	GPIF control output 1
26	CTL2	WEN / FLAGC	Output	GPIF control output 2
28	CTL3		Output	GPIF control output 3
30	CTL4		Output	GPIF control output 4
32	CTL5		Output	GPIF control output 5
34	RXD0		Input	Serial Port 0 TTL RxD (Do not use if U1 is populated)
36	TXD0		Output	Serial Port 0 TTL RxD (Do not use if U1 is populated)
38	+5V		N/A	Unregulated +5V from the USB bus (250mA total)
40	RDY0	EF / ACK / SLRD	Input	GPIF input signal 0
42	RDY1	FF / SLWR	Input	GPIF input signal 1
44	RDY2		Input	GPIF input signal 2
46	RDY3		Input	GPIF input signal 3
48	RDY4		Input	GPIF input signal 4
50	RDY5		Input	GPIF input signal 5
52	RXD1		Input	Serial Port 1 TTL RxD (Do not use if U1 is populated)
54	TXD1		Output	Serial Port 1 TTL RxD (Do not use if U1 is populated)
56	+5V		N/A	Unregulated +5V from the USB bus (250mA total)
58	PE0	DATA0 / MOSI	I/O	Port E, Bit 0
60	PE1	DCLK / SCK	I/O	Port E, Bit 1
62	PE2	nCE	I/O	Port E, Bit 2
64	PE3	nCONFIG	I/O	Port E, Bit 3
66	PE4	nSTATUS	I/O	Port E, Bit 4
68	PE5	CONF_DONE / MISO	I/O	Port E, Bit 5
70	PE6	nSS0	I/O	Port E, Bit 6
72	PE7	GPIFADR8 / nSS1	I/O	Port E, Bit 7
74	WAKEUP_B		Input	USB Wakeup. Active low. (not used)
76	SW_PG		Output	Power good signal, Active high when +5V is good
78	T1		Input	Input for Timer1
80	+5V		N/A	+5V

Notes:

1) With pin 1 in the upper left, numbering starts with pin 1 and proceeds left to right, top to bottom.
2) The target interface connector is a Hirose FX8-80P-SV. The mating connector is FX8-80S-SV (3mm mating height)
3) +5V is the USB bus power. Do not exceed 400mA current drain. USB bus supplies 500mA, QuickUSB consumes 50mA and you should have a 50mA headroom.
4) RXD0, TXD0, RXD1 & TXD1 are TTL serial lines from the FX2. RXD0 and RXD1 are only usable when pins 9 and 12 respectively of U2 are disconnected.
5) SPI functionality is provided on DATA0, DCLK and nSS0-9

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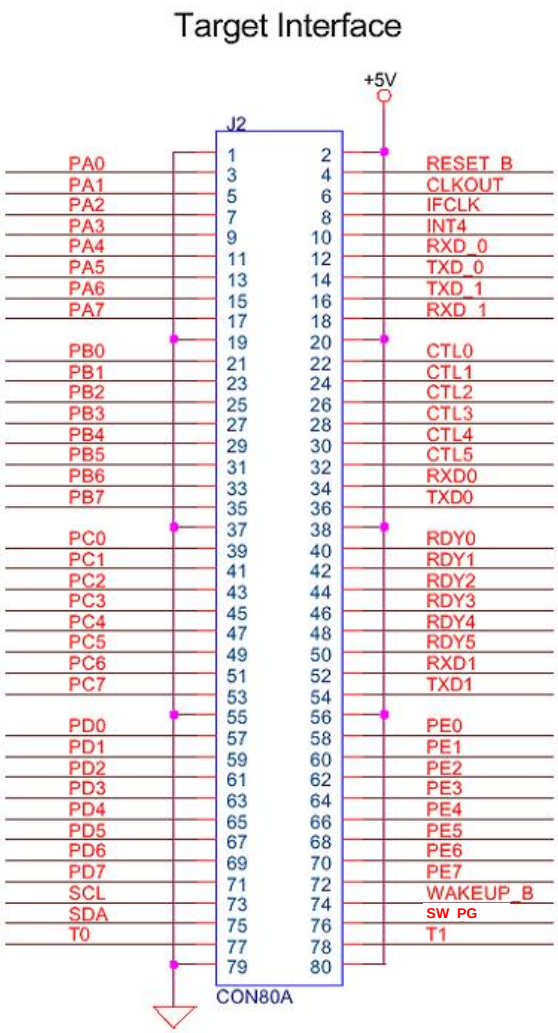
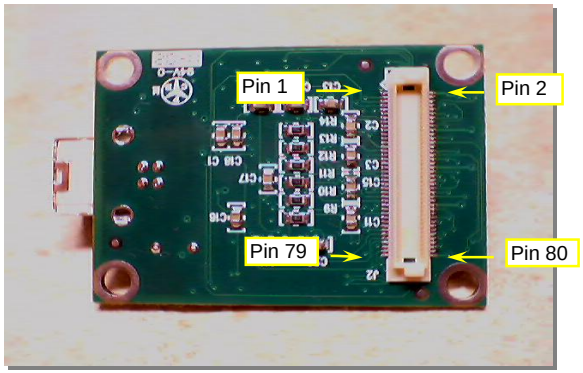
Schematic Symbol



Hirose FX8-80P-SV Connector

Photograph



Mechanical Drawing