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Project Report

**RTL Design and ASIC flow of a 32-Bit RIC-V Architecture**

**Course Project for Digital ASIC Design (ECCE 621)**

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**Submitted to:**

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**Introduction**

This project requires the design of a 32-bit RISC-V architecture that perform 10 different instructions. All the conventional digial design procedures have been thoroughly followed throughout this project work, beginning from high-level simulation and HDL coding. The RTL and Testbenches were coded using verilog (SystemVerilog) and were simulated using both modelSim and Vivado. Additionally, the gate-level netlis and layout design were performed using Synopsys Design Compiler (DC Compiler for short) and IC compiler II (ICC2), respectively.

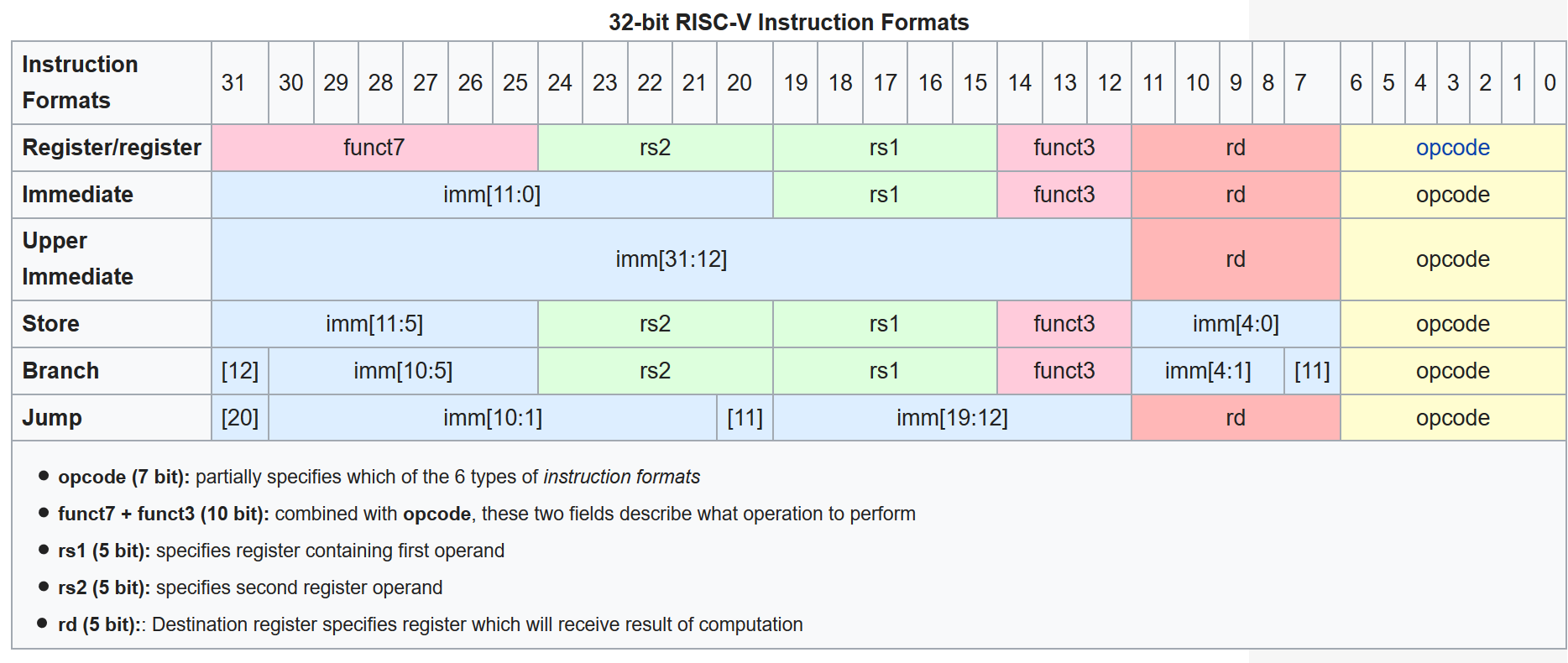
**Design Structure and Setup**

The RISC-V architectural design on this project consists of six different modules (excluding the top module) as shown in Figure-1. The module under the name “program\_counter” fetches instructions from the intruction memory and feeds them to the decoder. The decoder interprets (decrypts) all the received instruction and generates corresponding control signals based on th instruction format given in table-1. These controls signals then drive the associated modules to perform a particular operation.

Diagram, schematic

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Figure-1: The schematic view of verilog RTL

The ALU Unit is responsible for arithmetic and logical operations. Additionally, the branching operation has been embedd inside the ALU unit. This was done with the mere reason that as we have only two branching operations we prefered to include them inside the ALU unit instead of creating a separate module. Doing so would also minimize the uneccesary power and resource utilization associated with the wiring. Moreover, the design consists of three different memory units each of them with a unique purpose and functionality. These are, the Register File, Data Memory and the Instruction Memory. Another important point to note here is that the bit size of the alu control signal that goes to the ALU unit from the decoder has been reduced to three because it sufficiently satisfies the requirements for this project, and Graphical user interface

Description automatically generatedusing a 6-bit or higher would only lead to the wastage of resources and power (particularly for this project).

Figure-2: Simulation Results from Vivado schematic of verilog RTL

Table-1: RISC-V Instruction Format schematic of verilog RTL

Diagram, schematic

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Figure-3: The Schematic of RIC-V when synthesized on vivado for Artix 7 FPGA

**Synthesis Using Synopsys DC Compiler**

The RTL design of this project has also been synthesized into a gate-level netlist using DC compiler. The

schematic diagram shown in figure-4 is obtained after running synthesis on the design using Global Foundry’s 22nm standard cell library. The design on this project capable of running at a maximum frequency of 2MHz (clock period of 500 ps) with out violations. Details about the timinig constraints and report is given in the below illustration.

Table

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Listing-1: Timing report obtained from synthesi using DC compiler

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Listing-2: Area report obtained from synthesi using DC compiler

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Listing-3: power report obtained from synthesi using DC compiler

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Figure-4: The Schematic diagram of RIC-V when synthesized on DC compiler

**Place and Route**

The figure below is obtained after place and route has also been carried out using IC Compiler II (ICC-II for short)

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Figure-5: The Schematic diagram of RIC-V, obtained from ICC-II

**Conclusion**

The flow of the design of RISC-V architecture of this project was thoroughly monitored both for FPGA and ASIC design flow, and decent results were observed in both cases. Generally, the processor is capable of running at a maximum frequency of 2.0 GHz (the synthesis was undertaken with clock period of 500ns, assuming the default unit of time in DC compiler is in nanoseconds) without any timing violations. This chip occupies an area of 0.085mm2 assuming 22nm GF technology, and a total power consumption of 202.3191mW. It is also worth mentioning that this architecture is designed for only a limited number of instructions and operations. However, this work can be expanded in the future to accommodate all the remaining instruction.