W806 MCU Chip Specification

v2.0

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1 Overview

The W806 chip is a secure IoT MCU chip. The chip integrates 32-bit CPU processor, built-in UART, GPIO, SPI, SDIO,

I 2C, I 2S, PSRAM, 7816, ADC, LCD, TouchSensor and other digital interfaces; support TEE security engine, support a variety of hardware

Decryption algorithm, built-in DSP, floating-point unit and security engine, support code security permission setting, built-in 1MB Flash memory, support

Multiple security measures such as firmware encrypted storage, firmware signature, security debugging, and security upgrade ensure product security features. Suitable for small household appliances, smart

Smart home, smart toys, industrial control, medical monitoring and other extensive IoT fields.

2 features

ÿ Chip Appearance

- ÿ QFN56 package, 6mm x 6mm

ÿ MCU Features

- ÿ Integrated 32-bit XT804 processor, operating frequency 240MHz, built-in DSP, floating point unit and security engine
- ÿ Built-in 1MB Flash, 288KB RAM
- ÿ Integrated PSRAM interface, supports up to 64MB external PSRAM memory
- ÿ Integrated 6-way UART high-speed interface
- ÿ Integrated 4 channels of 16-bit ADC, the highest sampling rate is 1KHz
- ÿ Integrates a high-speed SPI interface (slave interface), supporting up to 50MHz
- ÿ Integrates a master/slave SPI interface
- ÿ Integrate 1 SDIO_HOST interface, support SDIO2.0, SDHC, MMC4.2
- ÿ Integrate 1 SDIO_DEVICE, support SDIO2.0, the highest throughput rate is 200Mbps
- ÿ Integrated 1 I 2C controller

ÿ Integrated GPIO controller, supports up to 44 GPIOs

ÿ Integrated 5-way PWM interface

ÿ Integrated 1-way Duplex I 2S controller

ÿ Integrated LCD controller, support 4x32 interface

ÿ Integrate a 7816 interface

ÿ Integrate 15 Touch Sensors

ÿ Security Features

ÿ MCU built-in Tee security engine, the code can distinguish safe world/non-safe world

ÿ Integrated SASC/TIPC, memory and internal modules/interfaces can be configured with security attributes to prevent non-secure code access

ÿ Enable firmware signature mechanism to achieve secure Boot/upgrade

ÿ Equipped with firmware encryption function to enhance code security

ÿ Firmware encryption keys are distributed using asymmetric algorithms to enhance key security

ÿ Hardware encryption module: RC4256, AES128, DES/3DES, SHA1/MD5, CRC32, 2048 RSA, true random number sending

living organ

ÿ Low Power Mode

ÿ Single 3.3V power supply

ÿ Support work, sleep, standby, shutdown working modes

ÿ Standby power consumption is less than 10uA

3 chip structure

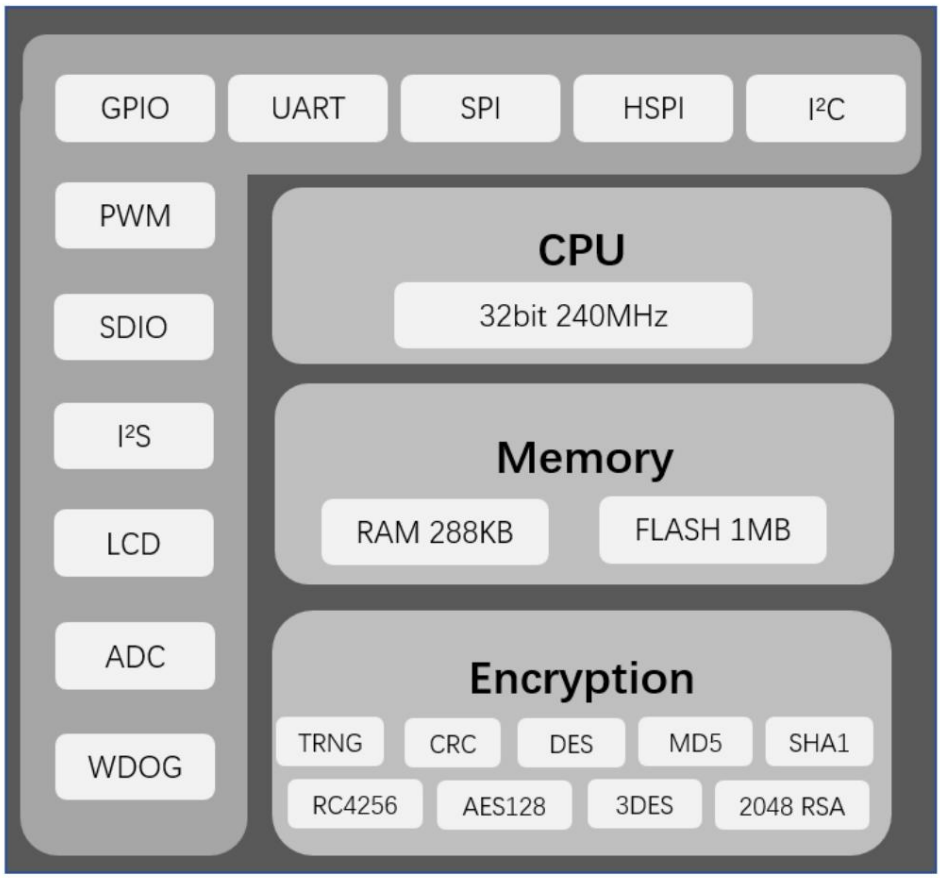

Figure 3-1 W806 chip block diagram

4 Functional description

4.1 SDIO HOST controller

The SDIO HOST device controller provides a digital interface capable of accessing Secure Digital Input Output (SDIO) and MMC cards. were able

Access SDIO devices and SD card devices compatible with SDIO 2.0 protocol. The main interfaces are CK, CMD and 4 data lines.

ÿ Compatible with SD Card Specification 1.0/1.1/2.0(SDHC)

ÿ Compatible with SDIO Memory Card Specification 1.1.0

ÿ Compatible with MMC specification 2.0~4.2

ÿ Configurable interface clock rate, support host rate 0~50MHz

ÿ Support standard MMC interface

ÿ Support up to 1024 bytes Block

ÿ Support soft reset function

ÿ Automatic Command/Response CRC generation/verification

ÿ Automatic data CRC generation/checking

ÿ Configurable timeout detection

ÿ Support SPI, 1-bit SD and 4-bit SD modes

ÿ Support DMA data transfer

4.2 SDIO Device Controller

SDIO2.0 device-side interface to complete the data interaction with the host. Internally integrates 1024Byte asynchronous FIFO to complete the data between the host and the chip interact.

ÿ Compatible with SDIO Card Specification 2.0

ÿ Support host rate 0~50MHz

ÿ Support up to 1024 bytes Block

ÿ Support soft reset function

ÿ Support SPI, 1-bit SD and 4-bit SD modes

4.3 High Speed SPI Device Controller

Compatible with the general SPI physical layer protocol, by agreeing on the data format for interaction with the host, the host can access the device at a high speed, and the maximum supported operating frequency is 50Mbpsÿ

ÿ Compatible with general SPI protocol

ÿ Selectable level interrupt signal

ÿ Support up to 50Mbps rate

ÿ Simple frame format, full hardware analysis and DMA

4.4 DMA Controller

Support up to 8 channels, 16 DMA request sources, support linked list structure and register control.

ÿ Amba2.0 standard bus interface, 8 DMA channels

ÿ Support DMA operation based on memory linked list structure

ÿ Software configures 16 hardware request sources

ÿ Support 1, 4-burst operation mode

ÿ Support byte, half-word, word operations

ÿ The source and destination addresses are unchanged or sequentially incremented, configurable or cyclically operate within a predefined address range

ÿ Synchronous DMA request and DMA response hardware interface timing

4.5 Clock and Reset

Support chip clock and reset system control, clock control includes clock frequency conversion, clock shutdown and adaptive gating; reset control includes system and

And the soft reset control of the sub-module.

4.6 Memory Manager

Support the configuration of sending and receiving buffer size, as well as control information such as the base address of MAC access buffer, the number of buffers, and the upper limit of frame aggregation.

4.7 FLASH controller

ÿ Provide bus access FLASH interface

ÿ Provide system bus and data bus access arbitration

ÿ Realize the CACHE cache system to improve the access speed of the FLASH interface

ÿ Provide compatibility with different QFlash

4.8 RSA encryption module

RSA operation hardware coprocessor, providing Montgomery (FIOS algorithm) modular multiplication operation function. Cooperate with RSA software library to realize RSA algorithm.

Supports 128-bit to 2048-bit modular multiplication.

4.9 General hardware encryption module

The encryption module automatically completes the encryption of the source address space data of the specified length, and automatically writes the encrypted data back to the specified destination address space after completion;

Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG.

- ÿ Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG encryption algorithm
- ÿ DES/3DES supports both ECB and CBC modes
- ÿ AES supports three modes: ECB, CBC and CTR
- ÿ CRC supports CRC8, CRC16_MODBUS, CRC16_CCITT and CRC32 four modes
- ÿ CRC supports input/output reverse
- ÿ SHA1/MD5/CRC supports continuous multi-packet encryption
- ÿ Built-in true random number generator, also supports seed seed to generate pseudo-random numbers

4.10 I2C Controller

APB bus protocol standard interface, only supports the main device controller, I²C working frequency support can be configured, 100K-400K.

4.11 Master/Slave SPI Controller

Supports synchronous SPI master-slave functionality. Its working clock is the internal bus clock of the system. Its characteristics are as follows:

- ÿ 8-word-deep FIFOs for transmit and receive paths
- ÿ master supports 4 formats of Motorola SPI (CPOL, CPHA), TI timing, macrowire timing
- ÿ slave supports 4 formats of Motorola SPI (CPOL, CPHA);

ÿ Support full duplex and half duplex

ÿ The master device supports bit transmission, up to 65535bit transmission

ÿ The slave device supports transmission modes of various byte lengths

ÿ The maximum clock frequency of SPI_Clk input from the device is 1/6 of the system clock

4.12 UART Controller

ÿ The device side conforms to the APB bus interface protocol

ÿ Support interrupt or polling mode

ÿ Support DMA transfer mode, each send and receive has 32-byte FIFO

ÿ Programmable baud rate

ÿ 5-8bit data length, and parity polarity can be configured

ÿ 1 or 2 stop bits configurable

ÿ Support RTS/CTS flow control

ÿ Support Break frame sending and receiving

ÿ Overrun, parity error, frame error, rx break frame interrupt instruction

ÿ Maximum 16-burst byte DMA operation

4.13 GPIO Controller

Configurable GPIO, software-controlled input and output, hardware-controlled input and output, configurable interrupt mode.

The GPIOA and GPIOB registers have different starting addresses, but the functions are the same.

4.14 Timers

Microsecond and millisecond timing (the number of counts is configured according to the clock frequency), and six configurable 32-bit counters are realized. When the counting configured by the corresponding calculator is completed

When successful, a corresponding interrupt is generated.

4.15 Watchdog Controller

Support "watchdog" function. Observe the correctness of software behavior and allow a global reset after a system crash. "Watchdog" generates a periodic

The system software must respond to the interrupt and clear the interrupt flag; if the interrupt flag has not been cleared for a long time due to system crash, then

Generate a hard reset to perform a global reset of the system.

4.16 PWM Controller

ÿ 5-channel PWM signal generation function

ÿ 2-channel input signal capture function (PWM0 and PWM4 two channels)

ÿ Frequency range: 3Hz~160KHz

ÿ Maximum accuracy of duty cycle: 1/256, counter width for inserting dead zone: 8bit

4.17 I²S Controller

ÿ Support AMBA APB bus interface, 32bit single read and write operations

ÿ Support master and slave mode, can work duplex

ÿ Support 8/16/24/32 bit width, the highest sampling frequency is 128KHz

ÿ Support mono and stereo mode

ÿ Compatible with I²S and MSB justified data format, compatible with PCM A/B format

ÿ Support DMA request read and write operations. Only word-by-word operations are supported

4.18 7816/UART Controller

ÿ The device side conforms to the APB bus interface protocol

ÿ Support interrupt or polling mode

ÿ Support DMA transfer mode, each send and receive has 32-byte FIFO

ÿ DMA can only operate by byte, the maximum 16-burst byte DMA operation

Compatible with UART and 7816 interface functions:

Serial function:

ÿ Programmable baud rate

ÿ 5-8bit data length, and parity polarity can be configured

ÿ 1 or 2 stop bits configurable

ÿ Support RTS/CTS flow control

ÿ Support Break frame sending and receiving

ÿ Overrun, parity error, frame error, rx break frame interrupt instruction

7816 interface function:

ÿ Compatible with ISO-7816-3 T=0.T=1 mode

ÿ Compatible with EVM2000 protocol

ÿ Configurable guard time (11 ETU-267 ETU)

ÿ Forward/reverse convention software configurable

ÿ Support sending/receiving parity check and retransmission function

ÿ Support 0.5 and 1.5 stop bit configuration

4.19 PSRAM Interface Controller

W806 has a PSRAM controller with built-in SPI/QSPI interface, supports external PSRAM device access, and provides PSRAM read, write and erase in bus mode.

operate. The highest read and write speed is 80MHz.

ÿ Supports read and write access to external PSRAM

ÿ Configurable as SPI and QSPI

ÿ SPI/QSPI clock frequency can be configured

ÿ Support BURST INC mode access

ÿ Support PSRAM semi-sleep mode

4.20 ADC

The acquisition module based on Sigma-Delta ADC completes the acquisition of up to 4 channels of analog signals, and the sampling rate is controlled by an external input clock.

It can collect the input voltage and also collect the chip temperature, and supports input calibration and temperature compensation calibration.

4.21 Touch key controller

The basic functions of the module are as follows:

ÿ Support up to 15 channels of Touch Sensor scanning

ÿ Record the scanning results of each Touch Sensor

ÿ Report scan results through interrupts

5 Pin definition

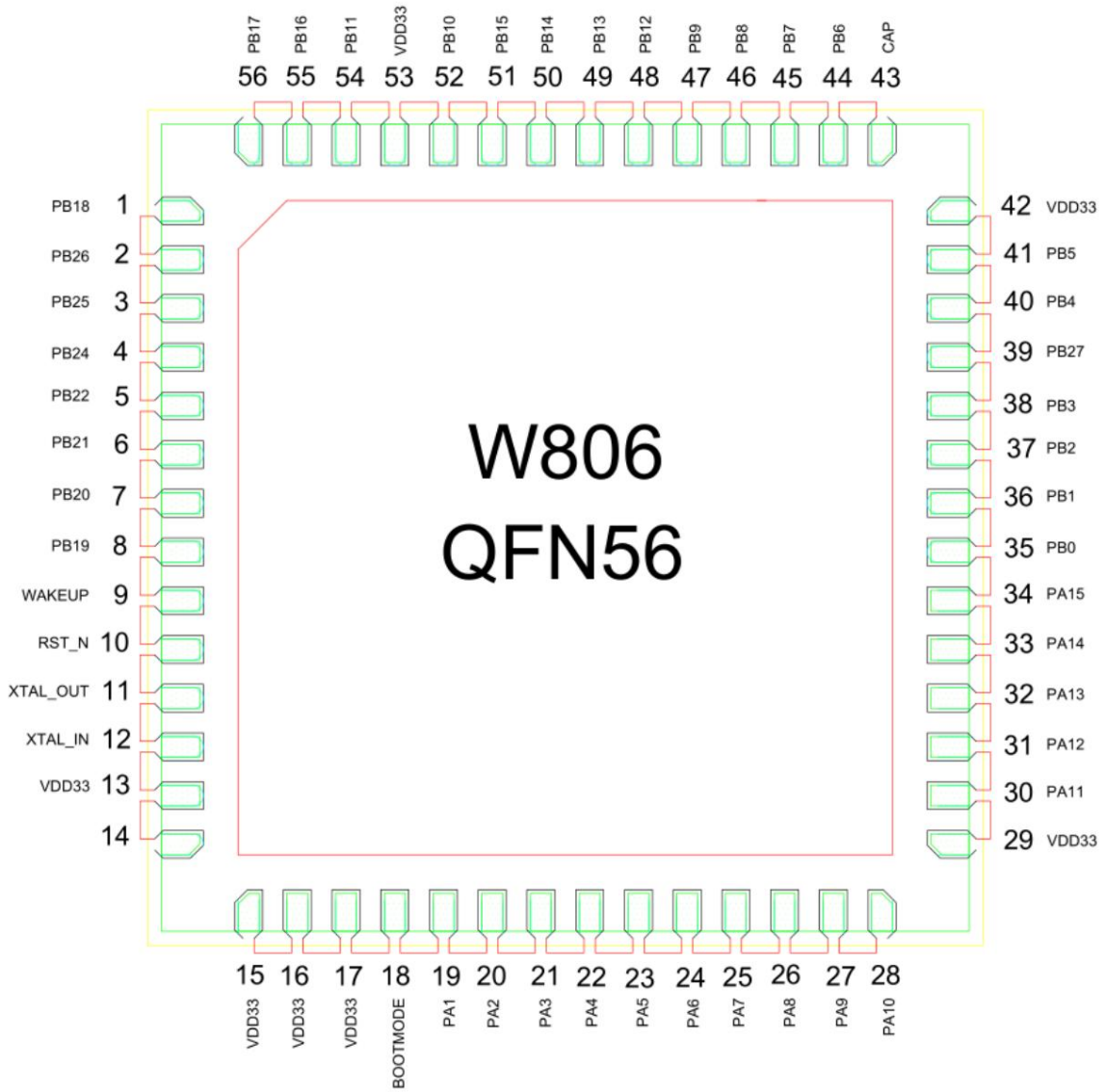

Figure 6-1 Pin layout diagram (QFN32)

Table 6-1 Pin assignment definition (QFN56)

No.	Name	Type	Pin Function After Reset	multiplexing function	Pull-up and pull-down ability
1	PB_18	I/O	GPIO, input, high impedance	UART5_TX/LCD_SEG30	UP/DOWN
2	PB_26	I/O	GPIO, input, high impedance	LSPI_MOSI/PWM4/LCD_SEG1	UP/DOWN
3	PB_25	I/O	GPIO, input, high impedance	LSPI_MISO/PWM3/LCD_COM0	UP/DOWN
4	PB_24	I/O	GPIO, input, high impedance	LSPI_CK/PWM2/LCD_SEG2	UP/DOWN
5	PB_22	I/O	GPIO, input, high impedance	UART0_CTS/PCM_CK/LCD_COM2	UP/DOWN
6	PB_21	I/O	GPIO, input, high impedance	UART0_RTS/PCM_SYNC/LCD_COM1	UP/DOWN
7	PB_20	I/O	UART_RX	UART0_RX/PWM1/UART1_CTS/I2C_SCL	UP/DOWN
8	PB_19	I/O	UART_TX	UART0_TX/PWM0/UART1_RTS/I2C_SDA	UP/DOWN
9	WAKEUP	I	WAKEUP Wake up function		DOWN
10	RESET	I	RESET Reset		UP
11	XTAL_OUT	O	External crystal oscillator output		
12	XTAL_IN	I	External crystal oscillator input		
13	VDD33	P	chip power supply, 3.3V		
14	NC				
15	VDD33	P	chip power supply, 3.3V		
16	VDD33	P	chip power supply, 3.3V		
17	VDD33	P	chip power supply, 3.3V		
18	BOOTMODE	I/O	BOOTMODE	I2S_MCLK/LSPI_CS/PWM2/I2S_DO	UP/DOWN
19	PA_1	I/O	JTAG_CK	JTAG_CK/I2C_SCL/PWM3/I2S_LRCK/ADC_1	UP/DOWN
20	PA_2	I/O	GPIO, input, high impedance	UART1_RTS/UART2_TX/PWM0/UART3_RTS/ADC_4	UP/DOWN
21	PA_3	I/O	GPIO, input, high impedance	UART1_CTS/UART2_RX/PWM1/UART3_CTS/ADC_3	UP/DOWN
22	PA_4	I/O	JTAG_SWO	JTAG_SWO/I2C_SDA/PWM4/I2S_BCK/ADC_2	UP/DOWN
23	PA_5	I/O	GPIO, input, high impedance	UART3_TX/UART2_RTS/PWM_BREAK/UART4_RTS	UP/DOWN
24	PA_6	I/O	GPIO, input, high impedance	UART3_RX/UART2_CTS/NULL/UART4_CTS/LCD_SEG31	UP/DOWN
25	PA_7	I/O	GPIO, input, high impedance	PWM4/LSPI_MOSI/I2S_MCK/I2S_DI/LCD_SEG3/Touch_1	UP/DOWN
26	PA_8	I/O	GPIO, input, high impedance	PWM_BREAK/UART4_TX/UART5_TX/I2S_BCLK/LCD_SEG4	UP/DOWN
27	PA_9	I/O	GPIO, input, high impedance	MMC_CLK/UART4_RX/UART5_RX/I2S_LRCLK/LCD_SEG5/TOUCH_2	UP/DOWN
28	PA_10	I/O	GPIO, input, high impedance	MMC_CMD/UART4_RTS/PWM0/I2S_DO/LCD_SEG6/TOUCH_3	UP/DOWN
29	VDD33	P	chip power supply, 3.3V		
30	PA_11	I/O	GPIO, input, high impedance	MMC_DAT0/UART4_CTS/PWM1/I2S_DI/LCD_SEG7	UP/DOWN
31	PA_12	I/O	GPIO, input, high impedance	MMC_DAT1/UART5_TX/PWM2/LCD_SEG8/TOUCH_14	UP/DOWN
32	PA_13	I/O	GPIO, input, high impedance	MMC_DAT2/UART5_RX/PWM3/LCD_SEG9	UP/DOWN

33	PA_14	I/O GPIO, input, high impedance MMC_DAT3/UART5_CTS/PWM4/LCD_SEG10/TOUCH_15	UP/DOWN
34	PA_15	I/O GPIO, input, high impedance PSRAM_CK/UART5_RTS/PWM_BREAK/LCD_SEG11	UP/DOWN
35	PB_0	I/O GPIO, input, high impedance PWM0/LSPI_MISO/UART3_TX/PSRAM_CK/LCD_SEG12/Touch_4	UP/DOWN
36	PB_1	I/O GPIO, input, high impedance PWM1/LSPI_CK/UART3_RX/PSRAM_CS/LCD_SEG13/Touch_5	UP/DOWN
37	PB_2	I/O GPIO, input, high impedance PWM2/LSPI_CK/UART2_TX/PSRAM_D0/LCD_SEG14/Touch_6	UP/DOWN
38	PB_3	I/O GPIO, input, high impedance PWM3/LSPI_MISO/UART2_RX/PSRAM_D1/LCD_SEG15/Touch_7	UP/DOWN
39	PB_27	I/O GPIO, input, high impedance PSRAM_CS/UART0_TX/LCD_COM3	UP/DOWN
40	PB_4	I/O GPIO, input, high impedance LSPI_CS/UART2_RTS/UART4_TX/PSRAM_D2/LCD_SEG16/Touch_8	UP/DOWN
41	PB_5	I/O GPIO, input, high impedance LSPI_MOSI/UART2_CTS/UART4_RX/PSARM_D3/LCD_SEG17/Touch_9	UP/DOWN
42	VDD33	P chip power supply, 3.3V	
43	CAP	I External capacitor, 1μF	
44	PB_6	I/O GPIO, input, high impedance UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK/LCD_SEG18/Touch_10	UP/DOWN
45	PB_7	I/O GPIO, input, high impedance UART1_RX/MMC_CMD/HSPI_INT/SDIO_CMD/LCD_SEG19/Touch_11	UP/DOWN
46	PB_8	I/O GPIO, input, high impedance I2S_BCK/MMC_D0/PWM_BREAK/SDIO_D0/LCD_SEG20/Touch_12	UP/DOWN
47	PB_9	I/O GPIO, input, high impedance I2S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/LCD_SEG21/Touch_13	UP/DOWN
48	PB_12	I/O GPIO, input, high impedance HSPI_CK/PWM0/UART5_CTS/I2S_BCLK/LCD_SEG24	UP/DOWN
49	PB_13	I/O GPIO, input, high impedance HSPI_INT/PWM1/UART5_RTS/I2S_LRCLK/LCD_SEG25	UP/DOWN
50	PB_14	I/O GPIO, input, high impedance HSPI_CS/PWM2/LSPI_CS/I2S_DO/LCD_SEG26	UP/DOWN
51	PB_15	I/O GPIO, input, high impedance HSPI_DI/PWM3/LSPI_CK/I2S_DI/LCD_SEG27	UP/DOWN
52	PB_10	I/O GPIO, input, high impedance I2S_DI/MMC_D2/HSPI_DI/SDIO_D2/LCD_SEG22	UP/DOWN
53	VDD33	P chip power supply, 3.3V	
54	PB_11	I/O GPIO, input, high impedance I2S_DO/MMC_D3/HSPI_DO/SDIO_D3/LCD_SEG23	UP/DOWN
55	PB_16	I/O GPIO, input, high impedance HSPI_DO/PWM4/LSPI_MISO/UART1_RX/LCD_SEG28	UP/DOWN
56	PB_17	I/O GPIO, input, high impedance UART5_RX/PWM_BREAK/LSPI_MOSI/I2S_MCLK/LCD_SEG29	UP/DOWN

Note: 1. I = Input, O = Output, P = Power

6 Electrical Characteristics

6.1 Limit parameters

Table 7-1 Limit parameters

parameter	name	minimum value	typical value	maximum value	unit
supply voltage	VDD	3.0	3.3	3.6	IN
Input Logic Level Low	WILL	-0.3		0.8	IN
Input logic level high	HIV	2.0		VDD+0.3	IN
Input Pin Capacitance	cpad			2	pF
output logic level low	VOL			0.4	IN
output logic level high	VOH	2.4			IN
Output maximum drive capacity	IMAX			24	mA
storage temperature range	TSTR	-40ÿ		+125ÿ	ÿ
range of working temperature	TOPR	-40ÿ		+85ÿ	ÿ

7 Package Information

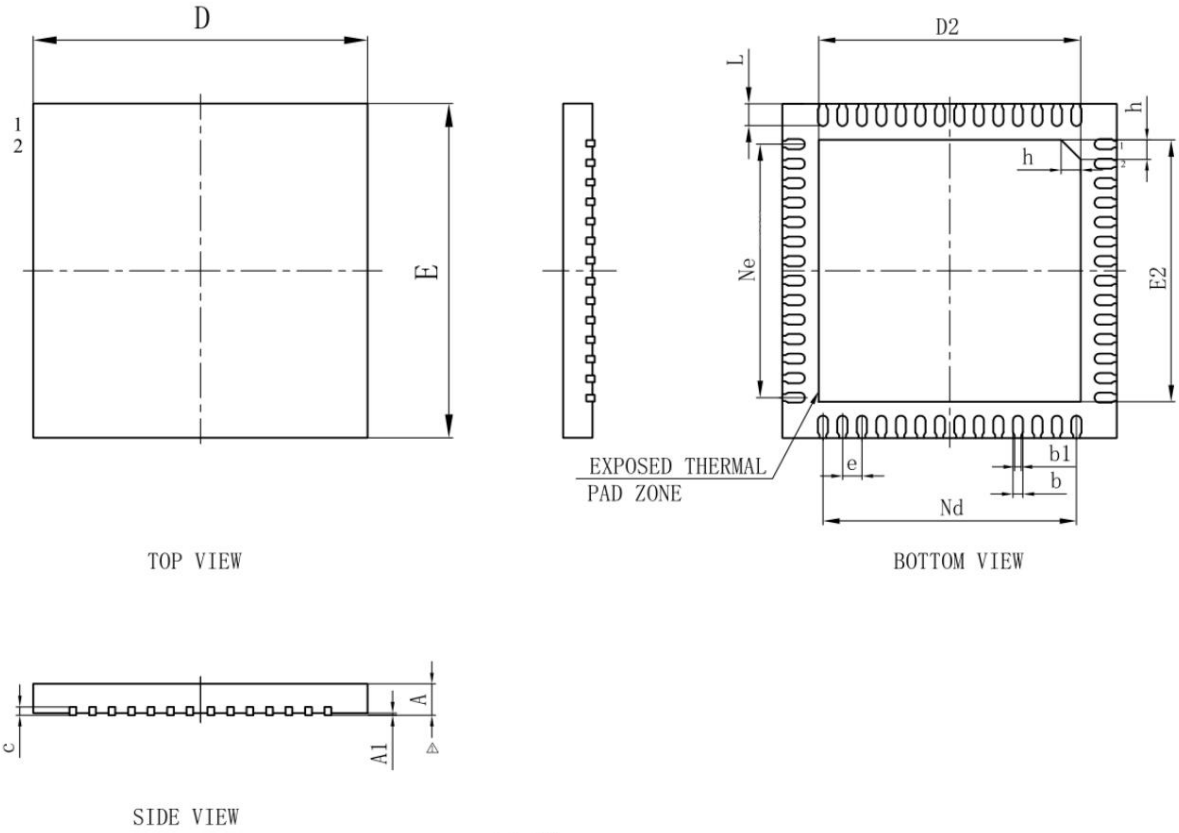

Figure 8-1 W806 package parameters

Table 8-1 W806 Package Parameters

SYMBOL	MILLIMETER		
	MIN	NAME	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		

c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.60	4.70	4.80
and	0.35BSC		
Yes	4.55BSC		
Nd	4.55BSC		
AND	5.90	6.00	6.10
E2	4.60	4.70	4.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F carrier size	193x193		