High performance ARM®-based 32-bit MCU, with up to 128KB Flash, USB FS 2.0, CAN, 7 timers, ADC & 9 comm. interfaces, 1.8-5.5V

Features

ÿ ARM® 32-bit Cortex-M4 CPU, the highest frequency is 72/96 MHz ÿ
Storage ÿ 64/128 KB FLASH memory ÿ FLASH interface with FLASH
Turbo module, greatly improving the performance of programs
running from FLASH (H series only) ÿ FLASH work The speed is 32MHz, and the waiting period can be set according
to this (H series only) ÿ 20/32 KB SRAM ÿ CRC calculation unit ÿ Reset and power management ÿ Digital and I/O
power supply: VDD = 1.8 – 5.5V ÿ Analog power supply: VDDA = 1.8 – 5.5V ÿ Power-on/power-down (POR/PDR)
reset ÿ Programmable voltage detection (PVD) ÿ Low power modes: sleep, stop, standby ÿ Clock management ÿ 4 – 16
MHz crystal oscillator ÿ 32 KHz oscillation ÿ Internal 8 MHz RC oscillator ÿ Internal 40 KHz RC oscillator ÿ PLL for CPU
clock ÿ Up to 80 fast I/Os

ÿ All can be mapped to external interrupt
vector ÿ Most can tolerate external 5V level when powered
by 3V ÿ DMA controller ÿ 7 channels ÿ Peripherals supported:
TIMER/ADC/SPI/I 2C/USART

ÿ 2 12-bit, 1us ADCs (up to 10 channels) ÿ Conversion
range: 0 – 5.5 V ÿ Temperature sensor ÿ 7
timers ÿ 1 16-bit advanced timer, motor control
PWM with dead time and brake function ÿ 3 16-bit
timer, up to 4 input IC/OC/OCN, support quadrature coding input ÿ PWM support
input clock of PLLCLK*2 (H series only) ÿ Independent watchdog and system watchdog
timer ÿ SysTick timing ÿ Communication interface ÿ 2 I 2C interfaces, SMBus/PMBus ÿ 3
USART (with ISO7816 interface, LIN, IrDA, modem control signal) ÿ 2 SPI (48 Mbit/s),
support 4-16 bit data frame, With I 2S interface ÿ CAN interface ÿ USB 2.0 full speed interface

- Debug mode
  - 2-wire serial debug (SWD) or 4-wire JTAG
- 96-bit unique ID
- Packaging
  - LQFP48/64/100
  - UFQFPN48

Note: This specification applies to editions C and subsequent IC.

Table of contents

1 Introduction

This data sheet provides ordering information and device electrical characteristics for

the FCM32x103. For information on the ARM® Cortex-M4 core, please refer to the Cortex-M4 Technical Reference Manual.

2 Description

The FCM32x103 microcontroller contains a 32-bit high-performance ARM Cortex-M4 RISC core that can work at 72/96 MHz, with high-speed embedded Storage (up to 128 Kbytes FLASH and 32 Kbytes SRAM), rich high-performance peripherals and I/O. Standard on all models Communication interfaces (I2C, SPI/I2S, USART), USB full-speed device, 2 12-bit ADCs, 3 general-purpose 16-bit timers, 1 16-bit advanced control PWM timer.

The FCM32x103 microcontrollers can operate in the 1.8~5.5V power supply range and -40 to 125C temperature range. Comprehensive power saving mode applies for low power applications.

The FCM32x103 microcontrollers are available in a variety of different hard packages, from 48 to 100 PIN. Depending on the package, different peripherals are included. The table below provides the complete peripheral range of the FCM32x103.

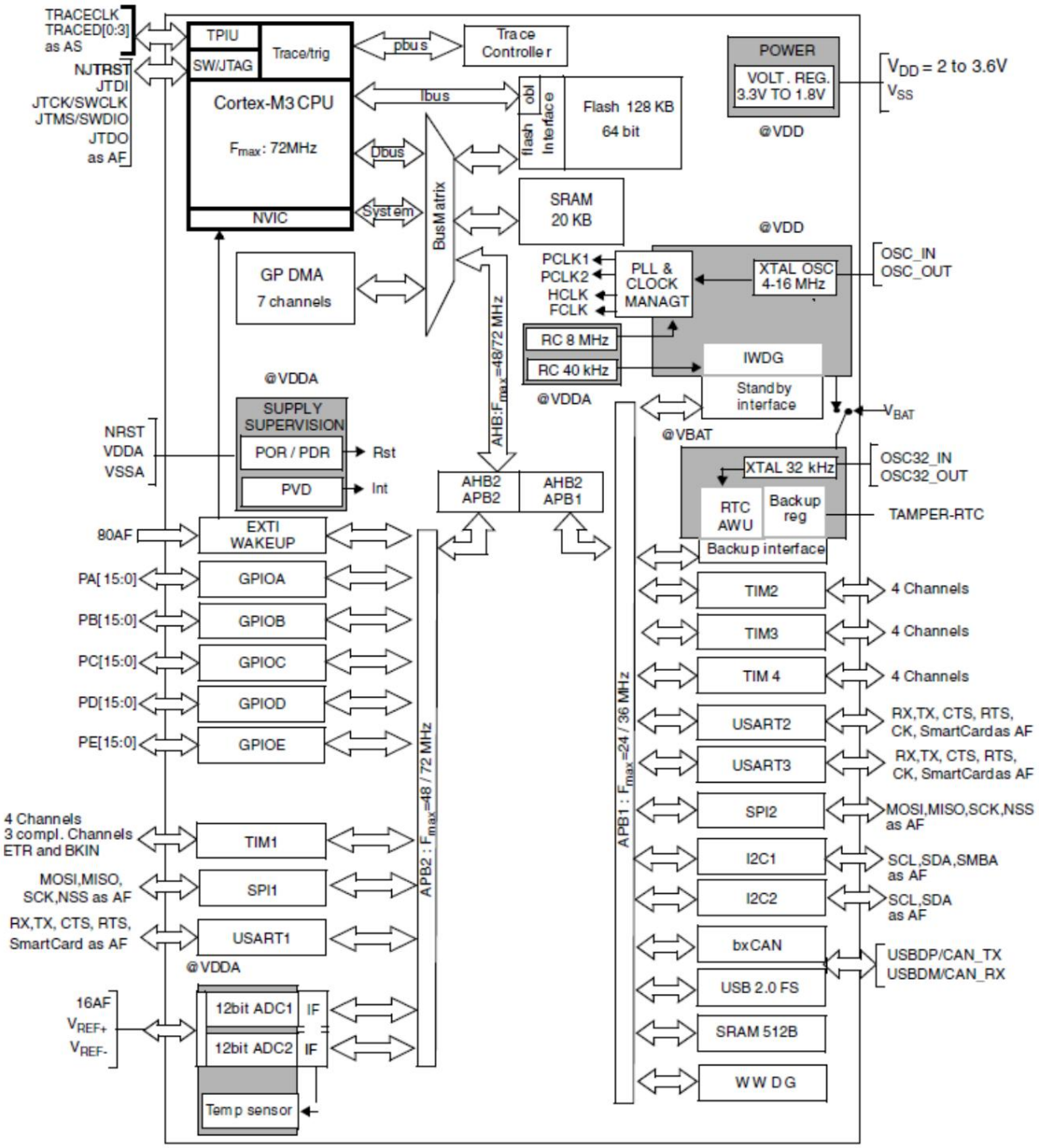
These features make the FCM32x103 microcontrollers ideal for a wide range of applications such as motor drives, application control and user interface, hand handheld devices, A/V receivers and digital TVs, PC peripherals, gaming peripherals, GPS platforms, industrial applications, PLCs, printers, scanners equipment, alarm systems, video connections and HVAC.

FCM32x103 medium-density device features and peripheral counts

Peripheral		FCM32x103Cx		FCM32x103Rx		FCM32x103Vx	
Flash(Kbytes)		64	128	64	128	64	128
SRAM(Kbytes)		20/32					
Timers	Advanced control	1 (16-bit)					
	General purpose	3 (16-bit)					
Comm. interfaces	SPI/I2S(1)	2/2		2/2		2/2	
	I2C	2					
	USART	3					
	CAN	1					
	USB	1					
12-bit ADC (number of channels)		2 10		2 16			
GPIOs		37		51		80	
Max. CPU frequency		72/96MHz					
Flash Turbo		Y(H103)					
Operating voltage		1.8~5.5V					
operating temperature		-40~125					
Packages		LQFP48 UFQFPN48		LQFP64		LQFP100	

1. SPI1/2 interface can work in SPI mode or I 2S audio mode

Block diagram



3 Function overview

3.1 ARM® Cortex-M4 Core

The ARM® Cortex-M4 processor is a 32-bit core for embedded systems developed for applications requiring low pin count, low power consumption, fast response to interrupts, and computing power for MCU applications.

The ARM® Cortex-M4 processor has excellent code efficiency and higher performance compared to 8- and 16-bit devices.

3.2 Storage

The device has the following features:

- 20/32 KB built-in SRAM, running at the same clock speed as CPU (0 wait cycle) • Non-volatile memory (FLASH) is divided into 3 parts:
  - 64/128 KB FLASH storage for program and data
  - System Memory is used to store boot programs and UIDs, etc.
  - Option Bytes

The option word is used for FLASH write protection (in units of 4KB) and read protection of the entire FLASH, with the following options:

- Level 0: no read protection
- Level 1: FLASH read protection, cannot read or write to FLASH through the debug interface or boot from RAM

• Integrate FLASH Turbo module, greatly reduce the waiting period required to execute programs from FLASH, improve performance • FLASH operating speed is 32MHz (full voltage range), the FLASH waiting period (LATENCY) can be set accordingly

3.3 Boot Mode

At startup, the boot pin and the boot select option bits are used to select from the following three boot modes: • Boot from user FLASH • Boot from System Memory • Boot from built-in SRAM

Boot loader is located in System Memory.

3.4 Cyclic Redundancy Detection Computation Unit (CRC)

The CRC calculation unit is used to return CRC results from 32-bit data and polynomials. • Fully programmable polynomials and sizes (7, 8, 16, 32 bits) • 8, 16, 32 bit data sizes • Single 32 bit input/output data register • Input buffering to avoid bus stalls during computation

• 32-bit data requires only 4 AHB clocks • General purpose 8-bit registers can be used for temporary storage • Optional data inversion

3.5 Power Management

3.5.1 Power supply

• VDD = 1.8 – 5.5V: External power supply for I/O and internal voltage regulator. Available through the VDD pin. • VDDA = 1.8 – 5.5V: External analog power supply for ADC, reset circuit, RC oscillator and PLL. VDDA voltage must total is >=VDD voltage and must be powered first.

3.5.2 Power Monitoring

The device integrates power-on reset (POR) and power-down reset (PDR) circuits.

POR/PDR is always active and ensures normal operation above 1.8V. The MCU remains in reset when the supply voltage is below a specified threshold voltage (VPOR/PDR) and does not require an external reset circuit. • POR only monitors VDD voltage. In the startup phase, VDDA is required to be powered first and >=VDD voltage. • The PDR monitors the VDD and VDDA voltages. VDDA voltage monitoring can be turned off by programming the option word to reduce power consumption.

The device also integrates a programmable voltage monitor (PVD) that monitors VDD by comparing the VDD and VPVD threshold voltages. An interrupt is generated when VDD is below or above VDD . The interrupt service routine can generate warning messages and/or put the MCU into safe mode. PVD is enabled by software.

3.5.3 Voltage Regulator

The regulator has two modes of operation and is always enabled after reset. • Master mode (MR) is used for normal operation (Run) • Low power mode (LPR) can be used in Stop mode, because at this time the power demand is reduced In Standby mode, the voltage regulator goes into low power mode, the MCU The core, SRAM, and registers stop working, and the data is kept and will not be lost.

3.5.4 Low Power Mode

FCM32x103 supports three power-saving modes, which can be selected according to different power consumption, fast startup time, and wake-up source: • Sleep mode In Sleep mode, only the CPU is stopped. So the peripherals continue to work and the CPU can be woken up by interrupts/ events.

• Stop Mode Stop mode

achieves very low power consumption while maintaining SRAM and register contents. All clocks in the 1.5V region are stopped and the PLL, HSI RC and HSE crystal oscillator circuits are turned off. The regulator can be placed in MR or LPR mode.

The MCU can be woken up by any EXTI line in Stop mode. EXTI sources can be 16 external lines, PVD output, RTC alarm, I2C1, USART1 or CEC.

I2C1 , USART1 and CEC can be configured to enable the HSI RC oscillator to process incoming data. If the regulator is configured in LPR mode at this point, it will switch to MR mode before clocking the peripherals.

• Standby mode

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is configured in LPR mode. The PLL, HSI RC and HSE crystal oscillator circuits are also turned off. SRAM and register contents are not lost, and the I/O remains in the analog input state.

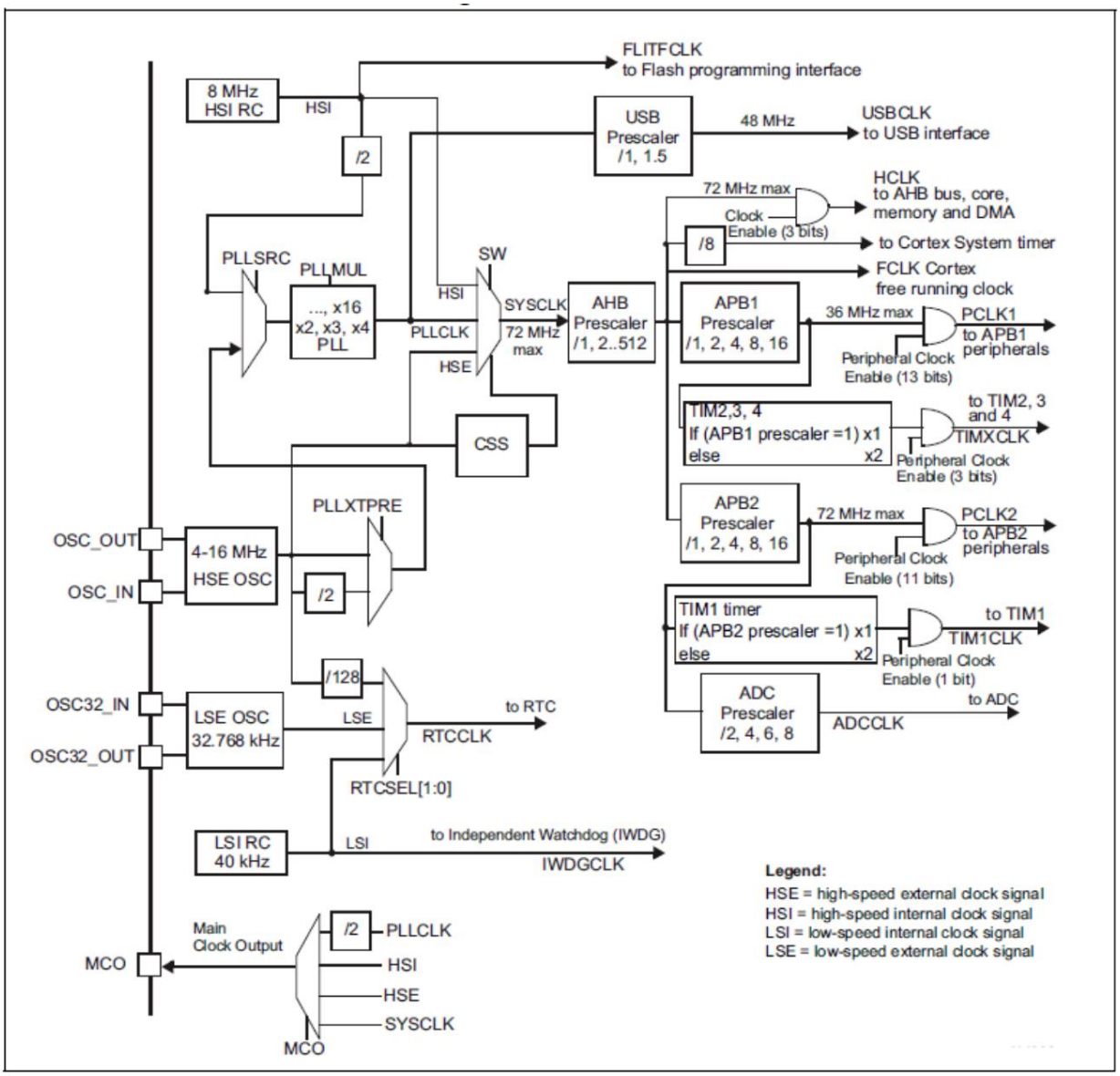
The MCU is taken out of Standby mode by external reset (NRST pin), IWDG reset, rising edge on WKUP pin or RTC event.

Note: RTC, IWDG, and their corresponding clock sources do not stop after entering Stop/Standby mode.

3.6 Clock

During MCU startup, the internal RC 8MHz oscillator is selected as the CPU clock. An external 4-16MHz crystal oscillator can also be selected, with clock failure monitoring. If this oscillator detects a failure, the system automatically switches back to the internal RC oscillator. Interrupts can be generated when the clock fails. Also, interrupts can be generated when this clock is used directly or indirectly for the PLL input. Various prescalers can be used to configure the AHB/APB clock. The maximum clock frequency of AHB and APB is 96MHz.

clock tree



FCM32H103 has the following performance

improvements: • ARM Cortex-M4 can run at 96MHz • FLASH

interface with FLASH Turbo acceleration module, greatly improving the performance of programs running from FLASH • PLLCLK/

SYSCLK/AHBCLK/PCLK can run at the highest 96MHz • USART highest communication speed increased

- SPI maximum communication speed has been improved

• TIM1 PWM can select PLLCLK*2 as the clock (PCLK needs to be PLLCLK at this time), up to 192MHz

3.7 GPIO

Each GPIO can be configured by software as an output (push-pull or open-circuit), an input (with/without pull-up, pull-down), or peripheral additional functions.

Most GPIOs are multiplexed with analog and digital additional functions.

The I/O configuration can be locked by specifying a sequence of operations.

3.8 DMA

7-channel general-purpose DMA manages store-to-store, peripheral-to-store, and store-to-peripheral data transfers.

DMA supports ring buffer management, requiring no user code intervention when the controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and supports software triggering. DMA is configured by software, and the transfer size for source and destination is unlimited.

DMA can be used for major peripherals: SPI , I2S , I2C, USART, TIMx timers and ADC.

DMA key features: •

Supports up to 7 independently configurable channels (requests) • Each

channel is connected to a dedicated hardware DMA request, which can also be triggered by

software • 4 levels of programmable priorities • Source/destination configurable independent

Transfer size (byte, half word, word), source/destination address is configured separately Support circular buffer management

(circular buffer management) 3 event flags (half transfer complete, transfer complete, transfer error), the event flag phase or

- for Generates a single interrupt • Memory-to-memory transfers • Peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral

transfers • FLASH, SRAM, peripheral as source or destination • Programmable transfer size up to 65535

3.9 Interrupts and Events

3.9.1 Nested Vectored Interrupt Controller (NVIC)

The FCM3x103x family integrates a nested vectored interrupt controller that supports up to 43 maskable interrupt channels (excluding the Cortex-M3's 16 interrupt lines) and 16 priority levels. • Tightly coupled NVIC provides low-latency interrupt processing • Interrupt entry vector table address is directly transferred to the CPU core • Allows earlier processing of interrupts • Handles late high-priority interrupts • Supports tail chaining • Automatically saves processor state

3.9.2 Extended Interrupt/Event Controller (EXTI)

The extended interrupt/event controller consists of 19 edge detection lines for generating interrupt/event requests and waking up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge or edge), and can also be individually masked. A scratchpad register contains the interrupt request status. EXTI can detect external inputs shorter than the internal APB2 clock period. Up to 80 GPIOs can be connected to 16 external interrupt lines.

3.10 ADC

2 12-bit ADC analog-to-digital converters with up to 16 external and 2 internal (temperature sensor, voltage reference) channels, can Convert in single shot or scan mode. In scan mode, selected groups of analog inputs can be converted automatically.

Additional logic functions are built into the ADC interface:

• Simultaneous sample and hold

• Interleaved sample and hold

• Single use

The ADC supports DMA.

An analog watchdog can monitor one, some or all of the selected channels with high precision. When the switching voltage exceeds the threshold setting, it will An interrupt is generated.

3.10.1 Temperature Sensor (TS)

The temperature sensor generates a voltage VSENSE that varies linearly with temperature .

The temperature sensor is internally connected to the ADC_IN16 input channel, which is used to convert the sensor output voltage to a digital value.

3.10.2 Internal Voltage Reference (VREFINT)

The internal reference voltage (VREFINT) provides a regulated (reference) voltage output for the ADC. VREFINT is internally connected to the IC ADC_IN17 Input channel.

3.11 Timers and Watchdogs

The FCM32x103 family contains up to 3 general purpose timers and 1 advanced timer.

Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	CCP channels	Complementary outputs
Advanced control	TIM1	16-bit	up, down, Up/down	1~65536 Yes		4	Yes
General purpose	TIM2	16-bit	up, down, Up/down	1~65536 Yes		4	No
	TIM3	16-bit	up, down, Up/down	1~65536 Yes		4	No
	TIM4	16-bit	up, down, Up/down	1~65536 Yes		4	No

3.11.1 Advanced Timer **TIM1**

The advanced timer TIM1 can be used for 6-channel 3-phase PWM. Its complementary output has programmable dead time. It can also be used as a complete general purpose timer. Four independent channels can be used as: • Input Capture IC • Output Compare OC • PWM (Edge or Center-Aligned mode) • Single Pulse Output If configured as a standard 16-bit timer, it functions the same as TIMx. If configured as 16-bit PWM, it has a fully modulated duty cycle (0%-100%). In the debug mode of the MCU, the timer can also work.

Most of the functions of the TIM1 are the same as those of other standard timers. Advanced timers can be cascaded and synchronized with other timers.

3.11.2 General timer **TIM2/3/4**

The FCM32x103 has 3 general purpose timers. Each general purpose timer can be used to generate PWM, or just for simple timing purposes.

The **TIM2/3/4**

FCM32x103 contains three synchronous 4-channel general purpose timers. TIMx consists of a 16-bit prescaler and a 16-bit auto-reload up/down counter. They contain 4 independent channels, each of which can be used for input capture/output compare, PWM or single-click mode output. A total of 12 input capture/output compare channels are available.

TIM2/3/4 can be cascaded or connected with TIM1 for synchronization.

TIM2/3/4 can support quadrature encoded signals, or digital outputs of 1~3 Hall sensors. The timer can run in debug mode.

3.11.3 Independent Watchdog **IWDG**

The IWDG is based on an 8-bit prescaler and a 12-bit down counter and supports user-defined refresh windows. Its clock is provided by an internal 40KHz independent RC timer, which works independently of the main clock. Can work in Stop/Standby mode. It can be used to reset the system's watchdog in the event of a problem, or as a free-running timer in an application. It is configurable via hardware or software via Configuration Words.

IWDG can work in Debug mode.

3.11.4 System Window Watchdog **WWDG**

WWDG is a 7-bit down counter and is free running. It can be used to reset the system's watchdog in the event of a problem. The WWDG clock is derived from the APB clock PCLK. It has early warning interruption capability.

WWDG can work in Debug mode.

3.11.5 SysTick Timer

This stepper is dedicated to real-time operating systems, but can also be used as a standard down counter. • 24-bit down counter • Auto-reload • When counting to 0, a maskable system interrupt can be generated

3.12 Real Time Clock (RTC) and Backup Registers

The backup registers are 10 16-bit registers for storing 20 bytes of user data. They are not reset by the system or upon waking up from Standby mode.

RTC is a continuously running counter, which can be used with software to realize the calendar function.
The RTC clock source can be:
• 32768 Hz external crystal • Ceramic oscillator or other oscillator • Internal low power RC oscillator (40KHz) • High speed external clock/ 128

3.13I2C _

I2C can work in multi-master or slave mode. Standard mode (100 kbit/s), fast mode (400 kbit/s) are supported.
I2C supports dual slave addresses (7-bit only) and 7/10-bit address addressing in master mode, with built-in hardware CRC generation/check function.
The I2C interface can be operated via DMA.

3.14 USART

UART is a universal asynchronous transceiver interface, which provides industry-standard duplex data exchange capability, using a programmable baud rate generator to support a very wide range of baud rates. It supports full-duplex, half-duplex communication, or multi-host communication. Also supports LIN (Local Interconnect Network), smartcard protocol and IrDA (Infrared Data Association) SIR ENDEC specification and modem operation (CTS/RTS). DMA can be used to achieve high-speed data exchange.

3.15SPI/I2S

The SPI interface is used to communicate with external devices using the SPI protocol. SPI supports half-duplex, full-duplex, and simple synchronous serial communication. When configured as a master (MASTER), it provides a communication clock (SCK) to an external slave (SLAVE). The interface can also be configured in multi-host mode.

A standard I2S interface (multiplexed with SPI1 pin) supports 4 different audio formats and can be used in half-duplex mode in master/slave mode to communicate. Can be configured in 16/24 or 32 bit data format, 16 or 32 bit data precision. 8-bit programmable linear prescaler

The frequency converter sets the audio sampling frequency at 8-192 kHz. In master mode, a 256-bit sampling clock can be output to external devices.

3.16CAN

CAN supports CAN 2.0A/B protocol. Specification 2.0A covers standard message format (11-bit identifier), 2.0B covers standard and extensions Message format (11-bit/29-bit identifier).

CAN is compatible with the PeliCAN mode of the Philips SJA1000.

CAN interrupt

Position	Priority	Type of priority	Acronym	Description	Address
30	37	Settable	CEC_CAN	CAN interrupts	0x0000 00B8

CAN address

The CAN base is assigned at 0x4000_6400. CAN does not share RAM with USB.

3.17USB

The FCM32x103 has built-in full-speed USB peripherals that support the USB2.0 protocol. Internal USB PHY supports USB FS signaling. USB includes Software-configured endpoints that support sleep/wakeup. USB comes with 1 KB cache. USB requires a high precision 48MHz clock to work,

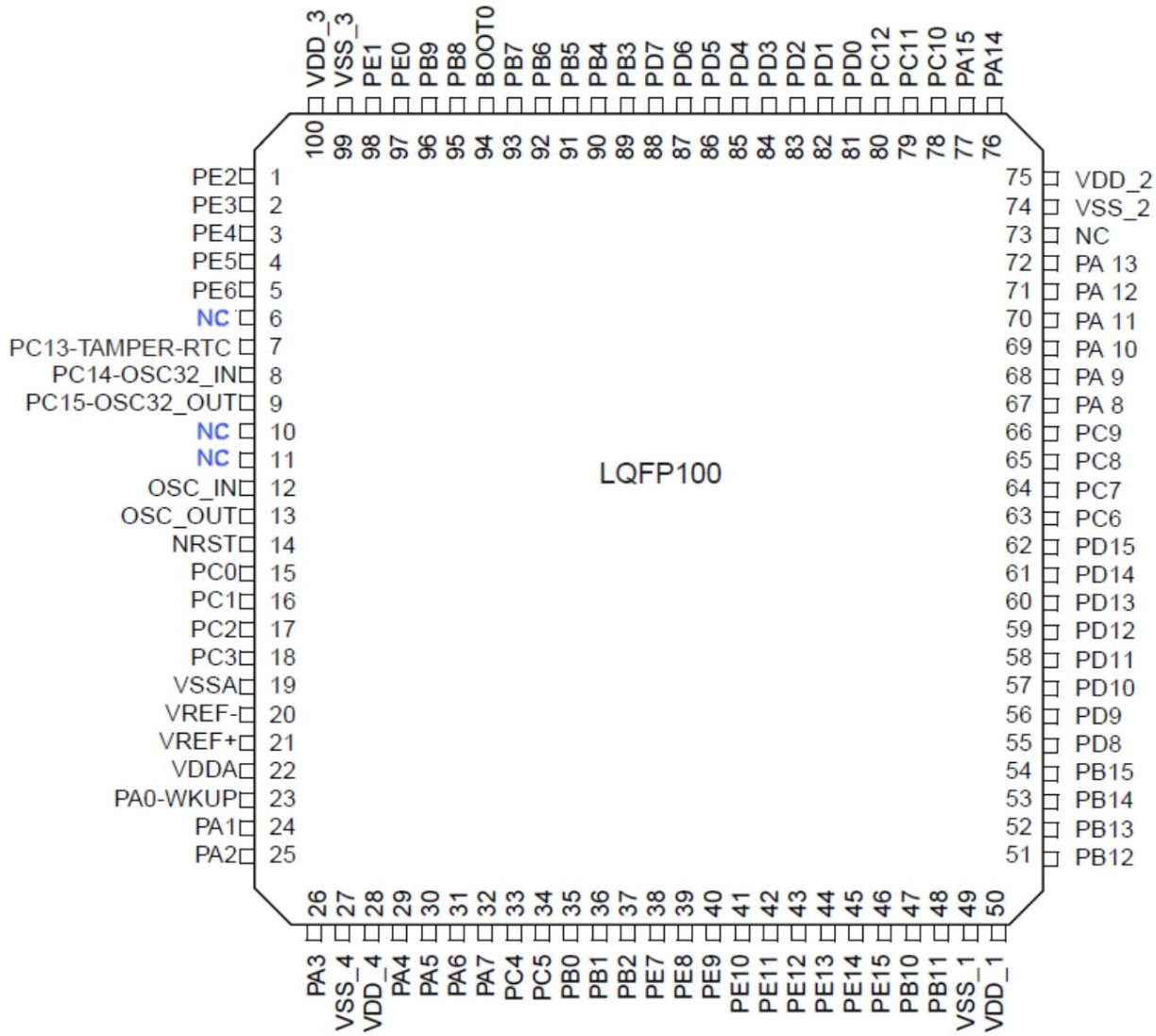
It can be realized by external crystal oscillator + PLL.

3.18SWJ-DP

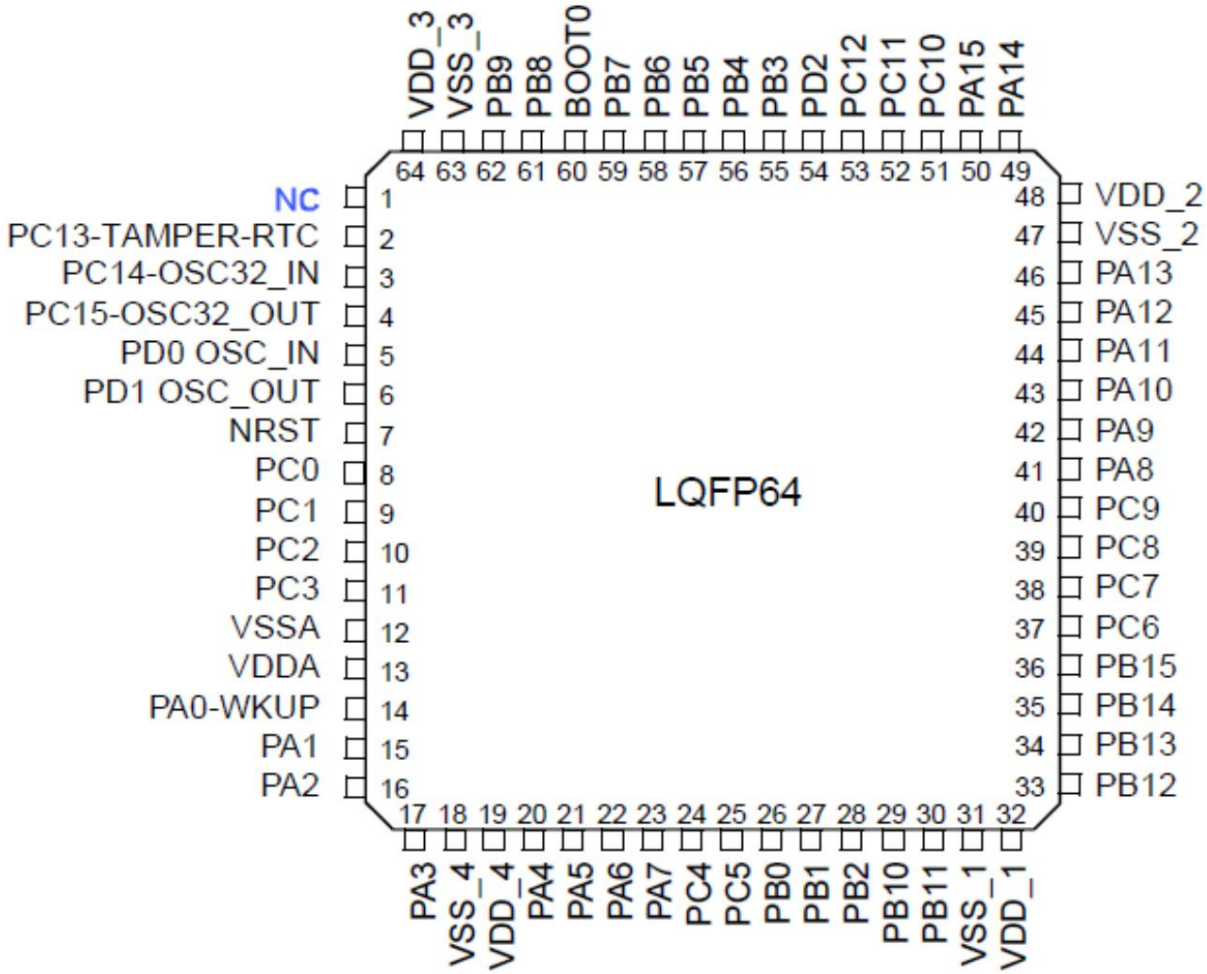
The ARM SWJ-DP interface is used to debug/program the MCU, and supports SWD/JTAG.

4 pin information

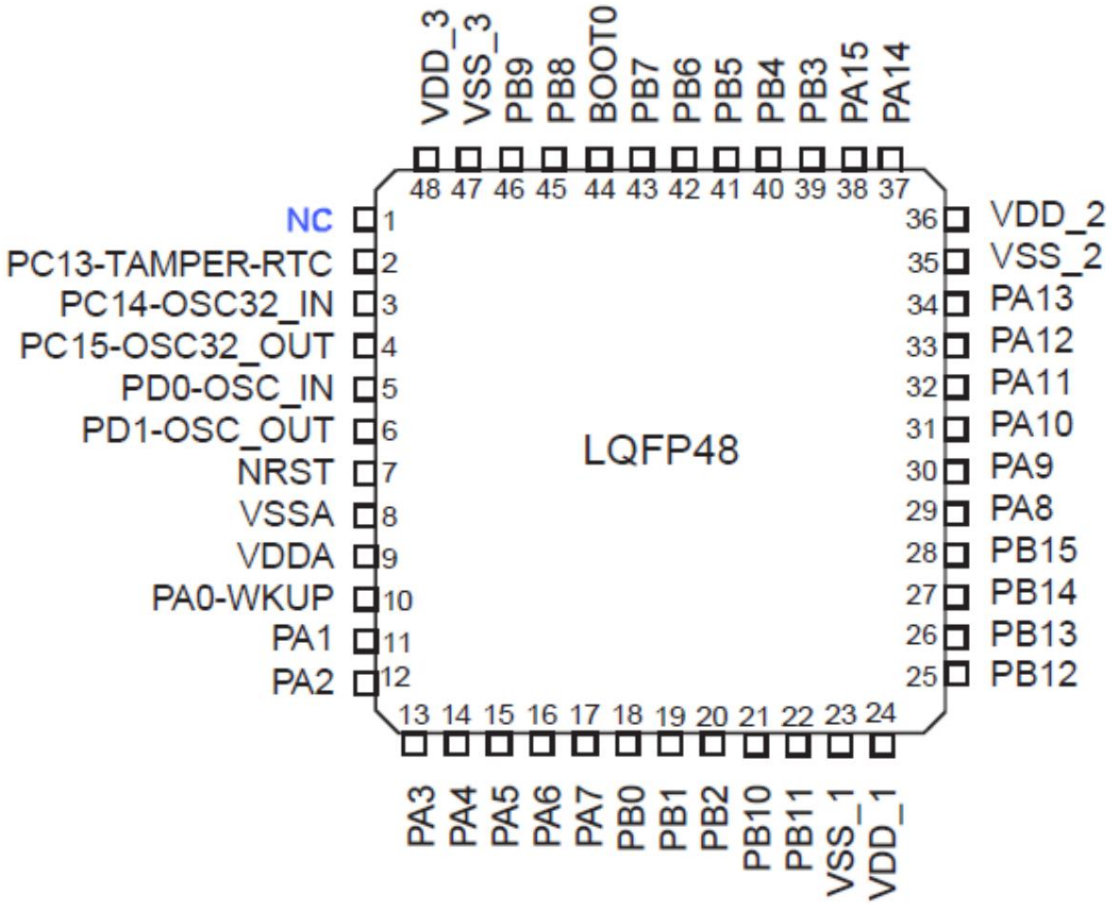
FCM32x103 LQFP100 pinout



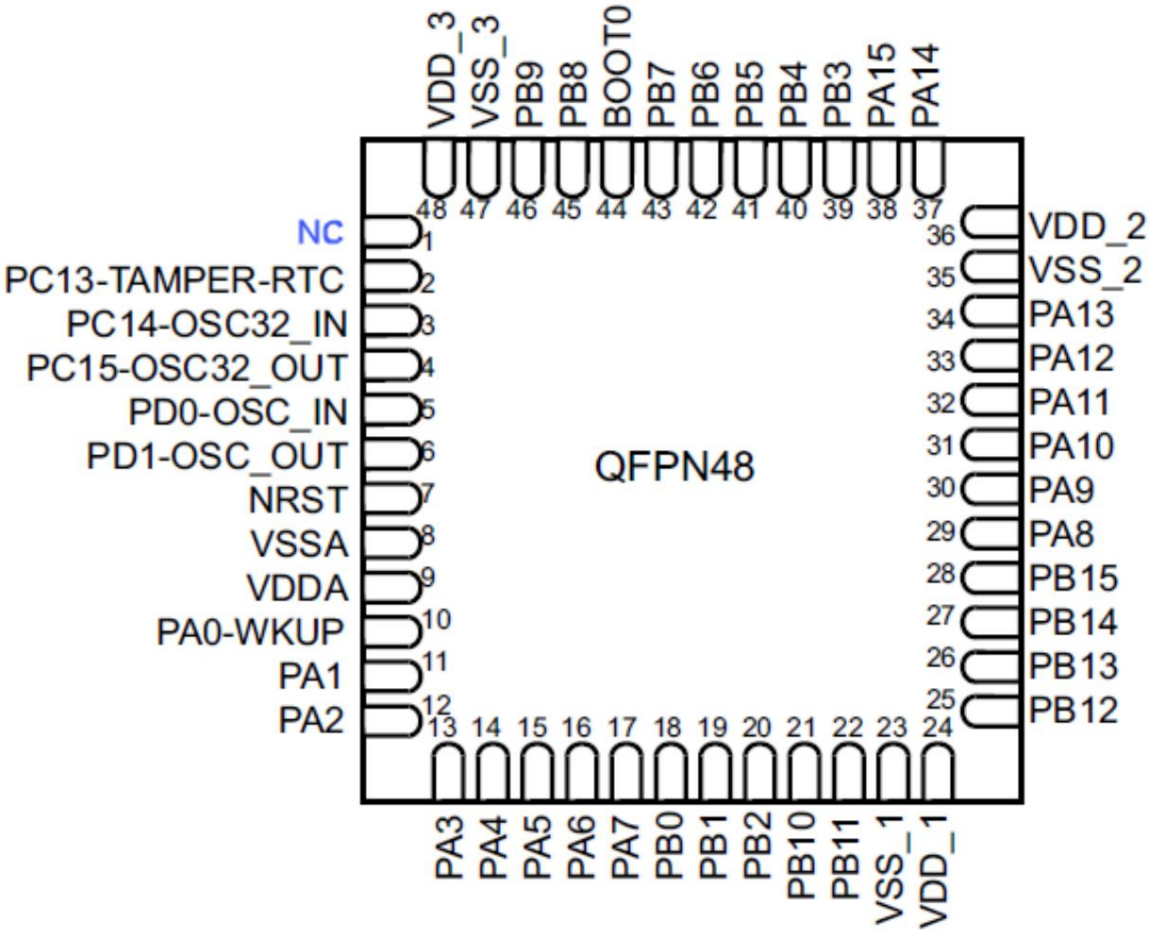
FCM32x103 LQFP64 pinout



FCM32x103 LQFP48 pinout



FCM32x103 UFQFPN48 pinout



FCM32x103 pin definitions

Pins			Pin name	Type(1)	I/O Level(2)	Main function(3) (afterreset)	Alternate functions(4)	
LQFP64	LQFP48	LQFP100					Default	Remap
-	-	1	PE2	I/O	FT	PE2	TRACECK	-
-	-	2	PE3	I/O	FT	PE3	TRACED0	-
-	-	3	PE4	I/O	FT	PE4	TRACED1	-
-	-	4	PE5	I/O	FT	PE5	TRACED2	-
-	-	5	PE6	I/O	FT	PE6	TRACED3	-
1	1	6	NC	-	-	-	-	-
2	2	7	PC13-TAMPER RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
3	3	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
4	4	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
-	-	10	NC	-	-	-	-	-
-	-	11	NC	-	-	-	-	
5	5	12	OSC_IN	I	-	OSC_IN	-	PD0(7)
6	6	13	OSC_OUT	O	-	OSC_OUT		PD1(7)
7	7	14	NRST	I/O	-	NRST	-	-
-	8	15	PC0	I/O	-	PC0	ADC12_IN10	-
-	9	16	PC1	I/O	-	PC1	ADC12_IN11	-
-	10	17	PC2	I/O	-	PC2	ADC12_IN12	-
-	11	18	PC3	I/O	-	PC3	ADC12_IN13	-
8	12	19	VSSA	S	-	VSSA	-	-
-	-	20	VREF-	S	-	VREF-	-	-
-	-	twenty one	VREF+	S	-	VREF+	-	-
9	13	twenty two	VDDA	S	-	VDDA	-	-
10	14	23	PA0-WKUP	I/O	-	PA0	WKUP/ USART2_CTS(9)/ ADC12_IN0/ TIM2_CH1_	-

							ETR(9)	
11	15	twenty four	PA1	I/O	-	PA1	USART2_RTS(9)/ ADC12_IN1/ TIM2_CH2(9)	-
12 16		25	PA2	I/O	-	PA2	USART2_TX(9)/ ADC12_IN2/ TIM2_CH3(9)	-
13 17		26	PA3	I/O	-	PA3	USART2_RX(9)/ ADC12_IN3/ TIM2_CH4(9)	-
-	18	27	VSS_4	S	-	VSS_4	-	-
-	19	28	VDD_4	S	-	VDD_4	-	-
14 20		29	PA4	I/O	-	PA4	SPI1_NSS(9)/ USART2_CK(9)/ ADC12_IN4	-
15 21		30	PA5	I/O	-	PA5	SPI1_SCK(9)/ ADC12_IN5	-
16 22		31	PA6	I/O	-	PA6	SPI1_MISO(9)/ ADC12_IN6/ TIM3_CH1(9)	TIM1_BKIN
17 23		32	PA7	I/O	-	PA7	SPI1_MOSI(9)/ ADC12_IN7/ TIM3_CH2(9)	TIM1_CH1N
-	twenty four	33	PC4	I/O	-	PC4	ADC12_IN14	-
-	25	34	PC5	I/O	-	PC5	ADC12_IN15	-
18 26		35	PB0	I/O	-	PB0	ADC12_IN8/ TIM3_CH3(9)	TIM1_CH2N
19 27		36	PB1	I/O	-	PB1	ADC12_IN9/ TIM3_CH4(9)	TIM1_CH3N
20 28		37	PB2	I/O	FT	PB2/BOOT1	-	-
-	-	38	PE7	I/O	FT	PE7	-	TIM1_ETR
-	-	39	PE8	I/O	FT	PE8	-	TIM1_CH1N
-	-	40	PE9	I/O	FT	PE9	-	TIM1_CH1
-	-	41	PE10	I/O	FT	PE10	-	TIM1_CH2N
-	-	42	PE11	I/O	FT	PE11	-	TIM1_CH2
-	-	43	PE12	I/O	FT	PE12	-	TIM1_CH3N
-	-	44	PE13	I/O	FT	PE13	-	TIM1_CH3
-	-	45	PE14	I/O	FT	PE14	-	TIM1_CH4
-	-	46	PE15	I/O	FT	PE15	-	TIM1_BKIN
twenty one	29 47		PB10	I/O	FT	PB10	I2C2_SCL/	TIM2_CH3

							USART3_TX(9)	
22 30	48		PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(9)	TIM2_CH4
23 31		49	VSS_1	S	-	VSS_1	-	-
24 32		50	VDD_1	S	-	VDD_1	-	-
25 33		51	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK(9)/ TIM1_BKIN(9)	-
26 34		52	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(9)/ TIM1_CH1N (9)	-
27 35		53	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(9) TIM1_CH2N (9)	-
28 36		54	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(9)	-
-	-	55	PD8	I/O	FT	PD8	-	USART3_TX
-	-	56	PD9	I/O	FT	PD9	-	USART3_RX
-	-	57	PD10	I/O	FT	PD10	-	USART3_CK
-	-	58	PD11	I/O	FT	PD11	-	USART3_CTS
-	-	59	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS
-	-	60	PD13	I/O	FT	PD13	-	TIM4_CH2
-	-	61	PD14	I/O	FT	PD14	-	TIM4_CH3
-	-	62	PD15	I/O	FT	PD15	-	TIM4_CH4
-	37	63	PC6	I/O	FT	PC6	-	TIM3_CH1
	38	64	PC7	I/O	FT	PC7	-	TIM3_CH2
	39	65	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	66	PC9	I/O	FT	PC9	-	TIM3_CH4
29 41		67	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(9)/ MCO	-
30 42		68	PA9	I/O	FT	PA9	USART1_TX(9)/ TIM1_CH2(9)	-
31	43	69	PA10	I/O	FT	PA10	USART1_RX(9)/ TIM1_CH3(9)	-
32 44		70	PA11	I/O	FT	PA11	USART1_CTS/ CANRX(9)/ USBDM/	-

							TIM1_CH4(9)	
33 45		71	PA12	I/O	FT	PA12	USART1_RTS/ CANTX(9) /USBDP TIM1_ETR(9)	-
34 46		72	PA13	I/O	FT JTMS/SWDIO		-	PA13
-	-	73	Not connected					-
35 47		74	VSS_2	S	-	VSS_2	-	-
36 48		75	VDD_2	S	-	VDD_2	-	-
37 49		76	PA14	I/O FT		JTCK/SWCLK	-	PA14
38 50		77	PA15	I/O FT		JTDI	-	TIM2_CH1_ ETR/PA15 /SPI1_NSS
-	51	78	PC10	I/O FT		PC10	-	USART3_TX
-	52	79	PC11	I/O FT		PC11	-	USART3_RX
-	53	80	PC12	I/O FT		PC12	-	USART3_CK
-	-	81	PD0	I/O FT		PD0	-	CANRX
-	-	82	PD1	I/O FT		PD1	-	CANTX
	54	83	PD2	I/O FT		PD2	TIM3_ETR	-
-	-	84	PD3	I/O FT		PD3	-	USART2_CTS
-	-	85	PD4	I/O FT		PD4	-	USART2_RTS
-	-	86	PD5	I/O FT		PD5	-	USART2_TX
-	-	87	PD6	I/O FT		PD6	-	USART2_RX
-	-	88	PD7	I/O FT		PD7	-	USART2_CK
39 55		89	PB3	I/O FT		JTDO	-	TIM2_CH2 / PB3 TRACESWO SPI1_SCK
40 56		90	PB4	I/O FT		JNTRST	-	TIM3_CH1/ PB4/ SPI1_MISO
41	57	91	PB5	I/O		PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
42 58		92	PB6	I/O FT		PB6	I2C1_SCL(9)/ TIM4_CH1(9)	USART1_TX
43 59		93	PB7	I/O FT		PB7	I2C1_SDA(9)/ TIM4_CH2(9)	USART1_RX
44 60		94	BOOT0	I		BOOT0	-	-
45 61		95	PB8	I/O	FT	PB8	TIM4_CH3(9)	I2C1_SCL /

								CANRX
46	62	96		PB9	I/O	FT	PB9	TIM4_CH4(9)	I2C1_SDA/ CANTX
-	-	97		PE0	I/O	FT	PE0	TIM4_ETR	-
-	-	98		PE1	I/O	FT	PE1	-	-
47	63	99		VSS_3	S	-	VSS_3	-	-
48	64	100		VDD_3	S	-	VDD_3	-	-

1. I = input, O = output, S = supply.

2. FT = 5 V tolerant.

5 Memory Map

The difference between FCM32x1038/xB is that the end addresses of the program memory space are 0x0800FFFF and 0x0801FFFF respectively.

FCM32x1038/xB Peripheral Register Boundary Addresses

Bus	Boundary address	Size	Peripheral
AHB	0xA000 0000 – 0xA000 0FFF 4KB		-
	0x9000 0000 – 0x9FFF FFFF 2GB		-
	0x8000 0000 – 0x8FFF FFFF 2GB		-
	0x7000 0000 – 0x7FFF FFFF 2GB		-
	0x6C00 0000 – 0x6FFF FFFF 64MB		-
	0x6800 0000 – 0x6BFF FFFF 64MB		-
	0x6400 0000 – 0x67FF FFFF 64MB		-
	0x6000 0000 – 0x63FF FFFF 64MB		-
	0x4800 0000 – 0x5FFF FFFF ~384 MB		-
	0x4002 4400 – 0x47FF FFFF ~128MB		
AHB	0x4002 4000 – 0x4002 43FF 1KB		-
	0x4002 3400 – 0x4002 3FFF 3KB		-
	0x4002 3000 – 0x4002 33FF 1KB		CRC
	0x4002 2400 – 0x4002 2FFF 3KB		-
	0x4002 2000 – 0x4002 23FF 1KB		Flash memory interface
	0x4002 1400 – 0x4002 1FFF 3KB		-
	0x4002 1000 – 0x4002 13FF 1KB		RCC
	0x4002 0400 – 0x4002 0FFF 3KB		-
	0x4002 0000 – 0x4002 03FF 1KB		DMA
	0x4001 8000 – 0x4001 FFFF 32KB		-
APB	0x4001 5C00 – 0x4001 7FFF 9KB		-
	0x4001 5800 – 0x4001 5BFF 1KB		-
	0x4001 4C00 – 0x4001 57FF 3KB		-
	0x4001 4800 – 0x4001 4BFF 1KB		-
	0x4001 4400 – 0x4001 47FF 1KB		-
	0x4001 4000 – 0x4001 43FF 1KB		-
	0x4001 3C00 – 0x4001 3FFF 1KB		-
	0x4001 3800 – 0x4001 3BFF 1KB		USART1
	0x4001 3400 – 0x4001 37FF 1KB		-
	0x4001 3000 – 0x4001 33FF 1KB		SPI1/I2S1
	0x4001 2C00 – 0x4001 2FFF 1KB		TIM1
	0x4001 2800 – 0x4001 2BFF 1KB		ADC2
	0x4001 2400 – 0x4001 27FF 1KB		ADC1
	0x4001 2000 – 0x4001 23FF 1KB		-
	0x4001 1C00 – 0x4001 1FFF 1KB		-

	0x4001 1800 – 0x4001 1BFF 1KB		GPIOE
	0x4001 1400 – 0x4001 17FF 1KB		GPIOD
	0x4001 1000 – 0x4001 13FF 1KB		GPIOC
	0x4001 0C00 – 0x4001 0FFF 1KB		GPIOB
	0x4001 0800 – 0x4001 0BFF 1KB		GPIOA
	0x4001 0400 – 0x4001 07FF 1KB		EXTI
	0x4001 0000 – 0x4001 03FF 1KB		AFIO
	0x4000 8000 – 0x4000 FFFF 32KB		-
	0x4000 7C00 – 0x4000 7FFF 1KB		-
	0x4000 7800 – 0x4000 7BFF 1KB		-
	0x4000 7400 – 0x4000 77FF 1KB		-
	0x4000 7000 – 0x4000 73FF 1KB		PWR
	0x4000 6C00 – 0x4000 6FFF 1KB		BKP
	0x4000 6800 – 0x4000 6BFF 1KB		-
	0x4000 6400 – 0x4000 67FF 1KB		CAN
	0x4000 6000 – 0x4000 63FF 1KB		USB RAM
	0x4000 5C00 – 0x4000 5FFF 1KB		USB
	0x4000 5800 – 0x4000 5BFF 1KB		I2C2
	0x4000 5400 – 0x4000 57FF 1KB		I2C1
	0x4000 4C00 – 0x4000 53FF 2KB		-
	0x4000 4800 – 0x4000 4BFF 1KB		USART3
	0x4000 4400 – 0x4000 47FF 1KB		USART2
	0x4000 3C00 – 0x4000 43FF 2KB		-
	0x4000 3800 – 0x4000 3BFF 1KB		SPI2
	0x4000 3400 – 0x4000 37FF 1KB		-
	0x4000 3000 – 0x4000 33FF 1KB		IWDG
	0x4000 2C00 – 0x4000 2FFF 1KB		WWDG
	0x4000 2800 – 0x4000 2BFF 1KB		RTC
	0x4000 2400 – 0x4000 27FF 1KB		-
	0x4000 2000 – 0x4000 23FF 1KB		-
	0x4000 1800 – 0x4000 1FFF 2KB		-
	0x4000 1400 – 0x4000 17FF 1KB		-
	0x4000 0C00 – 0x4000 13FF 2KB		-
	0x4000 0800 – 0x4000 0BFF 1KB		TIM4
	0x4000 0400 – 0x4000 07FF 1KB		TIM3
	0x4000 0000 – 0x4000 03FF 1KB		TIM2

6 Electrical Characteristics

6.1 Parameter conditions

All voltages are referenced to VSS unless otherwise specified.

6.1.1 Min/Max

Unless otherwise specified, min/max values are guaranteed for worst case conditions at ambient temperature. Mains supply and frequency are tested at ambient temperature of 25C.

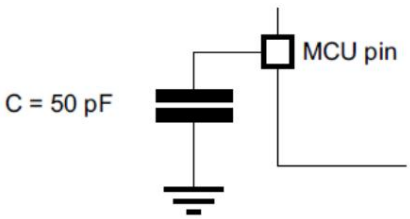
6.1.2 Typical values

Typical values are based on 25C and VDD=VDDA=3.3V unless otherwise specified. These values are design values, not test results.

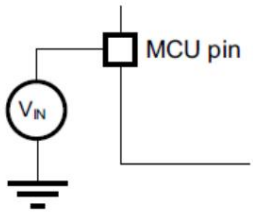
6.1.3 Typical curve

Unless otherwise specified, all typical curves are design reference values, not test results.

6.1.4 Load capacitance



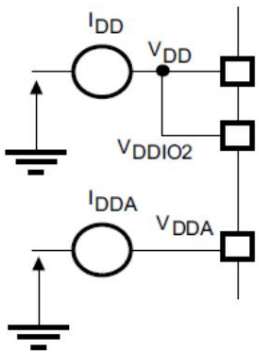
6.1.5 Pin Input Voltage



6.1.6 Power supply

Filter capacitors should be connected to each pair of power supplies (VDD/VSS, VDDA/VSSA, etc.), and the capacitors should be placed as close to the pins as possible on the PCB.

6.1.7 Current consumption measurement



6.2 Absolute Maximum

Exceeding the absolute maximum values may cause damage to the device.

Voltage characteristics

Symbol	Ratings	Min	Max	Unit
VDD-VSS	External main supply voltage	-0.3	5.8	V
VDDIO2-VSS	External I/O supply voltage	-0.3	5.8	V
VDDA-VSS	External analog supply voltage	-0.3	5.8	V
VDD-VDDA	Allowed voltage difference for VDD>VDDA	-	0.3	V
VBAT-VSS	External backup supply voltage	-0.3	5.8	V
VIN	Input voltage on FT and FTf pins	VSS-0.3	VDDIOx+ 0.3V	
	Input voltage on TTa pins	VSS-0.3	5.8	V

	Input voltage on any other pins	VSS-0.3	5.8	V
|ÿVDDx|	Variations between different VDD power pins	-	50	mV
|VSSx-VSS|	Variations between all the different grounds pins	-	50	mV
VESD(HBM)	Electrostatic discharge voltage		3000	V

6.3 Working conditions

6.3.1 General working conditions

normal working conditions

Symbol Parameter		Conditions	Min	Max	Unit
fHCLK	Internal AHB clock frequency -		0	100	MHz
fPCLK	Internal APB clock frequency -		0	100	MHz
VDD	Standard operating voltage	-	1.8	5.5	V
VDDIO2	I/O supply voltage		1.65	5.5	V
VDDA	Analog operating voltage		VDD	5.5	V
VBAT	Backup operating voltage		2.1	5.5	V
VIN	I/O input voltage	TC and RST I/O	-0.3	VDDIOx+0.3	V
		TTa I/O	-0.3	VDDA+0.3	
		FT and FTf I/O	-0.3	5.5	
PD	Power dissipation at TA=85C LQFP48		-	350	mW
		UFQFPN48	-	600	
		LQFP32		350	
		UFQFPN32		500	
		UFQFPN28		170	
		TSSOP20		250	
TA	Ambient temperature for the suffix 6 version	Maximum power dissipation -40		85	C
		Low power dissipation	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation -40		105	C
		Low power dissipation	-40	125	
TJ	Junction temperature range Suffix 6 version		-40	105	C
		Suffix 7 version	-40	125	

6.3.2 Power-on/power-off working conditions

Symbol Parameter		Conditions	Min	Max	Unit
tVDD	VDD rise time rate	-	0	ÿ	

	VDD fall time rate		20	ÿ	us/V
tVDDA	VDDA rise time rate	-	0	ÿ	
	VDDA fall time rate		20	ÿ	

6.3.3 Built-in reset/power control

Built-in reset and power control module features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPOR/PDR	Power on/down reset threshold	Falling edge	1.51	1.58	1.65V	
		Rising edge	1.54	1.62	1.70	
VPDRhyst	PDR hysteresis	-	-	40	-	mV
tRSTTEMPO	Reset temporization	-	1.5	2.5	4.5 ms	

Programmable Voltage Detect (PVD) Features

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPVD0	PVD threshold 0	Falling edge	1.59	1.67	1.75	V
		Rising edge	1.75	1.83	1.91	
VPVD1	PVD threshold 1	Falling edge	1.75	1.83	1.91	
		Rising edge	1.90	1.98	2.06	
VPVD2	PVD threshold 2	Falling edge	1.90	1.98	2.06	
		Rising edge	2.06	2.14	2.22	
VPVD3	PVD threshold 3	Falling edge	2.06	2.14	2.22	
		Rising edge	2.21	2.29	2.37	
VPVD4	PVD threshold 4	Falling edge	2.21	2.29	2.37	
		Rising edge	2.35	2.43	2.51	
VPVD5	PVD threshold 5	Falling edge	2.35	2.43	2.51	
		Rising edge	2.49	2.57	2.65	
VPVD6	PVD threshold 6	Falling edge	2.49	2.57	2.65	
		Rising edge	2.64	2.72	2.80	
VPVD7	PVD threshold 7	Falling edge	2.64	2.72	2.80	
		Rising edge	2.80	2.88	2.96	
VPVDhyst	PVD hysteresis	-	-	160	-	mV
IDD (PVD)	PVD current consumption -			0.15		uA

6.3.4 Built-in reference voltage

Built-in reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREFINT	Internal reference voltage	-40C<TA<+105	1.16	1.20	1.26V	

tSTART	ADC_IN17 buffer startup time -			-	10	us
tS_vrefint	ADC sampling time when reading the internal reference voltage	-	8	-	-	us
ÿVREFINNT	Internal reference voltage spread over the temperature range	VDDA=3V	-	-	10mV	
TCoeff	Temperature coefficient	-	-	-	100ppm/C	

6.3.5 Supply current

Typical Supply Current Consumption (VDD+VDDA @ **3.3V)**

Symbol	Parameter	Conditions	Min	Typ	Max Unit	
IDD+IDDA	Run from Flash memory	All peripherals enabled, HSI 8MHz		4.92		mA
		All peripherals enabled, HSI + PLL 72MHz		26.7		
	Stop mode	Regulator in run mode, all oscillators OFF		18.2		uA
		Regulator in low-power mode, all oscillators OFF		7.5		
	Standby mode	Regulator in low-power mode, all oscillators OFF		7.2		uA

6.3.6 Low power mode wake-up time

Low-power mode wakeup timings

Symbol	Parameter	Conditions	Min	Typ	Max Unit	
tWUSTOP	Wakeup from stop mode	Regulator in run mode	-	2.8	5	us
tSTART		Regulator in low power mode		4.6	10	
tWUSTANNDBY	Wakeup from standby mode -		-	50	-	
tWUSLEEP	Wakeup from sleep mode	-	4 SYSCLK cycles			

6.3.7 External clock source

High-speed external user clock characteristics

Symbol	Parameter	Min	Typ Max		Unit
fHSE_EXT	User external clock source frequency	-	8	twenty four	MHz
VHSEH	OSC_IN input pin high level voltage	0.7*VDDIOx	-	VDDIOx	V
VHSEL	OSC_IN input pin low level voltage	VSS	-	0.3*VDDIOx	
tW(HSEH) tW(HSEL)	OSC_IN high or low time	15	-	-	ns
tr(HSE) tf(HSE)	OSC_IN rise or fall time	-	-	20	

Low-speed external user clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
fLSE_EXT	User external clock source frequency	-	32.768 1000		KHz
VLSEH	OSC32_IN input pin high level voltage	0.7*VDDIOx	-	VDDIOx	V
VLSEL	OSC32_IN input pin low level voltage	VSS	-	0.3*VDDIOx	
tW(LSEH) tW(LSEL)	OSC32_IN high or low time	450	-	-	ns
tr(LSE) tf(LSE)	OSC32_IN rise or fall time	-	-	50	

HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fOSC_IN	Oscillator frequency	-	4	8	16	MHz
RF	Feedback resistor	-	-	200	-	Kÿ
IDD	HSE current consumption	VDD=3.3V, Rm=45 ÿ , CL=10pF@8MHz		0.57		mA
gm	Oscillator transconductance	Startup	10	-	-	mA/V
tSU(HSE)	Startup time	VDD is stabilized	-	2	-	ms

LSE oscillator characteristics(fLSE=32.768KHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IDD	LSE current consumption	low drive capability			360	nA
		medium-low drive capability			450	
		medium-high drive capability			540	
		high drive capability			700	
gm	Oscillator transconductance	low drive capability	5	-	-	uA/V
		medium-low drive capability				
		medium-high drive capability				
		high drive capability	25			
tSU(LSE)	Startup time	VDDIOx is stabilized	-	2	-	s

6.3.8 Internal Clock Source Characteristics

HSI8 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSI	Freqency	-		8		MHz
DuCy	Duty cycle	-	45	-	55%	
ACCHSI48	Accuracy of the HSI oscillator(factory calibrated)	TA=-40 to 105 @SS	-1.84		2.00%	
		TA=-40 to 105@TT	-1.58		1.76	
		TA=-40 to 105@FF	-1.24		1.72	
tSU(HSI8)	HSI8 oscillator startup time	-			6	us
IDDA(HSI8)	HSI8 oscillator power consumption	-		643	801	uA

LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fLSI	Freqency	-	31.9	40	55.5KHz	
tSU(LSI)	LSI oscillator startup time	-			100	us
IDDA(LSI)	LSI oscillator power consumption	-		400		nA

6.3.9 PLL characteristics

PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
fPLL_IN	PLL input clock	1	8	twenty four	MHz
tPLL_OUT	PLL multiplier output clock	16		96	MHz
tLOCK	PLL lock time	30		100	us
IDDA (PLL)	PLL power consumption			350uA	
JitterPLL	Cycle-to-cycle jitter			300	ps

6.3.10 Storage Features

Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tPROG	16-bit programming time	TA=-40 to +125			20	us
tERASE	Page(1KB) erase time				5	ms
tME	Mass erase time				40	ms
IDD	Supply current	Write mode			3.5 mA	
		Erase mode			2	mA
NEND	Enndurance	TA=-40 to +125	20			kcycle
tRET	Data retention	TA=25C	100			Year

6.3.11 EMC characteristics

EMC characteristics

Symbol	Parameter	Conditions	Level/Class
VFESD	Voltage limits to be applied on any I/O pin to induce a functional disturbance		
VEFTB	Fast transient voltage burst limits to be applied through 100pF on VDD and VSS pins to induce a functional disturbance		

EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [fHSE/fHCLK] 8/48MHz	Unit
SEMI	Peak level	VDD=3.6V, TA=25C, LQFP48 package compliant with IEC 61967-2	0.1 to 30MHz		dBuV
			30 to 130MHz		
			130MHz to 1GHz		
			EMI level		-

6.3.12 Electrically sensitive characteristics

ESD absolute maximum ratings

Symbol	Parameter	Conditions	Packages	Class	Maxi value	Unit
VESD voltage	(HBM) Electrostatic discharge (human body model)	TA=+25C, conforming to JESD22-A114	All	2	2000V	
VESD(CDM)	Electrostatic discharge voltage (charge device model)	TA=+25C, conforming to AEC-Q100-011	All	C6	1000V	

6.3.13 I/O Current Injection Characteristics

I/O current injection susceptibility

Symbol	Parameter	Functional susceptibility		Unit
		Negative injection	Positive injection	
IINJ	Injected current	-5	+5	mA

6.3.14 I/O port characteristics

I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage	TC and TTa I/O			0.3*VDDIOx	V
		FT and FTf I/O			0.475*VDDIOx-0.2	
		All I/Os			0.3*VDDIOx	
VIH	High level input voltage	TC and TTa I/O	0.445*VDDIOx+0.4			V
		FT and FTf I/O	0.5*VDDIOx+0.2			
		All I/Os	0.7*VDDIOx			
Vhys	Schmitt trigger hysteresis	TC and TTa I/O		200		mV
		FT and FTf I/O		100		
ilkg	Input leakage leakage current	TC,FT and FTf I/O TTa in digital mode VSS<=VIN<=VDDIOx			±0.1	uA
		TTa in digital mode VDDIOx<=VIN<=VDDA			1	
		TTa in analog mode VSS<=VIN<=VDDA			±0.2	
		FT and FTf I/O VDDIOx<=VIN<=5V			10	
RPU	Weak pull-up resistor	VIN=VSS		40		Kÿ
RPD	Weak pull-down resistor	VIN=-VDDIOX		40		Kÿ
CIO	I/O pin capacitance			5		pF

Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VOL	Output low level voltage for an I/O pin CMOS port		-	0.4V	
VOH	Output high level voltage for an I/O pin	|IIO| = 8mA VDDIOx>= 2.7V	VDDIOx-0.4	-	
VOL	Output low level voltage for an I/O pin	TTL port	-	0.4V	
VOH	Output high level voltage for an I/O pin	|IIO| = 8mA VDDIOx>= 2.7V	2.4	-	
VOL	Output low level voltage for an I/O pin	|IIO| = 20mA VDDIOx>= 2.7V	-	1.3V	
VOH	Output high level voltage for an I/O pin		VDDIOx-1.3	-	
VOL	Output low level voltage for an I/O pin	|IIO| = 6mA VDDIOx>= 2.7V	-	0.4V	
VOH	Output high level voltage for an I/O pin		VDDIOx-0.4	-	
VOL	Output low level voltage for an I/O pin	|IIO| = 4mA	-	0.4V	

VOH	Output high level voltage for an I/O pin	VDDIOx>= 2.7V	VDDIOx-0.4	-	
VOLFm+	Output low level voltage for an FTf I/O pin in FM+ mode	|IIO| = 20mA VDDIOx>= 2.7V	-	0.4V	
		|IIO| = 10mA	-	0.4	

I/O AC characteristics

OSPEEDRy [1:0]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	fmax(IO)out	Maximum frequency	CL=50pF, VDDIOx>=2V	-	2	MHz
	tf(IO)out	Output fall time		-	38	ns
	tr(IO)out	Output rise time		-	39	
x1	fmax(IO)out	Maximum frequency	CL=50pF, VDDIOx>=2V	-	10	MHz
	tf(IO)out	Output fall time		-	25	ns
	tr(IO)out	Output rise time		-	25	
11	fmax(IO)out	Maximum frequency	CL=30pF, VDDIOx>=2.7V	-	50	MHz
			CL=50pF, VDDIOx>=2.7V	-	30	
			CL=50pF, 2V<=VDDIOx<2.7V	-	20	
	tf(IO)out	Output fall time	CL=30pF, VDDIOx>=2.7V	-	6.5	ns
			CL=50pF, VDDIOx>=2.7V	-	9	
			CL=50pF, 2V<=VDDIOx<2.7V	-	15.5	
	tr(IO)out	Output rise time	CL=30pF, VDDIOx>=2.7V	-	6.6	
			CL=50pF, VDDIOx>=2.7V	-	8.6	
			CL=50pF, 2V<=VDDIOx<2.7V	-	39	
Fm+ configuration	fmax(IO)out	Maximum frequency	CL =50pF, VDDIOx>=2V	-	2	MHz
	tf(IO)out	Output fall time		-	15.5	ns
	tr(IO)out	Output rise time		-	39	
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

6.3.15 **NRST** pin characteristics

NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL(NRST)	NRST input low level voltage	-	-	-	0.3*VDD	V
VIH(NRST)	NRST input high level voltage	-	0.445*VDD+0.4	-	-	
Vhys(NRST)	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
RPU	Weak pull-up resistor	VIN=VSS	-	40	-	Kÿ
VF(NRST)	NRST input filtered pulse	-	-	-	100	ns

VNF(NRST)	NRST input not filtered pulse	2.7<VDD<3.6	300	-	-	ns
		2.0<VDD<3.6	500	-	-	

6.3.16 ADC Characteristics

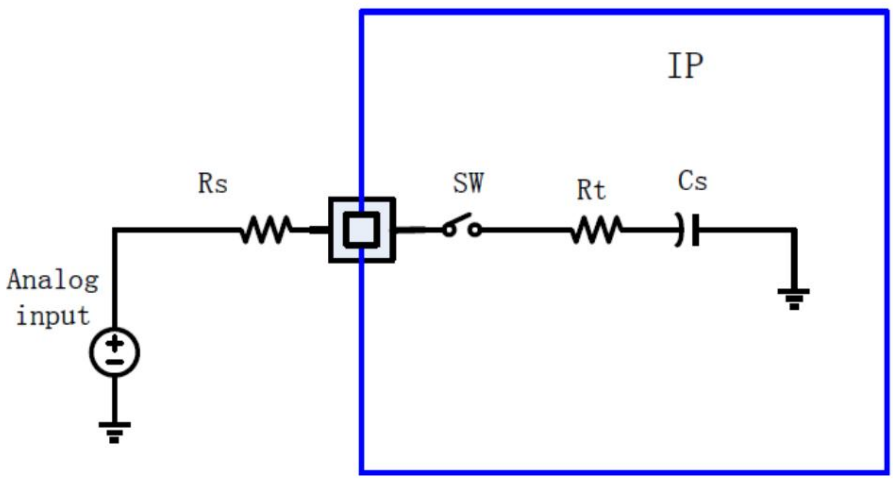
ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analog supply voltage	-	1.8	3.3	5.5	V
IDD(ADC)	Current consumption of the ADC	VDDA=3.3V	-	1.1	-	mA
fADC	ADC clock frequency	-	-	-	16	MHz
fS	Sampling rate	12-bit resolution	0.03	-	1	MHz
fTRIG	External trigger frequency	12-bit resolution	-	-	18	1/fADC
VAIN	Conversion voltage range		0		VDDA	V
Rt	Input resistor during sampling	VDDA=3V		0.5		kÿ
Cs	Internal sample and hold capacitor			26	30	pF
tS	sampling time	fADC=16MHz	4	-	-	1/fADC
tSTAB	Stabilization time		32	-	-	1/fADC
tCONV	Total conversion time	12-bit resolution		12		1/fADC

ADC accuracy

Symbol	Parameter	Conditions	Typ	Max	Unit
ET	Total unadjusted error	fPCLK=48MHz, fADC=16MHz,RAIN<10kÿ VDDA=3V to 3.6V TA=25C	±1.5	-	LSB
EO	offset error		±1.5	±3.0	
EG	Gain error		±2	±5	
ED	Differential linearity error		±0.6	±1.5	
EL	Integral linearity error		±1.5	±3.0	

Analog Input Equivalent Circuit



$$Rs = \frac{Tsamp}{10\ddot{y}Cs} \ddot{y} Rt$$

RAIN max for fADC = 16 MHz

Ts(cycles)	**ts(us)**	**RAIN max** (kÿ)
4	0.35	0.33
7.5	0.47	1.1
13.5	0.84	2.3
28.5	1.78	5.4
41.5	2.59	8.1
55.5	3.47	11.1
71.5	4.47	14.4
239.5	14.97	49.4

6.3.17 Temperature sensor characteristics

TS characteristics

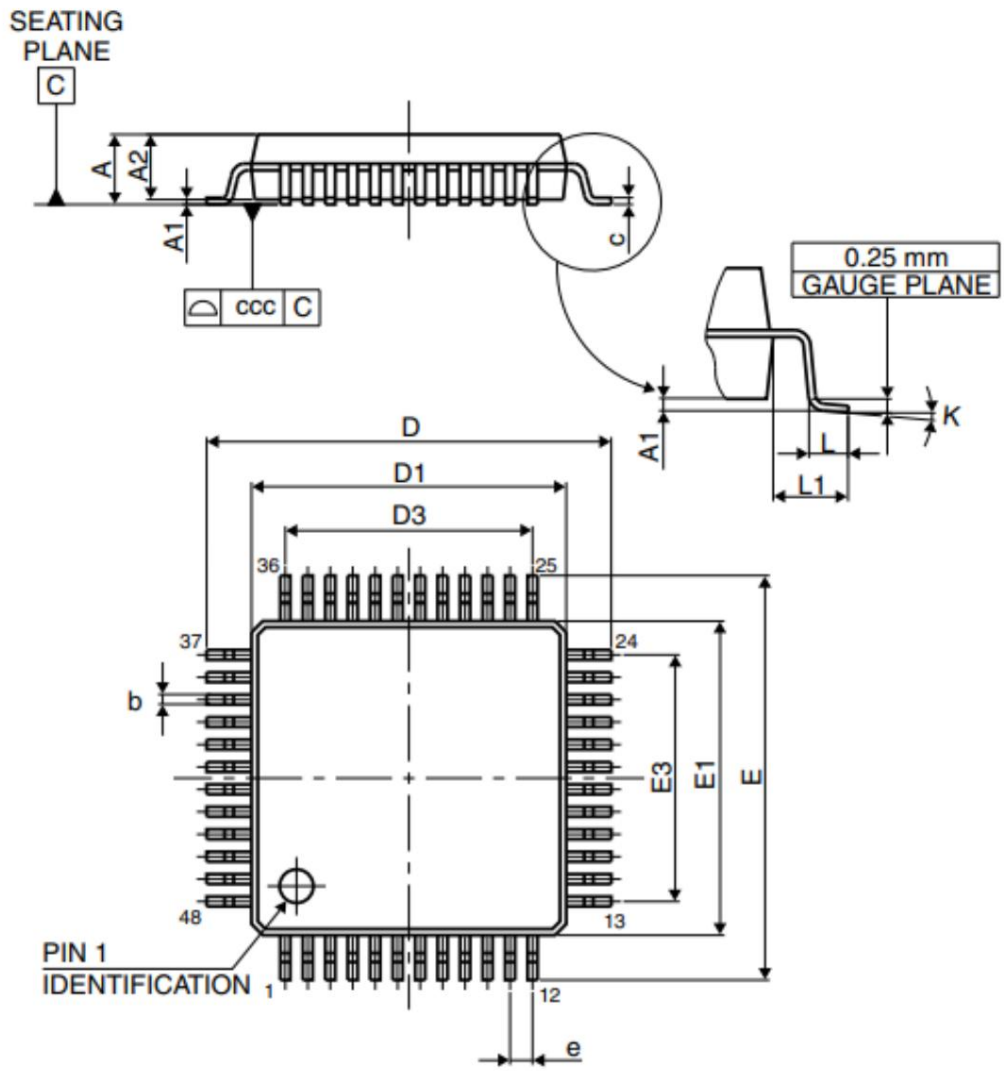
Symbol	**Parameter**	**Min Typ**	**Max Unit**		
TL	VSENSE linearity with temperature	-	±1	±2	C
Avg_Slope	Average slope	4.2	4.28 4.36	mV/C	
V30	Voltage at 30C	1.423	1.425 1.43	V	
tSTART	ADC_IN16 buffer startup time	1	-	5	us
tS_temp	ADC sampling time when reading the temperature	4	-	-	us

7 Package Information

7.1 LQFP48 Package Information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

LQFP48 package outline



LQFP48 package mechanical data

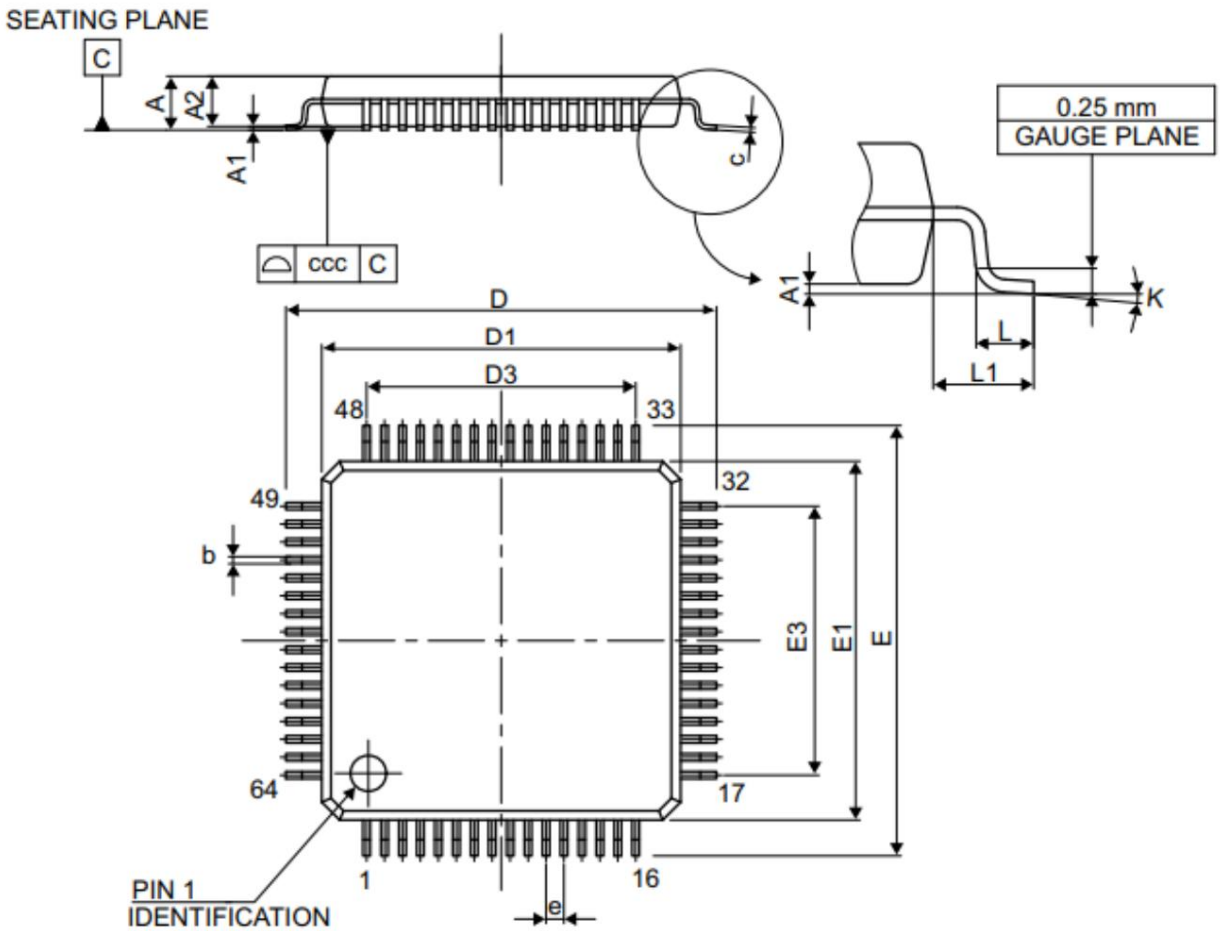
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 LQFP64 Package Information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

LQFP64 package outline



LQFP64 package mechanical data

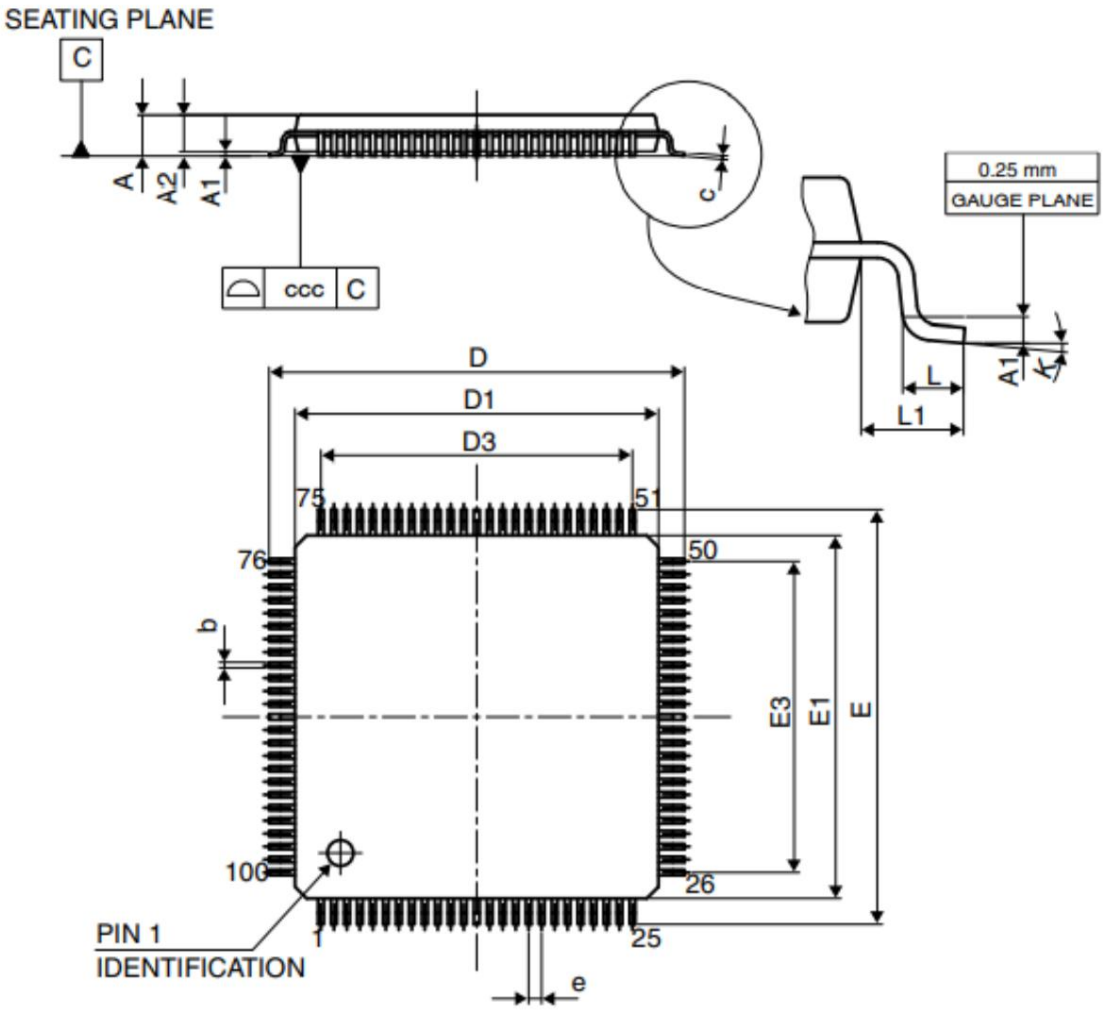
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 LQFP100 Package Information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

LQFP100 package outline



LQFP100 package mechanical data

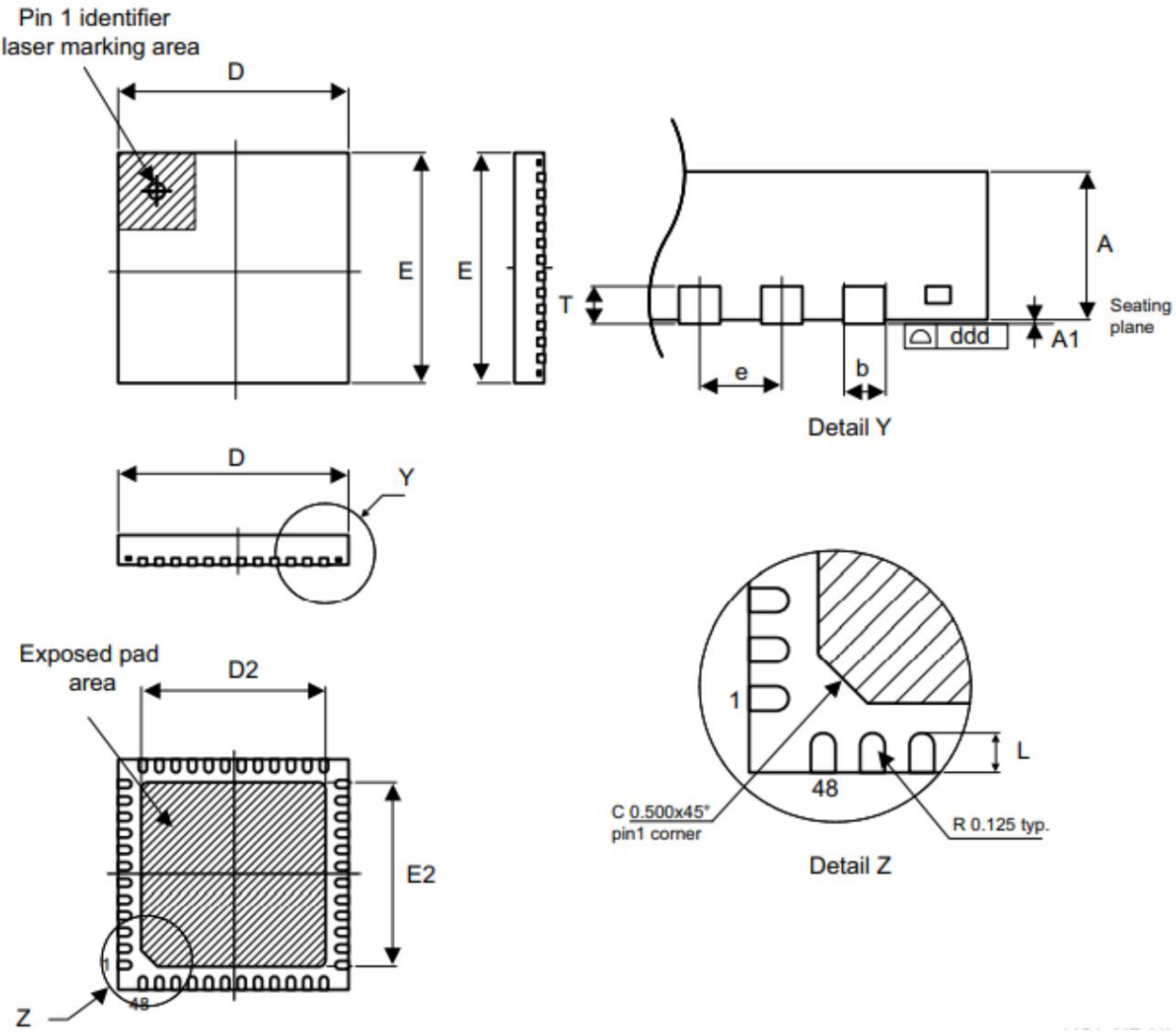
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.2	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.00	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-8	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.4 UFQFPN48 Package Information

UFQFPN48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

UFQFPN48 package outline



UFQFPN48 package outline

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Device Codes

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest FCM sales office.

Ordering information scheme

Example: FCM32 H 103 C B T 6 -x

Device family

FCM32 = ARM-based 32-bit microcontroller

Product type

F = General purpose

H = High performance

Device subfamily

103 = performance line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

8 = 64 Kbytes

B = 128 Kbytes

Package

T = LQFP

U = UFQFPN

Temperature range

6 = -40 to 85ÿ

7 = -40 to 105ÿ

8 = -40 to 125ÿ

Options

x = Revision code

9 Version History

Date	Revision	Author	Changes
2021/5/6	0.10	Dick Hou	The first version, suitable for C version IC

10 other