THM3060

Multiple Protocols Contactless Reader IC

Version 1.1

Contact us

Name: Beijing Tsinghua Tongfang Microelectronics Company
Address: Floor 11, Quantum Plaza, No 27 Zhi Chun Road, Hai Dian District, Beijing
Post code: 100191
Tel: +86-10-82351818
Fax: +86-10-82357168
E-mail: support@tsinghuaic.com
Website: www.tsinghuaic.com

Version

Version No.	Main modification	Data	Author
V0.1	Initial version	2009-5	DingYM
V1.0	Modified the twenty fourth pin of the THM3060 in the UART interface chart and the SPI interface chart.	2009-7	DingYM
V1.1	Add reset method of register description	2009-8	DingYM
V1.2	Modified the description in Page14, Figure 1. Pin22, XTAL3 : O Test Pin , No Connection Pin21, XTAL4 : I Test Pin ,Connected to DGND	2009-10	MengQY
V1.2	Modified the Pin22(XTAL3) and Pin21(XTAL4) of the THM3060 in the Page 52, Figure 57.	2009-10	MengQY
V1.2	Modified the Pin22(XTAL3) and Pin21(XTAL4) of the THM3060 in the Page 54, Figure 59.	2009-10	MengQY
V1.2	Modified the Pin22(XTAL3) and Pin21(XTAL4) of the THM3060 in the Page 56, Figure 60.	2009-10	MengQY

Abbreviations

ISO/IEC14443	Contactless integrated circuit(s) cards-- Proximity cards International Standard
ISO/IEC15693	Contactless integrated circuit(s) cards-- Proximity cards International Standard
TYPE-A	Type-A protocol defined by the ISO/IEC14443
TYPE-B	Type-B protocol defined by the ISO/IEC14443
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
SCLK	Slave Clock (The SPI clock SCLK has to be generated by the master)
MOSI	Master Out Slave In
MISO	Master In Slave Out
SS_N	Slave Select
SLOT	Timeslot at Initialization and anti-collision stage
UID	Unique ID
PAUSE	a low level signal modulated according to ISO14443 and ISO15693
ETU	Element of Time Unit
EGT	Extra Guard Time
EOF	End of Frame
SOF	Start of Frame
BPS	Bits Per Second
CRC	Cyclic Redundancy Code
RFU	Reserved For Use
NC	Not Connected
EEPROM	Electrically Erasable Programmable Read-Only Memory

CONTENTS

FIGURES

1 Introduction

1.1 Description

The THM3060 is a multi-protocol contactless reader IC. It's Conforming to ISO/IEC14443 Type A/B and ISO/IEC15693 standards. It supports contactless communication with higher baud rates up to 848 KBPS. The THM3060 has built-in receiving amplifier, digital demodulation circuit and clock circuit.

1.2 Features

- Compatible with the ISO/IEC 14443 A/B
- Supports higher baud rates up to 848 KBPS
- Compatible with the ISO/IEC 15693
- Host interface selectable: UART,SPI and "Transparent" mode
- Max frame size up to 512 bytes
- internal oscillator to connect a 13.56 MHz quartz
- Embedded hardware CRC and receiver timer
- integrated analog circuit for reception
- Interrupt request output
- Standby mode
- 3.3V or 5V operation[1]
- LQFP48 package

1 Optimum AVDD :3~3.6V.

2 Block diagram of functions

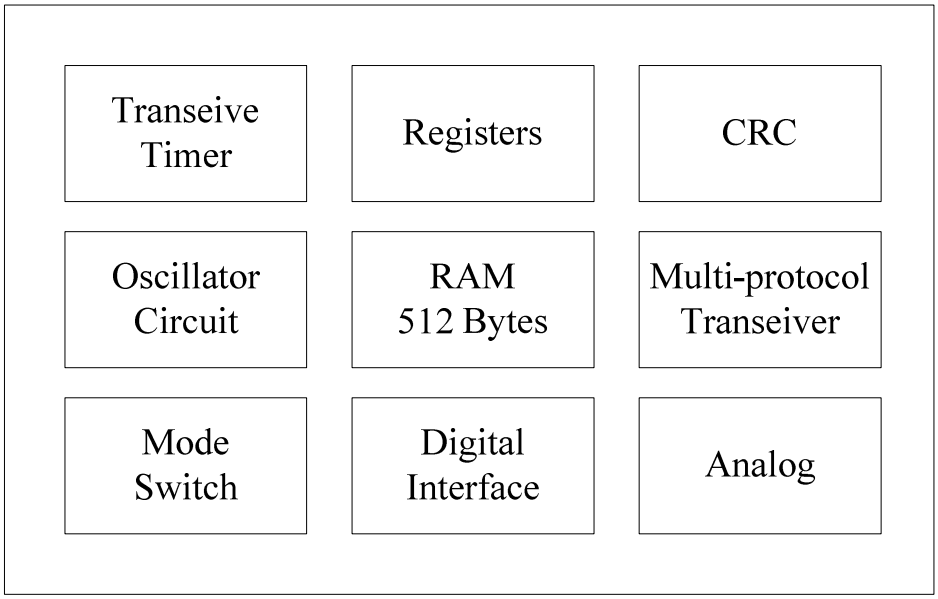


Figure 2 block diagram of the THM3060

3 PIN

3.1 Pin chart（LQFP-48）

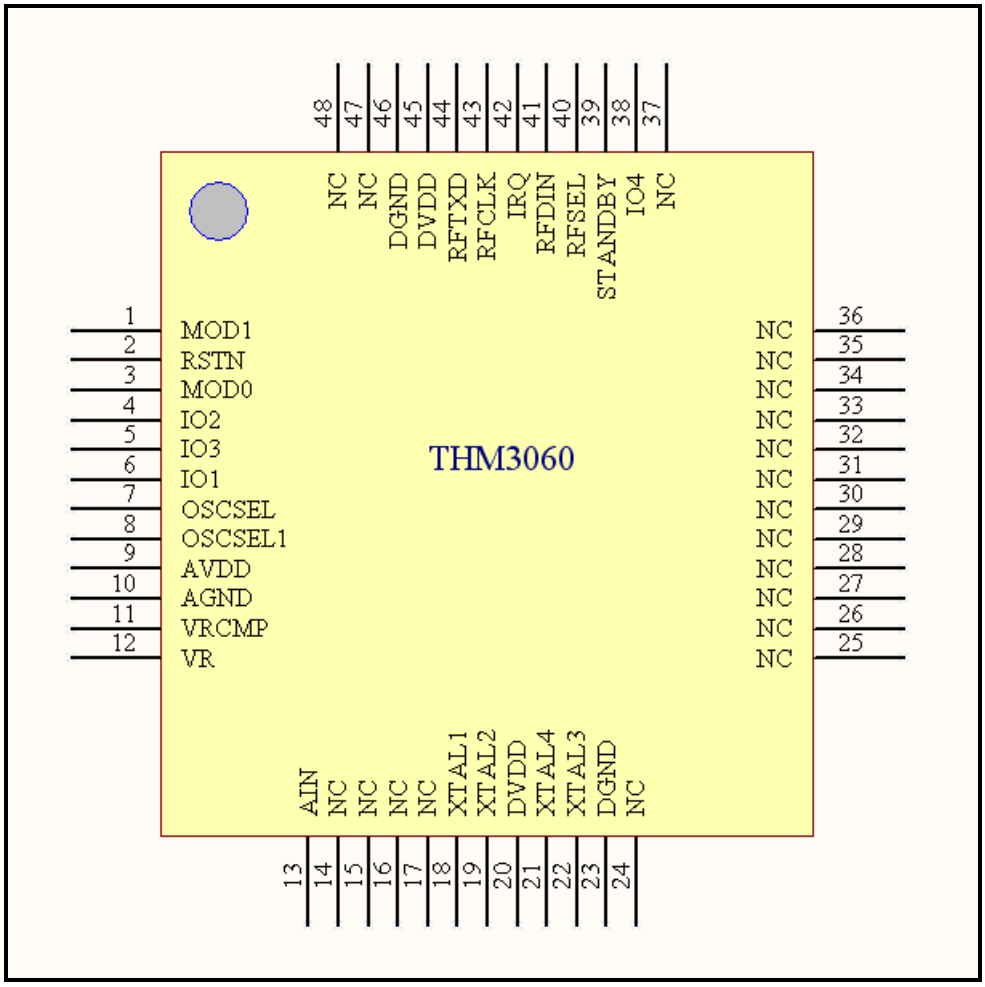


Figure 3 Pin diagram (LQFP-48)

3.2 Pin description

Pin	Symbol	Type[2]	Description		
			SPI mode[3]	UART mode	Transparent mode
6	IO1	I/O	SCLK, Input with internal weak pull-up	No Connect, Input with internal weak pull-up	Input with internal weak pull-up, RF protocols select
4	IO2	I/O	MOSI, Input with internal weak pull-up, Master Out Slave In	No Connect, Input with internal weak pull-up	Input with internal weak pull-up, RF protocols select
5	IO3	O	MISO, Output, Master In Slave Out, Output high-Z (With internal weak pull-up) when SS_N is high	TXD, Output, UART Transmit Output	RCD, Output, Receive data output
38	IO4	I	SS_N, Input, Low validity, Slave Select with internal weak pull-up	RXD , Input, UART Receive Input with internal weak pull-up	TRD, Input, Transmit Data input with internal weak pull-up
2	RSTN	I	Reset input with internal weak pull-up, Low validity		
18	XTAL1	I	Crystal Oscillator Input		
19	XTAL2	O	Crystal Oscillator Output		
1	MOD1	I	Host Interface Selection 1		
3	MOD0	I	Host Interface Selection 0		
42	IRQ	O	Interrupt Request Output		
39	STANDBY	I	Standby mode control，High for Standby mode and Low for Normal mode		
40	RF_SEL	I	Test Pin , Connected to DVDD		
41	RF_DIN	I	Test Pin , Connected to DGND		
13	AIN	I	Input of detection signal		
12	VR	I	Reference Voltage 1, connected with external de-coupling capacitor		
11	VRCMP	I	Reference Voltage 2, connect with external de-coupling capacitor		
44	RFTXD	O	Modulation Signal Output pin. When the carrier is closed, this pin is		

[2] I for Input, O for Output, P for Power
[3] MOD1 and MOD0 decide the host interface: SPI mode, UART mode and Transparent mode

			low and the large current output pin with maximum current of 30mA.
43	RFCLK	O	Carrier output pin. When the carrier is opened, this pin output is the 13.56MHz square wave and the large current output pin with maximum current of 30mA.
45	DVDD	P	Digital Power Supply
46	DGND	P	Digital Ground
20	DVDD	P	Digital Power Supply
23	DGND	P	Digital Ground
10	AGND	P	Analog Ground
9	AVDD	P	Analog Power Supply
7	OSC_SEL	I	Test Pin , Connected to DVDD
8	OSC_SEL1	I	Test Pin , Connected to DGND
22	XTAL3	O	Test Pin , No Connection
21	XTAL4	I	Test Pin , Connected to DGND

Figure 4 Functions of pins

4 Host interfaces

4.1 Interface types

The THM3060 Host interfaces (UART, SPI, transparent) are selectable. Different interfaces can be selected by the input of MOD1 and MOD0.

MOD1	MOD0	Interface mode	function
0	0	SPI interface mode	The THM3060 acts as a slave device during the SPI communication.
0	1	UART interface mode	The UART mode is specified with fixed baud rate of 115200，no parity bit, 8 bit data and 1 stop bit. Supports half-duplex communication, Byte interval is used to mark the end of frame (~10ms).
1	0	Transparent interface mode	RF frames should be managed by the external circuit.
1	1	RFU	Reserved for future use.

Figure 5 Digital interfaces

4.2 SPI interface mode

4.2.1 Functions

When both MOD1, MOD0 are low, the THM3060 enters SPI mode

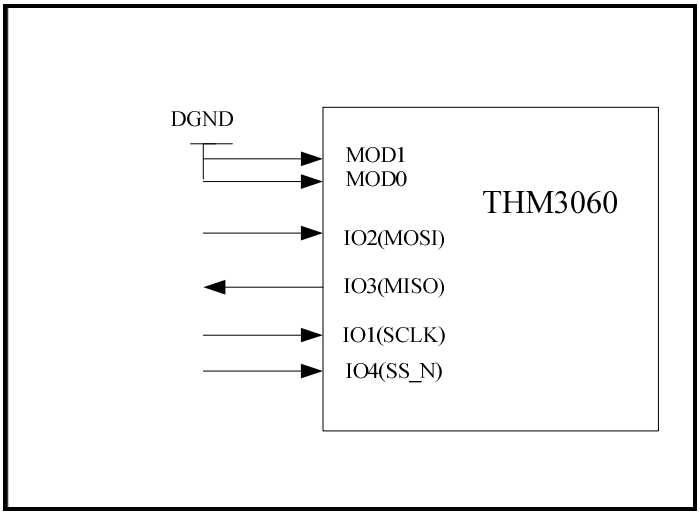


Figure 6 Diagram of SPI interface mode

4.2.2 Operation waveform

The normal state of clock in the SPI mode is 0, and which rising edge is effective (SS_N should maintain low when a frame transmits).
SPI protocol sequence:

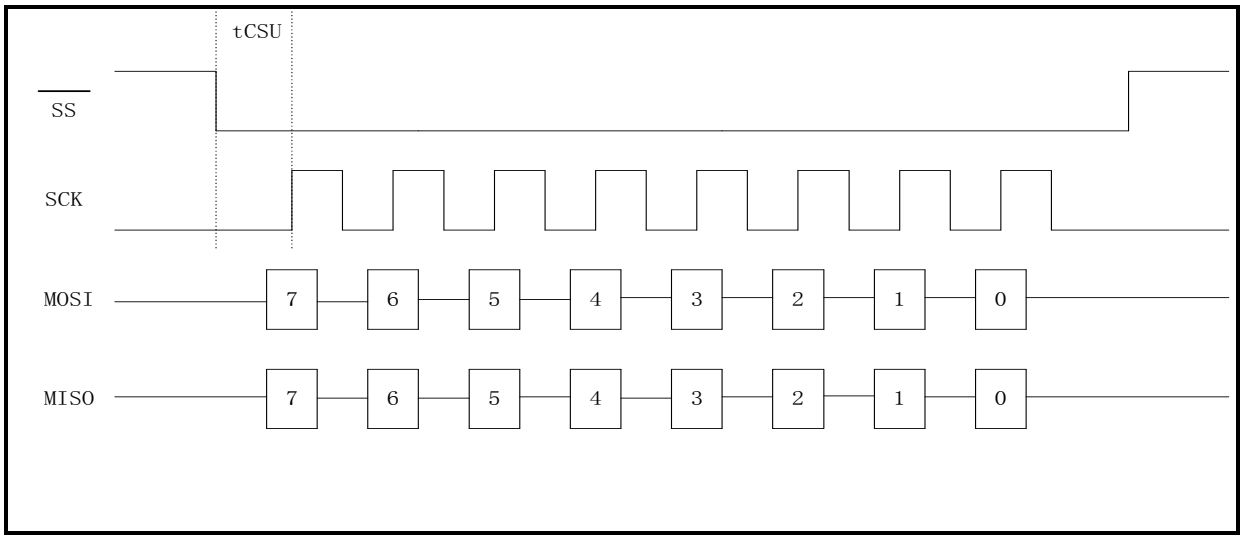


Figure 7 SPI protocol sequence

Note: tCSU time should be over 1μs. THM3060 is a SPI slave component, external SPI master can sends commands to complete the operation.

4.2.3 SPI Frames

command（1 byte）	data（0~N byte）

Figure 8 SPI frame

Command byte format

B7	B6~B0
1：write operation 0：read operation	Operation address

Figure 9 Command byte format

4.2.4 SPI operation

4.2.4.1 Write data to register

E.g. write data to address 0x82

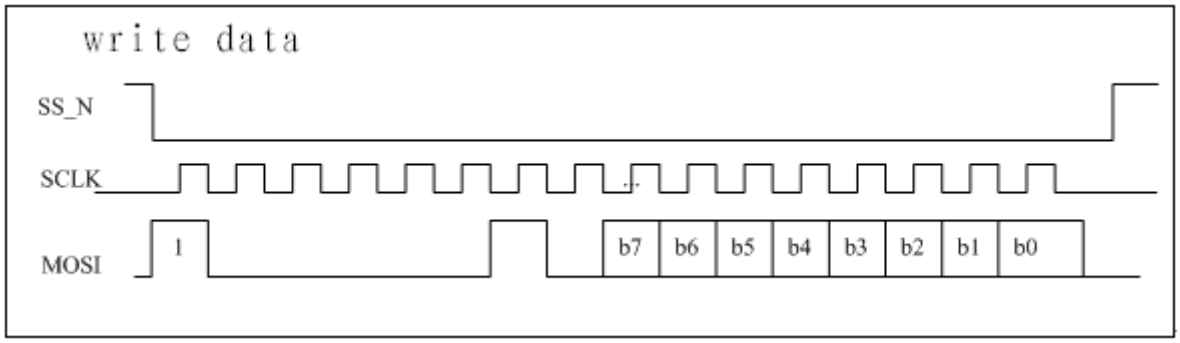


Figure 10 Writing under SPI interface mode

First, the SPI master output address 0x82. Then it outputs data to SPI interface. SS_N should maintain low until the frames are finished. The THM3060 samples the data at each rising edge of clock.

4.2.4.2 Read data from register

E.g. read data from address 0x02:

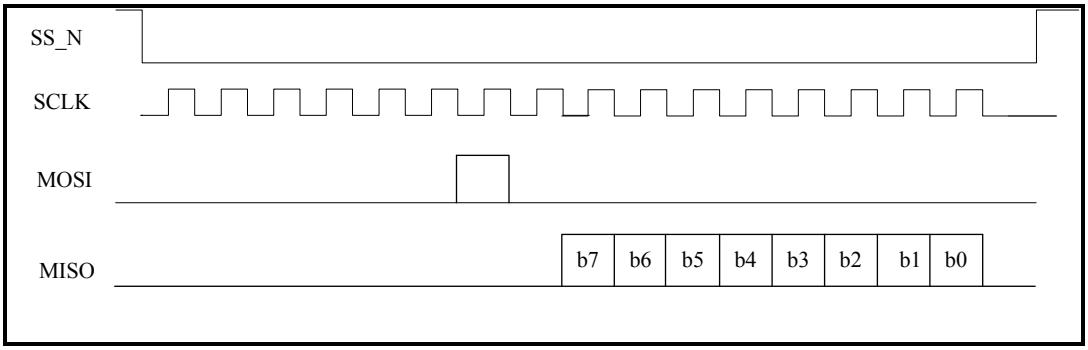


Figure 11 read register under SPI interface mode

First, the SPI master outputs address 0x02 while it output the clock. Then the THM3060 sends data by MISO.
The THM3060 output data at fall edge and the SPI master should sample the data at each rising edge of clock.

4.2.4.3 Write data to the buffer

Writing data to the buffer or register are similar. But the address should be written is fixed to 0x80. The data length shouldn't exceed 512 bytes. Additionally, SS_N should maintain low.

4.2.4.4 Read data from the buffer

Read data from the buffer is similar to the register. But the address should be read is fixed to 0x00. The THM3060 output data length by the RSC register. Additionally, SS_N should maintain low during the read frame.

4.2.4.5 Note of SPI interface

1) The frequency of SPI interface signal clock must not exceed 2.5MHz.
2) It should be written 1 byte data to the register. Otherwise the data will be covered.
3) It could be written 1~n byte data to the buffer. The data will be written at where the pointer point.
4) It should be read 1 byte data from the register. The following data are invalid.
5) It should be read valid data from the buffer, the following data are invalid.

4.3 UART interface

When MOD1 is low and MOD0 is high, the THM3060 enters to UART interface mode.
The UART interface of the THM3060 only supports 115200 baud rate, a start bit, 8 data bits, 1 stop bit, without parity bit data format.

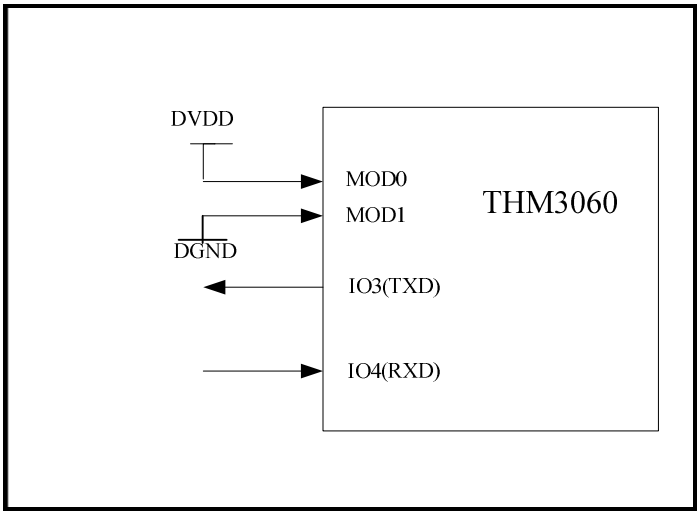


Figure 12 UART interface diagram

4.3.1 UART character structure

Each character of the UART interface, including a start bit, 8 data bits and 1 stop bit. MSB first.

Start bit	B7	B6	B5	B4	B3	B2	B1	B0	Stop bit
0	x	x	x	x	x	x	x	x	1

Figure 13 UART character structure

4.3.2 UART frame structure

UART characters constitute a UART frame, a UART frame is representative of a command. Each frame includes a command byte followed by 0 or more data bytes.

Command (1 byte)	data (0~N byte)

Figure 14 UART frame

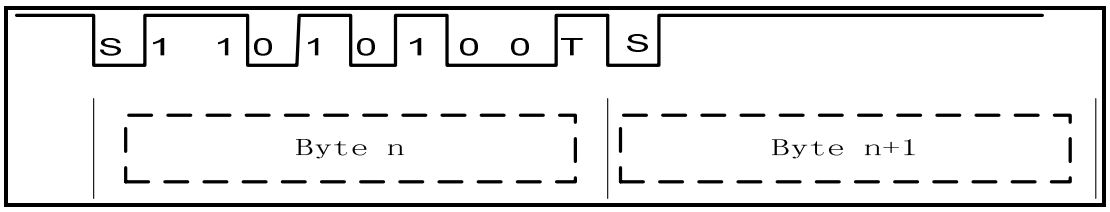
Command byte

B7	B6~B0
1：write operation 0：read operation	Register operation address

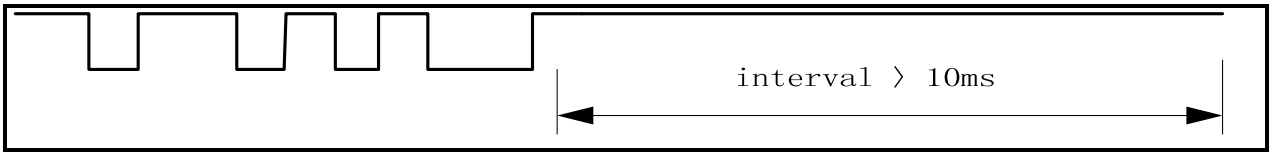
Figure 15 UART command byte

The UART interface defines a frame through the character spacing, when character interval more than

10 ms, it will be considered to be a different frame.



When character interval less than 10ms, it will be considered to be the same frame of data



When character interval more than 10ms, it will be considered to be a different frame.

4.3.3 UART interface operation

4.3.3.1 Write to data buffer

Data written to register 'DATA' will be written to data buffer of the THM3060, no more than 512 bytes of data could be written.

For example: write data 112233445566778899, the external microprocessor sends the following data via UART interface.

0x80	112233445566778899
Write to address 0x80 (DATA register)	Write data

Figure 16 writing data to data buffer under UART

4.3.3.2 Write to other registers

For example: write '0xC1' to the CRCSEL register

To write to address 0x84 with data '0xC1', the external microprocessor sends the following data via UART interface.

0x84	0xC1
Write to address 0x84 (CRCSEL register)	Write data

Figure 17 writing register under UART

4.3.3.3 Read data from the data buffer

The address to be read is 00 (DATA register read address). After the external microprocessor transmits '00' through the UART interface, the THM3060 would output all valid data within the buffer (number of valid data according to the RSC register).

4.3.3.4 Read data

For example: If the value of RSC register is 0x09, the data in the buffer are 112233445566778899

0x00
The external microprocessor sends read address 0x00

0x112233445566778899
THM3060 outputs

Figure 18 UART read data

4.3.3.5 Read other registers

For example: read data from CRCSEL register.

0x04
The external microprocessor sends read address 0x04

0xC1
THM3060 outputs

Figure 19 UART read register

4.4 Transparent interface

When MOD1 is high and MOD0 is low, the THM3060 works in the "transparent" mode.
As the name implies, "Transparent" mode will "transparently" provide the receiving and sending data. Under the "transparent" mode, users should code the transmission frames of the data according to relevant requirements and decode the received data frames. The transparent mode allows any

modification to the transmitted data frame and can receive the data frames that don't completely conform to the ISO/IEC14443 or ISO/IEC15693 standard. In this mode, the THM3060 can also receive and send data frames with more than 512 bytes.

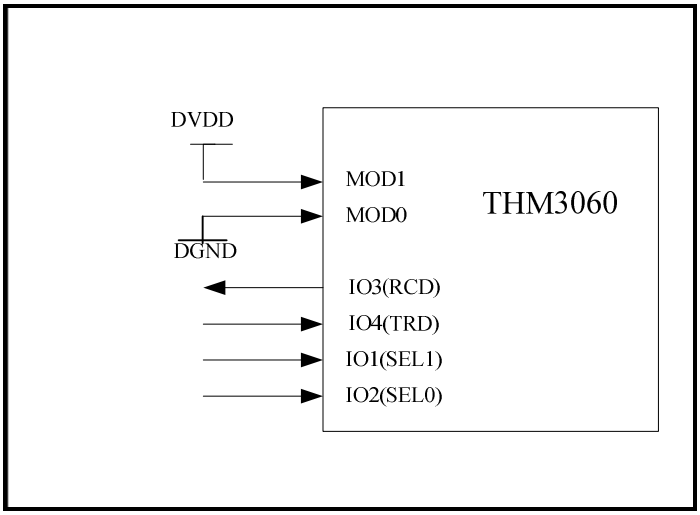


Figure 20 transparent interface diagram

TRD Input of transmitted data under the transparent mode. RCD is the Data output pin under the transparent mode. SEL1 and SEL2 pins are used for the protocol selection control.

Pin	Symbol	Function
38	IO4（TRD）	Output the Input data under "transparent" mode. The input is done by an external microprocessor.
5	IO3（RCD）	Data output pin.
6	IO1（SEL1）	The protocol selection signal 1.
4	IO2（SEL0）	The protocol selection signal 0.

Figure 21 transparent interface mode pin

SEL1	SEL0	function
0	0	ISO/IEC14443 TYPE-B standard
0	1	ISO/IEC14443 TYPE-A standard
1	0	ISO/IEC15693 standard
1	1	RFU

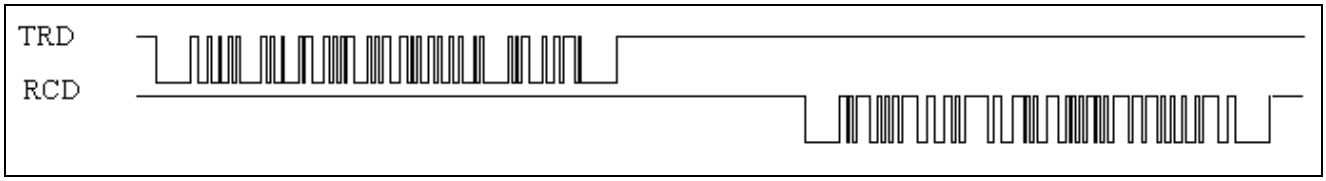


Figure 22 Diagram of signal transmission and receiving in

transparent mode（TYPE-B standard）

5 Register table

The highest bit represent reading when the value is 0 and represent writing when the value is 1. Other bits are register address.

The external microprocessor access to the corresponding register when communicate with THM3060. DATA register can be written or read many bytes once. The other registers can only be written or read one byte once.

5.1 Standard protocol register

5.1.1 Standard protocol register table

Write address	Read address	Description	Register	Reset value	R/W
0x80	0x00	Data register	DATA	xx	R/W
0x81	0x01	Protocol selection register	PSEL	0x00	R/W
0x82	0x02	TYPE-B protocol frame control register	FCONB	0x2A	R/W
0x83	0x03	TYPE-B protocol EGT control register	EGT	0x40	R/W
0x84	0x04	CRC control register	CRCSEL	0xC1	R/W
0x85	0x05	Receiving state register	RSTAT	0x00	R/W
0x86	0x06	Sending control register	SCON	0x00	R/W
0x87	0x07	Interrupt control register	INTCON	0x01	R/W
0x88	0x08	Upper 8 bits of the RSC (receive and send counter) register	RSCH	0x00	R
0x89	0x09	Lower 8 bits of the RSC register	RSCL	0x00	R
0x8A	0x0A	Upper 8 bits of the CRC register	CRCH	0xFF	R

0x8B	0x0B	Lower 8 bits of the CRC register	CRCL	0xFF	R
0x8C	0x0C	Upper 8 bits of TMR (receiving timer) register	TMRH	0x01	R/W
0x8D	0x0D	Lower 8 bits of TMR (receiving timer) register	TMRL	0x00	R/W
0x8E	0x0E	Collision bits position	BPOS	0x00	R
0x8F	0x0F	Reserved for Future Use	RFU		
0x90	0x10	Sending mode setting	SMOD	0x00	R/W
0x91	0x11	Pulse width setting	PWTH	0x27	R/W
0x92~0xFF	0x12~0x7F	Reserved for Future Use	RFU		

Figure 23 Standard protocol register table

5.1.2 Introduction to standard protocol register

5.1.2.1 DATA

DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Figure 24 DATA register

The data register is the “gate” of the data buffer. Writing or reading DATA can write or read data from data buffer.

5.1.2.2 PSEL

PSEL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Symbol	RFU	RFU	Protocol Selection		Sending Baud rate Selection		Receiving Baud rate Selection	
Function			00	ISO14443 TYPE-B standard	00	106KBPS	00	106KBPS
			01	ISO14443 TYPE-A standard	01	212KBPS	01	212KBPS
			10	ISO15693 standard	10	424KBPS	10	424KBPS

			11	RFU	11	848KBPS	11	848KBPS
Reset value	0	0	00	TYPE-B	00	106KBPS	00	106KBPS

Figure 25 PSEL register

The PSEL register is used for protocol selection. By setting the PSEL [5:4], you can choose different RF protocols. The THM3060 supports sending different baud rates by setting the PSEL [3:2] and receiving different baud rates by setting the PSEL [1:0].

5.1.2.3 FCONB

FCONB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
symbol	RFU	RFU	EOF width setting		SOF high level width setting		SOF low level width setting	
function			00	10 ETU[4]	00	2 ETU	00	10.00 ETU
			01	10.25 ETU	01	2.25 ETU	01	10.25 ETU
			10	10.5 ETU	10	2.5 ETU	10	10.5 ETU
			11	11 ETU	11	3 ETU	11	11 ETU
Reset value	0	0	10	10.5ETU	10	2.5 ETU	10	10.5 ETU

Figure 26 FCONB register

The FCONB register can set the duration of SOF and EOF of TYPE-B protocol. The unit is ETU with variable width at different baud rates.

5.1.2.4 EGT

EGT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Symbol	EGT width setting			RFU	RFU	RFU	RFU	RFU
function	000	0 ETU						
	001	1 ETU						

[4] ETU: The elementary time unit described in ISO/IEO14443 standard. The unit is ETU with variable width at different baudrates.

Baud rate	Definition（fc = 13.56MHz）	Time
106K	128/fc	About 9.44μs
212K	64/fc	About 4.72μs
424K	32/fc	About 2.36μs
848K	16/fc	About 1.18μs

	010	2 ETU					
	011	3 ETU					
	100	4 ETU					
	101	5 ETU					
	110	6 ETU					
	111	RFU					
Reset value	010	2 ETU	0	0	0	0	0

Figure 27 EGT register

The EGT register is used to set the width of EGT (A parameter of TYPE-B protocol) range of 0 to 6 ETU.

5.1.2.5 CRCSEL

DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Symbol	SCRC	RCRC	RFU	RFU	RFU	RFU	RFU	TMREN
function	1:Transmitting circuit generates the CRC automatically 0：Transmitting circuit doesn't generate the CRC automatically	1:receiving circuit judges the CRC 0:receiving circuit doesn't judge the CRC						1:Start to judge receiving time-out 0:stop judging receiving time-out
Reset value	1	1	0	0	0	0	0	1

Figure 28 CRC control register

There is a CRC circuit embedded in the THM3060. The THM3060 can select different CRC method automatically by setting the PSEL [5:4].

The CRCSEL register may control the hardware to decoding the CRC automatically. When the SCRC set, the transmitting circuit will send two-byte CRC after sending data in the buffer. That is to say, the numbers of data are equal to the value of RSC plus 2. When the RCRC set, the hardware judges the data by verifying CRC automatically. The value of RSTAT.CRCERR will be 1 if the CRC is invalid. If the CRC is correct, the RSC register will count the data after removing the length of CRC. So the number of data should be minus 2. When CRC is error, the RSC register will not minus 2 and the value of RSC are the number of all received data.

5.1.2.6 RSTAT

RSTAT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Symbol	IRQ	CERR	PERR	FERR	DATOVER	TMROVER	CRCERR	FEND
function	1：interrupt detected 0：no interrupt detected	1：Collision error detected when receiving data. 0：No collision detected.	1：Parity Error 0：parity correct	1：frame format error 0：frame format correct	1：Frame data overflow 0：frame data doesn't overflow	1：timeout 0：doesn't timeout	1:CRC error 0：CRC correct	1：data frame reception correct 0：data frame reception error
Reset value	0	0	0	0	0	0	0	0

Figure 29 RSTAT register

FEND =1 indicates the frame received complete. The receiving operation would be correct if all of the error bits are 0.

CRCERR =1 indicates the frame received complete but the CRC are error. This bit is valid when CRCSEL.RCRC=1.

TMROVER =1 indicates receiving timeout. The card fails to respond before the waiting time. This bit is valid when CRCSEL.TMREN =1.

FERR = 1 indicates data frame error for some reason (mostly because of signal interference. In that case, the circuit or antenna design should be adjusted) resulting in incorrect data received

DATOVER =1 indicates the data has overflowed. The number of received data exceeded 512.

PERR =1 Indicates the parity bit of data is error under TYPE-A standard. For ISO 14443 TYPE-B and the ISO15693 standard, this bit is useless.

CERR =1 indicates collision errors detected. If more than one card is within the RF-field during the card anti-collision phase, they will respond simultaneously. The THM3060 supports the algorithm defined in ISO14443-A and ISO15693 to resolve data-collisions of cards serial numbers by doing the anti-collision Procedure. After the procedure, the errors still may happen. So the data would be considered invalid. Additionally, this bit is meaningless to the ISO14443-B protocol.

IRQ =1 indicates receiving complete. The receiving operation would be correct if all of the error bits are 0. Recommend to use the IRQ to judge whether the process is finished, and then judge whether the error bit is 0 instead of judging the value of 'FEND' because the FEND will be set to 0 when FERR=1.

5.1.2.7 SCON

SCON	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Symbol	RFU	RFU	RFU	RFU	RFU	PTRCLR	START	CARRYON
Function						1：clear data buffer 0：data buffer works	1：start sending and receiving 0：stop sending and receiving	1：Open RF carrier 0：close RF carrier
Reset value	0	0	0	0	0	0	0	0

Figure 30 SCON register

CARRYON = 1. Open RF carrier and then the THM3060 output carrier to the RFCLK pin. An external power amplifier output the carrier to an external antenna. The antenna output RF power and then the card within the working volume will be activated.
CARRON =1. Close the RF carrier. RFCLK pin will output low.
START =1. Start sending and receiving processes. The THM3060 read buffer first and then send data to the card in RF field. Then write the receiving data into the buffer. After that procedure, the hardware will clear the START bit automatically.
The THM3060 data buffer is a 512-byte built-in SRAM. The external microprocessor accesses to the buffer through continuous communication with DATA register. There are two pointers inside The THM3060: a writing pointer and a reading pointer. When PTCLR = 1, the internal buffer writing pointer will return 0. To re-write data from the DATA register should start at address 0.

5.1.2.8 INTCON

INTCON	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Symbol	RFU	RFU	RFU	RFU	RFU	RFU	INTLEVEL	INTEN
function							1：The interruption Is valid when IRQ=1. 0：the interruption Is	1: Allowed the interruption signal output to the IRQ pin. 0：Disabled the interruption signal

							valid when IRQ=0	output to the IRQ pin.
Reset value	0	0	0	0	0	0	0	1

Figure 31 INTCON register

The interrupt control register controls the level to match the interrupt level of the external microprocessor and controls whether RSTAT signal output to the IRQ pin.

5.1.2.9 RSC

RSCH

RSCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	RFU	RFU	RFU	RFU	RFU	RFU		

RSCL

RSCL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Figure 32 RSC register

The sending and receiving counter register counts the numbers of the writing data from the external microprocessor or receiving data from the contactless card.
RSC = RSCH × 256 + RSCL. The maximum value is 512.
The RSC register is read-only.

5.1.2.10 CRC

CRCH

CRCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

CRCL

CRCL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Figure 33 CRC register

The CRC register is read-only. It shows the CRC result of last sending or receiving frame.

5.1.2.11 TMR

TMRH

TMRH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reset value	0	0	0	0	0	0	0	1

TMRL

TMRL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reset value	0	0	0	0	0	0	0	0

Figure 34 TMR register

The unit of the internal timer is 302μs. The internal timer is valid when CRCSEL.TMREN = 1 and it is used to set the maximum response time. The THM3060 will stop the receiving process if the card didn't respond before the preset time. Then the value of RSTAT.TMROVER will be set to 1.
The timer will not start when CRCSEL.TMREN = 0. In that case, the THM3060 will keep receiving until the value of SCON.START is equal to 0. You can get more information at chapter 8.

5.1.2.12 BITPOS

BITPOS	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	RFU	RFU	RFU	RFU	RFU	000：a collision at the bit 0 of last received byte 001：a collision at the bit 1 of last received byte 010：a collision at the bit 2 of last received byte 011：a collision at the bit 3 of last received byte 100：a collision at the bit 4 of last received byte 101：a collision at the bit 5 of last received byte 110：a collision at the bit 6 of last received byte 111：a collision at the bit 7 of last received byte		
Reset value	0	0	0	0	0	000		

Figure 35 BITPOS register

Used for the ISO/14443-A and the ISO/15693 protocol. The BITPOS register indicates the collision bit when the collision detected by THM3060. Users can confirm the next step in anti-collision process according to the value of the BITPOS register.

5.1.2.13 SMOD register for ISO/15693

SMOD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Symbol	RFU	RFU	RFU	RFU	RFU	SPUL	C_1_256	INDEX100
Function						1: Send EOF only 0: Normal Frames	1：Encoded as 1 / 256 0：Encoded as 1 / 4	1: Modulation index of 100% 0： 10~30% Modulation index of 10 ~ 30%
Reset value	0	0	0	0	0	0	0	0

Figure 36 SMOD register

The SMOD register sets RF frames according to the ISO15693 protocol. Note: The THM3060 supports only single subcarrier mode, but does not supports the dual subcarrier mode.
INDEX100：The modulation index was set to 100% or 10% ~30%.
C_1_256: Set data format of the ISO15693 protocol. The baud rates of data transfer are about 1.65KBPS in 1/256 coding format and 26.48KBPS in 1/4 coding format.
When SPUL=1 and the THM3060 enters the sending and receiving process (START = 1), the THM3060 will send an EOF only. In the some cases of ISO15693 protocol, sending an EOF is needed to acquire response of card.

5.1.2.14 PWTH for Type-A

DATA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
function			Set the pulse width under TYPE-A protocol. This register defines the width of the modulation pulse according to Wpause= (PWTH +1) / fc. The default value and the valid bit of the PWTH register changes with the baud rates. The bit0 to bit5 are valid at 106KBPS. The default value is 0x27. The bit0 to bit4 are valid at 212KBPS. The default value is 0x14. The bit0 to bit3 are valid at 424KBPS. The default value is 0x0b. The bit0 to bit2 are valid at 848KBPS. The default value is 0x07.					
Reset value	0	0	0x27					

Figure 37 PWTH register for TYPE-A standard

6 Data buffer

6.1 Buffer operation mechanism

The THM3060 has 512-byte built-in internal buffer. The external microprocessor writes data to data buffer via digital interface (SPI, UART) before THM3060 transmits data. The THM3060 counts during writing process automatically and then start to write data to the buffer from address 0x00. The number of bytes should not exceed 512.
The receiving process will be entered automatically after transmitting data, the counter will be cleared, and then THM3060 stores receiving data from address 0x00 (note: transmitting data will be overwritten). After receiving process, the external microprocessor can read receiving data from the data buffer.

6.2 Writing data

The external microprocessor writes data to internal buffer by using a SPI or UART frame as its unit. The address increases automatically. The addresses are not visible, but can be cleared by the SCON.PTCLR register. The external microprocessor writing data to the DATA register is equivalent to writing to data buffer.

6.3 Reading data

The external microprocessor reads data from address 0x00 in the internal buffer by using a SPI or UART frame as its unit. Reading data from the DATA register is equivalent to reading from data buffer.

6.4 Using data buffer

1) SCON.PTCTR =1. Clear the buffer.
2) SCON.PTCLR =0. Data buffer works.
3) Write data to the DATA register. (count automatically)
4) Start the transmitting and receiving process (SCON.START =1).
5) Judge the value of the RSTAT register and the RSC register.
6) Read data from DATA register.

7 Interruption signal

The THM3060 has IRQ pin to output the interruption signal. The external microprocessor can use the IRQ as an external interrupt input.

7.1 Related registers

RSTAT and INTCON are related to the IRQ. The RSTAT.IRQ register indicates internal interruption signal. The INTCON.INTEN register indicates whether the interruption signal output to the IRQ pin. The INTCON.INTLEVEL indicates the interruption active level.

RSTAT.IRQ	INTCON.INTEN	INTCON.INTLEVEL	IRQ pin
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure 38 IRQ output control

8 Internal timer

The THM3060 has a built-in receiving timer to set FWT and FDT. The receiving timer starts automatically after transmitting data. The value of RSTAT.TMROVER will be set to 1 if no response received by the THM3060 when timeout.

8.1 Related registers

The TMRH, TMRL, CRCSEL.TMREN and RSTAT.TMROVER registers relate to the internal timer.
The TMRH and TMRL registers are used to set the maximum response time and which unit is 302μs.
Tmax = 302 × TMRmax = 302 × 65535 = 19791570μs ≈ 20s
The timer is enabled when CRCSEL.TMREN = 1, and disabled when CRCSEL.TMREN = 0.
RSTAT.TMROVER = 1, which indicates a timeout exception. That is to say, the card doesn't response or card processing is not completed.

8.2 Use the internal timer

The card processing time is due to commands. So adjust waiting time of the THM3060 during a transaction is necessary. For example: the responding time of REQB according to TYPE-B protocol is less than 302μs. But some other commands just like writing EEPROM may need hundreds of milliseconds. It's not a better way to use a fix waiting time in different cases.

8.3 Start or stop timer

The Timer will start automatically after transmitting and stop after a card response. The timer will stop immediately when SCON.START=0 or CRCSEL.TMREN=0. And the transmitting and receiving process will also stop when SCON.START=0.

9 Transmitting circuit

9.1 Diagram of transmitting circuit

The THM3060 doesn't have the built-in power amplifier, so the external power amplifier is necessary, see Figure 38. The RF_CLK pin outputs 13.56MHz carrier signal, which will drive the 50ohm antenna (one side connect with GND, another side connect with ANTA) after being amplified by the power amplifier. RF-TXD drives the external circuit to modulate the amplitude of the carrier, and RF_TXD is to output the waveform of transmitting data. Adjusting the R5 resistor can change modulation index[5]. The usage of 'D1' in the figure is to adjust the modulation waveform instead of 'R5' at higher baud rates. The 'D1' is not necessary at 106KBPS and 212KBPS mode.

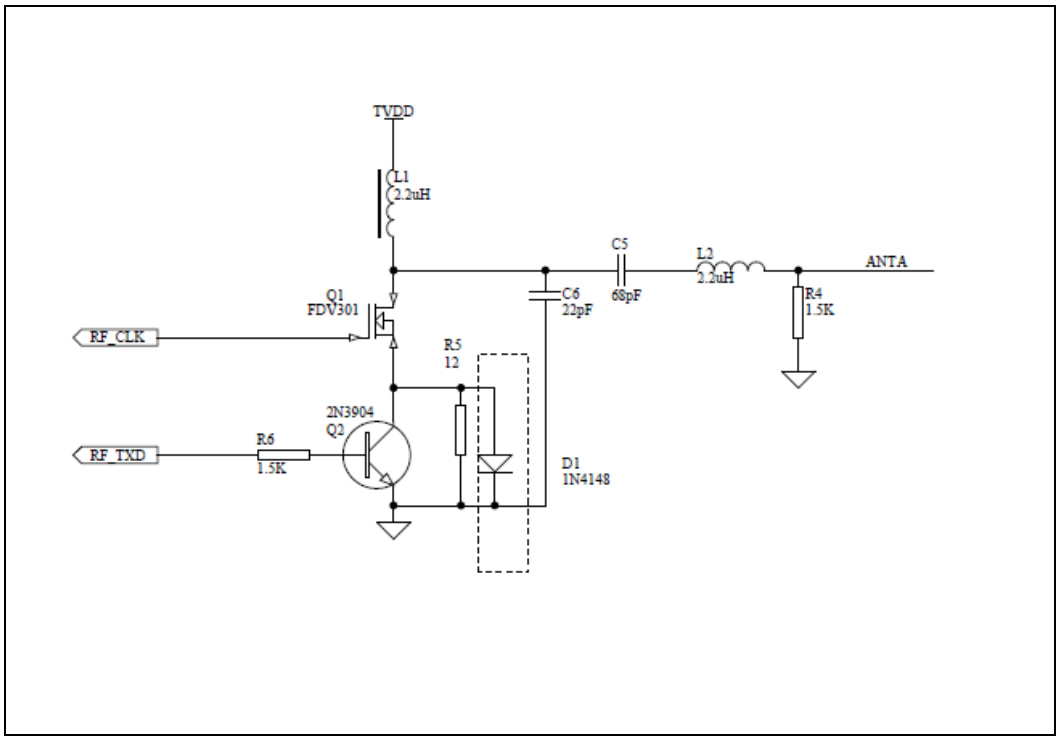


Figure 39 Diagram of transmitting circuit

9.2 Waveform of transmitting circuit

[5] The modulation index is 7%~14% as regulated by ISO/IEC14443, and the adjustment of R5 may lead to that the modulation index exceeds this range.

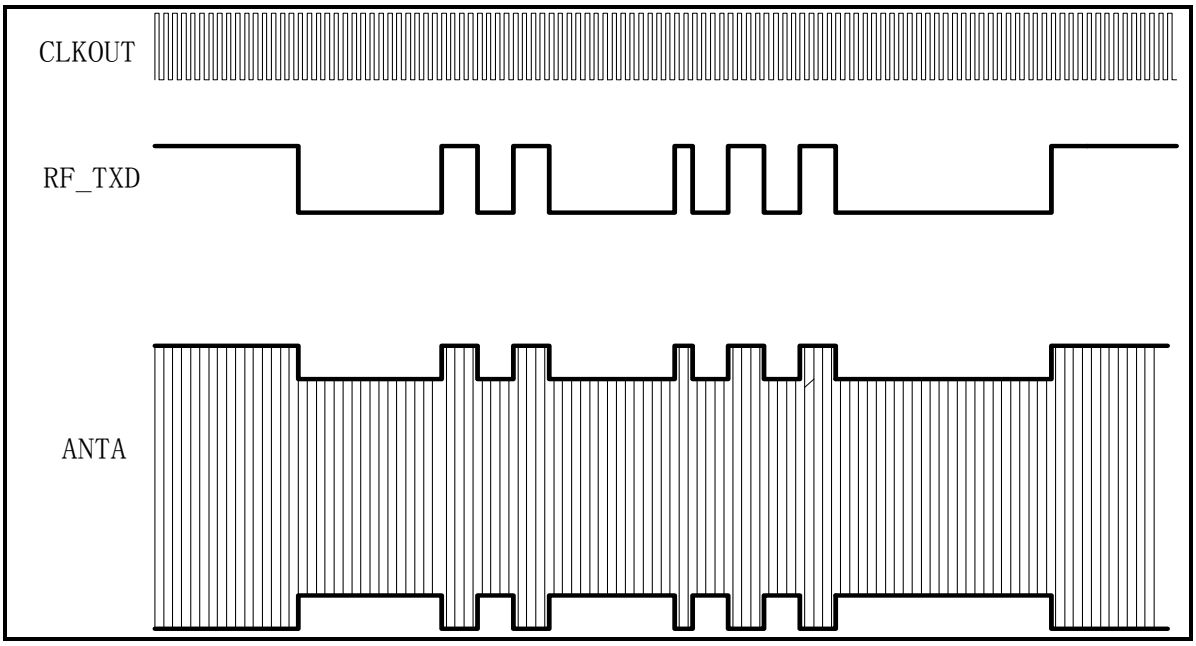


Figure 40 Waveform of transmitting circuit（TYPE-B）

10 Receiving circuit

The THM3060 has built-in receiving amplifying circuit and digital demodulation circuit that can amplify, digitally demodulate and decode the receiving data received from the card. The data of the card can be directly demodulated, decoded and stored in internal RAM except under the transparent mode. Under the transparent interface mode, the card's data waveform should be demodulated through the external microprocessor. The receiving circuit's input pin is the detection input signal pin AIN. The diode detector as shown in Figure 40 should be used. The positive pole (ANTA) of 'D1' is directly connected with one end of the antenna. Note: when the voltage of the transmitting circuit is larger than 5V, the voltage of AIN may exceed the limit of AVDD-0.7, and in this case the voltage-dividing circuit showed in Figure 41 should be used. R4 and R5 should be selected according to the actual voltage value.

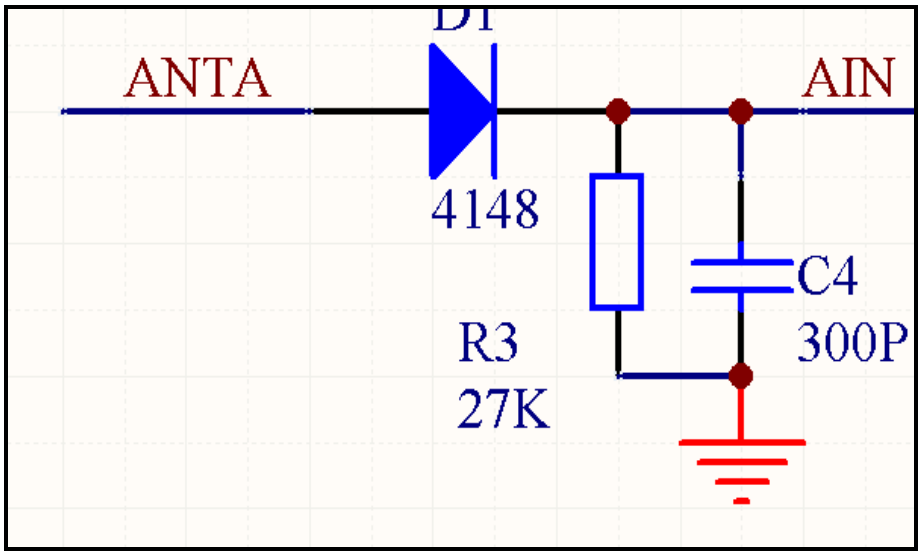


Figure 41 Detector circuit 1 (No partial voltage)

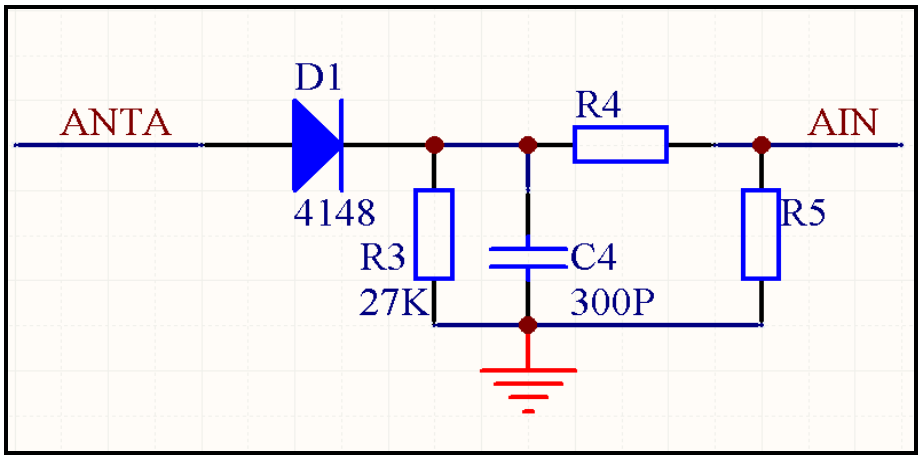


Figure 42 detector circuit（partial voltage）

11 Transmitting and receiving process

11.1 Initialization process

1) Set the RF protocol (default: ISO14443-B) and baud rate (default: 106KBPS) of the PSEL register.
2) Set the FCONB register. The default value can fulfill the normal requirement.
3) Set the CRCSEL register whether to encode CRC automatically and whether to enable time-out detection.
4) Set the TMR if time-out detection is enabled.

11.2 Turn on the RF carrier

5) Set SCON.CARRYON=1 to turn on the RF carrier.

11.3 Writing data

6) SCON.PTCTR =1. Clear the data buffer.
7) SCON.PTCLR =0. Data buffer works.
8) Write data to the DATA register. (count automatically）

11.4 Start transmitting data

9) Set SCON.START = 1

11.5 Wait for receiving complete

10) Waiting for IRQ signal generated by the IRQ pin or RSTAT.IRQ=1.

11.6 Judging the state

11) judging the receiving result according to the RSTAT register.。

11.7 Read receiving data

12) Read receiving data in data buffer according to the value of the RSC register if data is valid.

12 TYPE-A protocol application

12.1 Short frame

The ISO14443 TYPE-A standard has defined some kinds of short frame. The THM3060 identifies short frame automatically[6].

b6	b5	b4	b3	b2	b1	b0	Meaning
0	1	0	0	1	1	0	'26' = REQA
1	0	1	0	0	1	0	'52' = WUPA
0	1	1	0	1	0	1	'35' = Optional timeslot method, see Annex C
1	0	0	x	x	x	x	'40' to '4F' = Proprietary
1	1	1	1	x	x	x	'78' to '7F' = Proprietary
All other values							RFU

Figure 43 Coding of Short Frame

The THM3060 identifies all single-byte commands as a short frame and will not send CRC.

12.2 Anti-collision

Bit oriented anti-collision frames shall only be used during bit frame anti-collision loops under the ISO14443-A standard. The THM3060 provides a complete procedure to complete the anti-collision process.

For example: there are two cards in the working field with the UID: 0A223344 and 0A2A5566.

UID0								UID1								UID2								UID3							
0A								22								33								44							
0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	1	0
0A								2A								55								66							
0	1	0	1	0	0	0	0	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0
MSB							LSB	MSB							LSB	MSB							LSB	MSB							LSB

Figure 44 anti-collision diagram (LSB first)

1) The THM3060 shall transmit SEL and NVB(9320)
2) The two cards in field shall respond with their complete UID: 0A223344 and 0A2A5566. The first collision occurs at bit3 (at the second byte and then the THM3060 will quit the receiving

[6] The LSB is b1 in ISO/IEC14443 protocol. In this document, the LSB is b0.

process. Now the second byte is 0x02 and RSTAT.CERR=1. BITPOS register will be 0x03. Then the value of RSC register is 0x02. The data in internal buffer are 0A02.

3) The THM3060 sends “93 34 0A 02” (34: The upper 4 bits are called “Byte count” and specify the integer part of the number of all valid data bits transmitted by the THM3060 (including SEL and NVB) divided by 8. The lower 4 bits are called “bit count” and specify the number of all valid data bits transmitted by the THM3060 (including SEL and NVB) modulo 8.)
4) The card 1 responds with its remaining bits of UID. The card 2 does not respond.
5) The THM3060 composes bit0~bit3 bits of 0x02 and received bit4~bit7 bits to a complete byte 0x22. The remaining bytes are 33 44.
6) The RSC register is 3. The THM3060 shall read data 22 33 44 and constitute a complete UID with the last frame 0A.
7) The THM3060 sends 93 70 0A 22 33 44 （SELECT command） and selects card 1.

To operate card 2, the THM3060 should sends 93 34 0A 0A at step 3. Then the card 2 responds its remaining UID.

12.3 CRC encoding under TYPE-A standard

The TYPE A standard restricted the CRC of special frame (doesn’t including standard frame). The THM3060 judge special frame automatically. The operation of special frame is independent of the CRCSEL register.

Frame Types	commands	CRC encoding
Short frame	REQA ，WUPA and so on，refer to 12.1	Doesn’t encoding
Bit oriented anti-collision frame	93，95，97 and so on (except 9370, 9570 and 9770).	Doesn’t encoding
Standard frame	Other frames except short frame and bit oriented anti-collision frame.	According to the CRCSEL register.

Figure 45 CRC encoding

12.4 Change the baud rates

The THM3060 supports different baud rates (106K, 212K, 424K and 848K) communication according to the ISO14443-A protocol. Different baud rates between transmitting and receiving can be supported by set the PSEL register.
Note: baud rates setting should base on card requirements.

12.5 PAUSE width setting

Setting The PWTH register can change the width of PAUSE. The transmitting data format of TYPE-A is “Modified Miller”.

It's recommended that using the default setting because the default value has already according with the ISO/14443-A standard.

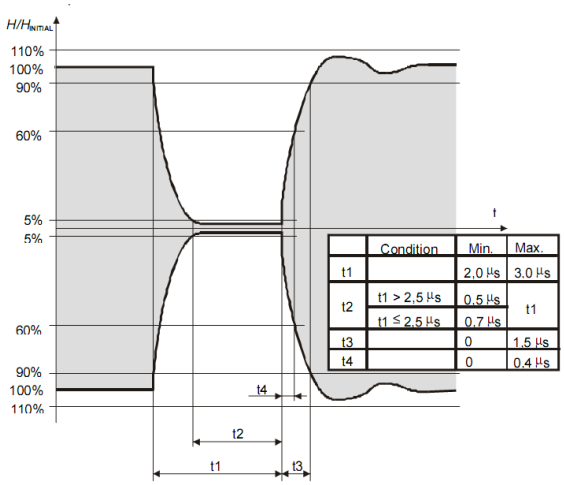


Figure 46 PAUSE[7]

12.6 Transmitting and receiving process

1) Set the protocol by the PSEL register (TYPE-A)
2) Set the CRCSEL register (generate CRC automatically)
3) Set the TMR register
4) Open the RF carrier (SCON)
5) Writing data (refer to Chapter 6:data buffer)
6) Start sending (SCON)
7) Judging the receiving state (RSTAT)
8) Reading data (refer to Chapter 6:data buffer)

Note: Pause can be set by the PWTH register[8].

[7] Refer to the ISO/IEC14443 standard
[8] THM3060 doesn't support dual-subcarrier. Please use single-subcarrier under the ISO/IEC15693 standard.

13 TYPE-B standard application

13.1 Baud rates setting

The THM3060 supports different baud rates (106KBPS, 212KBPS, 424KBPS and 848KBPS) communication according to the ISO14443-B standard. Different baud rates between transmitting and receiving can be supported by set the PSEL register.
Note: baud rates setting should base on the card requirement.

13.2 Frame format setting

Frame format can be changed by setting FCONB and EGT register. It's recommended that using the default setting because the default value is according with the ISO/14443-A standard.

13.3 Transmitting and receiving process

1) Set the protocol by the PSEL register (TYPE-B)
2) Set the CRCSEL register (generate CRC automatically)
3) Set the TMR register
4) Turn on the RF carrier (SCON)
5) Writing data（refer to Chapter 6:data buffer）
6) Start transmitting（SCON）
7) Judging the receiving state（RSTAT）
8) Reading data (refer to Chapter 6:data buffer)

Note: data format and baud rates can be changed by the FCONB, EGT and PSEL registers

14 ISO15693 standard application

14.1 Anti-collision process

The ISO15693 protocol supports two kinds of SLOT anti-collision (SLOT=1 and SLOT=16). When there are several cards in field, SLOT=16 (refer to the ISO/IEC15693 standard).
Now we descript the case only when SLOT=1.
Suppose there are two cards inside with its UID1 (F0946512000007E0) and UID2 (F096124567897823).

THM3060 commands	The card response
240100 CRC Inventory command	0000 F0946512000007E0 CRC （card 1） 0000 F096124567897823 CRC （card 2） Two cards respond simultaneously. the first collision occurs at bit1 at the second byte of UID
THM3060 received 0000F000 RSTAT.CERR =1, BITPOS = 1，indicates that collision occurred at bit1 at the last byte (2nd byte). Therefore, anti-collision value of the UID mask byte is 8 +2 = 10 (0x0A)	
THM3060 sends 24010AF000 CRC	0000 F0946512000007E0 CRC （card 1） The lower UID bit 0x0A corresponds to 0xF000. Therefore, card 1 responds only. Only card 2 responds If the THM3060 sends 24010AF002

14.2 Baud rates setting

The transmission rates depend on encoding scheme according to the ISO15693 protocol. The user can set the SMOD register to select coding format 1/256 and 1/4. The baud rates of data transfer are about 1.65KBPS with 1/256 coding format and 26.48KBPS with 1/4 coding format.

Receiving data rates depend on sending commands under the ISO15693[9]. There are two speed modes: high speed mode with 26.48KBPS and low speed mode with 6.62KBPS.

The THM3060 can set the sending rate only by the SMOD register. The sending rate is irrelevant to the PSEL register.

14.3 Transmitting and receiving process

1) Set the protocol by the PSEL register (ISO15693)
2) Set the CRCSEL register (generate CRC automatically)
3) Set the TMR register
4) Turn on the RF carrier (SCON)
5) Writing data（refer to Chapter 6:data buffer）
6) Start transmitting（SCON）
7) Judging the receiving state（RSTAT）
8) Reading data (refer to Chapter 6:data buffer)

Note: data format can be set by the SMOD register [10]。

[9] Refer to the ISO/IEC15693 standard

[10] THM3060 doesn't support dual-subcarrier. Please use single-subcarrier commands when using the ISO/IEC15693 standard.

15 Clock circuit

The THM3060 has built-in clock circuit with external crystal. The XTAL2 pin output CLK signal. The XTAL1 pin input CLK signal when using the external crystal. The circuit stops when STANDBY=1.

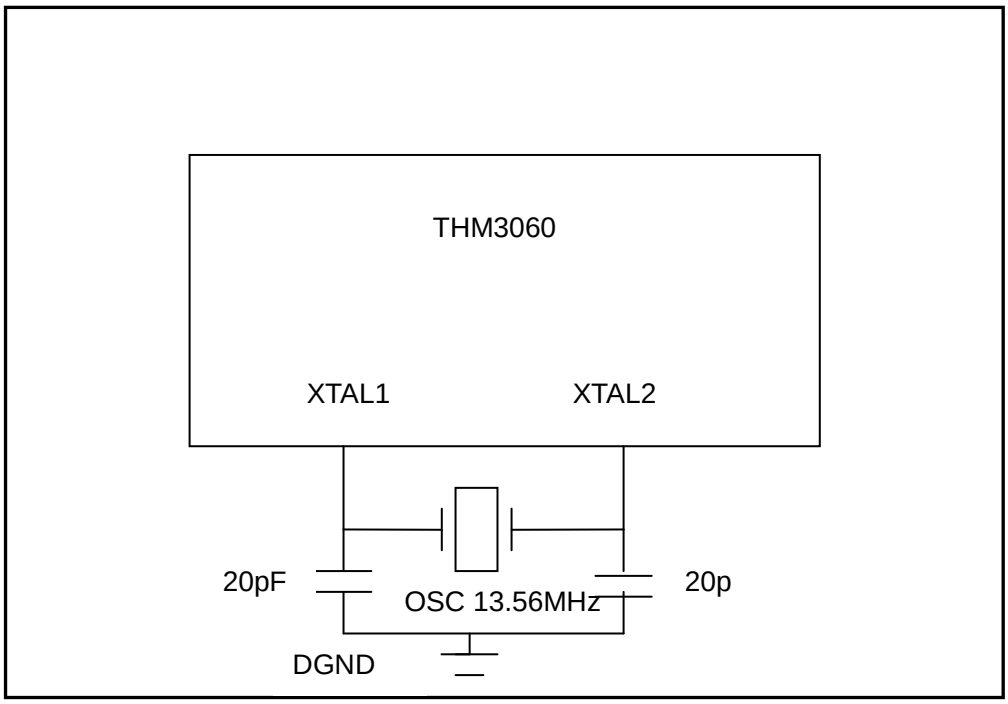


Figure 47 Clock circuit

16 Reset circuit

The THM3060's reset signal RSTN is active low, and the pulse width should exceed 5ms. The reset pin RSTN has pull-up resistor with a value of about 20KΩ. External circuit can be connected to reset the THM3060. An external capacitor can be used as power on reset.

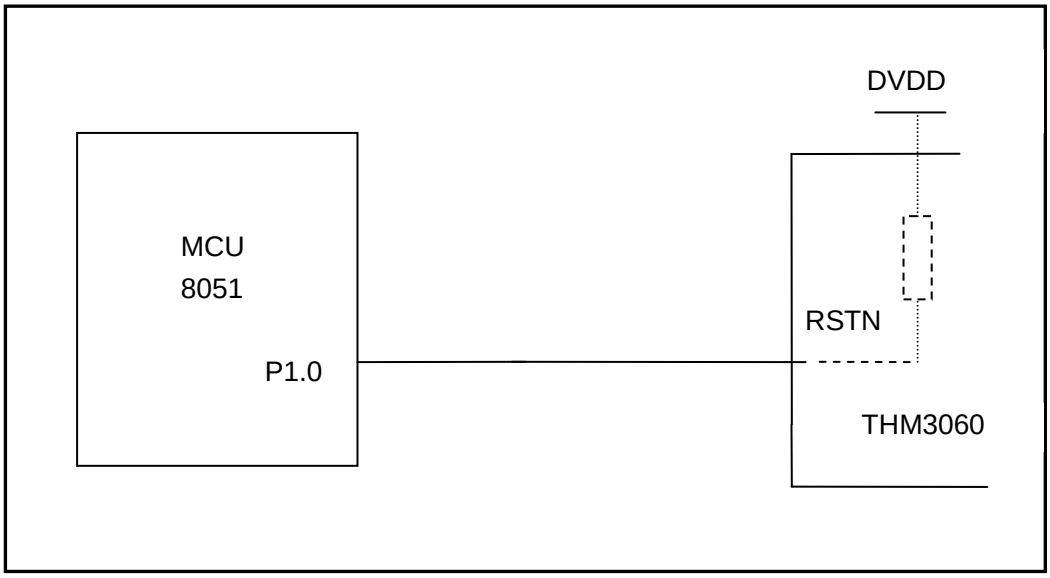


Figure 48 Reset circuit (reset via external controller）

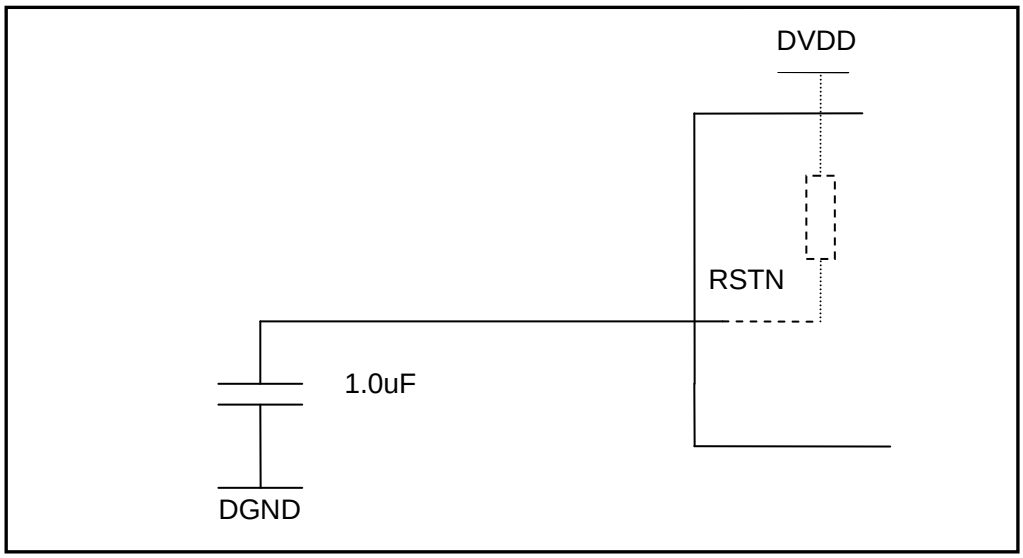


Figure 49 Reset circuit (power on reset)

17 Standby mode

The THM3060 enters standby mode when the standby pin is high level. In this mode, IO1, IO2, IO3 and IO4 input with internal weak pull-up. RFTXD and RFCLK maintain low and the internal clock circuit is closed.

17.1 Pin mode processing

Reducing power consumption to less than 10μA is useful in some applications. The leakage current of the MOD1 and the MOD0 pin will be 250μA due to the weak pull-up inside.
To resolve this problem, connected MOD1, MOD0 to standby can reduce the leakage of the STANDBY mode.

	SPI	UART	transparent
The pins connected with the standby pin	MOD1 MOD0	MOD1	MOD0

Figure 50 the pins connected with standby

17.2 The requirements of the external microprocessor

After the THM3060 enters standby mode, the pins connected with the standby pin should be set as figure 50.

Pins	Treatment
MOD1	Maintain high or output high resistance[11]
MOD0	Maintain high or output high resistance
IO1	Maintain high or output high resistance
IO2	Maintain high or output high resistance
IO3	Maintain high or output high resistance
IO4	Maintain high or output high resistance
IRQ	Consist with the THM3060 output
RSTN	Maintain high or output high resistance
STANDBY	Maintain high or output high resistance

Figure 51 state of the pins under standby mode

[11]Because pull-up resistor is inside the THM3060, the peripheral control unit can output high level or resistance to set the THM3060 pins high.

18 Electrical characteristics

18.1 Operating Condition Range

Symbol	Parameter	Conditions	MIN	MAX	UNIT
DVDD	Digital Supply Voltage	AGND = DGND =0V	3.0	5.5	V
AVDD	Analog Supply Voltage[12]	AGND = DGND= 0V	3.0	5.5	V
TA	Ambient Temperature	--	-40	50	˚C
tR	Digital Signal Input Rising Time	--		40	ns
tF	Digital Signal Input Falling Time	--		40	ns

Figure 52 Operating Condition Range

18.2 Absolute Maximum Ratings

Symbol	Parameter	Conditions	MIN	MAX	UNIT
DVDD	Digital Supply Voltage	DGND = 0V	-0.75	5.75	V
AVDD	Analog Supply Voltage	AGND = 0V	-0.75	5.75	V
VI	Input Voltage	DGND=AGND=0V	-0.75	5.75	V
IO	Output Current	RFTXD,RFCLK	-30	30	mA
		Other Pins	-10	10	mA
TSTG	Storage Temperature	No power supply bias	-85	150	˚C
TA	Ambient Temperature	Power supply bias available	-65	135	˚C

Figure 53 Absolute Maximum Ratings

[12] AVDD can work at 5V, but optimum voltage is at 3~3.6V.

18.3 DC Characteristics

The value in the table is effective under normal operation with temperate between 0˚C and 50˚C.

Symbol	Parameter	Conditions	MIN	MAX	UNIT
VIL	Input Low Voltage	DVDD = 3.3~5V	0	0.3*DVDD	V
VIH	Input High Voltage	DVDD=3.3~5V	0.7*DVDD	5.5	V
VOL	Output Low Voltage	IOL = 1.8mA , DVDD=5V	0.4	2.0	V
VOH	Output High Voltage	IOH = -1.8mA , DVDD=5V	VDD-1.0	5	V
ILI	Input Leakage Current	VI = -0.5~5.5V	-5	5	μA
CIO	I/O pin capacitance	f = 1.0MHz, TA = 25˚C		5	pF
Symbol	Parameter	Conditions	MIN	MAX	UNIT
IDD	Supply current	Normal mode, AVDD=DVDD=5V	20	30	mA
		Normal mode, AVDD=DVDD=3.3V	12	20	mA
		Standby mode, AVDD= DVDD=5V	5	9	μA
		Standby mode, AVDD= DVDD=3.3V	3	5	μA
		Normal mode, Including external transmission circuit AVDD=TVDD[13]=DVDD =5V	90	100	mA
		Normal mode, Including external transmission circuit AVDD=TVDD=DVDD =3.3V	60	70	mA

Figure 54 DC Characteristics

18.4 AC Characteristics

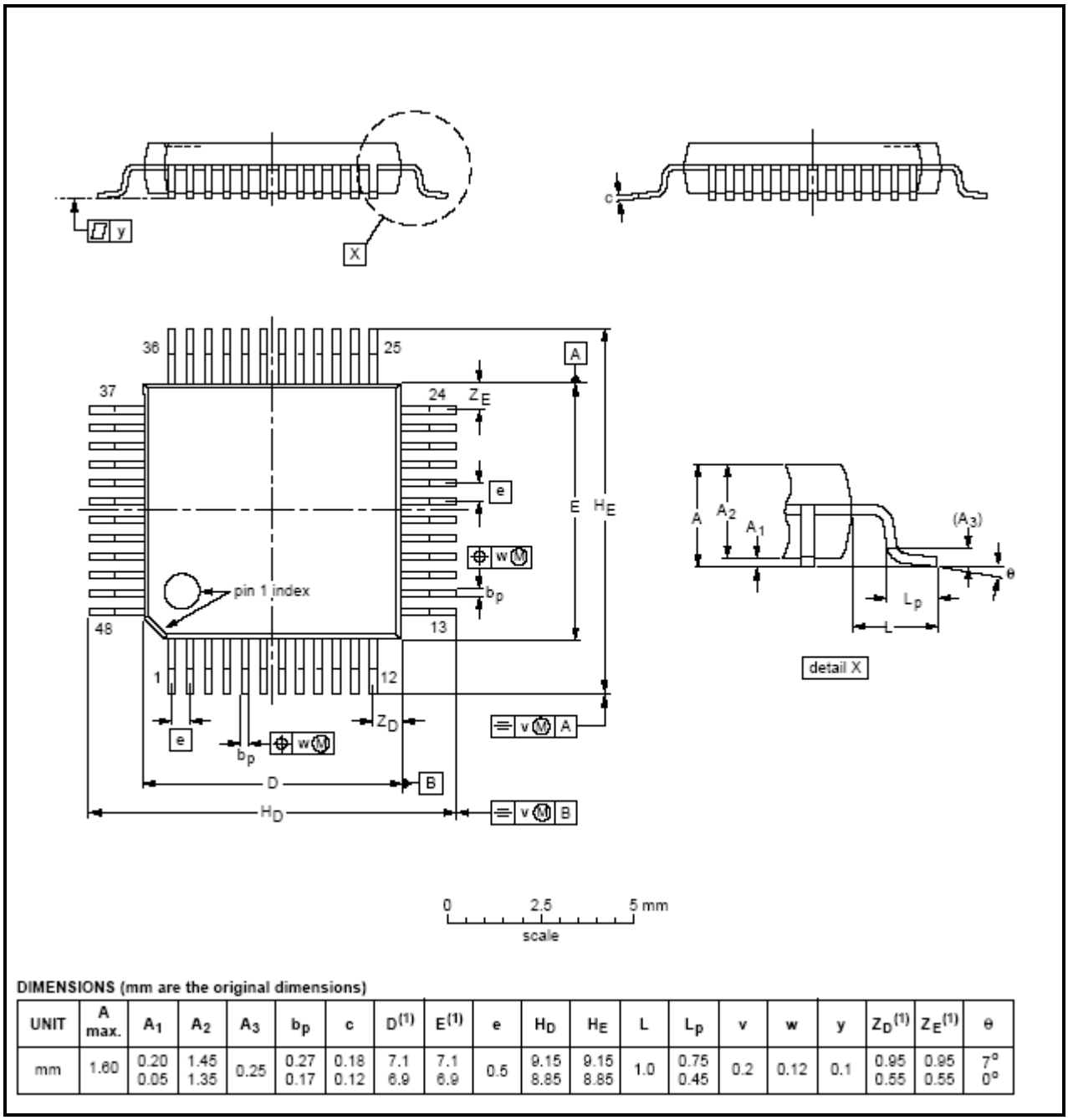
In normal mode (refer to figure 38, power supply are 5V)

Symbol	**Parameter**	**MIN**	**MAX**	**UNIT**
fosc	Clock Frequency	13.553	13.567	MHz
t1	RF closing time	1.0	2.0	μs
t2	RF opening time	1.0	1.5	μS

Figure 55 AC Characteristics

[13] TVDD is the power supply of external RF amplifier

19 Package （LQFP48）



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Figure 56 package diagram

20 Typical application

20.1 Power supply connection

There are three types of power supply in The THM3060 application circuit: TVDD is the power supply of amplifier circuit, AVDD is analog signal power supply and DVDD is digital signal power supply. When using 3.3V power supply, you can connect AVDD and DVDD together. TVDD can be connected to either 3.3V or other voltages such as 5V. Higher TVDD can get higher RF power output.

Note that, some component parameters may require appropriate changes when TVDD increases to make sure THM3060 working in the voltage range[14] . TGND, AGND and DGND should be connected together.

It's recommended those three block power layouts are designed for TVDD, AVDD, and DVDD. The three blocks connect to power supply separately using star-like mode. The TVDD should be nearing the output of power supply. Refer to Figure 56. For double layer printed circuit board design, filling the gap between components with copper connected to GND is preferred.

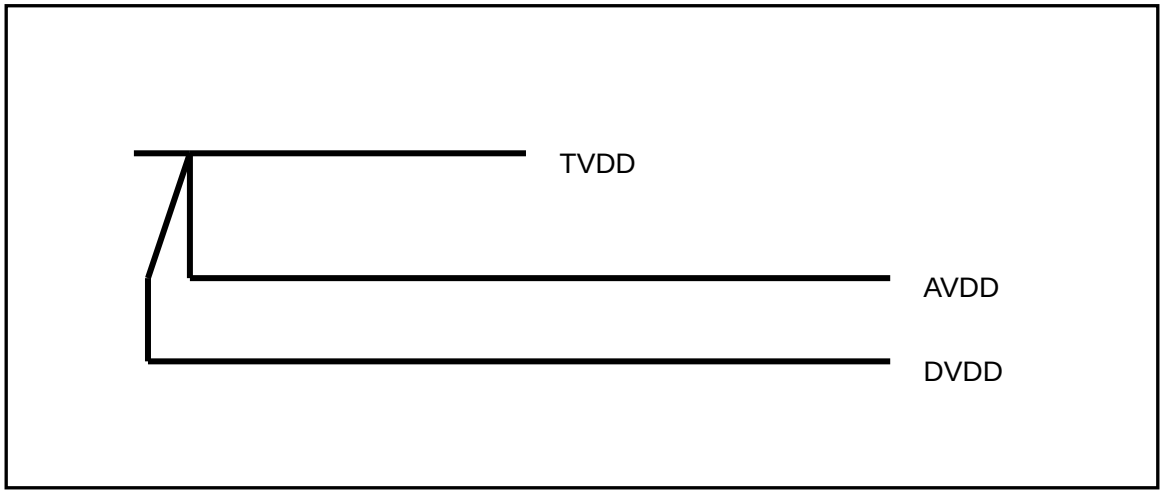


Figure 57 power supply connection diagram（TVDD =AVDD=DVDD=3V）

20.2 Transparent mode

The TRD input transmitting data and the RCD output card receiving data when THM3060 is working at "transparent" mode. You can select RF protocol (TYPE-A, TYPE-B or ISO15693) by setting SEL1 and SEL0.

When STANDBY is high, the THM3060 enters standby mode. When STANDBY is low, the THM3060 switches to normal mode.

[14] Parameters provided in this manual meets TVDD 3~5V applications.

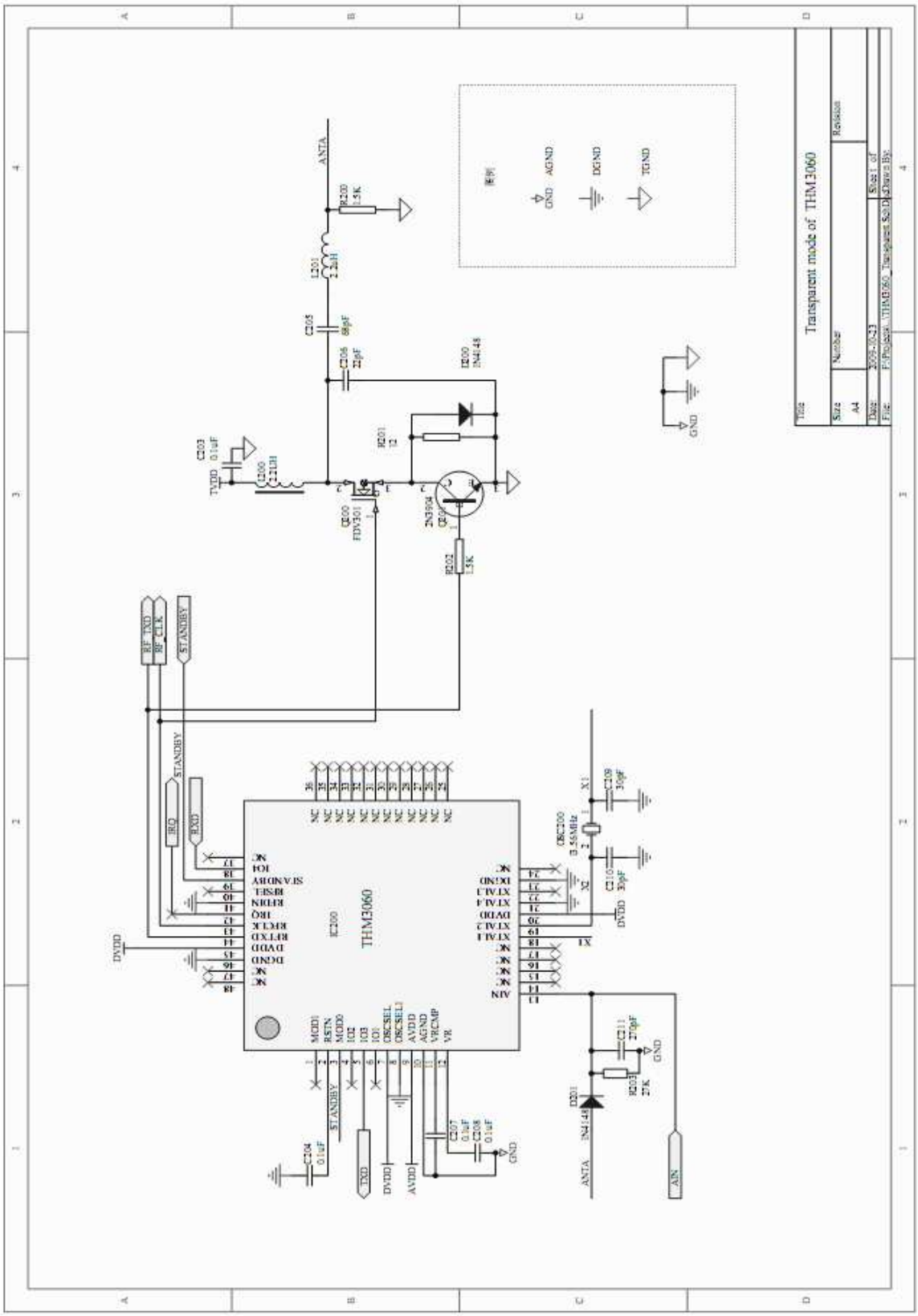


Figure 58 transparent interface mode diagram

20.3 SPI interface mode

The THM3060 are slave device in SPI mode. The MOSI, MISO, SS_N, SCLK pins can be connected via SPI interface or I/O pins of the external microprocessor.

SPI master can connect with multiple slaves. That is to say, one master can control several slave devices simultaneity. The THM3060 also can be connected as follow:

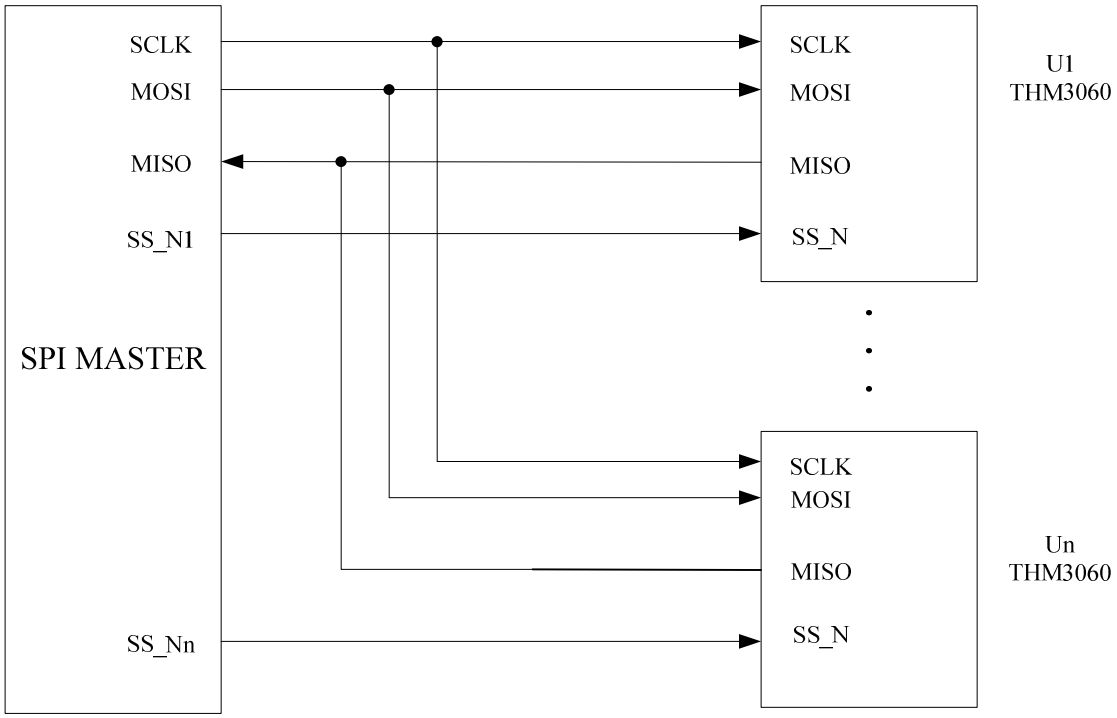


Figure 59 multi THM3060 interface connection diagram

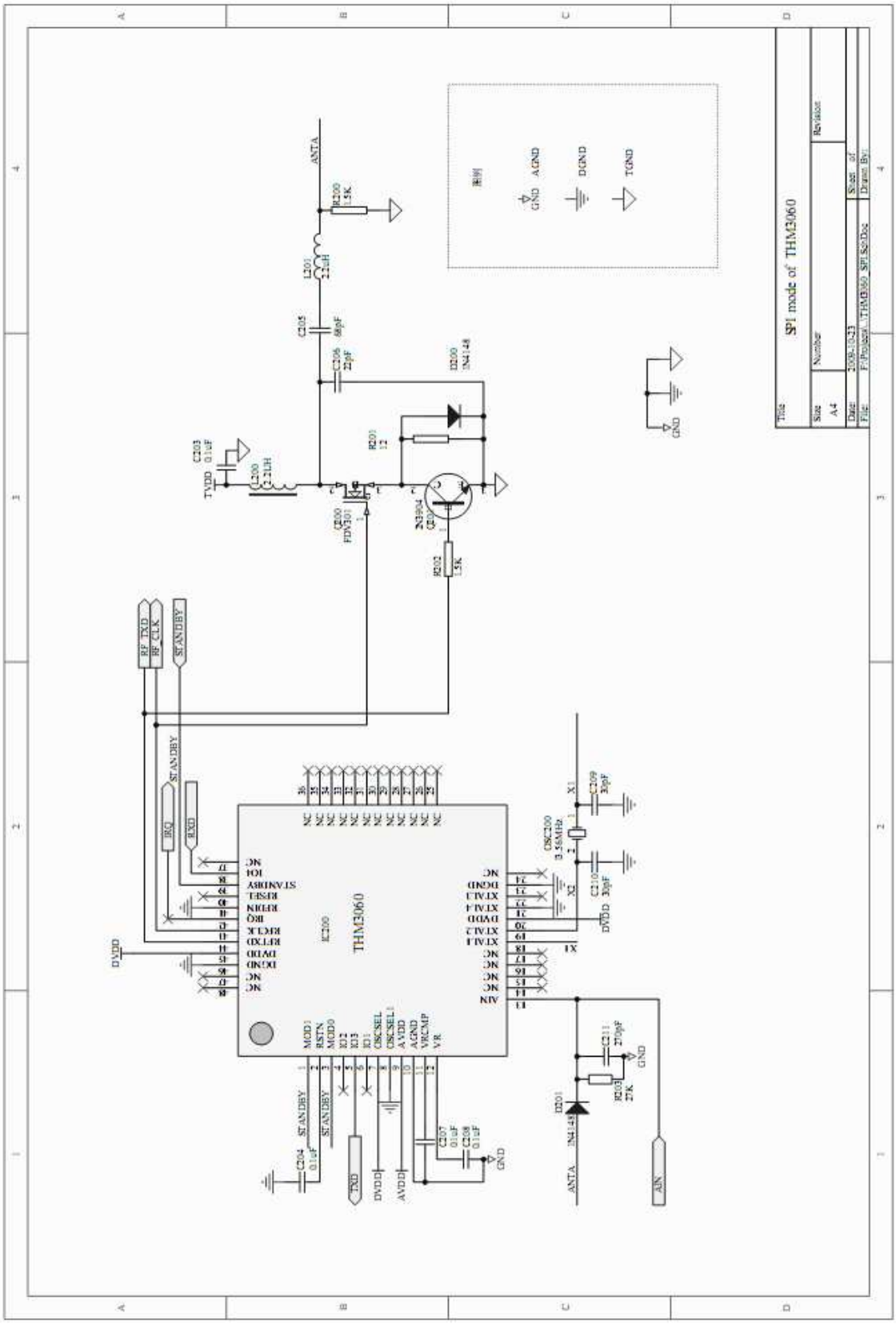


Figure 60 SPI interface mode application diagram

20.4 UART interface mode

The THM3060 can connect to PC via RS232-TTL level conversion device such as MAX232 in the UART interface mode. At this mode, the external microprocessor can be removed from the Reader circuits.

Similarly, the THM3060 can connect with a microprocessor with serial port. Note that, the THM3060 only supports 115200BPS baud rates with no parity, 8 bit data and 1 stop bit data format.

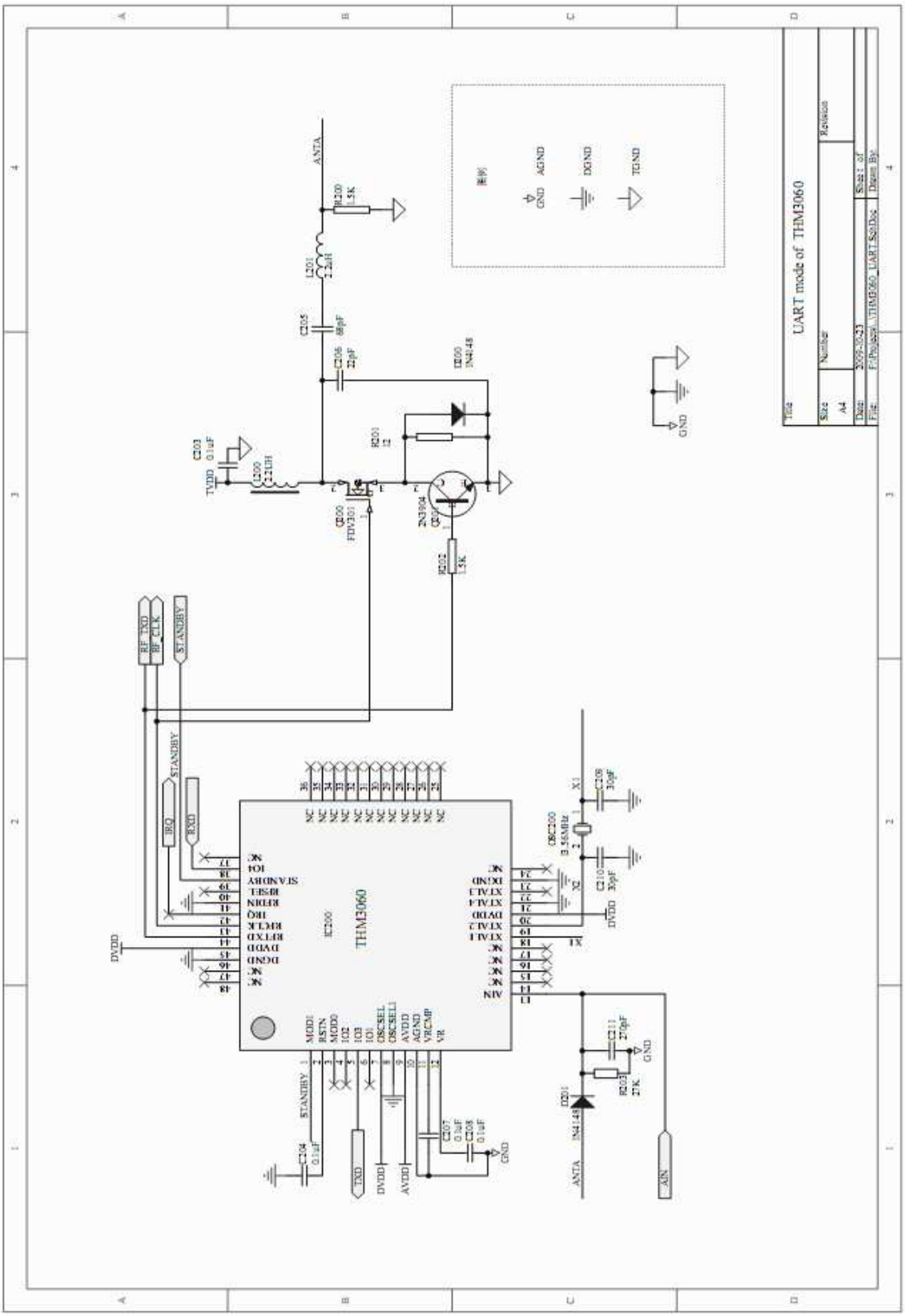


Figure 61 UART interface application diagram