Shanghai Fudan Microelectronics Group Company Limited

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FM17550
Contactless Transceiver IC

Short Datasheet

Oct. 2016

Trademarks

Contents

1 Product Overview

1.1 Introduction

The FM17550 is a highly integrated Transceiver IC for Contactless communication at 13.56MHz. The FM17550 Transceiver IC support Reader/Writer mode supporting ISO/IEC 14443A/B protocal.
The FM17550's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC14443A/B cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC14443A/B compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A/B framing and error detection. The FM17550 supports ISO/IEC14443A cards and transponders with transfer speeds from 106kbit/s to 424kbit/s in both directions. And can supports all layers of the ISO/IEC14443B reader/writer communication scheme, and provided that stardardized protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443B anticollision are correctly implemented.

1.2 Features

- **Supports ISO/IEC 14443A/M1 reader/writer mode**
- **Supports ISO/IEC 14443B reader/writer mode**
- **ISO/IEC14443A 106kbit/s and higher transfer speed at 212kbit/s and 424kbit/s**
- **Typical operating distance in reader/writer mode for communication to a ISO/IEC 14443A card up to 50mm (depending on the antenna size and tuning)**
- **Supports host interfaces**
  - SPI interface up to 10Mbit/s
  - I2C interface up to 400kbit/s in Fast Mode , and up to 3400kbit/s in High Speed Mode
  - Serial UART in different transfer speeds up to 1228.8kbit/s, framing according to the RS232 interface with voltage levels according pad voltage supply
- **Comfortable 64 byte send and receive FIFO-buffer**
- **Flexible interrupt modes**
- **Multiple low-power modes**
  - Soft power down mode
  - Hard power down mode
  - Deep power down mode （typical 1uA）
- **Low Power external Card Detect (LPCD) at Reader/writer mode**
- **Programmable timer**
- **Internal oscillator to connect 27.12MHz quartz**
- **Wide voltage supply: 2.2V ~ 3.6V**
- **Dedicated transmitter voltage supply up to 5.5V**
- **Integrated CRC Co-processor**
- **Programmable I/O pins**

1.3 Pinning information

1.3.1 QFN32 Pinning Assignment

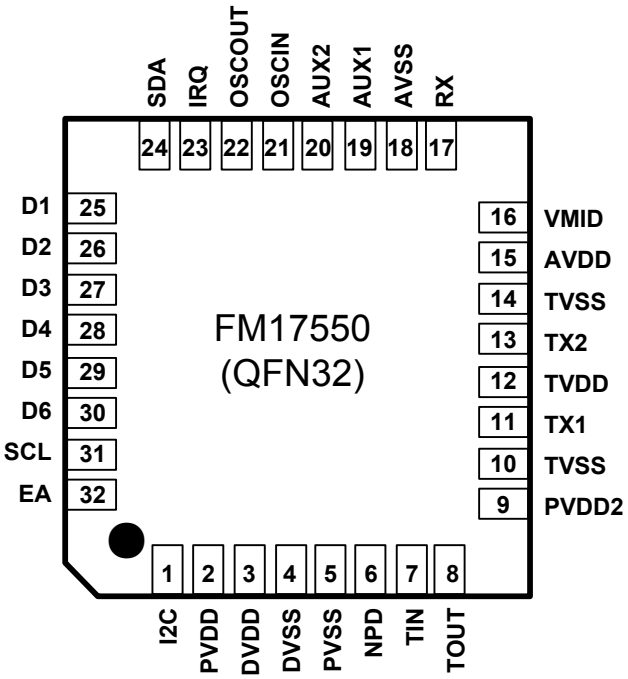

Fig 1-1 FM17550 QFN32 Pinning assignment

1.3.2 Pin description

Pin	Symbol	Type	Description
1	I2C	I	I2C-bus enable pin
2	PVDD	P	pin power supply
3	DVDD	P	chip power supply
4	DVSS	G	digital ground
5	PVSS	G	pin ground
6	NPD	I	power-down input, active low, reset chip when positive edge on NPD pin
7	TIN	I	test input
8	TOUT	O	test output
9	PVDD2	P	pin power supply for TIN and TOUT pin
10	TVSS	G	transmitter output 1 ground
11	TX1	O	transmitter 1 modulated 13.56MHz energy carrier output
12	TVDD	P	transmitter power supply
13	TX2	O	transmitter 2 modulated 13.56MHz energy carrier output
14	TVSS	G	transmitter output 2 ground
15	AVDD	P	analog power supply
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground

Pin	Symbol	Type	Description
19	AUX1	O	auxiliary outputs for test
20	AUX2	O	auxiliary outputs for test
21	OSCIN	I	crystal oscillator input; also input for externally generated clock (27.12MHz)
22	OSCOUT	O	crystal oscillator output
23	IRQ	O	interrupt request output, indicates an interrupt event
24	SDA	IO	I2C-bus serial data line input/output
	NSS	I	SPI signal input
	URX	I	UART input
25	D1	IO	test port
	ADR5	I	I2C-bus address 5 input
26	D2	IO	test port
	ADR4	I	I2C-bus address 4 input
27	D3	IO	test port
	ADR3	I	I2C-bus address 3 input
28	D4	IO	test port
	ADR2	I	I2C-bus address 2 input
29	D5	IO	test port
	ADR1	I	I2C-bus address 1 input
	SCK	I	SPI serial clock input
	DTRQ	O	UART request to send output to microcontroller
30	D6	IO	test port
	ADR0	I	I2C-bus address 0 input
	MOSI	I	SPI master out, slave in
	MX	O	UART output to microcontroller
31	SCL	I	I2C-bus clock input/output
	MISO	O	SPI master in, slave out
	UTX	O	UART data output to microcontroller
32	EA	I	external address input for coding I2C-bus address

Table 1-1 FM17550 QFN32 PIN description

2 Characteristics

2.1 Limiting Values

Parameter	最小值	最大值	单位
AVDD,DVDD,PVDD,PVDD2	-0.5	4.0	V
TVDD	-0.5	6.0	V
ESD (HBM)		2K	V
ESD (CDM)		500	V

Table 2-1 FM17550 Limiting values

2.2 Reference Data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A	Working temperature		-40		+85	°C
AVDD	Analog supply voltage		2.2	3.0	3.6	V
DVDD[1]	Digital supply voltage		2.2	3.0	3.6	V
TVDD[2]	Transmitter supply voltage		2.2	3.0	5.5	V
PVDD[3]	Pin supply voltage		1.7		3.6	V
PVDD2[4]	Test pin supply voltage		1.7		3.6	V
I_{DPD}	Deep power-down current	AVDD=DVDD=TVDD=PVDD=3V NPD=0, enter DPD		1	10	uA
I_{HPD}	Hard power-down current (register retention)	AVDD=DVDD=TVDD=PVDD=3V NPD=0 , enter HPD		2	12	uA
I_{SPD}	Soft power-down current	AVDD=DVDD=TVDD=PVDD=3V enter SPD mode		35	60	uA
I_{LPCD}[6]	LPCD current	AVDD=DVDD=TVDD=PVDD=3V enter LPCD mode		2	6	uA
I_{AVDD}	analog supply current	AVDD=3V, receiver switched on		10	13	mA
		AVDD=3V, receiver switched off		6	8	mA
I_{TVDD}[5]	TVDD supply current	continuous wave V_{TVDD} =3.0V		60	100	mA

Table 2-2 FM17550 Reference data

[1] AVDD and DVDD must always be the same voltage.
[2] TVDD must always be the same or higher voltage than AVDD.
[3] PVDD must always be the same or lower voltage than AVDD.
[4] PVDD2 is better the same voltage with PVDD
[5] I_{TVDD} depends on TVDD and the external circuit connected to pins TX1 and TX2.
[6] I_{LPCD} in Tab2-2 is the current of LPCD-T1 stage. The actual average current of LPCD mode depend on the configurations of LPCD mode.
[7] I_{DPD}、I_{HPD}、I_{SPD}、I_{LPCD} is the total current for all supplies.

3 Ordering information

Device number	Package	Wrap	Operating Environment
FM17550-QNA-A-G	QFN32	tray	(-40℃ ~ +85℃)

Revision history

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Feb.2015	11		initial version
1.1	Jul.2015	11		modify reference data
1.2	Nov.2015	11		modify reference data
1.3	Oct.2016	10		Change PIN31 name from D7 to SCL

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