PSoC 4100/4200 Family

PSoC® 4 Registers TRM
(Technical Reference Manual)

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Register Mapping

The Register Mapping section discusses the registers and lists all the registers in mapping tables, in address order. For Architecture details, refer to PSoC 4100/4200 Family PSoC 4 Architecture Technical Reference Manual (TRM).

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Description	Explanation
RW	Read/Write	These bits can be both read and written.
R	Read only	These bits can only be read. Writing has no effect on the bit value.
W	Write only	These bits can only be written. Reading the bit returns the reset value.
RW1C	Read/Write '1' to clear	These bits can be read as well as cleared by writing '1'. Writing '0' has no effect on the bit value.
RW0C	Read/Write '0' to clear	These bits can be read as well as cleared by writing '0'. Writing '1' has no effect on the bit value.
RW1S	Read/Write '1' to set	These bits can be read as well as set by writing '1'. Writing '0' has no effect on the bit value.
None / Reserved	Reserved bits	Keep these bits at the default value
'x' in a register /bit field name	Multiple instances	Multiple instances/address ranges of the same register/bit field

Acronyms

This table lists the acronyms used in this document

Table 1-1. Acronyms

Symbol	Unit of Measure
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
API	application programming interface
APOR	analog power-on reset
BC	broadcast clock
BOM	bill of materials
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CAN	controller area network
CI	carry in
CMP	compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check

Table 1-1. Acronyms

Symbol	Unit of Measure
CSD	CapSense sigma delta
CT	continuous time
CTBm	continuous time block-mini
DAC	digital-to-analog converter
DC	direct current
DI	digital or data input
DMA	direct memory access
DNL	differential nonlinearity
DO	digital or data output
DSI	digital signal interface
DSM	deep-sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMIF	external memory interface
FB	feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
L2CAP	logical link control and adaptation protocol
LPCOMP	low-power comparator
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit

Table 1-1. Acronyms

Symbol	Unit of Measure
MSB	most significant byte
PC	program counter
PCH	program counter high
PCL	program counter low
PD	power down
PGA	programmable gain amplifier
PM	power management
PMA	PSoC memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSoC®	Programmable System-on-Chip
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SIE	serial interface engine
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SRSS	system resources sub-system
SROM	supervisory read only memory
SSADC	single slope ADC
SSC	supervisory system call
SYSCLK	system clock
SWD	single wire debug
TC	terminal count
TD	transaction descriptors
UART	universal asynchronous receiver/transmitter

Table 1-1. Acronyms

Symbol	Unit of Measure
UDB	universal digital block
USB	universal serial bus
USBIO	USB I/O
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset
XRES_N	external reset, active low

1 Cortex-M0 Registers

This section discusses the Cortex-M0 (CM0) registers. It lists all the registers in mapping tables, in address order.

1.1 Register Details

Register Name	Address
CM0_DWT_PID4	0xE0001FD0
CM0_DWT_PID0	0xE0001FE0
CM0_DWT_PID1	0xE0001FE4
CM0_DWT_PID2	0xE0001FE8
CM0_DWT_PID3	0xE0001FEC
CM0_DWT_CID0	0xE0001FF0
CM0_DWT_CID1	0xE0001FF4
CM0_DWT_CID2	0xE0001FF8
CM0_DWT_CID3	0xE0001FFC
CM0_BP_PID4	0xE0002FD0
CM0_BP_PID0	0xE0002FE0
CM0_BP_PID1	0xE0002FE4
CM0_BP_PID2	0xE0002FE8
CM0_BP_PID3	0xE0002FEC
CM0_BP_CID0	0xE0002FF0
CM0_BP_CID1	0xE0002FF4
CM0_BP_CID2	0xE0002FF8
CM0_BP_CID3	0xE0002FFC
CM0_SYST_CSR	0xE000E010
CM0_SYST_RVR	0xE000E014
CM0_SYST_CVR	0xE000E018
CM0_SYST_CALIB	0xE000E01C
CM0_ISER	0xE000E100
CM0_ICER	0xE000E180
CM0_ISPR	0xE000E200
CM0_ICPR	0xE000E280
CM0_IPR	0xE000E400

Register Name	Address
CM0_CPUID	0xE000ED00
CM0_ICSR	0xE000ED04
CM0_AIRCR	0xE000ED0C
CM0_SCR	0xE000ED10
CM0_CCR	0xE000ED14
CM0_SHPR2	0xE000ED1C
CM0_SHPR3	0xE000ED20
CM0_SHCSR	0xE000ED24
CM0_SCS_PID4	0xE000EFD0
CM0_SCS_PID0	0xE000EFE0
CM0_SCS_PID1	0xE000EFE4
CM0_SCS_PID2	0xE000EFE8
CM0_SCS_PID3	0xE000EFEC
CM0_SCS_CID0	0xE000EFF0
CM0_SCS_CID1	0xE000EFF4
CM0_SCS_CID2	0xE000EFF8
CM0_SCS_CID3	0xE000EFFC
CM0_ROM_SCS	0xE00FF000
CM0_ROM_DWT	0xE00FF004
CM0_ROM_BPU	0xE00FF008
CM0_ROM_END	0xE00FF00C
CM0_ROM_CSMT	0xE00FFFCC
CM0_ROM_PID4	0xE00FFFD0
CM0_ROM_PID0	0xE00FFFE0
CM0_ROM_PID1	0xE00FFFE4
CM0_ROM_PID2	0xE00FFFE8
CM0_ROM_PID3	0xE00FFFEC
CM0_ROM_CID0	0xE00FFFF0
CM0_ROM_CID1	0xE00FFFF4
CM0_ROM_CID2	0xE00FFFF8
CM0_ROM_CID3	0xE00FFFFC

1.1.1 CM0_DWT_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0001FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default Value: 4

1.1.2 CM0_DWT_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0001FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default Value: 10

1.1.3 CM0_DWT_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0001FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default Value: 176

1.1.4 CM0_DWT_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0001FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default Value: 11

1.1.5 CM0_DWT_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0001FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default Value: 0

1.1.6 CM0_DWT_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0001FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default Value: 13

1.1.7 CM0_DWT_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0001FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default Value: 224

1.1.8 CM0_DWT_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0001FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default Value: 5

1.1.9 CM0_DWT_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0001FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default Value: 177

1.1.10 CM0_BP_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0002FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default Value: 4

1.1.11 CM0_BP_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0002FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default Value: 11

1.1.12 CM0_BP_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0002FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default Value: 176

1.1.13 CM0_BP_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0002FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default Value: 11

1.1.14 CM0_BP_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0002FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default Value: 0

1.1.15 CM0_BP_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0002FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default Value: 13

1.1.16 CM0_BP_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0002FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default Value: 224

1.1.17 CM0_BP_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0002FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default Value: 5

1.1.18 CM0_BP_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0002FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default Value: 177

1.1.19 CM0_SYST_CSR

Systick Control & Status

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CM0_CLKSOURCE	CM0_TICKINT	CM0_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							CM0_COUNTFLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	CM0_COUNTFLAG	Indicates whether the counter has counted to 0 since the last read of this register: 0 timer has not counted to 0. 1 timer has counted to 0. COUNTFLAG is set to 1 by a count transition from 1 to 0. COUNTFLAG is cleared to 0 by a read of this register, and by any write to the Current Value register. Default Value: 0
2	CM0_CLKSOURCE	Indicates the SysTick clock source: 0 SysTick uses the optional external reference clock. 1 SysTick uses the processor clock. If no external clock is provided, this bit reads as one and ignores writes. Default Value: 0

1.1.19 CM0_SYST_CSR (continued)

1	CM0_TICKINT	Indicates whether counting to 0 causes the status of the SysTick exception to change to pending: 0 count to 0 does not affect the SysTick exception status. 1 count to 0 changes the SysTick exception status to pending. Changing the value of the counter to 0 by writing zero to the SysTick Current Value register to 0 never changes the status of the SysTick exception. Default Value: 0
0	CM0_ENABLE	Indicates the enabled status of the SysTick counter: 0 counter is disabled. 1 counter is operating. Default Value: 0

1.1.20 CM0_SYST_RVR

Systick Reload Value

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CM0_RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CM0_RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CM0_RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CM0_RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X

1.1.21 CM0_SYST_CVR

SysTick Current Value

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CM0_CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CM0_CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CM0_CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CM0_CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

1.1.22 CM0_SYST_CALIB

SysTick Calibration Value

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CM0_TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CM0_TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CM0_TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	None	RW	None					
Name	CM0_NOREF	CM0_SKEW	None [29:24]					

Bits	Name	Description
31	CM0_NOREF	Indicates whether the IMPLEMENTATION DEFINED reference clock is provided: 0 the reference clock is implemented. 1 the reference clock is not implemented. When this bit is 1, the CLKSOURCE bit of the SYST_CSR register is forced to 1 and cannot be cleared to 0. Default Value: 0
30	CM0_SKEW	Indicates whether the 10ms calibration value is exact: 0 10ms calibration value is exact. 1 10ms calibration value is inexact, because of the clock frequency. Default Value: X
23 : 0	CM0_TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is zero, the calibration value is not known. Default Value: X

1.1.23 CM0_ISER

Interrupt Set-Enable Register

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	CM0_SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	CM0_SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	CM0_SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	CM0_SETENA [31:24]							

Bits	Name	Description
31 : 0	CM0_SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.24 CM0_ICER

Interrupt Clear Enable Register

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRENA [31:24]							

Bits	Name	Description
31 : 0	CM0_CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.25 CM0_ISPR

Interrupt Set-Pending Register

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	CM0_SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	CM0_SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	CM0_SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	CM0_SETPEND [31:24]							

Bits	Name	Description
31 : 0	CM0_SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.26 CM0_ICPR

Interrupt Clear-Pending Register

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CM0_CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CM0_CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

1.1.27 CM0_IPR

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	CM0_PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	CM0_PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	CM0_PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	CM0_PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	CM0_PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	CM0_PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	CM0_PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	CM0_PRI_N0	Priority of interrupt number N. Default Value: 0

1.1.28 CM0_CPUID

CPUID Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	None				None			
Name	CM0_PARTNO [7:4]				CM0_REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	None				None			
Name	CM0_VARIANT [23:20]				CM0_CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	CM0_IMPLEMENTER	Implementer code for ARM. Default Value: 65
23 : 20	CM0_VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii. Default Value: 0
19 : 16	CM0_CONSTANT	Indicates the architecture, ARMv6-M Default Value: 12
15 : 4	CM0_PARTNO	Indicates part number, Cortex-M0 Default Value: 3104
3 : 0	CM0_REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p0. Default Value: 0

1.1.29 CM0_ICSR

Interrupt Control State Register

Address: 0xE000ED04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CM0_VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	CM0_VECTPENDING [15:12]				None [11:9]			CM0_VECTACTIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	CM0_ISRPREEMPT	CM0_ISRPENDING	None	CM0_VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	CM0_NMIPENDSET	None [30:29]		CM0_PENDSVSET	CM0_PENDSVCLR	CM0_PENDSTSETb	CM0_PENDSTCLR	None

Bits	Name	Description
31	CM0_NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	CM0_PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICT-ABLE. Default Value: 0
27	CM0_PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	CM0_PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
25	CM0_PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0

1.1.29 CM0_ICSR (continued)

23	CM0_ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0
22	CM0_ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	CM0_VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	CM0_VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

1.1.30 CM0_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					CM0_SYSRESETREQ	CM0_VECTCLRACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	None	None						
Name	CM0_ENDIANNESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CM0_VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CM0_VECTKEY [31:24]							

Bits	Name	Description
31 : 16	CM0_VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UNPREDICTABLE. Readback value is UNKNOWN. Default Value: X
15	CM0_ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default Value: 0
2	CM0_SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information. Default Value: 0
1	CM0_VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. Default Value: 0

1.1.31 CM0_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			CM0_SEVONPEND	None	CM0_SLEEPDEEP	CM0_SLEEPONEXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	CM0_SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information. Default Value: 0
2	CM0_SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default Value: 0
1	CM0_SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information. Default Value: 0

1.1.32 CM0_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None				None	None		
Name	None [7:4]				CM0_UNALIGN_TRP	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None						None	None
Name	None [15:10]						CM0_STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	CM0_STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	CM0_UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

1.1.33 CM0_SHPR2

System Handler Priority Register 2

Address: 0xE000ED1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	CM0_PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	CM0_PRI_11	Priority of system handler 11, SVCall Default Value: 0

1.1.34 CM0_SHPR3

System Handler Priority Register 3

Address: 0xE000ED20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	CM0_PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	CM0_PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	CM0_PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	CM0_PRI_14	Priority of system handler 14, PendSV Default Value: 0

1.1.35 CM0_SHCSR

System Handler Control and State Register

Address: 0xE000ED24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	CM0_SVCALLPENDED	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CM0_SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default Value: 0

1.1.36 CM0_SCS_PID4

System Control Space ROM Table Peripheral ID #4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default Value: 4

1.1.37 CM0_SCS_PID0

System Control Space ROM Table Peripheral ID #0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default Value: 8

1.1.38 CM0_SCS_PID1

System Control Space ROM Table Peripheral ID #1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default Value: 176

1.1.39 CM0_SCS_PID2

System Control Space ROM Table Peripheral ID #2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default Value: 11

1.1.40 CM0_SCS_PID3

System Control Space ROM Table Peripheral ID #3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default Value: 0

1.1.41 CM0_SCS_CID0

System Control Space ROM Table Component ID #0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default Value: 13

1.1.42 CM0_SCS_CID1

System Control Space ROM Table Component ID #1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default Value: 224

1.1.43 CM0_SCS_CID2

System Control Space ROM Table Component ID #2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default Value: 5

1.1.44 CM0_SCS_CID3

System Control Space ROM Table Component ID #3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default Value: 177

1.1.45 CM0_ROM_SCS

CM0 CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Offset to SCS ROM Table Default Value: 4293980163

1.1.46 CM0_ROM_DWT

CM0 CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Offset to DWT ROM Table Default Value: 4293926915

1.1.47 CM0_ROM_BPU

CM0 CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Offset to BPU ROM Table Default Value: 4293931011

1.1.48 CM0_ROM_END

CM0 CoreSight ROM Table End Marker

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	End marker in peripheral list Default Value: 0

1.1.49 CM0_ROM_CSMT

CM0 CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Memory Type Default Value: 1

1.1.50 CM0_ROM_PID4

CM0 CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default Value: 4

1.1.51 CM0_ROM_PID0

CM0 CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default Value: 113

1.1.52 CM0_ROM_PID1

CM0 CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default Value: 180

1.1.53 CM0_ROM_PID2

CM0 CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default Value: 11

1.1.54 CM0_ROM_PID3

CM0 CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default Value: 0

1.1.55 CM0_ROM_CID0

CM0 CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default Value: 13

1.1.56 CM0_ROM_CID1

CM0 CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default Value: 16

1.1.57 CM0_ROM_CID2

CM0 CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default Value: 5

1.1.58 CM0_ROM_CID3

CM0 CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CM0_VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CM0_VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CM0_VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CM0_VALUE [31:24]							

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default Value: 177

2 CPU Sub-System Registers

This section discusses the CPU Sub-System (CPUSS) registers. It lists all the registers in mapping tables, in address order.

2.1 Register Details

Register Name	Address
CPUSS_CONFIG	0x40000000
CPUSS_SYSREQ	0x40000004
CPUSS_SYSARG	0x40000008
CPUSS_INTR_SELECT	0x40000020

2.1.1 CPUSS_CONFIG

CPU Subsystem Configuration

Address: 0x40000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CPUSS_FLSH_ACC_BYPASS	CPUSS_VECS_IN_RAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CPUSS_FLSH_ACC_BYPASS	0: Normal operation 1: Flash Accellerator in bypass mode, functions as single 64b line buffer. Default Value: 0
0	CPUSS_VECS_IN_RAM	0: Vector Table is located at 0000_0000 in Flash 1: Vector Table is located at 2000_0000 in RAM Note that vectors for RESET and FAULT are always fetched from ROM. Value in Flash/RAM is ignored for these vectores. Default Value: 0

2.1.2 CPUSS_SYSREQ

System Request Register

Address: 0x40000004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CPUSS_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CPUSS_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	R	RW	RW	None		
HW Access	R	RW	RW	R	R	None		
Name	CPUSS_SYSREQ	CPUSS_HMASTER	CPUSS_ROM_ACCESS_EN	CPUSS_PRIVILEGED	CPUSS_NO_RST_OVR	None [26:24]		

Bits	Name	Description
31	CPUSS_SYSREQ	Firmware/ATE writes 1 to request a system call. This will lead to an immediate NMI (non mask-able interrupt). System call implementation will write 0 after servicing the request. Default Value: 0
30	CPUSS_HMASTER	0: Request was made by Cortex-M0 CPU firmware 1: Request was made by external debugger/ATE probe Note that any writes to this register while SYSREQ=1 will not change the value of HMASTER (such that the origin of a request can continue to be observed). Default Value: 0
29	CPUSS_ROM_ACCESS_EN	Indicates that access to ROM is currently enabled. This bit is used for debug purposes only. Default Value: 1
28	CPUSS_PRIVILEGED	Indicates whether the system is in privileged or user mode. This bit can only be set from ROM code. Any write to this register that is not originating from ROM will result in clearing this bit. Default Value: 1

2.1.2 CPUSS_SYSREQ (continued)

27	CPUSS_NO_RST_OVR	Disable Reset Vector fetch relocation: 0: CPU requests to locations 0000_0000 - 0000_0007 are redirected to SROM 1: CPU requests to locations 0000_0000 - 0000_0007 are made to flash. Note that this bit defaults to 0 on reset, ensuring actual reset vector fetches are always made to ROM . Default Value: 0
15 : 0	CPUSS_COMMAND	Opcode of the system call being requested. Default Value: 0

2.1.3 CPUSS_SYSARG

System Request Argument Register

Address: 0x40000008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CPUSS_ARG32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CPUSS_ARG32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CPUSS_ARG32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CPUSS_ARG32 [31:24]							

Bits	Name	Description
31 : 0	CPUSS_ARG32	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default Value: 0

2.1.4 CPUSS_INTR_SELECT

Interrupt Multiplexer Select Register

Address: 0x40000020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CPUSS_SELECT32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CPUSS_SELECT32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CPUSS_SELECT32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CPUSS_SELECT32 [31:24]							

Bits	Name	Description
31 : 0	CPUSS_SELECT32	When bit is set, NVIC IRQ is connected to DSI. Default Value: 0

3 CapSense Sigma-Delta Registers

This section discusses the CapSense Sigma-Delta (CSD) registers. It lists all the registers in mapping tables, in address order.

3.1 Register Details

Register Name	Address
CSD_ID	0x40080000
CSD_CONFIG	0x40080004
CSD_IDAC	0x40080008
CSD_COUNTER	0x4008000C
CSD_STATUS	0x40080010
CSD_INTR	0x40080014
CSD_INTR_SET	0x40080018

3.1.1 CSD_ID

ID & Revision Number

Address: 0x40080000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	CSD_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	CSD_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	CSD_REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	CSD_REVISION [31:24]							

Bits	Name	Description
31 : 16	CSD_REVISION	the version number is 0x0001 Default Value: 1
15 : 0	CSD_ID	the ID of CSD peripheral is 0xE0E1 Default Value: 57569

3.1.2 CSD_CONFIG

Configuration and Control

Address: 0x40080004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW1S	None			RW	RW
HW Access	R	R	RW1C	None			R	R
Name	CSD_PRS_12_8	CSD_PRS_SELECT	CSD_PRS_CLEAR	None [4:2]			CSD_SAMPLE_SYNC	CSD_DSI_SAMPLE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW		RW
HW Access	R	R	R	R	R	R		R
Name	CSD_COMP_PIN	CSD_COMP_MODE	CSD_REFBUF_EN	CSD_SENSE_EN	CSD_SENSE_COMP_BW	CSD_SHIELD_DELAY [10:9]		CSD_DSI_SENSE_EN

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	None	RW	RW	RW	RW
HW Access	R	R	R	None	R	R	R	R
Name	CSD_REFBUF_DRV	CSD_SENSE_INSEL	CSD_REBUF_OUTSEL	None	CSD_SENSE_COMP_EN	CSD_MUTUAL_CAP	CSD_POLARITY2	CSD_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW			None	RW
HW Access	R	R	R	R			None	R
Name	CSD_ENABLE	CSD_DDFTCOMP	CSD_ADFTEN	CSD_DDFTSEL [28:26]			None	CSD_REFBUF_DRV

Bits	Name	Description
31	CSD_ENABLE	Master enable of the CSD IP. Must be set to 1 for any CSD operation to function. Default Value: 0
30	CSD_DDFTCOMP	Reserved. Keep this bit at default value Default Value: 0
29	CSD_ADFTEN	Reserved. Keep this bit at default value Default Value: 0
28 : 26	CSD_DDFTSEL	Reserved. Keep this bit at default value Default Value: 0
24 : 23	CSD_REFBUF_DRV	Current drive strength for reference buffer. Default Value: 0

3.1.2 CSD_CONFIG (continued)

		0x0: OFF: Current drive mode OFF **0x1: DRV_1:** Lowest current drive mode **0x2: DRV_2:** Mid current drive mode **0x3: DRV_3:** Highest current drive mode
22	CSD_SENSE_INSEL	Selects how to connect the sensing comparator to the Cmod capacitor. Default Value: 0 **0x0: SENSE_CHANNEL1:** Use the Channel 1 sense line to conenct to Cmod. **0x1: SENSE_AMUXA:** Use the AMUXBUS-A bus to connect to Cmod.
21	CSD_REBUF_OUTSEL	Selects which AMUXBUS the reference buffer connects to. Default Value: 1 **0x0: AMUXA:** Connect to AMUXBUS-A (not normally used). **0x1: AMUXB:** Connect to AMUXBUS-B (normally used for all CSD operations).
19	CSD_SENSE_COMP_EN	Turns on the sense comparator circuit. Must be done some time before enable SENSE_EN. 0: Sense comparator is powered off. 1: Sense comparator is powered on. Default Value: 0
18	CSD_MUTUAL_CAP	Enables mutual cap sensing mode Default Value: 0 **0x0: SELFCAP:** Self-cap mode (configure sense line as CSD_SENSE) **0x1: MUTUALCAP:** Mutual-cap mode (configure Tx line as CSD_SENSE, Rx Line as AMUXA)
17	CSD_POLARITY2	For normal CSD operations this field is not used. When using the IDAC's for other-than-CSD purposes, this bit controls the IDAC2 polarity only. Default Value: 0 **0x0: VSSIO:** Normal: switch between Vssio and Cmod. For non-CSD application, IDAC2 will source current. **0x1: VDDIO:** Inverted: switch between Vddio and Cmod. For non-CSD application, IDAC2 will sink current.
16	CSD_POLARITY	Selects the polarity of the sensing operation. When using the IDAC's for other-than-CSD purposes, this bit controls the IDAC1 polarity only. Default Value: 0 **0x0: VSSIO:** Normal: switch between Vssio and Cmod. For non-CSD application, IDAC1 will source current. **0x1: VDDIO:** Inverted: switch between Vddio and Cmod. For non-CSD application, IDAC1 will sink current.

3.1.2 CSD_CONFIG (continued)

15	CSD_COMP_PIN	Connects either the Cmod or Csh_tank sense return line to the reference buffer comparator. This switch must be set to the same pin that is being charged up by the reference buffer (through the AMUXBUS settings in GPIO). Default Value: 0 **0x0: CHANNEL1:** Use the sense line designated as "Channel 1"; this is normally used to conenct Cmod. **0x1: CHANNEL2:** Use the sense line designated as "Channel 2"; this is normally used to connect Csh_tank.
14	CSD_COMP_MODE	Selects between charging of the Cmod/Csh_tank capacitor using the GPIO digital output buffer or the CSD reference buffer. Note that using the GPIO requires proper configuraiton of the GPIO pin. Default Value: 0 **0x0: CHARGE_BUF:** Use CSD Reference Buffer to charge capacitor. Capacitor must be connected to AMUXBUS-A/B (see REBUF_OUTSEL) and selected using COMP_PIN. **0x1: CHARGE_IO:** Use GPIO Driver to charge capacitor. Capacitor must be selected using COMP_PIN, and GPIO must be in AMUXB mode.
13	CSD_REFBUF_EN	Enables the reference buffer/comparator circuits for charging Cmod/Csh_tank using the mode selected in COMP_MODE. Default Value: 0
12	CSD_SENSE_EN	Enables the sense modulator output. Also turns on the IDAC compensation current as selected by CSD_IDAC. Default Value: 0
11	CSD_SENSE_COMP_BW	Selects bandwidth for sensing comparator Default Value: 1 **0x0: LOW:** Lower bandwidth **0x1: HIGH:** High bandwidth (default)
10 : 9	CSD_SHIELD_DELAY	Indicates the number of HFCLK cycles that csd_shield is delayed relative to csd_sense. Valid values are 0,1,2. Default Value: 0
8	CSD_DSI_SENSE_EN	Enables the use of the dsi_sense_in input instead of the internally generated modulation signal to drive csd_sense and csd_shield signals. Default Value: 0
7	CSD_PRS_12_8	Selects between 8 or 12b PRS sequence Default Value: 0 **0x0: 8B:** 8-bit PRS sequence (G(x)=X^8+X^4+X^3+X^2+1, period= 255) **0x1: 12B:** 12-bit PRS sequence (G(x)=X^12+X^9+X^3+X^2+1, period=4095)
6	CSD_PRS_SELECT	Selects between PRS or simple divide by 2 sense modulation. Default Value: 0 **0x0: DIV2:** Select simple divide-by-2 of clk_csd1 as output.

3.1.2 CSD_CONFIG (continued)

		0x1: PRS: Select PRS sequencer output, and start the sequencer.
5	CSD_PRS_CLEAR	When set, forces the pseudo-random generator to it's initial state. Note that it may take some time for this setting to take effect depending on the clock frequency used for clk_csd1. Hardware clears this bit at the same time PRS is cleared. Default Value: 0
1	CSD_SAMPLE_SYNC	Enables double synchronizing of sample input from DSI (only relevant when DSI_SAMPLE_EN=1). Default Value: 1
0	CSD_DSI_SAMPLE_EN	Enables the use of the DSI input instead of the comparator output to strobe COUNTER. 0: COUNTER counts CSD modulator output 1: COUNTER counts DSI input Default Value: 0

3.1.3 CSD_IDAC

IDAC Configuration

Address: 0x40080008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSD_IDAC1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	
HW Access	None					R	R	
Name	None [15:11]					CSD_IDAC 1_RANGE	CSD_IDAC1_MODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	CSD_IDAC2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None			RW	RW	
HW Access	None	R	None			R	R	
Name	None	CSD_FEED BACK_MO DE	None [29:27]			CSD_IDAC 2_RANGE	CSD_IDAC2_MODE [25:24]	

Bits	Name	Description
30	CSD_FEEDBACK_MODE	This bit controls whether, during CSD operation, the IDAC is controlled from the sampling flip-flop or directly from the comparator. Default Value: 0 **0x0: FLOP:** Use feedback from sampling flip-flop (used in most modes). **0x1: COMP:** Use feedback from comparator directly (used in single Cmod mutual cap sensing only)
26	CSD_IDAC2_RANGE	Current multiplier setting for IDAC2. Default Value: 0 **0x0: 4X:** Use 4X gain setting. **0x1: 8X:** Use 8X gain setting.

3.1.3 CSD_IDAC (continued)

25 : 24	CSD_IDAC2_MODE	Controls the usage mode of IDAC2 Default Value: 0 **0x0: OFF:** IDAC2 is not used. **0x1: FIXED:** IDAC2 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE:** IDAC2 is switched on and off depending on the result of the comparator. **0x3: DSI:** IDAC2 is controlled from dsi input dsi_idac2_en. It is connected to AMUXBUS-A or AMUXBUS-B depending on IDAC_SWAP setting.
22 : 16	CSD_IDAC2	Current setting for IDAC2 (7 bits). Default Value: 0
10	CSD_IDAC1_RANGE	Current multiplier setting for IDAC1. Default Value: 0 **0x0: 4X:** Use 4X gain setting. **0x1: 8X:** Use 8X gain setting.
9 : 8	CSD_IDAC1_MODE	Controls the usage mode of IDAC1 Default Value: 0 **0x0: OFF:** IDAC1 is not used. **0x1: FIXED:** IDAC1 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE:** IDAC1 is switched on and off depending on the result of the comparator. **0x3: DSI:** IDAC1 is controlled from dsi input dsi_idac1_en. It is connected to AMUXBUS-A or AMUXBUS-B depending on IDAC_SWAP setting.
7 : 0	CSD_IDAC1	Current setting for IDAC1 (8 bits). Default Value: 0

3.1.4 CSD_COUNTER

CSD Counter Register

Address: 0x4008000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CSD_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CSD_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CSD_PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	CSD_PERIOD [31:24]							

Bits	Name	Description
31 : 16	CSD_PERIOD	The remaining period (in clk_csd1 cycles) during which COUNTER will count the comparator output count. Firmware will write this field to the desired period, after which it will start counting down to 0. Upon completion of the sense operation, this field will be 0. Writing a non-0 value to this register initiates a sensing operation. It is assumed that the modulation is properly configured, all pins are properly selected and configured and that sense currents are flowing before this field is written. Default Value: 0
15 : 0	CSD_COUNTER	This field increments whenever the comparator is sampled and the sample is 1. Firmware typically writes 0 to this field whenever a new sense operation is initiated by writing a non-0 value to PERIOD. Default Value: 0

3.1.5 CSD_STATUS

Status Register

Address: 0x40080010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				CSD_SAMPLE	CSD_COMP_OUT	CSD_CSD_SENSE	CSD_CSD_CHARGE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CSD_SAMPLE	Output of main sensing comparator. Default Value: 0
2	CSD_COMP_OUT	Output of reference buffer comparator used to charge up Cmod or Csh_tank. Default Value: 0 **0x0: C_LT_VREF:** Ctank < Vref **0x1: C_GT_VREF:** Ctank > Vref
1	CSD_CSD_SENSE	Signal used to drive the Cs switches. Default Value: 0
0	CSD_CSD_CHARGE	Qualified, and possible inverted value of COMP_OUT that is used to drive GPIO's charging Cmod or Csh_tank. Default Value: 0

3.1.6 CSD_INTR

CSD Interrupt Request Register

Address: 0x40080014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CSD_CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD_CSD	The CSD IRQ bit is set. Firmware must clear this bit as part of the interrupt handler. Default Value: 0

3.1.7 CSD_INTR_SET

CSD Interrupt set register

Address: 0x40080018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CSD_CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD_CSD	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

4 Continuous Time Block Mini Registers

This section discusses the Continuous Time Block Mini (CTBM) registers. It lists all the registers in mapping tables, in address order.

4.1 Register Details

Register Name	Address
CTBM_CTB_CTRL	0x40100000
CTBM_OA_RES0_CTRL	0x40100004
CTBM_OA_RES1_CTRL	0x40100008
CTBM_COMP_STAT	0x4010000C
CTBM_INTR	0x40100020
CTBM_INTR_SET	0x40100024
CTBM_INTR_MASK	0x40100028
CTBM_INTR_MASKED	0x4010002C
CTBM_OA0_SW	0x40100080
CTBM_OA0_SW_CLEAR	0x40100084
CTBM_OA1_SW	0x40100088
CTBM_OA1_SW_CLEAR	0x4010008C
CTBM_CTB_SW_HW_CTRL	0x401000C0
CTBM_CTB_SW_STATUS	0x401000C4
CTBM_OA0_OFFSET_TRIM	0x40100F00
CTBM_OA0_SLOPE_OFFSET_TRIM	0x40100F04
CTBM_OA0_COMP_TRIM	0x40100F08
CTBM_OA1_OFFSET_TRIM	0x40100F0C
CTBM_OA1_SLOPE_OFFSET_TRIM	0x40100F10
CTBM_OA1_COMP_TRIM	0x40100F14

4.1.1 CTBM_CTB_CTRL

global CTB and power control

Address: 0x40100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CTBM_ENABLED	None [30:24]						

Bits	Name	Description
31	CTBM_ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default Value: 0

4.1.2 CTBM_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	
HW Access	None	R	R	R	None	R	R	
Name	None	CTBM_OA0_BYPASS_DSI_SYNC	CTBM_OA0_HYST_EN	CTBM_OA0_COMP_EN	None	CTBM_OA0_DRIVE_STR_SEL	CTBM_OA0_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				CTBM_OA0_PUMP_EN	None	CTBM_OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	CTBM_OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	CTBM_OA0_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
6	CTBM_OA0_BYPASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0

4.1.2 CTBM_OA_RES0_CTRL (continued)

5	CTBM_OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default Value: 0
4	CTBM_OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
2	CTBM_OA0_DRIVE_STR_SEL	Opamp0 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	CTBM_OA0_PWR_MODE	Opamp0 power level: 0=off Default Value: 0

4.1.3 CTBM_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	
HW Access	None	R	R	R	None	R	R	
Name	None	CTBM_OA1_BYPASS_DSI_SYNC	CTBM_OA1_HYST_EN	CTBM_OA1_COMP_EN	None	CTBM_OA1_DRIVE_STR_SEL	CTBM_OA1_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				CTBM_OA1_PUMP_EN	None	CTBM_OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	CTBM_OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	CTBM_OA1_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
6	CTBM_OA1_BYPASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0

4.1.3 CTBM_OA_RES1_CTRL (continued)

5	CTBM_OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default Value: 0
4	CTBM_OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
2	CTBM_OA1_DRIVE_STR_SEL	Opamp1 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	CTBM_OA1_PWR_MODE	Opamp1 power level: 0=off Default Value: 0

4.1.4 CTBM_COMP_STAT

Comparator status

Address: 0x4010000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CTBM_OA0_COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							CTBM_OA1_COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	CTBM_OA1_COMP	Opamp1 current comparator status Default Value: 0
0	CTBM_OA0_COMP	Opamp0 current comparator status Default Value: 0

4.1.5 CTBM_INTR

Interrupt request register

Address: 0x40100020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CTBM_COMP1	CTBM_COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CTBM_COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	CTBM_COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

4.1.6 CTBM_INTR_SET

Interrupt request set register

Address: 0x40100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CTBM_COMP1_SET	CTBM_COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CTBM_COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	CTBM_COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

4.1.7 CTBM_INTR_MASK

Interrupt request mask

Address: 0x40100028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CTBM_COMP1_MASK	CTBM_COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CTBM_COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	CTBM_COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

4.1.8 CTBM_INTR_MASKED

Interrupt request masked

Address: 0x4010002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CTBM_COMP1_MASKED	CTBM_COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CTBM_COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	CTBM_COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

4.1.9 CTBM_OA0_SW

Opamp0 switch control

Address: 0x40100080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				CTBM_OA0P_A30	CTBM_OA0P_A20	None	CTBM_OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	CTBM_OA0M_A81	None [13:9]					CTBM_OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		CTBM_OA0O_D81	None [20:19]		CTBM_OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	CTBM_OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default Value: 0
18	CTBM_OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	CTBM_OA0M_A81	Opamp0 negative terminal Opamp0 bottom Default Value: 0
8	CTBM_OA0M_A11	Opamp0 negative terminal P1 Default Value: 0
3	CTBM_OA0P_A30	Opamp0 positive terminal ctbbus0 Default Value: 0
2	CTBM_OA0P_A20	Opamp0 positive terminal P0 Default Value: 0
0	CTBM_OA0P_A00	Opamp0 positive terminal amuxbusa Default Value: 0

4.1.10 CTBM_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40100084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				CTBM_OA0P_A30	CTBM_OA0P_A20	None	CTBM_OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	CTBM_OA0M_A81	None [13:9]					CTBM_OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		CTBM_OA0O_D81	None [20:19]		CTBM_OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	CTBM_OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	CTBM_OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	CTBM_OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	CTBM_OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	CTBM_OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	CTBM_OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	CTBM_OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

4.1.11 CTBM_OA1_SW

Opamp1 switch control

Address: 0x40100088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None		RW1S	RW1S
HW Access	None			RW1C	None		RW1C	RW1C
Name	None [7:5]			CTBM_OA1P_A43	None [3:2]		CTBM_OA1P_A13	CTBM_OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	CTBM_OA1M_A82	None [13:9]					CTBM_OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		CTBM_OA1O_D82	None	CTBM_OA1O_D62	CTBM_OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	CTBM_OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default Value: 0
19	CTBM_OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default Value: 0
18	CTBM_OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	CTBM_OA1M_A82	Opamp1 negative terminal Opamp1 bottom Default Value: 0
8	CTBM_OA1M_A22	Opamp1 negative terminal P4 Default Value: 0
4	CTBM_OA1P_A43	Opamp1 positive terminal ctbbus1 Default Value: 0
1	CTBM_OA1P_A13	Opamp1 positive terminal P5 Default Value: 0

4.1.11 CTBM_OA1_SW (continued)

0	CTBM_OA1P_A03	Opamp1 positive terminal amuxbusb Default Value: 0

4.1.12 CTBM_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4010008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None		RW1C	RW1C
HW Access	None			A	None		A	A
Name	None [7:5]			CTBM_OA1P_A43	None [3:2]		CTBM_OA1P_A13	CTBM_OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	CTBM_OA1M_A82	None [13:9]					CTBM_OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		CTBM_OA1O_D82	None	CTBM_OA1O_D62	CTBM_OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	CTBM_OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	CTBM_OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	CTBM_OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	CTBM_OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	CTBM_OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
4	CTBM_OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	CTBM_OA1P_A13	see corresponding bit in OA1_SW Default Value: 0

4.1.12 CTBM_OA1_SW_CLEAR (continued)

0	CTBM_OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

4.1.13 CTBM_CTB_SW_HW_CTRL

CTB bus switch control status

Address: 0x401000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				CTBM_P3_HW_CTRL	CTBM_P2_HW_CTRL	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CTBM_P3_HW_CTRL	Pin P3 switches Default Value: 0
2	CTBM_P2_HW_CTRL	Pin P2 switches Default Value: 0

4.1.14 CTBM_CTB_SW_STATUS

CTB bus switch control status

Address: 0x401000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	R	R	R	None			
HW Access	None	W	W	W	None			
Name	None	CTBM_OA1O_D62_STAT	CTBM_OA1O_D52_STAT	CTBM_OA0O_D51_STAT	None [27:24]			

Bits	Name	Description
30	CTBM_OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	CTBM_OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	CTBM_OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

4.1.15 CTBM_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40100F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CTBM_OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	CTBM_OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

4.1.16 CTBM_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40100F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CTBM_OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	CTBM_OA0_SLOPE_OFFSET_TRIM	Opamp0 slope offset drift trim Default Value: 0

4.1.17 CTBM_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40100F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						CTBM_OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	CTBM_OA0_COMP_TRIM	Opamp0 Compenation Capacitor Trim Default Value: 0

4.1.18 CTBM_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40100F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CTBM_OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	CTBM_OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

4.1.19 CTBM_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40100F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CTBM_OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	CTBM_OA1_SLOPE_OFFSET_TRIM	Opamp1 slope offset drift trim Default Value: 0

4.1.20 CTBM_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40100F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						CTBM_OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	CTBM_OA1_COMP_TRIM	Opamp1 Compenation Capacitor Trim Default Value: 0

5 GPIO PORT Registers

This section discusses the GPIO PORT registers. It lists all the registers in mapping tables, in address order.

5.1 Register Details

Register Name	Address
PRT0_DR	0x40040000
PRT0_PS	0x40040004
PRT0_PC	0x40040008
PRT0_INTCFG	0x4004000C
PRT0_INTSTAT	0x40040010
PRT0_PC2	0x40040018
PRT1_DR	0x40040100
PRT1_PS	0x40040104
PRT1_PC	0x40040108
PRT1_INTCFG	0x4004010C
PRT1_INTSTAT	0x40040110
PRT1_PC2	0x40040118
PRT2_DR	0x40040200
PRT2_PS	0x40040204
PRT2_PC	0x40040208
PRT2_INTCFG	0x4004020C
PRT2_INTSTAT	0x40040210
PRT2_PC2	0x40040218
PRT3_DR	0x40040300
PRT3_PS	0x40040304
PRT3_PC	0x40040308
PRT3_INTCFG	0x4004030C
PRT3_INTSTAT	0x40040310
PRT3_PC2	0x40040318
PRT4_DR	0x40040400
PRT4_PS	0x40040404
PRT4_PC	0x40040408

Register Name	Address
PRT4_INTCFG	0x4004040C
PRT4_INTSTAT	0x40040410
PRT4_PC2	0x40040418

5.1.1 PRT0_DR

Port Output Data Register

Address: 0x40040000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT_DATAREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT_DATAREG	The data written to this register specifies the high ('1') or low ('0') state for a specific pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.2 PRT0_PS

Port Pin State Register

Address: 0x40040004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PRT_PINSTATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							PRT_PINSTATE_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	PRT_PINSTATE_FLT	Reads of this register return the logical state of the filtered pin. Default Value: 0
7 : 0	PRT_PINSTATE	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1: Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0: Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.3 PRT0_PC

Port Configuration Register

Address: 0x40040008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PRT_DM2 [7:6]		PRT_DM1 [5:3]			PRT_DM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	PRT_DM5	PRT_DM4 [14:12]			PRT_DM3 [11:9]			PRT_DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	PRT_DM7 [23:21]			PRT_DM6 [20:18]			PRT_DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PRT_SLOW	PRT_VTRIP_SEL

Bits	Name	Description
25	PRT_SLOW	This bit controls the output edge rate of all pins on the port: 0: fast. 1: slow. Default Value: 0
24	PRT_VTRIP_SEL	Alters the input buffer voltage. 0: CMOS 1: LVTTL Default Value: 0
23 : 21	PRT_DM7	The GPIO drive mode for Pin 7 See the description of DM0 for details. Default Value: 0
20 : 18	PRT_DM6	The GPIO drive mode for Pin 6. See the description of DM0 for details. Default Value: 0
17 : 15	PRT_DM5	The GPIO drive mode for Pin 5. See the description of DM0 for details. Default Value: 0
14 : 12	PRT_DM4	The GPIO drive mode for Pin 4. See the description of DM0 for details. Default Value: 0

5.1.3 PRT0_PC (continued)

11 : 9	PRT_DM3	The GPIO drive mode for Pin 3. See the description of DM0 for details. Default Value: 0
8 : 6	PRT_DM2	The GPIO drive mode for Pin 2. See the description of DM0 for details. Default Value: 0
5 : 3	PRT_DM1	The GPIO drive mode for Pin 1. See the description of DM0 for details. Default Value: 0
2 : 0	PRT_DM	The GPIO drive mode for a Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the IO-Matrix is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

5.1.4 PRT0_INTCFG

Port IRQ Configuration Register

Address: 0x4004000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT_INTTYPE3 [7:6]		PRT_INTTYPE2 [5:4]		PRT_INTTYPE1 [3:2]		PRT_INTTYPE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT_INTTYPE7 [15:14]		PRT_INTTYPE6 [13:12]		PRT_INTTYPE5 [11:10]		PRT_INTTYPE4 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			PRT_FLT_SELECT [20:18]			PRT_INTTYPE_FLT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	PRT_FLT_SELECT	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	PRT_INTTYPE_FLT	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	PRT_INTTYPE7	Sets which edge will trigger an IRQ for Pin 7. See the description of INTTYPE0 for details. Default Value: 0

5.1.4 PRT0_INTCFG (continued)

13 : 12	PRT_INTTYPE6	Sets which edge will trigger an IRQ for Pin 6. See the description of INTTYPE0 for details. Default Value: 0
11 : 10	PRT_INTTYPE5	Sets which edge will trigger an IRQ for Pin 5. See the description of INTTYPE0 for details. Default Value: 0
9 : 8	PRT_INTTYPE4	Sets which edge will trigger an IRQ for Pin 4. See the description of INTTYPE0 for details. Default Value: 0
7 : 6	PRT_INTTYPE3	Sets which edge will trigger an IRQ for Pin 3. See the description of INTTYPE0 for details. Default Value: 0
5 : 4	PRT_INTTYPE2	Sets which edge will trigger an IRQ for Pin 2. See the description of INTTYPE0 for details. Default Value: 0
3 : 2	PRT_INTTYPE1	Sets which edge will trigger an IRQ for Pin 1. See the description of INTTYPE0 for details. Default Value: 0
1 : 0	PRT_INTTYPE0	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

5.1.5 PRT0_INTSTAT

Port IRQ Status Register

Address: 0x40040010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	PRT_INTSTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							PRT_INTSTAT_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PRT_PS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PRT_PS_FLT

Bits	Name	Description
24	PRT_PS_FLT	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23 : 16	PRT_PS	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
8	PRT_INTSTAT_FLT	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
7 : 0	PRT_INTSTAT	Bit n indicates interrupt pending on pin #n. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.6 PRT0_PC2

Port Secondary Configuration Register

Address: 0x40040018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT_INP_DIS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT_INP_DIS	Disables the input buffer indepent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.7 PRT1_DR

Port Output Data Register

Address: 0x40040100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT0_DATAREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT0_DATAREG	The data written to this register specifies the high ('1') or low ('0') state for a specific pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.8 PRT1_PS

Port Pin State Register

Address: 0x40040104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PRT0_PINSTATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							PRT0_PINSTATE_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	PRT0_PINSTATE_FLT	Reads of this register return the logical state of the filtered pin. Default Value: 0
7 : 0	PRT0_PINSTATE	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1: Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0: Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.9 PRT1_PC

Port Configuration Register

Address: 0x40040108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PRT0_DM2 [7:6]		PRT0_DM1 [5:3]			PRT0_DM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	PRT0_DM5	PRT0_DM4 [14:12]			PRT0_DM3 [11:9]			PRT0_DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	PRT0_DM7 [23:21]			PRT0_DM6 [20:18]			PRT0_DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PRT0_SLOW	PRT0_VTRIP_SEL

Bits	Name	Description
25	PRT0_SLOW	This bit controls the output edge rate of all pins on the port: 0: fast. 1: slow. Default Value: 0
24	PRT0_VTRIP_SEL	Alters the input buffer voltage. 0: CMOS 1: LVTTL Default Value: 0
23 : 21	PRT0_DM7	The GPIO drive mode for Pin 7 See the description of DM0 for details. Default Value: 0
20 : 18	PRT0_DM6	The GPIO drive mode for Pin 6. See the description of DM0 for details. Default Value: 0
17 : 15	PRT0_DM5	The GPIO drive mode for Pin 5. See the description of DM0 for details. Default Value: 0
14 : 12	PRT0_DM4	The GPIO drive mode for Pin 4. See the description of DM0 for details. Default Value: 0

5.1.9 PRT1_PC (continued)

11 : 9	PRT0_DM3	The GPIO drive mode for Pin 3. See the description of DM0 for details. Default Value: 0
8 : 6	PRT0_DM2	The GPIO drive mode for Pin 2. See the description of DM0 for details. Default Value: 0
5 : 3	PRT0_DM1	The GPIO drive mode for Pin 1. See the description of DM0 for details. Default Value: 0
2 : 0	PRT0_DM	The GPIO drive mode for a Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the IO-Matrix is properly configured (HSIOM_PRT0_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

5.1.10 PRT1_INTCFG

Port IRQ Configuration Register

Address: 0x4004010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT0_INTTYPE3 [7:6]		PRT0_INTTYPE2 [5:4]		PRT0_INTTYPE1 [3:2]		PRT0_INTTYPE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT0_INTTYPE7 [15:14]		PRT0_INTTYPE6 [13:12]		PRT0_INTTYPE5 [11:10]		PRT0_INTTYPE4 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			PRT0_FLT_SELECT [20:18]			PRT0_INTTYPE_FLT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	PRT0_FLT_SELECT	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	PRT0_INTTYPE_FLT	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	PRT0_INTTYPE7	Sets which edge will trigger an IRQ for Pin 7. See the description of INTTYPE0 for details. Default Value: 0

5.1.10 PRT1_INTCFG (continued)

13 : 12	PRT0_INTTYPE6	Sets which edge will trigger an IRQ for Pin 6. See the description of INTTYPE0 for details. Default Value: 0
11 : 10	PRT0_INTTYPE5	Sets which edge will trigger an IRQ for Pin 5. See the description of INTTYPE0 for details. Default Value: 0
9 : 8	PRT0_INTTYPE4	Sets which edge will trigger an IRQ for Pin 4. See the description of INTTYPE0 for details. Default Value: 0
7 : 6	PRT0_INTTYPE3	Sets which edge will trigger an IRQ for Pin 3. See the description of INTTYPE0 for details. Default Value: 0
5 : 4	PRT0_INTTYPE2	Sets which edge will trigger an IRQ for Pin 2. See the description of INTTYPE0 for details. Default Value: 0
3 : 2	PRT0_INTTYPE1	Sets which edge will trigger an IRQ for Pin 1. See the description of INTTYPE0 for details. Default Value: 0
1 : 0	PRT0_INTTYPE0	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

5.1.11 PRT1_INTSTAT

Port IRQ Status Register

Address: 0x40040110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	PRT0_INTSTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							PRT0_INTSTAT_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PRT0_PS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PRT0_PS_FLT

Bits	Name	Description
24	PRT0_PS_FLT	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23 : 16	PRT0_PS	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
8	PRT0_INTSTAT_FLT	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
7 : 0	PRT0_INTSTAT	Bit n indicates interrupt pending on pin #n. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.12 PRT1_PC2

Port Secondary Configuration Register

Address: 0x40040118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT0_INP_DIS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT0_INP_DIS	Disables the input buffer indepent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.13 PRT2_DR

Port Output Data Register

Address: 0x40040200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT2_DATAREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT2_DATAREG	The data written to this register specifies the high ('1') or low ('0') state for a specific pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.14 PRT2_PS

Port Pin State Register

Address: 0x40040204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PRT2_PINSTATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							PRT2_PINSTATE_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	PRT2_PINSTATE_FLT	Reads of this register return the logical state of the filtered pin. Default Value: 0
7 : 0	PRT2_PINSTATE	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1: Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0: Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.15 PRT2_PC

Port Configuration Register

Address: 0x40040208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PRT2_DM2 [7:6]		PRT2_DM1 [5:3]			PRT2_DM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	PRT2_DM5	PRT2_DM4 [14:12]			PRT2_DM3 [11:9]			PRT2_DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	PRT2_DM7 [23:21]			PRT2_DM6 [20:18]			PRT2_DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PRT2_SLOW	PRT2_VTRIP_SEL

Bits	Name	Description
25	PRT2_SLOW	This bit controls the output edge rate of all pins on the port: 0: fast. 1: slow. Default Value: 0
24	PRT2_VTRIP_SEL	Alters the input buffer voltage. 0: CMOS 1: LVTTL Default Value: 0
23 : 21	PRT2_DM7	The GPIO drive mode for Pin 7 See the description of DM0 for details. Default Value: 0
20 : 18	PRT2_DM6	The GPIO drive mode for Pin 6. See the description of DM0 for details. Default Value: 0
17 : 15	PRT2_DM5	The GPIO drive mode for Pin 5. See the description of DM0 for details. Default Value: 0
14 : 12	PRT2_DM4	The GPIO drive mode for Pin 4. See the description of DM0 for details. Default Value: 0

5.1.15 PRT2_PC (continued)

11 : 9	PRT2_DM3	The GPIO drive mode for Pin 3. See the description of DM0 for details. Default Value: 0
8 : 6	PRT2_DM2	The GPIO drive mode for Pin 2. See the description of DM0 for details. Default Value: 0
5 : 3	PRT2_DM1	The GPIO drive mode for Pin 1. See the description of DM0 for details. Default Value: 0
2 : 0	PRT2_DM	The GPIO drive mode for a Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the IO-Matrix is properly configured (HSIOM_PRT2_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

5.1.16 PRT2_INTCFG

Port IRQ Configuration Register

Address: 0x4004020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT2_INTTYPE3 [7:6]		PRT2_INTTYPE2 [5:4]		PRT2_INTTYPE1 [3:2]		PRT2_INTTYPE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT2_INTTYPE7 [15:14]		PRT2_INTTYPE6 [13:12]		PRT2_INTTYPE5 [11:10]		PRT2_INTTYPE4 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			PRT2_FLT_SELECT [20:18]			PRT2_INTTYPE_FLT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	PRT2_FLT_SELECT	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	PRT2_INTTYPE_FLT	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	PRT2_INTTYPE7	Sets which edge will trigger an IRQ for Pin 7. See the description of INTTYPE0 for details. Default Value: 0

5.1.16 PRT2_INTCFG (continued)

13 : 12	PRT2_INTTYPE6	Sets which edge will trigger an IRQ for Pin 6. See the description of INTTYPE0 for details. Default Value: 0
11 : 10	PRT2_INTTYPE5	Sets which edge will trigger an IRQ for Pin 5. See the description of INTTYPE0 for details. Default Value: 0
9 : 8	PRT2_INTTYPE4	Sets which edge will trigger an IRQ for Pin 4. See the description of INTTYPE0 for details. Default Value: 0
7 : 6	PRT2_INTTYPE3	Sets which edge will trigger an IRQ for Pin 3. See the description of INTTYPE0 for details. Default Value: 0
5 : 4	PRT2_INTTYPE2	Sets which edge will trigger an IRQ for Pin 2. See the description of INTTYPE0 for details. Default Value: 0
3 : 2	PRT2_INTTYPE1	Sets which edge will trigger an IRQ for Pin 1. See the description of INTTYPE0 for details. Default Value: 0
1 : 0	PRT2_INTTYPE0	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

5.1.17 PRT2_INTSTAT

Port IRQ Status Register

Address: 0x40040210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	PRT2_INTSTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							PRT2_INTSTAT_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PRT2_PS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PRT2_PS_FLT

Bits	Name	Description
24	PRT2_PS_FLT	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23 : 16	PRT2_PS	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
8	PRT2_INTSTAT_FLT	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
7 : 0	PRT2_INTSTAT	Bit n indicates interrupt pending on pin #n. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.18 PRT2_PC2

Port Secondary Configuration Register

Address: 0x40040218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT2_INP_DIS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT2_INP_DIS	Disables the input buffer indepent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.19 PRT3_DR

Port Output Data Register

Address: 0x40040300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT3_DATAREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT3_DATAREG	The data written to this register specifies the high ('1') or low ('0') state for a specific pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.20 PRT3_PS

Port Pin State Register

Address: 0x40040304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PRT3_PINSTATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							PRT3_PINSTATE_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	PRT3_PINSTATE_FLT	Reads of this register return the logical state of the filtered pin. Default Value: 0
7 : 0	PRT3_PINSTATE	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1: Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0: Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.21 PRT3_PC

Port Configuration Register

Address: 0x40040308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PRT3_DM2 [7:6]		PRT3_DM1 [5:3]			PRT3_DM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	PRT3_DM5	PRT3_DM4 [14:12]			PRT3_DM3 [11:9]			PRT3_DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	PRT3_DM7 [23:21]			PRT3_DM6 [20:18]			PRT3_DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PRT3_SLOW	PRT3_VTRIP_SEL

Bits	Name	Description
25	PRT3_SLOW	This bit controls the output edge rate of all pins on the port: 0: fast. 1: slow. Default Value: 0
24	PRT3_VTRIP_SEL	Alters the input buffer voltage. 0: CMOS 1: LVTTL Default Value: 0
23 : 21	PRT3_DM7	The GPIO drive mode for Pin 7 See the description of DM0 for details. Default Value: 0
20 : 18	PRT3_DM6	The GPIO drive mode for Pin 6. See the description of DM0 for details. Default Value: 0
17 : 15	PRT3_DM5	The GPIO drive mode for Pin 5. See the description of DM0 for details. Default Value: 0
14 : 12	PRT3_DM4	The GPIO drive mode for Pin 4. See the description of DM0 for details. Default Value: 0

5.1.21 PRT3_PC (continued)

11 : 9	PRT3_DM3	The GPIO drive mode for Pin 3. See the description of DM0 for details. Default Value: 0
8 : 6	PRT3_DM2	The GPIO drive mode for Pin 2. See the description of DM0 for details. Default Value: 0
5 : 3	PRT3_DM1	The GPIO drive mode for Pin 1. See the description of DM0 for details. Default Value: 0
2 : 0	PRT3_DM	The GPIO drive mode for a Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the IO-Matrix is properly configured (HSIOM_PRT3_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

5.1.22 PRT3_INTCFG

Port IRQ Configuration Register

Address: 0x4004030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT3_INTTYPE3 [7:6]		PRT3_INTTYPE2 [5:4]		PRT3_INTTYPE1 [3:2]		PRT3_INTTYPE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT3_INTTYPE7 [15:14]		PRT3_INTTYPE6 [13:12]		PRT3_INTTYPE5 [11:10]		PRT3_INTTYPE4 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			PRT3_FLT_SELECT [20:18]			PRT3_INTTYPE_FLT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	PRT3_FLT_SELECT	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	PRT3_INTTYPE_FLT	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	PRT3_INTTYPE7	Sets which edge will trigger an IRQ for Pin 7. See the description of INTTYPE0 for details. Default Value: 0

5.1.22 PRT3_INTCFG (continued)

13 : 12	PRT3_INTTYPE6	Sets which edge will trigger an IRQ for Pin 6. See the description of INTTYPE0 for details. Default Value: 0
11 : 10	PRT3_INTTYPE5	Sets which edge will trigger an IRQ for Pin 5. See the description of INTTYPE0 for details. Default Value: 0
9 : 8	PRT3_INTTYPE4	Sets which edge will trigger an IRQ for Pin 4. See the description of INTTYPE0 for details. Default Value: 0
7 : 6	PRT3_INTTYPE3	Sets which edge will trigger an IRQ for Pin 3. See the description of INTTYPE0 for details. Default Value: 0
5 : 4	PRT3_INTTYPE2	Sets which edge will trigger an IRQ for Pin 2. See the description of INTTYPE0 for details. Default Value: 0
3 : 2	PRT3_INTTYPE1	Sets which edge will trigger an IRQ for Pin 1. See the description of INTTYPE0 for details. Default Value: 0
1 : 0	PRT3_INTTYPE0	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

5.1.23 PRT3_INTSTAT

Port IRQ Status Register

Address: 0x40040310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	PRT3_INTSTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							PRT3_INTSTAT_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PRT3_PS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PRT3_PS_FLT

Bits	Name	Description
24	PRT3_PS_FLT	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23 : 16	PRT3_PS	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
8	PRT3_INTSTAT_FLT	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
7 : 0	PRT3_INTSTAT	Bit n indicates interrupt pending on pin #n. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.24 PRT3_PC2

Port Secondary Configuration Register

Address: 0x40040318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT3_INP_DIS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT3_INP_DIS	Disables the input buffer indepent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.25 PRT4_DR

Port Output Data Register

Address: 0x40040400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT4_DATAREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT4_DATAREG	The data written to this register specifies the high ('1') or low ('0') state for a specific pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.26 PRT4_PS

Port Pin State Register

Address: 0x40040404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PRT4_PINSTATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							PRT4_PINSTATE_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	PRT4_PINSTATE_FLT	Reads of this register return the logical state of the filtered pin. Default Value: 0
7 : 0	PRT4_PINSTATE	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1: Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0: Reads LOW if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

5.1.27 PRT4_PC

Port Configuration Register

Address: 0x40040408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PRT4_DM2 [7:6]		PRT4_DM1 [5:3]			PRT4_DM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	PRT4_DM5	PRT4_DM4 [14:12]			PRT4_DM3 [11:9]			PRT4_DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	PRT4_DM7 [23:21]			PRT4_DM6 [20:18]			PRT4_DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						PRT4_SLOW	PRT4_VTRIP_SEL

Bits	Name	Description
25	PRT4_SLOW	This bit controls the output edge rate of all pins on the port: 0: fast. 1: slow. Default Value: 0
24	PRT4_VTRIP_SEL	Alters the input buffer voltage. 0: CMOS 1: LVTTL Default Value: 0
23 : 21	PRT4_DM7	The GPIO drive mode for Pin 7 See the description of DM0 for details. Default Value: 0
20 : 18	PRT4_DM6	The GPIO drive mode for Pin 6. See the description of DM0 for details. Default Value: 0
17 : 15	PRT4_DM5	The GPIO drive mode for Pin 5. See the description of DM0 for details. Default Value: 0
14 : 12	PRT4_DM4	The GPIO drive mode for Pin 4. See the description of DM0 for details. Default Value: 0

5.1.27 PRT4_PC (continued)

11 : 9	PRT4_DM3	The GPIO drive mode for Pin 3. See the description of DM0 for details. Default Value: 0
8 : 6	PRT4_DM2	The GPIO drive mode for Pin 2. See the description of DM0 for details. Default Value: 0
5 : 3	PRT4_DM1	The GPIO drive mode for Pin 1. See the description of DM0 for details. Default Value: 0
2 : 0	PRT4_DM	The GPIO drive mode for a Pin 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the IO-Matrix is properly configured (HSIOM_PRT4_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

5.1.28 PRT4_INTCFG

Port IRQ Configuration Register

Address: 0x4004040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT4_INTTYPE3 [7:6]		PRT4_INTTYPE2 [5:4]		PRT4_INTTYPE1 [3:2]		PRT4_INTTYPE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PRT4_INTTYPE7 [15:14]		PRT4_INTTYPE6 [13:12]		PRT4_INTTYPE5 [11:10]		PRT4_INTTYPE4 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			PRT4_FLT_SELECT [20:18]			PRT4_INTTYPE_FLT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	PRT4_FLT_SELECT	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	PRT4_INTTYPE_FLT	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	PRT4_INTTYPE7	Sets which edge will trigger an IRQ for Pin 7. See the description of INTTYPE0 for details. Default Value: 0

5.1.28 PRT4_INTCFG (continued)

13 : 12	PRT4_INTTYPE6	Sets which edge will trigger an IRQ for Pin 6. See the description of INTTYPE0 for details. Default Value: 0
11 : 10	PRT4_INTTYPE5	Sets which edge will trigger an IRQ for Pin 5. See the description of INTTYPE0 for details. Default Value: 0
9 : 8	PRT4_INTTYPE4	Sets which edge will trigger an IRQ for Pin 4. See the description of INTTYPE0 for details. Default Value: 0
7 : 6	PRT4_INTTYPE3	Sets which edge will trigger an IRQ for Pin 3. See the description of INTTYPE0 for details. Default Value: 0
5 : 4	PRT4_INTTYPE2	Sets which edge will trigger an IRQ for Pin 2. See the description of INTTYPE0 for details. Default Value: 0
3 : 2	PRT4_INTTYPE1	Sets which edge will trigger an IRQ for Pin 1. See the description of INTTYPE0 for details. Default Value: 0
1 : 0	PRT4_INTTYPE0	Sets which edge will trigger an IRQ for Pin 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

5.1.29 PRT4_INTSTAT

Port IRQ Status Register

Address: 0x40040410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	PRT4_INTSTAT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							PRT4_INTSTAT_FLT

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PRT4_PS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PRT4_PS_FLT

Bits	Name	Description
24	PRT4_PS_FLT	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23 : 16	PRT4_PS	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
8	PRT4_INTSTAT_FLT	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
7 : 0	PRT4_INTSTAT	Bit n indicates interrupt pending on pin #n. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.30 PRT4_PC2

Port Secondary Configuration Register

Address: 0x40040418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRT4_INP_DIS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRT4_INP_DIS	Disables the input buffer indepent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. One bit is used for each pin: bit 0 for Pin 0, bit 1 for Pin 1 etc. Default Value: 0

6 High Speed I/O Matrix Registers

This section discusses the High Speed I/O Matrix (HSIOM) registers. It lists all the registers in mapping tables, in address order.

6.1 Register Details

Register Name	Address
HSIOM_PORT_SEL0	0x40010000
HSIOM_PORT_SEL1	0x40010004
HSIOM_PORT_SEL2	0x40010008
HSIOM_PORT_SEL3	0x4001000C
HSIOM_PORT_SEL4	0x40010010

6.1.1 HSIOM_PORT_SEL0

Port 0 control register.

Address: 0x40010000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects the connection of Pin 7. See the description of SEL0 for details. Default Value: 0
27 : 24	HSIOM_SEL6	Selects the connection of Pin 6. See the description of SEL0 for details. Default Value: 0
23 : 20	HSIOM_SEL5	Selects the connection of Pin 5. See the description of SEL0 for details. Default Value: 0
19 : 16	HSIOM_SEL4	Selects the connection of Pin 4. See the description of SEL0 for details. Default Value: 0
15 : 12	HSIOM_SEL3	Selects the connection of Pin 3. See the description of SEL0 for details. Default Value: 0
11 : 8	HSIOM_SEL2	Selects the connection of Pin 2. See the description of SEL0 for details. Default Value: 0
7 : 4	HSIOM_SEL1	Selects the connection of Pin 1. See the description of SEL0 for details. Default Value: 0

6.1.1 HSIOM_PORT_SEL0 (continued)

3 : 0	HSIOM_SEL0	Selects the connection of Pin 0. Note that the availability of DSI, Active, and Deep Sleep sources depends on the pin. Not all of the below mentioned connections are available on every pin. See the Pinouts section of the device datasheet to know the functions available for each pin. Default Value: 0 **0x0: GPIO:** Pin is regular firmware-controlled I/O or connected to dedicated hardware block (Opamp inputs/outputs, SARMUX, SAR reference, LPCOMP inputs) .See the device datasheet for details. Proper configurations of corresponding GPIO_PRT registers are required to use dedicated hardware signals. **0x1: GPIO_DSI:** Output is firmware controlled, but OE is controlled from DSI. **0x2: DSI_DSI:** Both Output and OE are controlled from DSI. **0x3: DSI_GPIO:** Output is controlled from DSI, but OE is firmware controlled. **0x4: CSD_SENSE:** Pin is a CSD sense pin (analog mode) **0x5: CSD_SHIELD:** Pin is a CSD shield pin (analog mode) **0x6: AMUXA:** Pin is connected to AMUXBUS A. **0x7: AMUXB:** Pin is connected to AMUXBUS B. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, digital IO driver is connected to csd_charge signal (and pin is also still connected to AMUXBUS B). **0x8: ACT_0:** Pin specific Active source #0. (TCPWM signals, EXTCLK pin). See the device datasheet for details. **0x9: ACT_1:** Pin specific Active source #1. (SCB UART signals). See the device datasheet for details. **0xa: ACT_2:** Reserved **0xb: ACT_3:** Reserved **0xc: LCD_COM:** LCD common pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xd: LCD_SEG:** LCD segment pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xe: DPSLP_0:** Pin specific DeepSleep source #0. (SCB I2C signals, SWD signals , WAKEUP pin). See the device datasheet for details. **0xf: DPSLP_1:** Pin specific DeepSleep source #1. (SCB SPI signals). See the device datasheet for details.

6.1.2 HSIOM_PORT_SEL1

Port 1 control register.

Address: 0x40010004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects the connection of Pin 7. See the description of SEL0 for details. Default Value: 0
27 : 24	HSIOM_SEL6	Selects the connection of Pin 6. See the description of SEL0 for details. Default Value: 0
23 : 20	HSIOM_SEL5	Selects the connection of Pin 5. See the description of SEL0 for details. Default Value: 0
19 : 16	HSIOM_SEL4	Selects the connection of Pin 4. See the description of SEL0 for details. Default Value: 0
15 : 12	HSIOM_SEL3	Selects the connection of Pin 3. See the description of SEL0 for details. Default Value: 0
11 : 8	HSIOM_SEL2	Selects the connection of Pin 2. See the description of SEL0 for details. Default Value: 0
7 : 4	HSIOM_SEL1	Selects the connection of Pin 1. See the description of SEL0 for details. Default Value: 0

6.1.2 HSIOM_PORT_SEL1 (continued)

3 : 0	HSIOM_SEL0	Selects the connection of Pin 0. Note that the availability of DSI, Active, and Deep Sleep sources depends on the pin. Not all of the below mentioned connections are available on every pin. See the Pinouts section of the device datasheet to know the functions available for each pin. Default Value: 0 **0x0: GPIO:** Pin is regular firmware-controlled I/O or connected to dedicated hardware block (Opamp inputs/outputs, SARMUX, SAR reference, LPCOMP inputs) .See the device datasheet for details. Proper configurations of corresponding GPIO_PRT registers are required to use dedicated hardware signals. **0x1: GPIO_DSI:** Output is firmware controlled, but OE is controlled from DSI. **0x2: DSI_DSI:** Both Output and OE are controlled from DSI. **0x3: DSI_GPIO:** Output is controlled from DSI, but OE is firmware controlled. **0x4: CSD_SENSE:** Pin is a CSD sense pin (analog mode) **0x5: CSD_SHIELD:** Pin is a CSD shield pin (analog mode) **0x6: AMUXA:** Pin is connected to AMUXBUS A. **0x7: AMUXB:** Pin is connected to AMUXBUS B. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, digital IO driver is connected to csd_charge signal (and pin is also still connected to AMUXBUS B). **0x8: ACT_0:** Pin specific Active source #0. (TCPWM signals, EXTCLK pin). See the device datasheet for details. **0x9: ACT_1:** Pin specific Active source #1. (SCB UART signals). See the device datasheet for details. **0xa: ACT_2:** Reserved **0xb: ACT_3:** Reserved **0xc: LCD_COM:** LCD common pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xd: LCD_SEG:** LCD segment pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xe: DPSLP_0:** Pin specific DeepSleep source #0. (SCB I2C signals, SWD signals , WAKEUP pin). See the device datasheet for details. **0xf: DPSLP_1:** Pin specific DeepSleep source #1. (SCB SPI signals). See the device datasheet for details.

6.1.3 HSIOM_PORT_SEL2

Port 2 control register.

Address: 0x40010008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects the connection of Pin 7. See the description of SEL0 for details. Default Value: 0
27 : 24	HSIOM_SEL6	Selects the connection of Pin 6. See the description of SEL0 for details. Default Value: 0
23 : 20	HSIOM_SEL5	Selects the connection of Pin 5. See the description of SEL0 for details. Default Value: 0
19 : 16	HSIOM_SEL4	Selects the connection of Pin 4. See the description of SEL0 for details. Default Value: 0
15 : 12	HSIOM_SEL3	Selects the connection of Pin 3. See the description of SEL0 for details. Default Value: 0
11 : 8	HSIOM_SEL2	Selects the connection of Pin 2. See the description of SEL0 for details. Default Value: 0
7 : 4	HSIOM_SEL1	Selects the connection of Pin 1. See the description of SEL0 for details. Default Value: 0

6.1.3 HSIOM_PORT_SEL2 (continued)

3 : 0	HSIOM_SEL0	Selects the connection of Pin 0. Note that the availability of DSI, Active, and Deep Sleep sources depends on the pin. Not all of the below mentioned connections are available on every pin. See the Pinouts section of the device datasheet to know the functions available for each pin. Default Value: 0 **0x0: GPIO:** Pin is regular firmware-controlled I/O or connected to dedicated hardware block (Opamp inputs/outputs, SARMUX, SAR reference, LPCOMP inputs) .See the device datasheet for details. Proper configurations of corresponding GPIO_PRT registers are required to use dedicated hardware signals. **0x1: GPIO_DSI:** Output is firmware controlled, but OE is controlled from DSI. **0x2: DSI_DSI:** Both Output and OE are controlled from DSI. **0x3: DSI_GPIO:** Output is controlled from DSI, but OE is firmware controlled. **0x4: CSD_SENSE:** Pin is a CSD sense pin (analog mode) **0x5: CSD_SHIELD:** Pin is a CSD shield pin (analog mode) **0x6: AMUXA:** Pin is connected to AMUXBUS A. **0x7: AMUXB:** Pin is connected to AMUXBUS B. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, digital IO driver is connected to csd_charge signal (and pin is also still connected to AMUXBUS B). **0x8: ACT_0:** Pin specific Active source #0. (TCPWM signals, EXTCLK pin). See the device datasheet for details. **0x9: ACT_1:** Pin specific Active source #1. (SCB UART signals). See the device datasheet for details. **0xa: ACT_2:** Reserved **0xb: ACT_3:** Reserved **0xc: LCD_COM:** LCD common pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xd: LCD_SEG:** LCD segment pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xe: DPSLP_0:** Pin specific DeepSleep source #0. (SCB I2C signals, SWD signals , WAKEUP pin). See the device datasheet for details. **0xf: DPSLP_1:** Pin specific DeepSleep source #1. (SCB SPI signals). See the device datasheet for details.

6.1.4 HSIOM_PORT_SEL3

Port 3 control register.

Address: 0x4001000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects the connection of Pin 7. See the description of SEL0 for details. Default Value: 0
27 : 24	HSIOM_SEL6	Selects the connection of Pin 6. See the description of SEL0 for details. Default Value: 0
23 : 20	HSIOM_SEL5	Selects the connection of Pin 5. See the description of SEL0 for details. Default Value: 0
19 : 16	HSIOM_SEL4	Selects the connection of Pin 4. See the description of SEL0 for details. Default Value: 0
15 : 12	HSIOM_SEL3	Selects the connection of Pin 3. See the description of SEL0 for details. Default Value: 0
11 : 8	HSIOM_SEL2	Selects the connection of Pin 2. See the description of SEL0 for details. Default Value: 0
7 : 4	HSIOM_SEL1	Selects the connection of Pin 1. See the description of SEL0 for details. Default Value: 0

6.1.4 HSIOM_PORT_SEL3 (continued)

3 : 0	HSIOM_SEL0	Selects the connection of Pin 0. Note that the availability of DSI, Active, and Deep Sleep sources depends on the pin. Not all of the below mentioned connections are available on every pin. See the Pinouts section of the device datasheet to know the functions available for each pin. Default Value: 0 **0x0: GPIO:** Pin is regular firmware-controlled I/O or connected to dedicated hardware block (Opamp inputs/outputs, SARMUX, SAR reference, LPCOMP inputs) .See the device datasheet for details. Proper configurations of corresponding GPIO_PRT registers are required to use dedicated hardware signals. **0x1: GPIO_DSI:** Output is firmware controlled, but OE is controlled from DSI. **0x2: DSI_DSI:** Both Output and OE are controlled from DSI. **0x3: DSI_GPIO:** Output is controlled from DSI, but OE is firmware controlled. **0x4: CSD_SENSE:** Pin is a CSD sense pin (analog mode) **0x5: CSD_SHIELD:** Pin is a CSD shield pin (analog mode) **0x6: AMUXA:** Pin is connected to AMUXBUS A. **0x7: AMUXB:** Pin is connected to AMUXBUS B. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, digital IO driver is connected to csd_charge signal (and pin is also still connected to AMUXBUS B). **0x8: ACT_0:** Pin specific Active source #0. (TCPWM signals, EXTCLK pin). See the device datasheet for details. **0x9: ACT_1:** Pin specific Active source #1. (SCB UART signals). See the device datasheet for details. **0xa: ACT_2:** Reserved **0xb: ACT_3:** Reserved **0xc: LCD_COM:** LCD common pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xd: LCD_SEG:** LCD segment pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xe: DPSLP_0:** Pin specific DeepSleep source #0. (SCB I2C signals, SWD signals , WAKEUP pin). See the device datasheet for details. **0xf: DPSLP_1:** Pin specific DeepSleep source #1. (SCB SPI signals). See the device datasheet for details.

6.1.5 HSIOM_PORT_SEL4

Port 4 control register.

Address: 0x40010010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects the connection of Pin 7. See the description of SEL0 for details. Default Value: 0
27 : 24	HSIOM_SEL6	Selects the connection of Pin 6. See the description of SEL0 for details. Default Value: 0
23 : 20	HSIOM_SEL5	Selects the connection of Pin 5. See the description of SEL0 for details. Default Value: 0
19 : 16	HSIOM_SEL4	Selects the connection of Pin 4. See the description of SEL0 for details. Default Value: 0
15 : 12	HSIOM_SEL3	Selects the connection of Pin 3. See the description of SEL0 for details. Default Value: 0
11 : 8	HSIOM_SEL2	Selects the connection of Pin 2. See the description of SEL0 for details. Default Value: 0
7 : 4	HSIOM_SEL1	Selects the connection of Pin 1. See the description of SEL0 for details. Default Value: 0

6.1.5 HSIOM_PORT_SEL4 (continued)

3 : 0	HSIOM_SEL0	Selects the connection of Pin 0. Note that the availability of DSI, Active, and Deep Sleep sources depends on the pin. Not all of the below mentioned connections are available on every pin. See the Pinouts section of the device datasheet to know the functions available for each pin. Default Value: 0 **0x0: GPIO:** Pin is regular firmware-controlled I/O or connected to dedicated hardware block (Opamp inputs/outputs, SARMUX, SAR reference, LPCOMP inputs) .See the device datasheet for details. Proper configurations of corresponding GPIO_PRT registers are required to use dedicated hardware signals. **0x1: GPIO_DSI:** Output is firmware controlled, but OE is controlled from DSI. **0x2: DSI_DSI:** Both Output and OE are controlled from DSI. **0x3: DSI_GPIO:** Output is controlled from DSI, but OE is firmware controlled. **0x4: CSD_SENSE:** Pin is a CSD sense pin (analog mode) **0x5: CSD_SHIELD:** Pin is a CSD shield pin (analog mode) **0x6: AMUXA:** Pin is connected to AMUXBUS A. **0x7: AMUXB:** Pin is connected to AMUXBUS B. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, digital IO driver is connected to csd_charge signal (and pin is also still connected to AMUXBUS B). **0x8: ACT_0:** Pin specific Active source #0. (TCPWM signals, EXTCLK pin). See the device datasheet for details. **0x9: ACT_1:** Pin specific Active source #1. (SCB UART signals). See the device datasheet for details. **0xa: ACT_2:** Reserved **0xb: ACT_3:** Reserved **0xc: LCD_COM:** LCD common pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xd: LCD_SEG:** LCD segment pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured). **0xe: DPSLP_0:** Pin specific DeepSleep source #0. (SCB I2C signals, SWD signals , WAKEUP pin). See the device datasheet for details. **0xf: DPSLP_1:** Pin specific DeepSleep source #1. (SCB SPI signals). See the device datasheet for details.

7 LCD Registers

This section discusses the LCD registers. It lists all the registers in mapping tables, in address order.

7.1 Register Details

Register Name	Address
LCD_ID	0x40090000
LCD_DIVIDER	0x40090004
LCD_CONTROL	0x40090008
LCD_DATA0	0x40090100
LCD_DATA1	0x40090200
LCD_DATA2	0x40090300
LCD_DATA3	0x40090400

7.1.1 LCD_ID

ID & Revision

Address: 0x40090000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	LCD_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	LCD_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	LCD_REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	LCD_REVISION [31:24]							

Bits	Name	Description
31 : 16	LCD_REVISION	the version number is 0x0001 Default Value: 1
15 : 0	LCD_ID	the ID of LCD controller peripheral is 0xF0F0 Default Value: 61680

7.1.2 LCD_DIVIDER

LCD Divider Register

Address: 0x40090004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LCD_SUBFR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LCD_SUBFR_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LCD_DEAD_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LCD_DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	LCD_DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	LCD_SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

7.1.3 LCD_CONTROL

LCD Configuration Register

Address: 0x40090008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW	RW	RW	RW	RW
HW Access	None	R		R	R	R	R	R
Name	None	LCD_BIAS [6:5]		LCD_OP_MODE	LCD_TYPE	LCD_LCD_MODE	LCD_HS_EN	LCD_LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LCD_COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LCD_LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LCD_LS_EN_STAT	LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0. The following procedure should be followed to disable the LS generator: 1. If LS_EN=0 we are done. Exit the procedure. 2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet. 3. Set LS_EN=0. 4. Wait until LS_EN_STAT=0. Default Value: 0

7.1.3 LCD_CONTROL (continued)

11 : 8	LCD_COM_NUM	The number of COM connections minus 2. So: 0: 2 COM's 1: 3 COM's ... 13: 15 COM's 14: 16 COM's 15: undefined Default Value: 0
6 : 5	LCD_BIAS	PWM bias selection Default Value: 0 **0x0: HALF:** 1/2 Bias **0x1: THIRD:** 1/3 Bias **0x2: FOURTH:** 1/4 Bias (not supported by LS generator) **0x3: FIFTH:** 1/5 Bias (not supported by LS generator)
4	LCD_OP_MODE	Driving mode configuration Default Value: 0 **0x0: PWM:** PWM Mode **0x1: CORRELATION:** Digital Correlation Mode
3	LCD_TYPE	LCD driving waveform type configuration. Default Value: 0 **0x0: TYPE_A:** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B:** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).
2	LCD_LCD_MODE	HS/LS Mode selection Default Value: 0 **0x0: LS:** Select Low Speed (32kHz) Generator (Works in Active, Sleep and DeepSleep power modes). **0x1: HS:** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).
1	LCD_HS_EN	High speed (HS) generator enable 1: enable 0: disable Default Value: 0
0	LCD_LS_EN	Low speed (LS) generator enable 1: enable 0: disable Default Value: 0

7.1.4 LCD_DATA0

LCD Pin Data Registers

Address: 0x40090100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LCD_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LCD_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LCD_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LCD_DATA [31:24]							

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

7.1.5 LCD_DATA1

LCD Pin Data Registers

Address: 0x40090200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LCD_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LCD_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LCD_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LCD_DATA [31:24]							

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

7.1.6 LCD_DATA2

LCD Pin Data Registers

Address: 0x40090300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LCD_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LCD_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LCD_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LCD_DATA [31:24]							

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 9-12 (COM9 is lsb). Default Value: 0

7.1.7 LCD_DATA3

LCD Pin Data Registers

Address: 0x40090400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LCD_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LCD_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LCD_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LCD_DATA [31:24]							

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 13-16 (COM13 is lsb). Default Value: 0

8 Low Power Comparator Registers

This section discusses the Low Power Comparator (LPCOMP) registers. It lists all the registers in mapping tables, in address order.

8.1 Register Details

Register Name	Address
LPCOMP_ID	0x400A0000
LPCOMP_CONFIG	0x400A0004
LPCOMP_INTR	0x400A000C
LPCOMP_INTR_SET	0x400A0010
LPCOMP_TRIM1	0x400AFF00
LPCOMP_TRIM2	0x400AFF04
LPCOMP_TRIM3	0x400AFF08
LPCOMP_TRIM4	0x400AFF0C

8.1.1 LPCOMP_ID

ID & Revision

Address: 0x400A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	LPCOMP_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	LPCOMP_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	LPCOMP_REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	LPCOMP_REVISION [31:24]							

Bits	Name	Description
31 : 16	LPCOMP_REVISION	the version number is 0x0001 Default Value: 1
15 : 0	LPCOMP_ID	the ID of LPCOMP peripheral is 0xE0E0 Default Value: 57568

8.1.2 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x400A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	LPCOMP_ENABLE1	LPCOMP_OUT1	LPCOMP_INTTYPE1 [5:4]		LPCOMP_FILTER1	LPCOMP_HYST1	LPCOMP_MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	LPCOMP_ENABLE2	LPCOMP_OUT2	LPCOMP_INTTYPE2 [13:12]		LPCOMP_FILTER2	LPCOMP_HYST2	LPCOMP_MODE2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	LPCOMP_ENABLE2	Enable comparator #2 Default Value: 0
14	LPCOMP_OUT2	Current output value of the comparator. Default Value: 0
13 : 12	LPCOMP_INTTYPE2	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

8.1.2 LPCOMP_CONFIG (continued)

11	LPCOMP_FILTER2	Enable the inline digital filter for the comparator Default Value: 0
10	LPCOMP_HYST2	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
9 : 8	LPCOMP_MODE2	Operating mode for the comparator Default Value: 0 **0x0: SLOW:** Slow operating mode (uses less power, <50uA) **0x1: FAST:** Fast operating mode (uses more power, <400uA) **0x2: ULP:** Ultra low power operting mode (uses ~2-4uA)
7	LPCOMP_ENABLE1	Enable comparator #1 Default Value: 0
6	LPCOMP_OUT1	Current output value of the comparator. Default Value: 0
5 : 4	LPCOMP_INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
3	LPCOMP_FILTER1	Enable the inline digital filter for the comparator Default Value: 0
2	LPCOMP_HYST1	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
1 : 0	LPCOMP_MODE1	Operating mode for the comparator Default Value: 0 **0x0: SLOW:** Slow operating mode (uses less power, <50uA) **0x1: FAST:** Fast operating mode (uses more power, <400uA) **0x2: ULP:** Ultra low power operting mode (uses ~2-4uA)

8.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x400A000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						LPCOMP_COMP2	LPCOMP_COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LPCOMP_COMP2	Comparator #2 generated an interrupt Default Value: 0
0	LPCOMP_COMP1	Comparator #1 generated an interrupt Default Value: 0

8.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x400A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						LPCOMP_COMP2	LPCOMP_COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LPCOMP_COMP2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	LPCOMP_COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

8.1.5 LPCOMP_TRIM1

LPCOMP Trim Register

Address: 0x400AFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			LPCOMP_COMP1_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	LPCOMP_COMP1_TRIMA	Trim A for Comparator #1 Default Value: 0

8.1.6 LPCOMP_TRIM2

LPCOMP Trim Register

Address: 0x400AFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			LPCOMP_COMP1_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	LPCOMP_COMP1_TRIMB	Trim B for Comparator #1 Default Value: 0

8.1.7 LPCOMP_TRIM3

LPCOMP Trim Register

Address: 0x400AFF08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			LPCOMP_COMP2_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	LPCOMP_COMP2_TRIMA	Trim A for Comparator #2 Default Value: 0

8.1.8 LPCOMP_TRIM4

LPCOMP Trim Register

Address: 0x400AFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			LPCOMP_COMP2_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	LPCOMP_COMP2_TRIMB	Trim B for Comparator #2 Default Value: 0

9 SAR ADC Registers

This section discusses the SAR ADC registers. It lists all the registers in mapping tables, in address order.

9.1 Register Details

Register Name	Address
SAR_CTRL	0x401A0000
SAR_SAMPLE_CTRL	0x401A0004
SAR_SAMPLE_TIME01	0x401A0010
SAR_SAMPLE_TIME23	0x401A0014
SAR_RANGE_THRES	0x401A0018
SAR_RANGE_COND	0x401A001C
SAR_CHAN_EN	0x401A0020
SAR_START_CTRL	0x401A0024
SAR_CHAN_CONFIG	0x401A0080
SAR_CHAN_WORK	0x401A0100
SAR_CHAN_RESULT	0x401A0180
SAR_CHAN_WORK_VALID	0x401A0200
SAR_CHAN_RESULT_VALID	0x401A0204
SAR_STATUS	0x401A0208
SAR_AVG_STAT	0x401A020C
SAR_INTR	0x401A0210
SAR_INTR_SET	0x401A0214
SAR_INTR_MASK	0x401A0218
SAR_INTR_MASKED	0x401A021C
SAR_SATURATE_INTR	0x401A0220
SAR_SATURATE_INTR_SET	0x401A0224
SAR_SATURATE_INTR_MASK	0x401A0228
SAR_SATURATE_INTR_MASKED	0x401A022C
SAR_RANGE_INTR	0x401A0230
SAR_RANGE_INTR_SET	0x401A0234
SAR_RANGE_INTR_MASK	0x401A0238
SAR_RANGE_INTR_MASKED	0x401A023C

Register Name	Address
SAR_INTR_CAUSE	0x401A0240
SAR_INJ_CHAN_CONFIG	0x401A0280
SAR_INJ_RESULT	0x401A0290
SAR_MUX_SWITCH0	0x401A0300
SAR_MUX_SWITCH_CLEAR0	0x401A0304
SAR_MUX_SWITCH_HW_CTRL	0x401A0340
SAR_MUX_SWITCH_STATUS	0x401A0348
SAR_PUMP_CTRL	0x401A0380

9.1.1 SAR_CTRL

Analog control register.

Address: 0x401A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	SAR_VREF_BYP_CAP_EN	SAR_VREF_SEL [6:4]			None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	SAR_PWR_CTRL_VREF [15:14]		SAR_SAR_HW_CTRL_NEGVREF	None	SAR_NEG_SEL [11:9]			None

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				SAR_SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	None		RW	
HW Access	R	R	R	R	None		R	
Name	SAR_ENABLED	SAR_SWITCH_DISABLE	SAR_DSI_MODE	SAR_DSI_SYNC_CONFIG	None [27:26]		SAR_ICONT_LV [25:24]	

Bits	Name	Description
31	SAR_ENABLED	- 0: SAR IP disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgaiting) on write. - 1: SAR IP enabled. Default Value: 0
30	SAR_SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note DSI and firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware or UDBs (through DSI) to set the switches to route the signal to be converted through the SARMUX Default Value: 0

9.1.1 SAR_CTRL (continued)

29	SAR_DSI_MODE	SAR sequencer takes configuration from DSI signals (note this also has the same effect as SWITCH_DISABLE==1) - 0: Normal mode, SAR sequencer operates according to CHAN_EN enables and CHAN_CONFIG channel configurations - 1: CHAN_EN, INJ_START_EN and channel configurations in CHAN_CONFIG and INJ_CHAN_CONFIG are ignored Default Value: 0
28	SAR_DSI_SYNC_CONFIG	- 0: bypass clock domain synchronisation of the DSI config signals. - 1: synchronize the DSI config signals to peripheral clock domain. Default Value: 1
25 : 24	SAR_ICONT_LV	SARADC low power mode. Default Value: 0 **0x0: NORMAL_PWR:** normal power (default), max clk_sar is 18MHz. **0x1: HALF_PWR:** 1/2 power mode, max clk_sar is 9MHz. **0x2: MORE_PWR:** 1.333 power mode, max clk_sar is 18MHz. **0x3: QUARTER_PWR:** 1/4 power mode, max clk_sar is 4.5MHz.
19 : 16	SAR_SPARE	Spare controls, not yet designated, for late changes done with an ECO Default Value: 0
15 : 14	SAR_PWR_CTRL_VREF	VREF buffer low power mode. Default Value: 0 **0x0: NORMAL_PWR:** normal power (default), no bypass cap, max clk_sar is 3MHz. **0x1: HALF_PWR:** 1/2 power mode, no bypass cap, max clk_sar is 1.5MHz. **0x2: THIRD_PWR:** 1/3 power mode, no bypass cap, max clk_sar is 1MHz. **0x3: QUARTER_PWR:** 1/4 power mode, with bypass cap, max clk_sar is 18MHz.
13	SAR_SAR_HW_CTRL_NEGVREF	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch. Default Value: 0
11 : 9	SAR_NEG_SEL	SARADC internal NEG selection for Single ended conversion Default Value: 0 **0x0: VSSA_KELVIN:** NEG input of SARADC is connected to "vssa_kelvin", gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high. **0x1: ART_VSSA:** NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC **0x2: P1:** NEG input of SARADC is connected to P1 pin of SARMUX **0x3: P3:** NEG input of SARADC is connected to P3 pin of SARMUX

9.1.1 SAR_CTRL (continued)

		0x4: P5: NEG input of SARADC is connected to P5 pin of SARMUX **0x5: P7:** NEG input of SARADC is connected to P7 pin of SARMUX **0x6: ACORE:** NEG input of SARADC is connected to an ACORE in AROUTE **0x7: VREF:** NEG input of SARADC is shorted with VREF input of SARADC.
7	SAR_VREF_BYP_CAP_EN	VREF bypass cap enable for when VREF buffer is on Default Value: 0
6 : 4	SAR_VREF_SEL	SARADC internal VREF selection. Default Value: 0 **0x0: VREF0:** VREF0 from PRB (VREF buffer on) **0x1: VREF1:** VREF1 from PRB (VREF buffer on) **0x2: VREF2:** VREF2 from PRB (VREF buffer on) **0x3: VREF_AROUTE:** VREF from AROUTE (VREF buffer on) **0x4: VBGR:** 1.024V from BandGap (VREF buffer on) **0x5: VREF_EXT:** External precision Vref direct from a pin (low impedance path). **0x6: VDDA_DIV_2:** Vdda/2 (VREF buffer on) **0x7: VDDA:** Vdda.

9.1.2 SAR_SAMPLE_CTRL

Sample control register.

Address: 0x401A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	SAR_AVG_SHIFT	SAR_AVG_CNT [6:4]			SAR_DIFFERENTIAL_SIGNED	SAR_SINGLE_ENDED_SIGNED	SAR_LEFT_ALIGN	SAR_SUB_RESOLU-TION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				SAR_DSI_SYNC_TRIGGER	SAR_DSI_TRIGGER_LEVEL	SAR_DSI_TRIGGER_EN	SAR_CONTINUOUS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	SAR_EOS_DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	SAR_EOS_DSI_OUT_EN	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware also a pulse is send on the dsi_eos signal. Default Value: 0
19	SAR_DSI_SYNC_TRIGGER	- 0: bypass clock domain synchronisation of the DSI trigger signal. - 1: synchronize the DSI trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1
18	SAR_DSI_TRIGGER_LEVEL	- 0: DSI trigger signal is a pulse input, a positive edge detected on the DSI trigger signal triggers a new scan. - 1: DSI trigger signal is a level input, as long as the DSI trigger signal remains high the SAR will do continuous scans. Default Value: 0

9.1.2 SAR_SAMPLE_CTRL (continued)

17	SAR_DSI_TRIGGER_EN	- 0: firmware trigger only: disable hardware (DSI) trigger. - 1: enable hardware (DSI) trigger (e.g. from TCPWM, GPIO or UDB). Default Value: 0
16	SAR_CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) or hardware (DSI) trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. Default Value: 0
7	SAR_AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in the sample resolution, i.e. 12 bits. Default Value: 0
6 : 4	SAR_AVG_CNT	Averaging Count for channels that have over sampling enabled (AVG_EN). A channel will be sampled back to back (1<<(AVG_CNT+1)) = [2..256] times before the result is stored and the next enabled channel is sampled (1st order accumulate and dump filter). If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). Default Value: 0
3	SAR_DIFFERENTIAL_SIGNED	Output data from a differential conversion as a signed value Default Value: 1 **0x0: UNSIGNED:** result data is unsigned (zero extended if needed) **0x1: SIGNED:** Default: result data is signed (sign extended if needed)
2	SAR_SINGLE_ENDED_SIGNED	Output data from a single ended conversion as a signed value Default Value: 0 **0x0: UNSIGNED:** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED:** result data is signed (sign extended if needed)
1	SAR_LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default Value: 0
0	SAR_SUB_RESOLUTION	Conversion resolution for channels that have sub-resolution enabled (RESOLUTION=1) (otherwise resolution is 12-bit). Default Value: 0 **0x0: 8B:** 8-bit. **0x1: 10B:** 10-bit.

9.1.3 SAR_SAMPLE_TIME01

Sample time specification ST0 and ST1

Address: 0x401A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAR_SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAR_SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAR_SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAR_SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAR_SAMPLE_TIME1	Sample time1 Default Value: 4
9 : 0	SAR_SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is half a clock less than specified here. The minimum sample time is 194ns, which is 3.5 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 4

9.1.4 SAR_SAMPLE_TIME23

Sample time specification ST2 and ST3

Address: 0x401A0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAR_SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAR_SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAR_SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAR_SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAR_SAMPLE_TIME3	Sample time3 Default Value: 4
9 : 0	SAR_SAMPLE_TIME2	Sample time2 Default Value: 4

9.1.5 SAR_RANGE_THRES

Global range detect threshold register.

Address: 0x401A0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAR_RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SAR_RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAR_RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SAR_RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	SAR_RANGE_HIGH	high threshold for range detect Default Value: 0
15 : 0	SAR_RANGE_LOW	low threshold for range detect Default Value: 0

9.1.6 SAR_RANGE_COND

Global range detect mode register.

Address: 0x401A001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	SAR_RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	SAR_RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW:** result < RANGE_LOW **0x1: INSIDE:** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE:** RANGE_HIGH <= result **0x3: OUTSIDE:** result < RANGE_LOW || RANGE_HIGH <= result

9.1.7 SAR_CHAN_EN

Enable bits for the channels

Address: 0x401A0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAR_CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SAR_CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default Value: 0

9.1.8 SAR_START_CTRL

Start control register (firmware trigger).

Address: 0x401A0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							SAR_FW_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SAR_FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default Value: 0

9.1.9 SAR_CHAN_CONFIG

Channel configuration register.

Address: 0x401A0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SAR_PORT_ADDR [6:4]			None	SAR_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAR_SAMPLE_TIME_SEL [13:12]		None	SAR_AVG_EN	SAR_RESOLUTION	SAR_DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	SAR_DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	SAR_DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAR_SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	SAR_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	SAR_RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0

9.1.9 SAR_CHAN_CONFIG (continued)

		0x0: 12B: 12-bit resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	SAR_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	SAR_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x6: AROUTE_VIRT:** AROUTE virtual port **0x7: SARMUX_VIRT:** SARMUX virtual port
2 : 0	SAR_PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default Value: 0

9.1.10 SAR_CHAN_WORK

Channel working data register

Address: 0x401A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SAR_WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	SAR_WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SAR_CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	SAR_CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	SAR_WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

9.1.11 SAR_CHAN_RESULT

Channel result data register

Address: 0x401A0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SAR_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SAR_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	SAR_CHAN_RESULT_VALID_MIR	SAR_RANGE_INTR_MIR	SAR_SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	SAR_CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	SAR_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SAR_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	SAR_RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

9.1.12 SAR_CHAN_WORK_VALID

Channel working data register valid bits

Address: 0x401A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SAR_CHAN_WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	SAR_CHAN_WORK_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_CHAN_WORK_VALID	If set the corresponding WORK data is valid, i.e. was already sampled during the current scan. Default Value: 0

9.1.13 SAR_CHAN_RESULT_VALID

Channel result data register valid bits

Address: 0x401A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SAR_CHAN_RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	SAR_CHAN_RESULT_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_CHAN_RESULT_VALID	If set the corresponding RESULT data is valid, i.e. was sampled during the last scan. Default Value: 0

9.1.14 SAR_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x401A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			SAR_CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	SAR_BUSY	SAR_SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	SAR_BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SAR_SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default Value: 0
4 : 0	SAR_CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default Value: 0

9.1.15 SAR_AVG_STAT

Current averaging status (for debug)

Address: 0x401A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SAR_CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SAR_CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				SAR_CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SAR_CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	SAR_CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default Value: 0
19 : 0	SAR_CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

9.1.16 SAR_INTR

Interrupt request register.

Address: 0x401A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	SAR_INJ_COLLISION_INTR	SAR_INJ_RANGE_INTR	SAR_INJ_SATURATE_INTR	SAR_INJ_EOC_INTR	SAR_DSI_COLLISION_INTR	SAR_FW_COLLISION_INTR	SAR_OVERFLOW_INTR	SAR_EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SAR_INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit. Default Value: 0
6	SAR_INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0
5	SAR_INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

9.1.16 SAR_INTR (continued)

4	SAR_INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit. Default Value: 0
3	SAR_DSI_COLLISION_INTR	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
2	SAR_FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
1	SAR_OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. Default Value: 0
0	SAR_EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

9.1.17 SAR_INTR_SET

Interrupt set request register

Address: 0x401A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	SAR_INJ_COLLISION_SET	SAR_INJ_RANGE_SET	SAR_INJ_SATURATE_SET	SAR_INJ_EOC_SET	SAR_DSI_COLLISION_SET	SAR_FW_COLLISION_SET	SAR_OVERFLOW_SET	SAR_EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SAR_INJ_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	SAR_INJ_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	SAR_INJ_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	SAR_INJ_EOC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	SAR_DSI_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	SAR_FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	SAR_OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

9.1.17 SAR_INTR_SET (continued)

0	SAR_EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

9.1.18 SAR_INTR_MASK

Interrupt mask register.

Address: 0x401A0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SAR_INJ_COLLISION_MASK	SAR_INJ_RANGE_MASK	SAR_INJ_SATURATE_MASK	SAR_INJ_EOC_MASK	SAR_DSI_COLLISION_MASK	SAR_FW_COLLISION_MASK	SAR_OVERFLOW_MASK	SAR_EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SAR_INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	SAR_INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	SAR_INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	SAR_INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	SAR_DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	SAR_FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SAR_OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

9.1.18 SAR_INTR_MASK (continued)

0	SAR_EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

9.1.19 SAR_INTR_MASKED

Interrupt masked request register

Address: 0x401A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SAR_INJ_COLLISION_MASKED	SAR_INJ_RANGE_MASKED	SAR_INJ_SATURATE_MASKED	SAR_INJ_EOC_MASKED	SAR_DSI_COLLISION_MASKED	SAR_FW_COLLISION_MASKED	SAR_OVERFLOW_MASKED	SAR_EOS_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SAR_INJ_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	SAR_INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	SAR_INJ_SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	SAR_INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	SAR_DSI_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	SAR_FW_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	SAR_OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

9.1.19 SAR_INTR_MASKED (continued)

0	SAR_EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

9.1.20 SAR_SATURATE_INTR

Saturate interrupt request register.

Address: 0x401A0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SAR_SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SAR_SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

9.1.21 SAR_SATURATE_INTR_SET

Saturate interrupt set request register

Address: 0x401A0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SAR_SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SAR_SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

9.1.22 SAR_SATURATE_INTR_MASK

Saturate interrupt mask register.

Address: 0x401A0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAR_SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SAR_SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

9.1.23 SAR_SATURATE_INTR_MASKED

Saturate interrupt masked request register

Address: 0x401A022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SAR_SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SAR_SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

9.1.24 SAR_RANGE_INTR

Range detect interrupt request register.

Address: 0x401A0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SAR_RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SAR_RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

9.1.25 SAR_RANGE_INTR_SET

Range detect interrupt set request register

Address: 0x401A0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SAR_RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SAR_RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

9.1.26 SAR_RANGE_INTR_MASK

Range detect interrupt mask register.

Address: 0x401A0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAR_RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SAR_RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

9.1.27 SAR_RANGE_INTR_MASKED

Range interrupt masked request register

Address: 0x401A023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SAR_RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SAR_RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SAR_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

9.1.28 SAR_INTR_CAUSE

Interrupt cause register

Address: 0x401A0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SAR_INJ_COLLISION_MASKED_MIR	SAR_INJ_RANGE_MASKED_MIR	SAR_INJ_SATURATE_MASKED_MIR	SAR_INJ_EOC_MASKED_MIR	SAR_DSI_COLLISION_MASKED_MIR	SAR_FW_COLLISION_MASKED_MIR	SAR_OVERFLOW_MASKED_MIR	SAR_EOS_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	SAR_RANGE_MASKED_RED	SAR_SATURATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	SAR_RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SAR_SATURATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	SAR_INJ_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
6	SAR_INJ_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
5	SAR_INJ_SATURATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
4	SAR_INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

9.1.28 SAR_INTR_CAUSE (continued)

3	SAR_DSI_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
2	SAR_FW_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	SAR_OVERFLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	SAR_EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

9.1.29 SAR_INJ_CHAN_CONFIG

Injection channel configuration register.

Address: 0x401A0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SAR_INJ_PORT_ADDR [6:4]			None	SAR_INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAR_INJ_SAMPLE_TIME_SEL [13:12]		None	SAR_INJ_AVG_EN	SAR_INJ_RESOLU-TION	SAR_INJ_DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	SAR_INJ_START_EN	SAR_INJ_TAILGATING	None [29:24]					

Bits	Name	Description
31	SAR_INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default Value: 0
30	SAR_INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	SAR_INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	SAR_INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0

9.1.29 SAR_INJ_CHAN_CONFIG (continued)

9	SAR_INJ_RESOLUTION	Resolution for this channel. Default Value: 0 **0x0: 12B:** 12-bit resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	SAR_INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	SAR_INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x6: AROUTE_VIRT:** AROUTE virtual port **0x7: SARMUX_VIRT:** SARMUX virtual port
2 : 0	SAR_INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default Value: 0

9.1.30 SAR_INJ_RESULT

Injection channel result register

Address: 0x401A0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SAR_INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SAR_INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	SAR_INJ_EOC_INTR_MIR	SAR_INJ_RANGE_INTR_MIR	SAR_INJ_SATURATE_INTR_MIR	SAR_INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	SAR_INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
30	SAR_INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
29	SAR_INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
28	SAR_INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
15 : 0	SAR_INJ_RESULT	SAR conversion result of the channel. Default Value: Undefined

9.1.31 SAR_MUX_SWITCH0

SARMUX Firmware switch controls

Address: 0x401A0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	SAR_MUX_FW_P7_VPLUS	SAR_MUX_FW_P6_VPLUS	SAR_MUX_FW_P5_VPLUS	SAR_MUX_FW_P4_VPLUS	SAR_MUX_FW_P3_VPLUS	SAR_MUX_FW_P2_VPLUS	SAR_MUX_FW_P1_VPLUS	SAR_MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	SAR_MUX_FW_P7_VMINUS	SAR_MUX_FW_P6_VMINUS	SAR_MUX_FW_P5_VMINUS	SAR_MUX_FW_P4_VMINUS	SAR_MUX_FW_P3_VMINUS	SAR_MUX_FW_P2_VMINUS	SAR_MUX_FW_P1_VMINUS	SAR_MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	SAR_MUX_FW_SARBUS1_VPLUS	SAR_MUX_FW_SARBUS0_VPLUS	SAR_MUX_FW_AMUXBUSB_VMINUS	SAR_MUX_FW_AMUXBUSA_VMINUS	SAR_MUX_FW_AMUXBUSB_VPLUS	SAR_MUX_FW_AMUXBUSA_VPLUS	SAR_MUX_FW_TEMP_VPLUS	SAR_MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [31:30]		SAR_MUX_FW_P7_COREIO3	SAR_MUX_FW_P6_COREIO2	SAR_MUX_FW_P5_COREIO1	SAR_MUX_FW_P4_COREIO0	SAR_MUX_FW_SARBUS1_VMINUS	SAR_MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	SAR_MUX_FW_P7_COREIO3	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with '1' to set bit. Default Value: 0
28	SAR_MUX_FW_P6_COREIO2	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with '1' to set bit. Default Value: 0
27	SAR_MUX_FW_P5_COREIO1	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with '1' to set bit. Default Value: 0
26	SAR_MUX_FW_P4_COREIO0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with '1' to set bit. Default Value: 0

9.1.31 SAR_MUX_SWITCH0 (continued)

25	SAR_MUX_FW_SARBUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0
24	SAR_MUX_FW_SARBUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	SAR_MUX_FW_SARBUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0
22	SAR_MUX_FW_SARBUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	SAR_MUX_FW_AMUXBUSB_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	SAR_MUX_FW_AMUXBUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	SAR_MUX_FW_AMUXBUSB_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	SAR_MUX_FW_AMUXBUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	SAR_MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit. Default Value: 0
16	SAR_MUX_FW_VSSA_VMINUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0
15	SAR_MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit. Default Value: 0
14	SAR_MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit. Default Value: 0
13	SAR_MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit. Default Value: 0
12	SAR_MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit. Default Value: 0
11	SAR_MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit. Default Value: 0
10	SAR_MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit. Default Value: 0

9.1.31 SAR_MUX_SWITCH0 (continued)

9	SAR_MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit. Default Value: 0
8	SAR_MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit. Default Value: 0
7	SAR_MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit. Default Value: 0
6	SAR_MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit. Default Value: 0
5	SAR_MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit. Default Value: 0
4	SAR_MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit. Default Value: 0
3	SAR_MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit. Default Value: 0
2	SAR_MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit. Default Value: 0
1	SAR_MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit. Default Value: 0
0	SAR_MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit. Default Value: 0

9.1.32 SAR_MUX_SWITCH_CLEAR0

SARMUX Firmware switch control clear

Address: 0x401A0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	SAR_MUX_FW_P7_VPLUS	SAR_MUX_FW_P6_VPLUS	SAR_MUX_FW_P5_VPLUS	SAR_MUX_FW_P4_VPLUS	SAR_MUX_FW_P3_VPLUS	SAR_MUX_FW_P2_VPLUS	SAR_MUX_FW_P1_VPLUS	SAR_MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	SAR_MUX_FW_P7_VMINUS	SAR_MUX_FW_P6_VMINUS	SAR_MUX_FW_P5_VMINUS	SAR_MUX_FW_P4_VMINUS	SAR_MUX_FW_P3_VMINUS	SAR_MUX_FW_P2_VMINUS	SAR_MUX_FW_P1_VMINUS	SAR_MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	SAR_MUX_FW_SARBUS1_VPLUS	SAR_MUX_FW_SARBUS0_VPLUS	SAR_MUX_FW_AMUXBUSB_VMINUS	SAR_MUX_FW_AMUXBUSA_VMINUS	SAR_MUX_FW_AMUXBUSB_VPLUS	SAR_MUX_FW_AMUXBUSA_VPLUS	SAR_MUX_FW_TEMP_VPLUS	SAR_MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [31:30]		SAR_MUX_FW_P7_COREIO3	SAR_MUX_FW_P6_COREIO2	SAR_MUX_FW_P5_COREIO1	SAR_MUX_FW_P4_COREIO0	SAR_MUX_FW_SARBUS1_VMINUS	SAR_MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	SAR_MUX_FW_P7_COREIO3	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
28	SAR_MUX_FW_P6_COREIO2	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
27	SAR_MUX_FW_P5_COREIO1	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
26	SAR_MUX_FW_P4_COREIO0	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

9.1.32 SAR_MUX_SWITCH_CLEAR0 (continued)

25	SAR_MUX_FW_SARBUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
24	SAR_MUX_FW_SARBUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	SAR_MUX_FW_SARBUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	SAR_MUX_FW_SARBUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
21	SAR_MUX_FW_AMUXBUSB_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	SAR_MUX_FW_AMUXBUSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	SAR_MUX_FW_AMUXBUSB_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	SAR_MUX_FW_AMUXBUSA_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	SAR_MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	SAR_MUX_FW_VSSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	SAR_MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	SAR_MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	SAR_MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	SAR_MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	SAR_MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	SAR_MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	SAR_MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	SAR_MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	SAR_MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	SAR_MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	SAR_MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	SAR_MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

9.1.32 SAR_MUX_SWITCH_CLEAR0 (continued)

3	SAR_MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
2	SAR_MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	SAR_MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	SAR_MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

9.1.33 SAR_MUX_SWITCH_HW_CTRL

SARMUX switch hardware control

Address: 0x401A0340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SAR_MUX_HW_CTRL_P7	SAR_MUX_HW_CTRL_P6	SAR_MUX_HW_CTRL_P5	SAR_MUX_HW_CTRL_P4	SAR_MUX_HW_CTRL_P3	SAR_MUX_HW_CTRL_P2	SAR_MUX_HW_CTRL_P1	SAR_MUX_HW_CTRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	SAR_MUX_HW_CTRL_SARBUS1	SAR_MUX_HW_CTRL_SARBUS0	None [21:20]		SAR_MUX_HW_CTRL_AMUX-BUSB	SAR_MUX_HW_CTRL_AMUXBU-SA	SAR_MUX_HW_CTRL_TEMP	SAR_MUX_HW_CTRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	SAR_MUX_HW_CTRL_SARBUS1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus1 switches. Default Value: 0
22	SAR_MUX_HW_CTRL_SARBUS0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus0 switches. Default Value: 0
19	SAR_MUX_HW_CTRL_AMUXBUSB	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusb switches. Default Value: 0
18	SAR_MUX_HW_CTRL_AMUXBUSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusa switches. Default Value: 0

9.1.33 SAR_MUX_SWITCH_HW_CTRL (continued)

17	SAR_MUX_HW_CTRL_TEMP	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for temp switch. Default Value: 0
16	SAR_MUX_HW_CTRL_VSSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for vssa switch. Default Value: 0
7	SAR_MUX_HW_CTRL_P7	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P7 switches. Default Value: 0
6	SAR_MUX_HW_CTRL_P6	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P6 switches. Default Value: 0
5	SAR_MUX_HW_CTRL_P5	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P5 switches. Default Value: 0
4	SAR_MUX_HW_CTRL_P4	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P4 switches. Default Value: 0
3	SAR_MUX_HW_CTRL_P3	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P3 switches. Default Value: 0
2	SAR_MUX_HW_CTRL_P2	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P2 switches. Default Value: 0
1	SAR_MUX_HW_CTRL_P1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P1 switches. Default Value: 0
0	SAR_MUX_HW_CTRL_P0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P0 switches. Default Value: 0

9.1.34 SAR_MUX_SWITCH_STATUS

SARMUX switch status

Address: 0x401A0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SAR_MUX_FW_P7_VPLUS	SAR_MUX_FW_P6_VPLUS	SAR_MUX_FW_P5_VPLUS	SAR_MUX_FW_P4_VPLUS	SAR_MUX_FW_P3_VPLUS	SAR_MUX_FW_P2_VPLUS	SAR_MUX_FW_P1_VPLUS	SAR_MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SAR_MUX_FW_P7_VMINUS	SAR_MUX_FW_P6_VMINUS	SAR_MUX_FW_P5_VMINUS	SAR_MUX_FW_P4_VMINUS	SAR_MUX_FW_P3_VMINUS	SAR_MUX_FW_P2_VMINUS	SAR_MUX_FW_P1_VMINUS	SAR_MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SAR_MUX_FW_SARBUS1_VPLUS	SAR_MUX_FW_SARBUS0_VPLUS	SAR_MUX_FW_AMUXBUSB_VMINUS	SAR_MUX_FW_AMUXBUSA_VMINUS	SAR_MUX_FW_AMUXBUSB_VPLUS	SAR_MUX_FW_AMUXBUSA_VPLUS	SAR_MUX_FW_TEMP_VPLUS	SAR_MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						SAR_MUX_FW_SARBUS1_VMINUS	SAR_MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	SAR_MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
24	SAR_MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
23	SAR_MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
22	SAR_MUX_FW_SARBUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

9.1.34 SAR_MUX_SWITCH_STATUS (continued)

21	SAR_MUX_FW_AMUXBUSB_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
20	SAR_MUX_FW_AMUXBUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
19	SAR_MUX_FW_AMUXBUSB_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
18	SAR_MUX_FW_AMUXBUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
17	SAR_MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
16	SAR_MUX_FW_VSSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
15	SAR_MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
14	SAR_MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
13	SAR_MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
12	SAR_MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
11	SAR_MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
10	SAR_MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
9	SAR_MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
8	SAR_MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
7	SAR_MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
6	SAR_MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
5	SAR_MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
4	SAR_MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
3	SAR_MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
2	SAR_MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
1	SAR_MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
0	SAR_MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

9.1.35 SAR_PUMP_CTRL

Switch pump control

Address: 0x401A0380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							SAR_CLOCK_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	SAR_ENABLED	None [30:24]						

Bits	Name	Description
31	SAR_ENABLED	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted. Default Value: 0
0	SAR_CLOCK_SEL	Clock select: 0=external clock, 1=internal clock (deprecated). Default Value: 0

10 Serial Communications Block Registers

This section discusses the Serial Communications Block (SCB) registers. It lists all the registers in mapping tables, in address order.

10.1 Register Details

Register Name	Address
SCB0_CTRL	0x40060000
SCB0_STATUS	0x40060004
SCB0_SPI_CTRL	0x40060020
SCB0_SPI_STATUS	0x40060024
SCB0_UART_CTRL	0x40060040
SCB0_UART_TX_CTRL	0x40060044
SCB0_UART_RX_CTRL	0x40060048
SCB0_UART_RX_STATUS	0x4006004C
SCB0_I2C_CTRL	0x40060060
SCB0_I2C_STATUS	0x40060064
SCB0_I2C_M_CMD	0x40060068
SCB0_I2C_S_CMD	0x4006006C
SCB0_I2C_CFG	0x40060070
SCB0_TX_CTRL	0x40060200
SCB0_TX_FIFO_CTRL	0x40060204
SCB0_TX_FIFO_STATUS	0x40060208
SCB0_TX_FIFO_WR	0x40060240
SCB0_RX_CTRL	0x40060300
SCB0_RX_FIFO_CTRL	0x40060304
SCB0_RX_FIFO_STATUS	0x40060308
SCB0_RX_MATCH	0x40060310
SCB0_RX_FIFO_RD	0x40060340
SCB0_RX_FIFO_RD_SILENT	0x40060344
SCB0_EZ_DATA	0x40060400
SCB0_INTR_CAUSE	0x40060E00
SCB0_INTR_I2C_EC	0x40060E80
SCB0_INTR_I2C_EC_MASK	0x40060E88

Register Name	Address
SCB0_INTR_I2C_EC_MASKED	0x40060E8C
SCB0_INTR_SPI_EC	0x40060EC0
SCB0_INTR_SPI_EC_MASK	0x40060EC8
SCB0_INTR_SPI_EC_MASKED	0x40060ECC
SCB0_INTR_M	0x40060F00
SCB0_INTR_M_SET	0x40060F04
SCB0_INTR_M_MASK	0x40060F08
SCB0_INTR_M_MASKED	0x40060F0C
SCB0_INTR_S	0x40060F40
SCB0_INTR_S_SET	0x40060F44
SCB0_INTR_S_MASK	0x40060F48
SCB0_INTR_S_MASKED	0x40060F4C
SCB0_INTR_TX	0x40060F80
SCB0_INTR_TX_SET	0x40060F84
SCB0_INTR_TX_MASK	0x40060F88
SCB0_INTR_TX_MASKED	0x40060F8C
SCB0_INTR_RX	0x40060FC0
SCB0_INTR_RX_SET	0x40060FC4
SCB0_INTR_RX_MASK	0x40060FC8
SCB0_INTR_RX_MASKED	0x40060FCC
SCB1_CTRL	0x40070000
SCB1_STATUS	0x40070004
SCB1_SPI_CTRL	0x40070020
SCB1_SPI_STATUS	0x40070024
SCB1_UART_CTRL	0x40070040
SCB1_UART_TX_CTRL	0x40070044
SCB1_UART_RX_CTRL	0x40070048
SCB1_UART_RX_STATUS	0x4007004C
SCB1_I2C_CTRL	0x40070060
SCB1_I2C_STATUS	0x40070064
SCB1_I2C_M_CMD	0x40070068
SCB1_I2C_S_CMD	0x4007006C
SCB1_I2C_CFG	0x40070070
SCB1_TX_CTRL	0x40070200
SCB1_TX_FIFO_CTRL	0x40070204
SCB1_TX_FIFO_STATUS	0x40070208
SCB1_TX_FIFO_WR	0x40070240
SCB1_RX_CTRL	0x40070300
SCB1_RX_FIFO_CTRL	0x40070304
SCB1_RX_FIFO_STATUS	0x40070308
SCB1_RX_MATCH	0x40070310
SCB1_RX_FIFO_RD	0x40070340

Register Name	Address
SCB1_RX_FIFO_RD_SILENT	0x40070344
SCB1_EZ_DATA	0x40070400
SCB1_INTR_CAUSE	0x40070E00
SCB1_INTR_I2C_EC	0x40070E80
SCB1_INTR_I2C_EC_MASK	0x40070E88
SCB1_INTR_I2C_EC_MASKED	0x40070E8C
SCB1_INTR_SPI_EC	0x40070EC0
SCB1_INTR_SPI_EC_MASK	0x40070EC8
SCB1_INTR_SPI_EC_MASKED	0x40070ECC
SCB1_INTR_M	0x40070F00
SCB1_INTR_M_SET	0x40070F04
SCB1_INTR_M_MASK	0x40070F08
SCB1_INTR_M_MASKED	0x40070F0C
SCB1_INTR_S	0x40070F40
SCB1_INTR_S_SET	0x40070F44
SCB1_INTR_S_MASK	0x40070F48
SCB1_INTR_S_MASKED	0x40070F4C
SCB1_INTR_TX	0x40070F80
SCB1_INTR_TX_SET	0x40070F84
SCB1_INTR_TX_MASK	0x40070F88
SCB1_INTR_TX_MASKED	0x40070F8C
SCB1_INTR_RX	0x40070FC0
SCB1_INTR_RX_SET	0x40070FC4
SCB1_INTR_RX_MASK	0x40070FC8
SCB1_INTR_RX_MASKED	0x40070FCC

10.1.1 SCB0_CTRL

Generic control register.

Address: 0x40060000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SCB0_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					SCB0_EZ_MODE	SCB0_EC_OP_MODE	SCB0_EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB0_BLOCK	SCB0_ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	SCB0_ENABLED	None [30:26]					SCB0_MODE [25:24]	

Bits	Name	Description
31	SCB0_ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	SCB0_MODE	Mode of operation (3: Reserved) Default Value: 3

10.1.1 SCB0_CTRL (continued)

		0x0: I2C: Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	SCB0_BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	SCB0_ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). This field is used in the I2C mode, to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. This field is used in the multi-processor UART receiver mode, to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
10	SCB0_EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola mode 0 is supported and the trasmitter should use continuous data frames; i.e. data frames. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	SCB0_EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola mode 0 is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	SCB0_EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola mode 0 is supported. In UART mode this field should be '0'. Default Value: 0

10.1.1 SCB0_CTRL (continued)

3 : 0	SCB0_OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15] (at a system frequency of 48 MHz, the maximum bit rate is 12 Mbps). In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and SPI_CTRL.LATE_MISO_SAMPLE: - MEDIAN is '0' and LATE_MISO_SAMPLE is '0': IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and LATE_MISO_SAMPLE is '1': IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and LATE_MISO_SAMPLE is '0': IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and LATE_MISO_SAMPLE is '1': IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The above requirements provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. IP clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. IP clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. IP clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. IP clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. IP clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. IP clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

10.1.2 SCB0_STATUS

Generic status register.

Address: 0x40060004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							SCB0_EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SCB0_EC_BUSY	Inidicates whether the externaly clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

10.1.3 SCB0_SPI_CTRL

SPI control register.

Address: 0x40060020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			SCB0_LATE_MISO_SAMPLE	SCB0_CPOL	SCB0_CPHA	SCB0_SELECT_PREDE	SCB0_CONTINUOUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SCB0_LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	SCB0_MASTER_MODE	None [30:28]			SCB0_SLAVE_SELECT [27:26]		SCB0_MODE [25:24]	

Bits	Name	Description
31	SCB0_MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SCB0_SLAVE_SELECT	Selects one of the four SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	SCB0_MODE	Submode of SPI operation (3: Reserved). Default Value: 3

10.1.3 SCB0_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	SCB0_LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master mode. Not applicable in National Semiconductors submode. When '0', the SPI master MISO line is connected to the SPI MISO pin. When '1', the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
4	SCB0_LATE_MISO_SAMPLE	Only applicable in master mode. Changes the SCLK edge on which MISO is captured. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	SCB0_CPOL	Only applicable in SPI Motorola submode. Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	SCB0_CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured. - CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SCB0_SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0

10.1.3 SCB0_SPI_CTRL (continued)

0	SCB0_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are send out with slave deselection. This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported. Default Value: 0

10.1.4 SCB0_SPI_STATUS

SPI status register.

Address: 0x40060024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							SCB0_BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB0_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SCB0_EZ_ADDR	SPI slave EZ address. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
0	SCB0_BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

10.1.5 SCB0_UART_CTRL

UART control register.

Address: 0x40060040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SCB0_LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SCB0_MODE [25:24]	

Bits	Name	Description
25 : 24	SCB0_MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	SCB0_LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line is connected to the TX pin and the receiver RX line is connected to the RX pin. When '1', the transmitter TX line is connected to the receiver RX line. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

10.1.6 SCB0_UART_TX_CTRL

UART transmitter control register.

Address: 0x40060044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		SCB0_PARITY_ENABLED	SCB0_PARITY	None	SCB0_STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							SCB0_RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	SCB0_RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	SCB0_PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	SCB0_PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	SCB0_STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

10.1.7 SCB0_UART_RX_CTRL

UART receiver control register.

Address: 0x40060048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	SCB0_POLARITY	SCB0_PARITY_ENABLED	SCB0_PARITY	None	SCB0_STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SCB0_SKIP_START	SCB0_LIN_MODE	None	SCB0_MP_MODE	SCB0_DROP_ON_FRAME_ERROR	SCB0_DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				SCB0_BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	SCB0_BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

10.1.7 SCB0_UART_RX_CTRL (continued)

13	SCB0_SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	SCB0_LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	SCB0_MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	SCB0_DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	SCB0_DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	SCB0_POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	SCB0_PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	SCB0_PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

10.1.7 SCB0_UART_RX_CTRL (continued)

2 : 0	SCB0_STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

10.1.8 SCB0_UART_RX_STATUS

UART receiver status register.

Address: 0x4006004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SCB0_BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				SCB0_BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	SCB0_BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

10.1.9 SCB0_I2C_CTRL

I2C control register.

Address: 0x40060060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SCB0_LOW_PHASE_OVS [7:4]				SCB0_HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	SCB0_S_NOT_READY_DATA_NACK	SCB0_S_NOT_READY_ADDR_NACK	SCB0_S_READY_DATA_ACK	SCB0_S_READY_ADDR_ACK	SCB0_S_GENERAL_IGNORE	None	SCB0_M_NOT_READY_DATA_NACK	SCB0_M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SCB0_LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	SCB0_MASTER_MODE	SCB0_SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	SCB0_MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SCB0_SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	SCB0_LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

10.1.9 SCB0_I2C_CTRL (continued)

15	SCB0_S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	SCB0_S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	SCB0_S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	SCB0_S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	SCB0_S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	SCB0_M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	SCB0_M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

10.1.9 SCB0_I2C_CTRL (continued)

7 : 4	SCB0_LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8
3 : 0	SCB0_HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

10.1.10 SCB0_I2C_STATUS

I2C status register.

Address: 0x40060064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None			R
HW Access	None		W	W	None			W
Name	None [7:6]		SCB0_M_READ	SCB0_S_READ	None [3:1]			SCB0_BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB0_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SCB0_EZ_ADDR	I2C slave EZ address. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
5	SCB0_M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	SCB0_S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

10.1.10 SCB0_I2C_STATUS (continued)

0	SCB0_BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

10.1.11 SCB0_I2C_M_CMD

I2C master command register.

Address: 0x40060068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			SCB0_M_STOP	SCB0_M_NACK	SCB0_M_ACK	SCB0_M_START_ON_IDLE	SCB0_M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SCB0_M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	SCB0_M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	SCB0_M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

10.1.11 SCB0_I2C_M_CMD (continued)

1	SCB0_M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	SCB0_M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

10.1.12 SCB0_I2C_S_CMD

I2C slave command register.

Address: 0x4006006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						SCB0_S_NACK	SCB0_S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SCB0_S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	SCB0_S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

10.1.13 SCB0_I2C_CFG

I2C configuration register.

Address: 0x40060070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SCB0_SCL_FILT_TRIM [7:6]		SCB0_SCL_FILT_HYS [5:4]		SCB0_SDA_FILT_TRIM [3:2]		SCB0_SDA_FILT_HYS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				SCB0_SDA_FILT_OUT_TRIM [11:10]		SCB0_SDA_FILT_OUT_HYS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB0_SDA_FILT_ENABLED	SCB0_SDA_FILT_HS

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [31:28]				SCB0_SDA_FILT_OUT_ENABLED	SCB0_SDA_FILT_OUT_HS	SCB0_SCL_FILT_ENABLED	SCB0_SCL_FILT_HS

Bits	Name	Description
27	SCB0_SDA_FILT_OUT_ENABLED	I2C SDA output delay filter enabled. Default Value: 0
26	SCB0_SDA_FILT_OUT_HS	When '0': 50 ns filter. When '1': 10 ns filter. Default Value: 0
25	SCB0_SCL_FILT_ENABLED	I2C SCL filter enabled. Default Value: 1
24	SCB0_SCL_FILT_HS	When '0': 50 ns filter. When '1': 10 ns filter. Default Value: 0
17	SCB0_SDA_FILT_ENABLED	I2C SDA filter enabled. Default Value: 1
16	SCB0_SDA_FILT_HS	When '0': 50 ns filter. When '1': 10 ns filter. Default Value: 0

10.1.13 SCB0_I2C_CFG (continued)

11 : 10	SCB0_SDA_FILT_OUT_TRIM	Trim bits for the I2C SDA filter in the SDA output path (for SCL to SDA hold delay). Default Value: 3
9 : 8	SCB0_SDA_FILT_OUT_HYS	Trim bits for the I2C SDA filter in the SDA output path (for SCL to SDA hold delay). Default Value: 2
7 : 6	SCB0_SCL_FILT_TRIM	Trim bits for the I2C SCL filter. Default Value: 2
5 : 4	SCB0_SCL_FILT_HYS	Trim bits for the I2C SCL filter. Default Value: 2
3 : 2	SCB0_SDA_FILT_TRIM	Trim bits for the I2C SDA filter. Default Value: 2
1 : 0	SCB0_SDA_FILT_HYS	Trim bits for the I2C SDA filter. Default Value: 2

10.1.14 SCB0_TX_CTRL

Transmitter control register.

Address: 0x40060200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SCB0_DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							SCB0_MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	SCB0_ENABLED	None [30:24]						

Bits	Name	Description
31	SCB0_ENABLED	Transmitter enabled. The transmitter should be enabled for all protocols that transmit data (from either the EZ memory or from the TX FIFO). If not enabled, the protocol may not function as it does not get data to transmit. Default Value: 0
8	SCB0_MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	SCB0_DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

10.1.15 SCB0_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40060204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					SCB0_TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB0_FREEZE	SCB0_CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	SCB0_FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	SCB0_CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
2 : 0	SCB0_TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the amount of this field, a transmitter trigger event is generated. Default Value: 0

10.1.16 SCB0_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40060208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				SCB0_USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SCB0_SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					SCB0_RD_PTR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					R		
HW Access	None					W		
Name	None [31:27]					SCB0_WR_PTR [26:24]		

Bits	Name	Description
26 : 24	SCB0_WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
18 : 16	SCB0_RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SCB0_SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
3 : 0	SCB0_USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to 8. Default Value: 0

10.1.17 SCB0_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40060240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	SCB0_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	SCB0_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCB0_DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Default Value: 0

10.1.18 SCB0_RX_CTRL

Receiver control register.

Address: 0x40060300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SCB0_DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SCB0_MEDIAN	SCB0_MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	SCB0_ENABLED	None [30:24]						

Bits	Name	Description
31	SCB0_ENABLED	Receiver enabled. The receiver should be enabled for all protocols that receive data (to either the EZ memory or to the RX FIFO). If not enabled, the protocol may not function or received data may get lost. Default Value: 0
9	SCB0_MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	SCB0_MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	SCB0_DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

10.1.19 SCB0_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40060304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					SCB0_TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB0_FREEZE	SCB0_CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	SCB0_FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	SCB0_CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
2 : 0	SCB0_TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the amount of this field, a receiver trigger event is generated. Default Value: 7

10.1.20 SCB0_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40060308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				SCB0_USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SCB0_SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					SCB0_RD_PTR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					R		
HW Access	None					W		
Name	None [31:27]					SCB0_WR_PTR [26:24]		

Bits	Name	Description
26 : 24	SCB0_WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
18 : 16	SCB0_RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SCB0_SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
3 : 0	SCB0_USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to 8. Default Value: 0

10.1.21 SCB0_RX_MATCH

Slave address and mask register.

Address: 0x40060310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCB0_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SCB0_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	SCB0_MASK	Slave device address mask. This field is a 8 bit mask that specifies which of the ADDR field bits in the SCB0_RX_MATCH_ADDR register take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	SCB0_ADDR	Slave device address. For UART multi-processor moden all eight bits a reused. For I2C, bit 0 of the register is not used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the next 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

10.1.22 SCB0_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40060340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SCB0_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB0_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCB0_DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB0_RX_FIFO_RD_SILENT register. Default Value: Undefined

10.1.23 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40060344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SCB0_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB0_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCB0_DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Default Value: Undefined

10.1.24 SCB0_EZ_DATA

EZ memory location registers.

Address: 0x40060400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SCB0_EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	SCB0_EZ_DATA	Data in EZ memory location. Default Value: Undefined

10.1.25 SCB0_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40060E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SCB0_SPI_EC	SCB0_I2C_EC	SCB0_RX	SCB0_TX	SCB0_S	SCB0_M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SCB0_SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	SCB0_I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	SCB0_RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	SCB0_TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	SCB0_S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	SCB0_M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

10.1.26 SCB0_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40060E80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					SCB0_EZ_WRITE_STOP	SCB0_EZ_STOP	SCB0_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB0_EZ_WRITE_STOP	STOP detection after a write transfer occurred (only available in EZ mode). Active on detected STOP. Only generated when a write transfer to the EZ memory occurred between the STOP and the preceding START (note that multiple REPEATED STARTs may have happened in between the START and STOP). If a write transfer only modified the EZ address, and not the EZ memory, this event is NOT generated. Only used in EZ mode and when EC_OP is '1'. Default Value: 0
1	SCB0_EZ_STOP	STOP detection (only available in EZ mode). Active on detected STOP. Only used in EZ mode and when EC_OP is '1'. Default Value: 0
0	SCB0_WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

10.1.27 SCB0_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40060E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SCB0_EZ_WRITE_STOP	SCB0_EZ_STOP	SCB0_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB0_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB0_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB0_WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.28 SCB0_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40060E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					SCB0_EZ_WRITE_STOP	SCB0_EZ_STOP	SCB0_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB0_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB0_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB0_WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

10.1.29 SCB0_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40060EC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					SCB0_EZ_WRITE_STOP	SCB0_EZ_STOP	SCB0_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB0_EZ_WRITE_STOP	STOP detection after a write transfer occurred. Active on detected STOP (deselection) when externally clocked operation is on (only available in EZ mode). If a write transfer only transferred the EZ address, this event will not be generated. This event is an indication that a EZ memory location may have changed contents. Only used in EZ mode and when EC_OP is '1'. Default Value: 0
1	SCB0_EZ_STOP	STOP detection. Active on detected STOP (deselection) when externally clocked operation is on (only available in EZ mode). Only used in EZ mode and when EC_OP is '1'. Default Value: 0
0	SCB0_WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

10.1.30 SCB0_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40060EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SCB0_EZ_WRITE_STOP	SCB0_EZ_STOP	SCB0_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB0_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB0_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB0_WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.31 SCB0_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40060ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					SCB0_EZ_WRITE_STOP	SCB0_EZ_STOP	SCB0_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB0_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB0_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB0_WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

10.1.32 SCB0_INTR_M

Master interrupt request register.

Address: 0x40060F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			SCB0_I2C_STOP	None	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SCB0_SPI_DONE	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB0_SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Only used when EC_OP is '0'. Default Value: 0
8	SCB0_I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Only used when EC_OP is '0'. Default Value: 0
4	SCB0_I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Only used when EC_OP is '0'. Default Value: 0

10.1.32 SCB0_INTR_M (continued)

2	SCB0_I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Only used when EC_OP is '0'. Default Value: 0
1	SCB0_I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Only used when EC_OP is '0'. Default Value: 0
0	SCB0_I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Only used when EC_OP is '0'. Default Value: 0

10.1.33 SCB0_INTR_M_SET

Master interrupt set request register

Address: 0x40060F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			SCB0_I2C_STOP	None	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SCB0_SPI_DONE	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB0_SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	SCB0_I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	SCB0_I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	SCB0_I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	SCB0_I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	SCB0_I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.34 SCB0_INTR_M_MASK

Master interrupt mask register.

Address: 0x40060F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			SCB0_I2C_STOP	None	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SCB0_SPI_DONE	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB0_SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB0_I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	SCB0_I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	SCB0_I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB0_I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB0_I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.35 SCB0_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40060F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			SCB0_I2C_STOP	None	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SCB0_SPI_DONE	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB0_SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB0_I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	SCB0_I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	SCB0_I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB0_I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB0_I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

10.1.36 SCB0_INTR_S

Slave interrupt request register.

Address: 0x40060F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	SCB0_I2C_GENERAL	SCB0_I2C_ADDR_MATCH	SCB0_I2C_START	SCB0_I2C_STOP	SCB0_I2C_WRITE_STOP	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SCB0_SPI_BUS_ERROR	SCB0_SPI_EZ_STOP	SCB0_SPI_EZ_WRITE_STOP	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is '0'. Default Value: 0
10	SCB0_SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occured. Only used when EC_OP is '0'. Default Value: 0
9	SCB0_SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Only used when EC_OP is '0'. Default Value: 0

10.1.36 SCB0_INTR_S (continued)

8	SCB0_I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behaviour. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is '0'. Default Value: 0
7	SCB0_I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Only used when EC_OP is '0'. Default Value: 0
6	SCB0_I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Only used when EC_OP is '0'. Default Value: 0
5	SCB0_I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is NOT set. Instead the Firmware can rely on I2C_ADDR_MATCH and I2C_GENERAL. Only used when EC_OP is '0'. Default Value: 0
4	SCB0_I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers seperated by a REPEATED START can be distinguished and potentially treated seperately by the Firmware. Note that the second I2C transfer may be to a different slave address. Only used when EC_OP is '0'. Default Value: 0
3	SCB0_I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). In non EZ mode, the event is detected on any I2C write transfer intended for this slave. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an EZ address, will not result in this event being detected). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers seperated by a REPEATED START can be distinguished and potentially treated seperately by the Firmware. Note that the second I2C transfer may be to a different slave address. Only used when EC_OP is '0'. Default Value: 0
2	SCB0_I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Only used when EC_OP is '0'. Default Value: 0

10.1.36 SCB0_INTR_S (continued)

1	SCB0_I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Only used when EC_OP is '0'. Default Value: 0
0	SCB0_I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behaviour. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is '0'. Default Value: 0

10.1.37 SCB0_INTR_S_SET

Slave interrupt set request register.

Address: 0x40060F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	SCB0_I2C_GENERAL	SCB0_I2C_ADDR_MATCH	SCB0_I2C_START	SCB0_I2C_STOP	SCB0_I2C_WRITE_STOP	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SCB0_SPI_BUS_ERROR	SCB0_SPI_EZ_STOP	SCB0_SPI_EZ_WRITE_STOP	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SCB0_SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SCB0_SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	SCB0_I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	SCB0_I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	SCB0_I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.37 SCB0_INTR_S_SET (continued)

5	SCB0_I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	SCB0_I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	SCB0_I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	SCB0_I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	SCB0_I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	SCB0_I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.38 SCB0_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40060F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SCB0_I2C_GENERAL	SCB0_I2C_ADDR_MATCH	SCB0_I2C_START	SCB0_I2C_STOP	SCB0_I2C_WRITE_STOP	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SCB0_SPI_BUS_ERROR	SCB0_SPI_EZ_STOP	SCB0_SPI_EZ_WRITE_STOP	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SCB0_SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SCB0_SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB0_I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	SCB0_I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	SCB0_I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.38 SCB0_INTR_S_MASK (continued)

5	SCB0_I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	SCB0_I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	SCB0_I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	SCB0_I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB0_I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB0_I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.39 SCB0_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40060F4C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SCB0_I2C_GENERAL	SCB0_I2C_ADDR_MATCH	SCB0_I2C_START	SCB0_I2C_STOP	SCB0_I2C_WRITE_STOP	SCB0_I2C_ACK	SCB0_I2C_NACK	SCB0_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SCB0_SPI_BUS_ERROR	SCB0_SPI_EZ_STOP	SCB0_SPI_EZ_WRITE_STOP	SCB0_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SCB0_SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SCB0_SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB0_I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	SCB0_I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	SCB0_I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

10.1.39 SCB0_INTR_S_MASKED (continued)

5	SCB0_I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	SCB0_I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	SCB0_I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	SCB0_I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB0_I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB0_I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

10.1.40 SCB0_INTR_TX

Transmitter interrupt request register.

Address: 0x40060F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	SCB0_EMPTY	None [3:2]		SCB0_NOT_FULL	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					SCB0_UART_ARB_LOST	SCB0_UART_DONE	SCB0_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB0_UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	SCB0_UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	SCB0_UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	SCB0_BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

10.1.40 SCB0_INTR_TX (continued)

6	SCB0_UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
5	SCB0_OVERFLOW	Attempt to write to a full TX FIFO. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
4	SCB0_EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in non EZ mode and when EC_OP is '0'. Default Value: 1
1	SCB0_NOT_FULL	TX FIFO is not full. Only used in non EZ mode and when EC_OP is '0'. Default Value: 1
0	SCB0_TRIGGER	Less entries in the TX FIFO than the value specified by TRIGGER_LEVEL in SCB0_TX_FIFO_CTL. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0

10.1.41 SCB0_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40060F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	SCB0_EMPTY	None [3:2]		SCB0_NOT_FULL	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					SCB0_UART_ARB_LOST	SCB0_UART_DONE	SCB0_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB0_UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SCB0_UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	SCB0_UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	SCB0_BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	SCB0_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	SCB0_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	SCB0_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 1

10.1.41 SCB0_INTR_TX_SET (continued)

1	SCB0_NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 1
0	SCB0_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.42 SCB0_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40060F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	SCB0_EMPTY	None [3:2]		SCB0_NOT_FULL	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					SCB0_UART_ARB_LOST	SCB0_UART_DONE	SCB0_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB0_UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SCB0_UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB0_UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	SCB0_BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	SCB0_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	SCB0_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	SCB0_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.42 SCB0_INTR_TX_MASK (continued)

1	SCB0_NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB0_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.43 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40060F8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	SCB0_EMPTY	None [3:2]		SCB0_NOT_FULL	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					SCB0_UART_ARB_LOST	SCB0_UART_DONE	SCB0_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB0_UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	SCB0_UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB0_UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	SCB0_BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	SCB0_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	SCB0_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	SCB0_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

10.1.43 SCB0_INTR_TX_MASKED (continued)

1	SCB0_NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB0_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

10.1.44 SCB0_INTR_RX

Receiver interrupt request register.

Address: 0x40060FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	None	SCB0_FULL	SCB0_NOT_EMPTY	None	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SCB0_BREAK_DETECT	SCB0_BAUD_DETECT	SCB0_PARITY_ERROR	SCB0_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	SCB0_BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

10.1.44 SCB0_INTR_RX (continued)

9	SCB0_PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	SCB0_FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	SCB0_BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	SCB0_UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
5	SCB0_OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
3	SCB0_FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
2	SCB0_NOT_EMPTY	RX FIFO is not empty. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
0	SCB0_TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB0_RX_FIFO_CTL. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0

10.1.45 SCB0_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40060FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	None	SCB0_FULL	SCB0_NOT_EMPTY	None	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SCB0_BREAK_DETECT	SCB0_BAUD_DETECT	SCB0_PARITY_ERROR	SCB0_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	SCB0_BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	SCB0_PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	SCB0_FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	SCB0_BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	SCB0_UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	SCB0_OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

10.1.45 SCB0_INTR_RX_SET (continued)

3	SCB0_FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	SCB0_NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	SCB0_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.46 SCB0_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40060FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	None	SCB0_FULL	SCB0_NOT_EMPTY	None	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SCB0_BREAK_DETECT	SCB0_BAUD_DETECT	SCB0_PARITY_ERROR	SCB0_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SCB0_BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SCB0_PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB0_FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	SCB0_BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	SCB0_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	SCB0_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.46 SCB0_INTR_RX_MASK (continued)

3	SCB0_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	SCB0_NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB0_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.47 SCB0_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40060FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	SCB0_BLOCKED	SCB0_UNDERFLOW	SCB0_OVERFLOW	None	SCB0_FULL	SCB0_NOT_EMPTY	None	SCB0_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SCB0_BREAK_DETECT	SCB0_BAUD_DETECT	SCB0_PARITY_ERROR	SCB0_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB0_BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	SCB0_BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	SCB0_PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB0_FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	SCB0_BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	SCB0_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	SCB0_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

10.1.47 SCB0_INTR_RX_MASKED (continued)

3	SCB0_FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	SCB0_NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB0_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

10.1.48 SCB1_CTRL

Generic control register.

Address: 0x40070000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SCB1_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					SCB1_EZ_MODE	SCB1_EC_OP_MODE	SCB1_EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB1_BLOCK	SCB1_ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	SCB1_ENABLED	None [30:26]					SCB1_MODE [25:24]	

Bits	Name	Description
31	SCB1_ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	SCB1_MODE	Mode of operation (3: Reserved) Default Value: 3

10.1.48 SCB1_CTRL (continued)

		0x0: I2C: Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	SCB1_BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	SCB1_ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). This field is used in the I2C mode, to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. This field is used in the multi-processor UART receiver mode, to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
10	SCB1_EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola mode 0 is supported and the trasmitter should use continuous data frames; i.e. data frames. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	SCB1_EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola mode 0 is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	SCB1_EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola mode 0 is supported. In UART mode this field should be '0'. Default Value: 0

10.1.48 SCB1_CTRL (continued)

3 : 0	SCB1_OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15] (at a system frequency of 48 MHz, the maximum bit rate is 12 Mbps). In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and SPI_CTRL.LATE_MISO_SAMPLE: - MEDIAN is '0' and LATE_MISO_SAMPLE is '0': IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and LATE_MISO_SAMPLE is '1': IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and LATE_MISO_SAMPLE is '0': IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and LATE_MISO_SAMPLE is '1': IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The above requirements provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. IP clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. IP clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. IP clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. IP clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. IP clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. IP clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

10.1.49 SCB1_STATUS

Generic status register.

Address: 0x40070004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							SCB1_EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SCB1_EC_BUSY	Inidicates whether the externaly clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

10.1.50 SCB1_SPI_CTRL

SPI control register.

Address: 0x40070020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			SCB1_LATE_MISO_SAMPLE	SCB1_CPOL	SCB1_CPHA	SCB1_SELECT_PREDE	SCB1_CONTINUOUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SCB1_LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	SCB1_MASTER_MODE	None [30:28]			SCB1_SLAVE_SELECT [27:26]		SCB1_MODE [25:24]	

Bits	Name	Description
31	SCB1_MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SCB1_SLAVE_SELECT	Selects one of the four SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	SCB1_MODE	Submode of SPI operation (3: Reserved). Default Value: 3

10.1.50 SCB1_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	SCB1_LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master mode. Not applicable in National Semiconductors submode. When '0', the SPI master MISO line is connected to the SPI MISO pin. When '1', the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
4	SCB1_LATE_MISO_SAMPLE	Only applicable in master mode. Changes the SCLK edge on which MISO is captured. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	SCB1_CPOL	Only applicable in SPI Motorola submode. Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	SCB1_CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured. - CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SCB1_SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0

10.1.50 SCB1_SPI_CTRL (continued)

0	SCB1_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are send out with slave deselection. This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported. Default Value: 0

10.1.51 SCB1_SPI_STATUS

SPI status register.

Address: 0x40070024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							SCB1_BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB1_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SCB1_EZ_ADDR	SPI slave EZ address. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
0	SCB1_BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

10.1.52 SCB1_UART_CTRL

UART control register.

Address: 0x40070040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SCB1_LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SCB1_MODE [25:24]	

Bits	Name	Description
25 : 24	SCB1_MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	SCB1_LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line is connected to the TX pin and the receiver RX line is connected to the RX pin. When '1', the transmitter TX line is connected to the receiver RX line. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

10.1.53 SCB1_UART_TX_CTRL

UART transmitter control register.

Address: 0x40070044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		SCB1_PARITY_ENABLED	SCB1_PARITY	None	SCB1_STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							SCB1_RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	SCB1_RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	SCB1_PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	SCB1_PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	SCB1_STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

10.1.54 SCB1_UART_RX_CTRL

UART receiver control register.

Address: 0x40070048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	SCB1_POLARITY	SCB1_PARITY_ENABLED	SCB1_PARITY	None	SCB1_STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SCB1_SKIP_START	SCB1_LIN_MODE	None	SCB1_MP_MODE	SCB1_DROP_ON_FRAME_ERROR	SCB1_DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				SCB1_BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	SCB1_BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

10.1.54 SCB1_UART_RX_CTRL (continued)

13	SCB1_SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	SCB1_LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	SCB1_MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	SCB1_DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	SCB1_DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	SCB1_POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	SCB1_PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	SCB1_PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

10.1.54 SCB1_UART_RX_CTRL (continued)

2 : 0	SCB1_STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

10.1.55 SCB1_UART_RX_STATUS

UART receiver status register.

Address: 0x4007004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SCB1_BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				SCB1_BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	SCB1_BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

10.1.56 SCB1_I2C_CTRL

I2C control register.

Address: 0x40070060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SCB1_LOW_PHASE_OVS [7:4]				SCB1_HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	SCB1_S_NOT_READY_DATA_NACK	SCB1_S_NOT_READY_ADDR_NACK	SCB1_S_READY_DATA_ACK	SCB1_S_READY_ADDR_ACK	SCB1_S_GENERAL_IGNORE	None	SCB1_M_NOT_READY_DATA_NACK	SCB1_M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SCB1_LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	SCB1_MASTER_MODE	SCB1_SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	SCB1_MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SCB1_SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	SCB1_LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

10.1.56 SCB1_I2C_CTRL (continued)

15	SCB1_S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	SCB1_S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	SCB1_S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	SCB1_S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	SCB1_S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	SCB1_M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	SCB1_M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

10.1.56 SCB1_I2C_CTRL (continued)

7 : 4	SCB1_LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8
3 : 0	SCB1_HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

10.1.57 SCB1_I2C_STATUS

I2C status register.

Address: 0x40070064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None			R
HW Access	None		W	W	None			W
Name	None [7:6]		SCB1_M_READ	SCB1_S_READ	None [3:1]			SCB1_BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB1_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SCB1_EZ_ADDR	I2C slave EZ address. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
5	SCB1_M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	SCB1_S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

10.1.57 SCB1_I2C_STATUS (continued)

0	SCB1_BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

10.1.58 SCB1_I2C_M_CMD

I2C master command register.

Address: 0x40070068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			SCB1_M_STOP	SCB1_M_NACK	SCB1_M_ACK	SCB1_M_START_ON_IDLE	SCB1_M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SCB1_M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	SCB1_M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	SCB1_M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

10.1.58 SCB1_I2C_M_CMD (continued)

1	SCB1_M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	SCB1_M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

10.1.59 SCB1_I2C_S_CMD

I2C slave command register.

Address: 0x4007006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						SCB1_S_NACK	SCB1_S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SCB1_S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	SCB1_S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

10.1.60 SCB1_I2C_CFG

I2C configuration register.

Address: 0x40070070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SCB1_SCL_FILT_TRIM [7:6]		SCB1_SCL_FILT_HYS [5:4]		SCB1_SDA_FILT_TRIM [3:2]		SCB1_SDA_FILT_HYS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				SCB1_SDA_FILT_OUT_TRIM [11:10]		SCB1_SDA_FILT_OUT_HYS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB1_SDA_FILT_ENABLED	SCB1_SDA_FILT_HS

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [31:28]				SCB1_SDA_FILT_OUT_ENABLED	SCB1_SDA_FILT_OUT_HS	SCB1_SCL_FILT_ENABLED	SCB1_SCL_FILT_HS

Bits	Name	Description
27	SCB1_SDA_FILT_OUT_ENABLED	I2C SDA output delay filter enabled. Default Value: 0
26	SCB1_SDA_FILT_OUT_HS	When '0': 50 ns filter. When '1': 10 ns filter. Default Value: 0
25	SCB1_SCL_FILT_ENABLED	I2C SCL filter enabled. Default Value: 1
24	SCB1_SCL_FILT_HS	When '0': 50 ns filter. When '1': 10 ns filter. Default Value: 0
17	SCB1_SDA_FILT_ENABLED	I2C SDA filter enabled. Default Value: 1
16	SCB1_SDA_FILT_HS	When '0': 50 ns filter. When '1': 10 ns filter. Default Value: 0

10.1.60 SCB1_I2C_CFG (continued)

11 : 10	SCB1_SDA_FILT_OUT_TRIM	Trim bits for the I2C SDA filter in the SDA output path (for SCL to SDA hold delay). Default Value: 3
9 : 8	SCB1_SDA_FILT_OUT_HYS	Trim bits for the I2C SDA filter in the SDA output path (for SCL to SDA hold delay). Default Value: 2
7 : 6	SCB1_SCL_FILT_TRIM	Trim bits for the I2C SCL filter. Default Value: 2
5 : 4	SCB1_SCL_FILT_HYS	Trim bits for the I2C SCL filter. Default Value: 2
3 : 2	SCB1_SDA_FILT_TRIM	Trim bits for the I2C SDA filter. Default Value: 2
1 : 0	SCB1_SDA_FILT_HYS	Trim bits for the I2C SDA filter. Default Value: 2

10.1.61 SCB1_TX_CTRL

Transmitter control register.

Address: 0x40070200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SCB1_DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							SCB1_MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	SCB1_ENABLED	None [30:24]						

Bits	Name	Description
31	SCB1_ENABLED	Transmitter enabled. The transmitter should be enabled for all protocols that transmit data (from either the EZ memory or from the TX FIFO). If not enabled, the protocol may not function as it does not get data to transmit. Default Value: 0
8	SCB1_MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	SCB1_DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

10.1.62 SCB1_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40070204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					SCB1_TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB1_FREEZE	SCB1_CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	SCB1_FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	SCB1_CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
2 : 0	SCB1_TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the amount of this field, a transmitter trigger event is generated. Default Value: 0

10.1.63 SCB1_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40070208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				SCB1_USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SCB1_SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					SCB1_RD_PTR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					R		
HW Access	None					W		
Name	None [31:27]					SCB1_WR_PTR [26:24]		

Bits	Name	Description
26 : 24	SCB1_WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
18 : 16	SCB1_RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SCB1_SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
3 : 0	SCB1_USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to 8. Default Value: 0

10.1.64 SCB1_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40070240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	SCB1_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	SCB1_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCB1_DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Default Value: 0

10.1.65 SCB1_RX_CTRL

Receiver control register.

Address: 0x40070300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SCB1_DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SCB1_MEDIAN	SCB1_MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	SCB1_ENABLED	None [30:24]						

Bits	Name	Description
31	SCB1_ENABLED	Receiver enabled. The receiver should be enabled for all protocols that receive data (to either the EZ memory or to the RX FIFO). If not enabled, the protocol may not function or received data may get lost. Default Value: 0
9	SCB1_MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	SCB1_MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	SCB1_DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

10.1.66 SCB1_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40070304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					SCB1_TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						SCB1_FREEZE	SCB1_CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	SCB1_FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	SCB1_CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
2 : 0	SCB1_TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the amount of this field, a receiver trigger event is generated. Default Value: 7

10.1.67 SCB1_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40070308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				SCB1_USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SCB1_SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					SCB1_RD_PTR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					R		
HW Access	None					W		
Name	None [31:27]					SCB1_WR_PTR [26:24]		

Bits	Name	Description
26 : 24	SCB1_WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
18 : 16	SCB1_RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SCB1_SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
3 : 0	SCB1_USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to 8. Default Value: 0

10.1.68 SCB1_RX_MATCH

Slave address and mask register.

Address: 0x40070310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCB1_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SCB1_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	SCB1_MASK	Slave device address mask. This field is a 8 bit mask that specifies which of the ADDR field bits in the SCB1_RX_MATCH_ADDR register take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	SCB1_ADDR	Slave device address. For UART multi-processor moden all eight bits a reused. For I2C, bit 0 of the register is not used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the next 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

10.1.69 SCB1_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40070340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SCB1_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB1_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCB1_DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB1_RX_FIFO_RD_SILENT register. Default Value: Undefined

10.1.70 SCB1_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40070344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SCB1_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SCB1_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCB1_DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Default Value: Undefined

10.1.71 SCB1_EZ_DATA

EZ memory location registers.

Address: 0x40070400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SCB1_EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	SCB1_EZ_DATA	Data in EZ memory location. Default Value: Undefined

10.1.72 SCB1_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40070E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SCB1_SPI_EC	SCB1_I2C_EC	SCB1_RX	SCB1_TX	SCB1_S	SCB1_M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SCB1_SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	SCB1_I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	SCB1_RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	SCB1_TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	SCB1_S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	SCB1_M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

10.1.73 SCB1_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40070E80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					SCB1_EZ_WRITE_STOP	SCB1_EZ_STOP	SCB1_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB1_EZ_WRITE_STOP	STOP detection after a write transfer occurred (only available in EZ mode). Active on detected STOP. Only generated when a write transfer to the EZ memory occurred between the STOP and the preceding START (note that multiple REPEATED STARTs may have happened in between the START and STOP). If a write transfer only modified the EZ address, and not the EZ memory, this event is NOT generated. Only used in EZ mode and when EC_OP is '1'. Default Value: 0
1	SCB1_EZ_STOP	STOP detection (only available in EZ mode). Active on detected STOP. Only used in EZ mode and when EC_OP is '1'. Default Value: 0
0	SCB1_WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

10.1.74 SCB1_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40070E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SCB1_EZ_WRITE_STOP	SCB1_EZ_STOP	SCB1_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB1_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB1_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB1_WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.75 SCB1_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40070E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					SCB1_EZ_WRITE_STOP	SCB1_EZ_STOP	SCB1_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB1_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB1_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB1_WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

10.1.76 SCB1_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40070EC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					SCB1_EZ_WRITE_STOP	SCB1_EZ_STOP	SCB1_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB1_EZ_WRITE_STOP	STOP detection after a write transfer occurred. Active on detected STOP (deselection) when externally clocked operation is on (only available in EZ mode). If a write transfer only transferred the EZ address, this event will not be generated. This event is an indication that a EZ memory location may have changed contents. Only used in EZ mode and when EC_OP is '1'. Default Value: 0
1	SCB1_EZ_STOP	STOP detection. Active on detected STOP (deselection) when externally clocked operation is on (only available in EZ mode). Only used in EZ mode and when EC_OP is '1'. Default Value: 0
0	SCB1_WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

10.1.77 SCB1_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40070EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SCB1_EZ_WRITE_STOP	SCB1_EZ_STOP	SCB1_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB1_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB1_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB1_WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.78 SCB1_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40070ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					SCB1_EZ_WRITE_STOP	SCB1_EZ_STOP	SCB1_WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SCB1_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB1_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB1_WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

10.1.79 SCB1_INTR_M

Master interrupt request register.

Address: 0x40070F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			SCB1_I2C_STOP	None	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SCB1_SPI_DONE	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB1_SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Only used when EC_OP is '0'. Default Value: 0
8	SCB1_I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Only used when EC_OP is '0'. Default Value: 0
4	SCB1_I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Only used when EC_OP is '0'. Default Value: 0

10.1.79 SCB1_INTR_M (continued)

2	SCB1_I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Only used when EC_OP is '0'. Default Value: 0
1	SCB1_I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Only used when EC_OP is '0'. Default Value: 0
0	SCB1_I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Only used when EC_OP is '0'. Default Value: 0

10.1.80 SCB1_INTR_M_SET

Master interrupt set request register

Address: 0x40070F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			SCB1_I2C_STOP	None	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SCB1_SPI_DONE	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB1_SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	SCB1_I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	SCB1_I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	SCB1_I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	SCB1_I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	SCB1_I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.81 SCB1_INTR_M_MASK

Master interrupt mask register.

Address: 0x40070F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			SCB1_I2C_STOP	None	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SCB1_SPI_DONE	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB1_SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB1_I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	SCB1_I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	SCB1_I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB1_I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB1_I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.82 SCB1_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40070F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			SCB1_I2C_STOP	None	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SCB1_SPI_DONE	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCB1_SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB1_I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	SCB1_I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	SCB1_I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB1_I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB1_I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

10.1.83 SCB1_INTR_S

Slave interrupt request register.

Address: 0x40070F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	SCB1_I2C_GENERAL	SCB1_I2C_ADDR_MATCH	SCB1_I2C_START	SCB1_I2C_STOP	SCB1_I2C_WRITE_STOP	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SCB1_SPI_BUS_ERROR	SCB1_SPI_EZ_STOP	SCB1_SPI_EZ_WRITE_STOP	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is '0'. Default Value: 0
10	SCB1_SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occured. Only used when EC_OP is '0'. Default Value: 0
9	SCB1_SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Only used when EC_OP is '0'. Default Value: 0

10.1.83 SCB1_INTR_S (continued)

8	SCB1_I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behaviour. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is '0'. Default Value: 0
7	SCB1_I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Only used when EC_OP is '0'. Default Value: 0
6	SCB1_I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Only used when EC_OP is '0'. Default Value: 0
5	SCB1_I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is NOT set. Instead the Firmware can rely on I2C_ADDR_MATCH and I2C_GENERAL. Only used when EC_OP is '0'. Default Value: 0
4	SCB1_I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers seperated by a REPEATED START can be distinguished and potentially treated seperately by the Firmware. Note that the second I2C transfer may be to a different slave address. Only used when EC_OP is '0'. Default Value: 0
3	SCB1_I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). In non EZ mode, the event is detected on any I2C write transfer intended for this slave. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an EZ address, will not result in this event being detected). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers seperated by a REPEATED START can be distinguished and potentially treated seperately by the Firmware. Note that the second I2C transfer may be to a different slave address. Only used when EC_OP is '0'. Default Value: 0
2	SCB1_I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Only used when EC_OP is '0'. Default Value: 0

10.1.83 SCB1_INTR_S (continued)

1	SCB1_I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Only used when EC_OP is '0'. Default Value: 0
0	SCB1_I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behaviour. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is '0'. Default Value: 0

10.1.84 SCB1_INTR_S_SET

Slave interrupt set request register.

Address: 0x40070F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	SCB1_I2C_GENERAL	SCB1_I2C_ADDR_MATCH	SCB1_I2C_START	SCB1_I2C_STOP	SCB1_I2C_WRITE_STOP	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SCB1_SPI_BUS_ERROR	SCB1_SPI_EZ_STOP	SCB1_SPI_EZ_WRITE_STOP	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SCB1_SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SCB1_SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	SCB1_I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	SCB1_I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	SCB1_I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.84 SCB1_INTR_S_SET (continued)

5	SCB1_I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	SCB1_I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	SCB1_I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	SCB1_I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	SCB1_I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	SCB1_I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.85 SCB1_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40070F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SCB1_I2C_GENERAL	SCB1_I2C_ADDR_MATCH	SCB1_I2C_START	SCB1_I2C_STOP	SCB1_I2C_WRITE_STOP	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SCB1_SPI_BUS_ERROR	SCB1_SPI_EZ_STOP	SCB1_SPI_EZ_WRITE_STOP	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SCB1_SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SCB1_SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB1_I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	SCB1_I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	SCB1_I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.85 SCB1_INTR_S_MASK (continued)

5	SCB1_I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	SCB1_I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	SCB1_I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	SCB1_I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SCB1_I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB1_I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.86 SCB1_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40070F4C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	SCB1_I2C_GENERAL	SCB1_I2C_ADDR_MATCH	SCB1_I2C_START	SCB1_I2C_STOP	SCB1_I2C_WRITE_STOP	SCB1_I2C_ACK	SCB1_I2C_NACK	SCB1_I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SCB1_SPI_BUS_ERROR	SCB1_SPI_EZ_STOP	SCB1_SPI_EZ_WRITE_STOP	SCB1_I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SCB1_SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SCB1_SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB1_I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	SCB1_I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	SCB1_I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

10.1.86 SCB1_INTR_S_MASKED (continued)

5	SCB1_I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	SCB1_I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	SCB1_I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	SCB1_I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	SCB1_I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB1_I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

10.1.87 SCB1_INTR_TX

Transmitter interrupt request register.

Address: 0x40070F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	SCB1_EMPTY	None [3:2]		SCB1_NOT_FULL	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					SCB1_UART_ARB_LOST	SCB1_UART_DONE	SCB1_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB1_UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	SCB1_UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	SCB1_UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	SCB1_BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

10.1.87 SCB1_INTR_TX (continued)

6	SCB1_UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
5	SCB1_OVERFLOW	Attempt to write to a full TX FIFO. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
4	SCB1_EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in non EZ mode and when EC_OP is '0'. Default Value: 1
1	SCB1_NOT_FULL	TX FIFO is not full. Only used in non EZ mode and when EC_OP is '0'. Default Value: 1
0	SCB1_TRIGGER	Less entries in the TX FIFO than the value specified by TRIGGER_LEVEL in SCB1_TX_FIFO_CTL. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0

10.1.88 SCB1_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40070F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	SCB1_EMPTY	None [3:2]		SCB1_NOT_FULL	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					SCB1_UART_ARB_LOST	SCB1_UART_DONE	SCB1_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB1_UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SCB1_UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	SCB1_UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	SCB1_BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	SCB1_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	SCB1_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	SCB1_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 1

10.1.88 SCB1_INTR_TX_SET (continued)

1	SCB1_NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 1
0	SCB1_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.89 SCB1_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40070F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	SCB1_EMPTY	None [3:2]		SCB1_NOT_FULL	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					SCB1_UART_ARB_LOST	SCB1_UART_DONE	SCB1_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB1_UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SCB1_UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB1_UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	SCB1_BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	SCB1_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	SCB1_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	SCB1_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.89 SCB1_INTR_TX_MASK (continued)

1	SCB1_NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB1_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.90 SCB1_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40070F8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	SCB1_EMPTY	None [3:2]		SCB1_NOT_FULL	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					SCB1_UART_ARB_LOST	SCB1_UART_DONE	SCB1_UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SCB1_UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	SCB1_UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB1_UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	SCB1_BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	SCB1_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	SCB1_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	SCB1_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

10.1.90 SCB1_INTR_TX_MASKED (continued)

1	SCB1_NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB1_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

10.1.91 SCB1_INTR_RX

Receiver interrupt request register.

Address: 0x40070FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	None	SCB1_FULL	SCB1_NOT_EMPTY	None	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SCB1_BREAK_DETECT	SCB1_BAUD_DETECT	SCB1_PARITY_ERROR	SCB1_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	SCB1_BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

10.1.91 SCB1_INTR_RX (continued)

9	SCB1_PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	SCB1_FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	SCB1_BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	SCB1_UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
5	SCB1_OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
3	SCB1_FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
2	SCB1_NOT_EMPTY	RX FIFO is not empty. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0
0	SCB1_TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB1_RX_FIFO_CTL. Only used in non EZ mode and when EC_OP is '0'. Default Value: 0

10.1.92 SCB1_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40070FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	None	SCB1_FULL	SCB1_NOT_EMPTY	None	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SCB1_BREAK_DETECT	SCB1_BAUD_DETECT	SCB1_PARITY_ERROR	SCB1_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	SCB1_BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	SCB1_PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	SCB1_FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	SCB1_BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	SCB1_UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	SCB1_OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

10.1.92 SCB1_INTR_RX_SET (continued)

3	SCB1_FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	SCB1_NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	SCB1_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

10.1.93 SCB1_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40070FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	None	SCB1_FULL	SCB1_NOT_EMPTY	None	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SCB1_BREAK_DETECT	SCB1_BAUD_DETECT	SCB1_PARITY_ERROR	SCB1_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SCB1_BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SCB1_PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	SCB1_FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	SCB1_BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	SCB1_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	SCB1_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.93 SCB1_INTR_RX_MASK (continued)

3	SCB1_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	SCB1_NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	SCB1_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

10.1.94 SCB1_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40070FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	SCB1_BLOCKED	SCB1_UNDERFLOW	SCB1_OVERFLOW	None	SCB1_FULL	SCB1_NOT_EMPTY	None	SCB1_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SCB1_BREAK_DETECT	SCB1_BAUD_DETECT	SCB1_PARITY_ERROR	SCB1_FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SCB1_BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	SCB1_BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	SCB1_PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	SCB1_FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	SCB1_BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	SCB1_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	SCB1_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

10.1.94 SCB1_INTR_RX_MASKED (continued)

3	SCB1_FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	SCB1_NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	SCB1_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

11 Programmable Clock Registers

This section discusses the Programmable Clock registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register Name	Address
CLK_DIVIDER_A	0x40020000
CLK_DIVIDER_B	0x40020040
CLK_DIVIDER_C	0x40020080
CLK_DIVIDER_FRAC_A	0x40020100
CLK_DIVIDER_FRAC_B	0x40020140
CLK_DIVIDER_FRAC_C	0x40020180
CLK_SELECT	0x40020200

11.1.1 CLK_DIVIDER_A

Clock Divider Configuration

Address: 0x40020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_A [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_A [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CLK_ENABLE_A	None [30:24]						

Bits	Name	Description
31	CLK_ENABLE_A	Enable divider A. Default Value: 0
15 : 0	CLK_DIVIDER_A	Divider value for divider A in the row. OUTPUT= INPUT / (DIVIDER_A+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction Default Value: 0

11.1.2 CLK_DIVIDER_B

Clock Divider Configuration

Address: 0x40020040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_B [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_B [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CLK_ENABLE_B	CLK_CASCADE_A_B	None [29:24]					

Bits	Name	Description
31	CLK_ENABLE_B	Enable divider B. Default Value: 0
30	CLK_CASCADE_A_B	Cascade divider A into divider B Default Value: 0
15 : 0	CLK_DIVIDER_B	Divider value for divider B in the row. OUTPUT= INPUT / (DIVIDER_B+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction . Also note that dividide by 1 does not work if CASCADE_A_B=1. Default Value: 0

11.1.3 CLK_DIVIDER_C

Clock Divider Configuration

Address: 0x40020080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_C [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_C [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CLK_ENABLE_C	CLK_CASCADE_B_C	None [29:24]					

Bits	Name	Description
31	CLK_ENABLE_C	Enable divider C. Default Value: 0
30	CLK_CASCADE_B_C	Cascade divider B into divider C Default Value: 0
15 : 0	CLK_DIVIDER_C	Divider value for divider C in the row. OUTPUT= INPUT / (DIVIDER_C+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction. Also note that dividide by 1 does not work if CASCADE_A_B=1. Default Value: 0

11.1.4 CLK_DIVIDER_FRAC_A

Frac Divider Configuration

Address: 0x40020100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_A [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_A [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			CLK_FRAC_A [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CLK_ENABLE_A	None [30:24]						

Bits	Name	Description
31	CLK_ENABLE_A	Enable divider A. Default Value: 0
20 : 16	CLK_FRAC_A	Fractional divider value: 0/32 .. 31/32 Default Value: 0
15 : 0	CLK_DIVIDER_A	Divider value for divider A in the row. OUTPUT= INPUT / (DIVIDER_A+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction. Default Value: 0

11.1.5 CLK_DIVIDER_FRAC_B

Frac Divider Configuration

Address: 0x40020140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_B [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_B [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			CLK_FRAC_B [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CLK_ENABLE_B	CLK_CASCADE_A_B	None [29:24]					

Bits	Name	Description
31	CLK_ENABLE_B	Enable divider B. Default Value: 0
30	CLK_CASCADE_A_B	Cascade divider A into divider B Default Value: 0
20 : 16	CLK_FRAC_B	Fractional divider value: 0/32 .. 31/32 Default Value: 0
15 : 0	CLK_DIVIDER_B	Divider value for divider B in the row. OUTPUT= INPUT / (DIVIDER_B+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction. Also note that dividide by 1 does not work if CASCADE_A_B=1. Default Value: 0

11.1.6 CLK_DIVIDER_FRAC_C

Frac Divider Configuration

Address: 0x40020180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_C [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CLK_DIVIDER_C [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			CLK_FRAC_C [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CLK_ENABLE_C	CLK_CASCADE_B_C	None [29:24]					

Bits	Name	Description
31	CLK_ENABLE_C	Enable divider C. Default Value: 0
30	CLK_CASCADE_B_C	Cascade divider B into divider C Default Value: 0
20 : 16	CLK_FRAC_C	Fractional divider value: 0/32 .. 31/32 Default Value: 0
15 : 0	CLK_DIVIDER_C	Divider value for divider C in the row. OUTPUT= INPUT / (DIVIDER_C+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction. Also note that dividide by 1 does not work if CASCADE_A_B=1. Default Value: 0

11.1.7 CLK_SELECT

Clock Routing Configuration

Address: 0x40020200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		CLK_DIVIDER_ABC [5:4]		CLK_DIVIDER_N [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	CLK_DIVIDER_ABC	Select which divider from row to use. Default Value: 0 **0x0: OFF:** Clock disabled **0x1: A:** Divider N-A **0x2: B:** Divider N-B **0x3: C:** Divider N-C
3 : 0	CLK_DIVIDER_N	Select divider bank row to source clock from. Addressed as following: 0 to NUMDIV-1: Non-fractional divider NUMDIV to NUMFRACDIV: Fractional divider E.g. PSOC4A NUMDIV=3, NUMFRACDIV=1 0 to 2: non-fractional divider 0 to 2 3: fractional divider 0 Default Value: 0

12 Supervisory Flash Registers

This section discusses the Supervisory Flash (SFLASH) registers. It lists all the registers in mapping tables, in address order.

12.1 Register Details

Register Name	Address
SFLASH_SILICON_ID	0x0FFFF244
SFLASH_HIB_KEY_DELAY	0x0FFFF250
SFLASH_DPSLP_KEY_DELAY	0x0FFFF252
SFLASH_CSD_TRIM1_HVIDAC	0x0FFFF260
SFLASH_CSD_TRIM2_HVIDAC	0x0FFFF261
SFLASH_CSD_TRIM1_CSD	0x0FFFF262
SFLASH_CSD_TRIM2_CSD	0x0FFFF263
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFFF264
SFLASH_SAR_TEMP_OFFSET	0x0FFFF266

12.1.1 SFLASH_SILICON_ID

Silicon ID

Address: 0x0FFFF244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SFLASH_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SFLASH_ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SFLASH_ID	Silicon ID Default Value: X

12.1.2 SFLASH_HIB_KEY_DELAY

Hibernate wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SFLASH_WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SFLASH_WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	SFLASH_WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

12.1.3 SFLASH_DPSLP_KEY_DELAY

DeepSleep wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SFLASH_WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SFLASH_WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	SFLASH_WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

12.1.4 SFLASH_CSD_TRIM1_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SFLASH_TRIM8 [7:0]							

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default Value: X

12.1.5 SFLASH_CSD_TRIM2_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF261

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SFLASH_TRIM8 [7:0]							

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default Value: X

12.1.6 SFLASH_CSD_TRIM1_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SFLASH_TRIM8 [7:0]							

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default Value: X

12.1.7 SFLASH_CSD_TRIM2_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF263

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SFLASH_TRIM8 [7:0]							

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default Value: X

12.1.8 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFFF264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SFLASH_TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SFLASH_TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	SFLASH_TEMP_MULTIPLIER	Multiplier value for SAR temperature Default Value: X

12.1.9 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFFF266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SFLASH_TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SFLASH_TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	SFLASH_TEMP_OFFSET	Offset value for SAR temperature sensor Default Value: X

13 System Resources Sub-System Registers

This section discusses the System Resources Sub-System (SRSS) registers. It lists all the registers in mapping tables, in address order.

13.1 Register Details

Register Name	Address
PWR_CONTROL	0x400B0000
PWR_INTR	0x400B0004
PWR_INTR_MASK	0x400B0008
PWR_KEY_DELAY	0x400B000C
PWR_VMON_CONFIG	0x400B0018
PWR_BOD_KEY	0x400B0028
PWR_STOP	0x400B002C
CLK_SELECT	0x400B0100
CLK_ILO_CONFIG	0x400B0104
CLK_IMO_CONFIG	0x400B0108
CLK_IMO_SPREAD	0x400B010C
WDT_CTRLOW	0x400B0200
WDT_CTRHIGH	0x400B0204
WDT_MATCH	0x400B0208
WDT_CONFIG	0x400B020C
WDT_CONTROL	0x400B0210
RES_CAUSE	0x400B0300
CLK_IMO_TRIM2	0x400BFF2C

13.1.1 PWR_CONTROL

Power Mode Control

Address: 0x400B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		RW	RW	RW			
Name	None [7:6]		LPM_READY	DEBUG_SESSION	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None						
HW Access	R	None						
Name	EXT_VCCD	None [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW1S	RW	None	RW1S	RW
HW Access	R	None	R	R	A	None	RW0C	R
Name	HIBER-NATE	None	LFCLK_SHORT	HIBERNATE_DISABLE	FIMO_DISABLE	None	HVMON_RELOAD	HVMON_ENABLE

Bits	Name	Description
31	HIBERNATE	Selects between HIBERNATE/DEEPSLEEP modes when Cortex-M0 enters low power mode (SleepDeep). Note: this bit is ignored when HIBERNATE_DISABLE=1. Default Value: 1 **0x0: DEEP_SLEEP:** Enter DeepSleep mode when CPU asserts SLEEPDEEP signal **0x1: HIBERNATE:** Enter Hibernate mode when CPU asserts SLEEPDEEP signal
29	LFCLK_SHORT	Short LFCLK and Deep-Sleep power rails in DeepSleep power mode. This mode selection affects the accuracy specifications of the ILO oscillator due to supply noise. See Data Sheet for more details. 0: Do not short power domains 1: Short power domains Default Value: 0

13.1.1 PWR_CONTROL (continued)

28	HIBERNATE_DISABLE	0: Normal operation, HIBERNATE works as described 1: HIBERNATE bit is ignored, Hibernate mode is permanently disabled (part will go to DeepSleep instead. Note: This bit is a write-once bit until the next reset. Default Value: 0
27	FIMO_DISABLE	This bit is asserted during the boot process 0: Forces IMO to operate at 12MHz, ignore its frequency and trim settings and operate independent on its external references. 1: Turns IMO into normal operational mode Default Value: 0
25	HVMON_RELOAD	Firmware writes 1 to reload HV State in hibernate shadow copy. Hardware clears this bit after reload was successful. Wait at least 9 cycles after writing/recalling NVL before reloading the HVMON. Default Value: 0
24	HVMON_ENABLE	0: HV State Monitoring is disabled 1: HV State Monitoring is automatically enable by sleep controller Default Value: 1
23	EXT_VCCD	Indicates that Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (PBOD) unless both Vddd and Vccd pins are supplied externally. Default Value: 0
5	LPM_READY	Indicates whether the low power mode regulators are ready to enter DEEPSLEEP or HIBERNATE mode. 0: If DEEPSLEEP or HIBERNATE mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and HIBERNATE work as described. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active Default Value: 0 **0x0: NO_SESSION:** No debug session active **0x1: SESSION_ACTIVE:** Debug session is active
3 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0 **0x0: RESET:** RESET state **0x1: ACTIVE:** ACTIVE state **0x2: SLEEP:** SLEEP state **0x3: DEEP_SLEEP:** DEEP_SLEEP state **0x4: HIBERNATE:** HIBERNATE state

13.1.2 PWR_INTR

Power System Interrupt Register

Address: 0x400B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	None
HW Access	None						A	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	Indicates an Low Voltage Detect interrupt Default Value: 0

13.1.3 PWR_INTR_MASK

Power System Interrupt Mask Register

Address: 0x400B0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	1: Propagate interrupt to CPU Default Value: 0

13.1.4 PWR_KEY_DELAY

Power System Key Register

Address: 0x400B000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: 780

13.1.5 PWR_VMON_CONFIG

Voltage Monitoring Trim and Configuration

Address: 0x400B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	VMON_DDFT_SEL [7:5]			LVD_SEL [4:1]				LVD_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						VMON_ADFT_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	VMON_ADFT_SEL	Reserved Default Value: 0
7 : 5	VMON_DDFT_SEL	Reserved Default Value: 0

13.1.5 PWR_VMON_CONFIG (continued)

4 : 1	LVD_SEL	Threshold selection for Low Voltage Detect circuit. Threshold variation is +/- 2.5% from these typical voltage choices: 0: 1.7500 V 1: 1.8000 V 2: 1.9000 V 3: 2.0000 V 4: 2.1000 V 5: 2.2000 V 6: 2.3000 V 7: 2.4000 V 8: 2.5000 V 9: 2.6000 V 10: 2.7000 V 11: 2.8000 V 12: 2.9000 V 13: 3.0000 V 14: 3.2000 V 15: 4.5000 V Default Value: 0
0	LVD_EN	Enable Low Voltage Detect circuit. Default Value: 0

13.1.6 PWR_BOD_KEY

BOD Detection Key

Address: 0x400B0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	KEY16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	KEY16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	KEY16	To detect brown-outs firmware should do this on boot: 1. Set key= KEY16 2. Set KEY16= 0x3A71 3. If key==0x3A71 this was a brown-out event. Default Value: X

13.1.7 PWR_STOP

STOP Mode Register

Address: 0x400B002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [23:18]						FREEZE	POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	STOP	None [30:24]						

Bits	Name	Description
31	STOP	Firmware sets this bit to enter STOP mode. Both UNLOCK and FREEZE must have been set correctly in a previous write operation. Otherwise, writes to this bit will affect the freeze override but will not actually set the STOP bit. The system will enter STOP mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Default Value: 0
17	FREEZE	Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. Two identical write cycles are required to freeze the IO explicitly. The first cycle instructs DEEPSLEEP and HIBERNATE peripherals whether they can override upcoming freeze command(s). UNLOCK setting does not affect this. If firmware writes FREEZE=1 and STOP=0, peripherals can override the freeze and remain functional according to their configuration. If firmware writes FREEZE=1 and STOP=1, peripherals cannot override the next freeze command. The second write cycle freezes the IO if UNLOCK is set and the peripheral does not override the freeze. While FREEZE=1, peripherals will automatically freeze according to the override directive when entering DEEPSLEEP or HIBERNATE, regardless of the UNLOCK setting. Default Value: 0
16	POLARITY	0: WAKEUP=0 will wakeup the part from STOP 1: WAKEUP=1 will wakeup the part from STOP Default Value: 0

13.1.7 PWR_STOP (continued)

15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or STOP fields to operate. Any other value in this register will cause FREEZE/STOP to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a STOP/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from STOP using XRES will reset this register. Default Value: 0

13.1.8 CLK_SELECT

Clock Select Register

Address: 0x400B0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PLL_SEL [7:6]		DBL_SEL [5:3]			DIRECT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW			RW
HW Access	A		R		R			R
Name	WDT_LOCK [15:14]		DPLLREF_SEL [13:12]		DPLLIN_SEL [11:9]			PLL_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW			RW	RW	
HW Access	None		R			R	R	
Name	None [23:22]		SYSCLK_DIV [21:19]			HALF_EN	HFCLK_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 19	SYSCLK_DIV	SYSCLK Pre-Scaler Value. Default Value: 0 **0x0: NO_DIV:** SYSCLK= HFCLK/1 **0x1: DIV_BY_2:** SYSCLK= HFCLK/2 **0x2: DIV_BY_4:** SYSCLK= HFCLK/4 **0x3: DIV_BY_8:** SYSCLK= HFCLK/8 **0x4: DIV_BY_16:** SYSCLK= HFCLK/16 **0x5: DIV_BY_32:** SYSCLK= HFCLK/32 **0x6: DIV_BY_64:** SYSCLK= HFCLK/64

13.1.8 CLK_SELECT (continued)

		0x7: DIV_BY_128: SYSCLK= HFCLK/128
18	HALF_EN	FLASH Wait-state selection. Default Value: 0
17 : 16	HFCLK_SEL	Selects the source for HFCLK. Default Value: 0 **0x0: DIRECT_SEL:** Source selected by DIRECT_SEL **0x1: DBL:** Reserved **0x2: PLL:** Output of PLL
15 : 14	WDT_LOCK	Prohibits writing to WDT_* registers and CLK_ILO/WCO_CONFIG registerst when not equal 0. Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all WATCHDOG registers at the same time. Default Value: 0 **0x0: NO_CHG:** No effect **0x1: CLR0:** Clears bit 0 **0x2: CLR1:** Clears bit 1 **0x3: SET01:** Sets both bits 0 and 1
13 : 12	DPLLREF_SEL	Selects a source for the reference (tracking) input of DPLL: 0: DSI_OUT[0] 1: DSI_OUT[1] 2: DSI_OUT[2] 3: DSI_OUT[3] Default Value: 0 **0x0: DSI0:** DSI_OUT[0] **0x1: DSI1:** DSI_OUT[1] **0x2: DSI2:** DSI_OUT[2] **0x3: DSI3:** DSI_OUT[3]
11 : 9	DPLLIN_SEL	Selects a source for the input of DPLL. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External-Crystal Oscillator (Crystal external, Oscilator internal)

13.1.8 CLK_SELECT (continued)

		0x4: DSI0: DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]
8 : 6	PLL_SEL	Selects a source for the input of the PLL. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External-Crystal Oscillator (Crystal external, Oscilator internal) **0x3: DPLL:** DPLL - DPLL Output **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]
5 : 3	DBL_SEL	Reserved Default Value: 0
2 : 0	DIRECT_SEL	Selects a source for HFCLK (when HFCLK_SEL=0) and DSI_IN[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note that using DSI_OUT[3:0] as HFCLK source will also result in undefined behavior. These values are available strictly to provide a clock in DSI_IN[0]. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External-Crystal Oscillator (Crystal external, Oscilator internal) **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2]

13.1.8 CLK_SELECT (continued)

0x7: DSI3:
DSI_OUT[3]

13.1.9 CLK_ILO_CONFIG

ILO Configuration

Address: 0x400B0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SATBIAS	TURBO	PD_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator Default Value: 0
2	SATBIAS	PFET bias Default Value: 1
		0x0: SATURATED: Enable saturated PFET bias
		0x1: SUBTHRESHOLD: Enable subthreshold PFET bias
1	TURBO	Turbo mode for faster startup from coma power down 0: turbo disabled 1: turbo enabled Default Value: 1
0	PD_MODE	Power down mode. Note: this bit must always be set to 0 and never changed. Behavior is un-defined when set to 1. Default Value: 0
		0x0: SLEEP: Sleep (faster startup - enables pulsegen block)

13.1.9 CLK_ILO_CONFIG (continued)

0x1: COMA:
Coma (slower startup)

13.1.10 CLK_IMO_CONFIG

IMO Configuration

Address: 0x400B0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	EN_FASTBIAS	FLASHPUMP_SEL	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW			RW
HW Access	R	R	R	R	R			R
Name	ENABLE	EN_CLK2X	EN_CLK36	TEST_USB_MODE	PUMP_SEL [27:25]			TEST_FASTBIAS

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO but not disconnect it from the power rail. Default Value: 1
30	EN_CLK2X	Reserved Default Value: 0
291 and PUMP_SEL3 3. If so, set EN_CLK36 =0 4. Enable interrupts Default Value: 0	EN_CLK36	Enables 36MHz secondary oscillator that can be used for Pump or Flash Pump. Note: Since there are two consumers of the 36MHz clock, care should be taken when clearing this bit. The correct procedure for clearing this bit is: 1. Disable interrupts 2. Check if both FLASHPUMP_SEL
28	TEST_USB_MODE	Reserved Default Value: 0

13.1.10 CLK_IMO_CONFIG (continued)

27 : 25	PUMP_SEL	Selects operating source for Pump clock. This clock is not guaranteed to be glitch free when changing IMO parameters or clock divider settings. 5-7: reserved, do not use Default Value: 0 **0x0: GND:** No clock, connect to GND **0x1: IMO:** Use main IMO output **0x2: DBL:** Use doubler output **0x3: CLK36:** Use 36MHz oscillator **0x4: FF1:** Use divided clock FF1
24	TEST_FASTBIAS	Reserved Default Value: 0
23	EN_FASTBIAS	Reserved Default Value: 1
22	FLASHPUMP_SEL	Selects operating source for SPCIF Timer/Flash Pump clock. Default Value: 0 **0x0: GND:** No clock, connect to gnd **0x1: CLK36:** Use 36MHz oscillator

13.1.11 CLK_IMO_SPREAD

IMO Spread Spectrum Configuration

Address: 0x400B010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			SS_VALUE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			SS_MAX [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	SS_MODE [31:30]		SS_RANGE [29:28]		None [27:24]			

Bits	Name	Description
31 : 30	SS_MODE	Spread Spectrum Mode. Default Value: 0 **0x0: OFF:** Off, do not change SS_VALUE **0x1: TRIANGLE:** Modulate using triangle wave (see SS_MAX) **0x2: LFSR:** Modulate using pseudo random sequence (using LFSR) **0x3: DSI:** Take value directly from DSI (synchronized by divided clock FF1)
29 : 28	SS_RANGE	Spread spectrum range (downspread when SS_VALUE=16). 3: reserved, do not use Default Value: 0 **0x0: M1:** 0 .. -1%

13.1.11 CLK_IMO_SPREAD (continued)

		0x1: M2: 0 .. -2% **0x2: M4:** 0 .. -4%
12 : 8	SS_MAX	Maximum counter value for spread spectrum. Counter will count from 0..SS_MAX..0 and keep repeating this indefinitely. Only works when SS_MODE=1. Default Value: 0
4 : 0	SS_VALUE	Current offset value for spread spectrum modulation. IMO supports values 0..16. Step size is determined by SS_RANGE. Value is encoded in proper thermometric format for IMO in hardware. Value can be modified in firmware only when SS_MODE=0. Default Value: 0

13.1.12 WDT_CTRLOW

Watchdog Counters 0/1

Address: 0x400B0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [7:0]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [15:8]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of WDT Counter 1 Default Value: 0
15 : 0	WDT_CTR0	Current value of WDT Counter 0 Default Value: 0

13.1.13 WDT_CTRHIGH

Watchdog Counter 2

Address: 0x400B0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of WDT Counter 2 Default Value: 0

13.1.14 WDT_MATCH

Watchdog counter match values

Address: 0x400B0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [7:0]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [15:8]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for Watchdog Counter 1 Default Value: 0
15 : 0	WDT_MATCH0	Match value for Watchdog Counter 0 Default Value: 0

13.1.15 WDT_CONFIG

Watchdog Counters Configuration

Address: 0x400B020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CASCADE0_1	WDT_CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CASCADE1_2	WDT_CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	LFCLK_SEL [31:30]		None	WDT_BITS2 [28:24]				

Bits	Name	Description
31 : 30	LFCLK_SEL	Select source for LFCLK: 0: ILO - Internal R/C Oscillator 1: WCO - Internal Crystal Oscillator 2-3: Reserved - do not use Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert when bit0 of WDT_CTR2 toggles (one int every tick) .. 31: Assert when bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0 **0x0: NOTHING:** Free running counter with no interrupt requests

13.1.15 WDT_CONFIG (continued)

		0x1: INT: Free running counter with interrupt request when a specified bit in CTR2 toggles (see WDT_BITS2)
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1=WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

13.1.16 WDT_CONTROL

Watchdog Counters Control

Address: 0x400B0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [7:4]				WDT_RESET0	WDT_INT0	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [15:12]				WDT_RESET1	WDT_INT1	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [23:20]				WDT_RESET2	WDT_INT2	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000_0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Default Value: 0
18	WDT_INT2	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to 3 LFCLK cycles. Default Value: 0
16	WDT_ENABLE2	Enable Counter 2 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0

13.1.16 WDT_CONTROL (continued)

11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Default Value: 0
10	WDT_INT1	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to 3 LFCLK cycles. Default Value: 0
8	WDT_ENABLE1	Enable Counter 1 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Default Value: 0
2	WDT_INT0	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. Default Value: 0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to 3 LFCLK cycles. Default Value: 0
0	WDT_ENABLE0	Enable Counter 0 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0

13.1.17 RES_CAUSE

Reset Cause Observation Register

Address: 0x400B0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	RESET_XRES	RESET_PBOD	RESET_HVBOD	RESET_SOFT	RESET_PROT_FAULT	RESET_LOCKUP	RESET_DSBOD	RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RESET_XRES	This field is not used and will always read 0. Default Value: 0
6	RESET_PBOD	This field is not used and will always read 0. Default Value: 0
5	RESET_HVBOD	This field is not used and will always read 0. Default Value: 0
4	RESET_SOFT	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0
3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default Value: 0
2	RESET_LOCKUP	This field is not used and will always read 0. Default Value: 0
1	RESET_DSBOD	This field is not used and will always read 0. Default Value: 0

13.1.17 RES_CAUSE (continued)

0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default Value: 0

13.1.18 CLK_IMO_TRIM2

IMO Trim Register

Address: 0x400BFF2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		FREQ [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	FREQ	Frequency to be selected (default 24MHz). Frequencies can be selected from 3 to 48MHz. [3-12] => [3MHz-12MHz] [14-25] => [13MHz-24MHz] [27-35] => [25MHz-33MHz] [37-43] => [34MHz-40MHz] [46-53] => [41MHz-48MHz] Default Value: 25

14 Timer-Counter-PWM Registers

This section discusses the Timer-Counter-PWM (TCPWM) registers. It lists all the registers in mapping tables, in address order.

14.1 Register Details

Register Name	Address
TCPWM_CTRL	0x40050000
TCPWM_CMD	0x40050008
TCPWM_INTR_CAUSE	0x4005000C

14.1.1 TCPWM_CTRL

TCPWM control register 0.

Address: 0x40050000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TCPWM_COUNTER_ENABLED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TCPWM_COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. When '0': counter disabled. When '1': counter enabled. Counter control information should only be modified when the counter is disabled. When a counter is disabled, the associated counter triggers in the MMIO CMD register are set to '0'. Default Value: 0

14.1.2 TCPWM_CMD

TCPWM command register.

Address: 0x40050008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [7:4]				TCPWM_COUNTER_CAPTURE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [15:12]				TCPWM_COUNTER_RELOAD [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [23:20]				TCPWM_COUNTER_STOP [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [31:28]				TCPWM_COUNTER_START [27:24]			

Bits	Name	Description
27 : 24	TCPWM_COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
19 : 16	TCPWM_COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
11 : 8	TCPWM_COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
3 : 0	TCPWM_COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

14.1.3 TCPWM_INTR_CAUSE

TCPWM Counter interrupt cause register.

Address: 0x4005000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				TCPWM_COUNTER_INT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TCPWM_COUNTER_INT	Counters interrupt signal active. Default Value: 0

15 TCPWM Counter Registers

This section discusses the TCPWM Counter (TCPWM_CNT) registers. It lists all the registers in mapping tables, in address order.

15.1 Register Details

Register Name	Address
TCPWM_CNT0_CTRL	0x40050100
TCPWM_CNT0_STATUS	0x40050104
TCPWM_CNT0_COUNTER	0x40050108
TCPWM_CNT0_CC	0x4005010C
TCPWM_CNT0_CC_BUFF	0x40050110
TCPWM_CNT0_PERIOD	0x40050114
TCPWM_CNT0_PERIOD_BUFF	0x40050118
TCPWM_CNT0_TR_CTRL0	0x40050120
TCPWM_CNT0_TR_CTRL1	0x40050124
TCPWM_CNT0_TR_CTRL2	0x40050128
TCPWM_CNT0_INTR	0x40050130
TCPWM_CNT0_INTR_SET	0x40050134
TCPWM_CNT0_INTR_MASK	0x40050138
TCPWM_CNT0_INTR_MASKED	0x4005013C
TCPWM_CNT1_CTRL	0x40050140
TCPWM_CNT1_STATUS	0x40050144
TCPWM_CNT1_COUNTER	0x40050148
TCPWM_CNT1_CC	0x4005014C
TCPWM_CNT1_CC_BUFF	0x40050150
TCPWM_CNT1_PERIOD	0x40050154
TCPWM_CNT1_PERIOD_BUFF	0x40050158
TCPWM_CNT1_TR_CTRL0	0x40050160
TCPWM_CNT1_TR_CTRL1	0x40050164
TCPWM_CNT1_TR_CTRL2	0x40050168
TCPWM_CNT1_INTR	0x40050170
TCPWM_CNT1_INTR_SET	0x40050174
TCPWM_CNT1_INTR_MASK	0x40050178

Register Name	Address
TCPWM_CNT1_INTR_MASKED	0x4005017C
TCPWM_CNT2_CTRL	0x40050180
TCPWM_CNT2_STATUS	0x40050184
TCPWM_CNT2_COUNTER	0x40050188
TCPWM_CNT2_CC	0x4005018C
TCPWM_CNT2_CC_BUFF	0x40050190
TCPWM_CNT2_PERIOD	0x40050194
TCPWM_CNT2_PERIOD_BUFF	0x40050198
TCPWM_CNT2_TR_CTRL0	0x400501a0
TCPWM_CNT2_TR_CTRL1	0x400501a4
TCPWM_CNT2_TR_CTRL2	0x400501a8
TCPWM_CNT2_INTR	0x400501b0
TCPWM_CNT2_INTR_SET	0x400501b4
TCPWM_CNT2_INTR_MASK	0x400501b8
TCPWM_CNT2_INTR_MASKED	0x400501bC
TCPWM_CNT3_CTRL	0x400501c0
TCPWM_CNT3_STATUS	0x400501c4
TCPWM_CNT3_COUNTER	0x400501c8
TCPWM_CNT3_CC	0x400501cC
TCPWM_CNT3_CC_BUFF	0x400501d0
TCPWM_CNT3_PERIOD	0x400501d4
TCPWM_CNT3_PERIOD_BUFF	0x400501d8
TCPWM_CNT3_TR_CTRL0	0x400501e0
TCPWM_CNT3_TR_CTRL1	0x400501e4
TCPWM_CNT3_TR_CTRL2	0x400501e8
TCPWM_CNT3_INTR	0x400501f0
TCPWM_CNT3_INTR_SET	0x400501f4
TCPWM_CNT3_INTR_MASK	0x400501f8
TCPWM_CNT3_INTR_MASKED	0x400501fC

15.1.1 TCPWM_CNT0_CTRL

Counter control register

Address: 0x40050100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CNT0_PWM_STOP_ON_KILL	CNT0_PWM_SYNC_KILL	CNT0_AUTO_RELOAD_PERIOD	CNT0_AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CNT0_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		CNT0_QUADRATURE_MODE [21:20]		None	CNT0_ONE_SHOT	CNT0_UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					CNT0_MODE [26:24]		

Bits	Name	Description
26 : 24	CNT0_MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

15.1.1 TCPWM_CNT0_CTRL (continued)

21 : 20	CNT0_QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	CNT0_ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	CNT0_UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	CNT0_GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

15.1.1 TCPWM_CNT0_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	CNT0_PWM_STOP_ON_KILL	When '1', the kill/stop event stops the counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	CNT0_PWM_SYNC_KILL	When '1', the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). When '0' the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present (asynchronous kill). In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. In aynchronous kill mode, STOP_EDGE should be RISING_EDGE. This field has a function in PWM and PWM_DT modes only. Default Value: 0
1	CNT0_AUTO_RELOAD_PERIOD	When '1', the hardware automatically updates the PERIOD register during a terminal count with an active switch event. Default Value: 0
0	CNT0_AUTO_RELOAD_CC	When '1', the hardware automatically updates the CC register during a terminal count with an active switch event. Default Value: 0

15.1.2 TCPWM_CNT0_STATUS

Counter status register

Address: 0x40050104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							CNT0_DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CNT0_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	CNT0_RUNNING	None [30:24]						

Bits	Name	Description
31	CNT0_RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	CNT0_GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	CNT0_DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

15.1.3 TCPWM_CNT0_COUNTER

Counter count register

Address: 0x40050108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT0_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT0_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT0_COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

15.1.4 TCPWM_CNT0_CC

Counter compare/capture register

Address: 0x4005010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT0_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT0_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT0_CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

15.1.5 TCPWM_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40050110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT0_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT0_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT0_CC	Additional buffer for counter CC register. Default Value: 65535

15.1.6 TCPWM_CNT0_PERIOD

Counter period register

Address: 0x40050114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT0_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT0_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT0_PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

15.1.7 TCPWM_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40050118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT0_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT0_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT0_PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

15.1.8 TCPWM_CNT0_TR_CTRL0

Counter trigger control register 0

Address: 0x40050120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CNT0_COUNT_SEL [7:4]				CNT0_CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	CNT0_STOP_SEL [15:12]				CNT0_RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				CNT0_START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	CNT0_START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	CNT0_STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	CNT0_RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	CNT0_COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

15.1.8 TCPWM_CNT0_TR_CTRL0 (continued)

3 : 0	CNT0_CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

15.1.9 TCPWM_CNT0_TR_CTRL1

Counter trigger control register 1

Address: 0x40050124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CNT0_STOP_EDGE [7:6]		CNT0_RELOAD_EDGE [5:4]		CNT0_COUNT_EDGE [3:2]		CNT0_CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						CNT0_START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	CNT0_START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	CNT0_STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

15.1.9 TCPWM_CNT0_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	CNT0_RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	CNT0_COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CNT0_CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

15.1.10 TCPWM_CNT0_TR_CTRL2

Counter trigger control register 2

Address: 0x40050128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		CNT0_UNDERFLOW_MODE [5:4]		CNT0_OVERFLOW_MODE [3:2]		CNT0_CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	CNT0_UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	CNT0_OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

15.1.10 TCPWM_CNT0_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CNT0_CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

15.1.11 TCPWM_CNT0_INTR

Interrupt request register.

Address: 0x40050130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CNT0_CC_MATCH	CNT0_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT0_CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	CNT0_TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

15.1.12 TCPWM_CNT0_INTR_SET

Interrupt set request register.

Address: 0x40050134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CNT0_CC_MATCH	CNT0_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT0_CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	CNT0_TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

15.1.13 TCPWM_CNT0_INTR_MASK

Interrupt mask register.

Address: 0x40050138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CNT0_CC_MATCH	CNT0_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT0_CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	CNT0_TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

15.1.14 TCPWM_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4005013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CNT0_CC_MATCH	CNT0_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT0_CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	CNT0_TC	Logical and of corresponding request and mask bits. Default Value: 0

15.1.15 TCPWM_CNT1_CTRL

Counter control register

Address: 0x40050140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CNT1_PWM_STOP_ON_KILL	CNT1_PWM_SYNC_KILL	CNT1_AUTO_RELOAD_PERIOD	CNT1_AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CNT1_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		CNT1_QUADRATURE_MODE [21:20]		None	CNT1_ONE_SHOT	CNT1_UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					CNT1_MODE [26:24]		

Bits	Name	Description
26 : 24	CNT1_MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

15.1.15 TCPWM_CNT1_CTRL (continued)

21 : 20	CNT1_QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	CNT1_ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	CNT1_UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	CNT1_GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

15.1.15 TCPWM_CNT1_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	CNT1_PWM_STOP_ON_KILL	When '1', the kill/stop event stops the counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	CNT1_PWM_SYNC_KILL	When '1', the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). When '0' the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present (asynchronous kill). In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. In aynchronous kill mode, STOP_EDGE should be RISING_EDGE. This field has a function in PWM and PWM_DT modes only. Default Value: 0
1	CNT1_AUTO_RELOAD_PERIOD	When '1', the hardware automatically updates the PERIOD register during a terminal count with an active switch event. Default Value: 0
0	CNT1_AUTO_RELOAD_CC	When '1', the hardware automatically updates the CC register during a terminal count with an active switch event. Default Value: 0

15.1.16 TCPWM_CNT1_STATUS

Counter status register

Address: 0x40050144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							CNT1_DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CNT1_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	CNT1_RUNNING	None [30:24]						

Bits	Name	Description
31	CNT1_RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	CNT1_GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	CNT1_DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

15.1.17 TCPWM_CNT1_COUNTER

Counter count register

Address: 0x40050148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT1_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT1_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT1_COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

15.1.18 TCPWM_CNT1_CC

Counter compare/capture register

Address: 0x4005014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT1_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT1_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT1_CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

15.1.19 TCPWM_CNT1_CC_BUFF

Counter buffered compare/capture register

Address: 0x40050150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT1_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT1_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT1_CC	Additional buffer for counter CC register. Default Value: 65535

15.1.20 TCPWM_CNT1_PERIOD

Counter period register

Address: 0x40050154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT1_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT1_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT1_PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

15.1.21 TCPWM_CNT1_PERIOD_BUFF

Counter buffered period register

Address: 0x40050158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT1_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT1_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT1_PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

15.1.22 TCPWM_CNT1_TR_CTRL0

Counter trigger control register 0

Address: 0x40050160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CNT1_COUNT_SEL [7:4]				CNT1_CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	CNT1_STOP_SEL [15:12]				CNT1_RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				CNT1_START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	CNT1_START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	CNT1_STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	CNT1_RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	CNT1_COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

15.1.22 TCPWM_CNT1_TR_CTRL0 (continued)

3 : 0	CNT1_CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

15.1.23 TCPWM_CNT1_TR_CTRL1

Counter trigger control register 1

Address: 0x40050164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CNT1_STOP_EDGE [7:6]		CNT1_RELOAD_EDGE [5:4]		CNT1_COUNT_EDGE [3:2]		CNT1_CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						CNT1_START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	CNT1_START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	CNT1_STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

15.1.23 TCPWM_CNT1_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	CNT1_RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	CNT1_COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CNT1_CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

15.1.24 TCPWM_CNT1_TR_CTRL2

Counter trigger control register 2

Address: 0x40050168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		CNT1_UNDERFLOW_MODE [5:4]		CNT1_OVERFLOW_MODE [3:2]		CNT1_CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	CNT1_UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	CNT1_OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

15.1.24 TCPWM_CNT1_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CNT1_CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

15.1.25 TCPWM_CNT1_INTR

Interrupt request register.

Address: 0x40050170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CNT1_CC_MATCH	CNT1_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT1_CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	CNT1_TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

15.1.26 TCPWM_CNT1_INTR_SET

Interrupt set request register.

Address: 0x40050174

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CNT1_CC_MATCH	CNT1_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT1_CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	CNT1_TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

15.1.27 TCPWM_CNT1_INTR_MASK

Interrupt mask register.

Address: 0x40050178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CNT1_CC_MATCH	CNT1_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT1_CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	CNT1_TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

15.1.28 TCPWM_CNT1_INTR_MASKED

Interrupt masked request register

Address: 0x4005017C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CNT1_CC_MATCH	CNT1_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT1_CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	CNT1_TC	Logical and of corresponding request and mask bits. Default Value: 0

15.1.29 TCPWM_CNT2_CTRL

Counter control register

Address: 0x40050180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CNT2_PWM_STOP_ON_KILL	CNT2_PWM_SYNC_KILL	CNT2_AUTO_RELOAD_PERIOD	CNT2_AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CNT2_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		CNT2_QUADRATURE_MODE [21:20]		None	CNT2_ONE_SHOT	CNT2_UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					CNT2_MODE [26:24]		

Bits	Name	Description
26 : 24	CNT2_MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

15.1.29 TCPWM_CNT2_CTRL (continued)

21 : 20	CNT2_QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	CNT2_ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	CNT2_UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	CNT2_GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

15.1.29 TCPWM_CNT2_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	CNT2_PWM_STOP_ON_KILL	When '1', the kill/stop event stops the counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	CNT2_PWM_SYNC_KILL	When '1', the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). When '0' the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present (asynchronous kill). In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. In aynchronous kill mode, STOP_EDGE should be RISING_EDGE. This field has a function in PWM and PWM_DT modes only. Default Value: 0
1	CNT2_AUTO_RELOAD_PERIOD	When '1', the hardware automatically updates the PERIOD register during a terminal count with an active switch event. Default Value: 0
0	CNT2_AUTO_RELOAD_CC	When '1', the hardware automatically updates the CC register during a terminal count with an active switch event. Default Value: 0

15.1.30 TCPWM_CNT2_STATUS

Counter status register

Address: 0x40050184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							CNT2_DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CNT2_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	CNT2_RUNNING	None [30:24]						

Bits	Name	Description
31	CNT2_RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	CNT2_GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	CNT2_DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

15.1.31 TCPWM_CNT2_COUNTER

Counter count register

Address: 0x40050188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT2_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT2_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT2_COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

15.1.32 TCPWM_CNT2_CC

Counter compare/capture register

Address: 0x4005018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT2_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT2_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT2_CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

15.1.33 TCPWM_CNT2_CC_BUFF

Counter buffered compare/capture register

Address: 0x40050190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT2_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT2_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT2_CC	Additional buffer for counter CC register. Default Value: 65535

15.1.34 TCPWM_CNT2_PERIOD

Counter period register

Address: 0x40050194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT2_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT2_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT2_PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

15.1.35 TCPWM_CNT2_PERIOD_BUFF

Counter buffered period register

Address: 0x40050198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT2_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT2_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT2_PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

15.1.36 TCPWM_CNT2_TR_CTRL0

Counter trigger control register 0

Address: 0x400501a0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CNT2_COUNT_SEL [7:4]				CNT2_CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	CNT2_STOP_SEL [15:12]				CNT2_RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				CNT2_START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	CNT2_START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	CNT2_STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	CNT2_RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	CNT2_COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

15.1.36 TCPWM_CNT2_TR_CTRL0 (continued)

3 : 0	CNT2_CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

15.1.37 TCPWM_CNT2_TR_CTRL1

Counter trigger control register 1

Address: 0x400501a4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CNT2_STOP_EDGE [7:6]		CNT2_RELOAD_EDGE [5:4]		CNT2_COUNT_EDGE [3:2]		CNT2_CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						CNT2_START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	CNT2_START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	CNT2_STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

15.1.37 TCPWM_CNT2_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	CNT2_RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	CNT2_COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CNT2_CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

15.1.38 TCPWM_CNT2_TR_CTRL2

Counter trigger control register 2

Address: 0x400501a8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		CNT2_UNDERFLOW_MODE [5:4]		CNT2_OVERFLOW_MODE [3:2]		CNT2_CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	CNT2_UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	CNT2_OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

15.1.38 TCPWM_CNT2_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CNT2_CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

15.1.39 TCPWM_CNT2_INTR

Interrupt request register.

Address: 0x400501b0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CNT2_CC_MATCH	CNT2_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT2_CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	CNT2_TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

15.1.40 TCPWM_CNT2_INTR_SET

Interrupt set request register.

Address: 0x400501b4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CNT2_CC_MATCH	CNT2_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT2_CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	CNT2_TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

15.1.41 TCPWM_CNT2_INTR_MASK

Interrupt mask register.

Address: 0x400501b8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CNT2_CC_MATCH	CNT2_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT2_CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	CNT2_TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

15.1.42 TCPWM_CNT2_INTR_MASKED

Interrupt masked request register

Address: 0x400501bC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CNT2_CC_MATCH	CNT2_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT2_CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	CNT2_TC	Logical and of corresponding request and mask bits. Default Value: 0

15.1.43 TCPWM_CNT3_CTRL

Counter control register

Address: 0x400501c0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CNT3_PWM_STOP_ON_KILL	CNT3_PWM_SYNC_KILL	CNT3_AUTO_RELOAD_PERIOD	CNT3_AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CNT3_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		CNT3_QUADRATURE_MODE [21:20]		None	CNT3_ONE_SHOT	CNT3_UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					CNT3_MODE [26:24]		

Bits	Name	Description
26 : 24	CNT3_MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

15.1.43 TCPWM_CNT3_CTRL (continued)

21 : 20	CNT3_QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	CNT3_ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	CNT3_UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	CNT3_GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

15.1.43 TCPWM_CNT3_CTRL (continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	CNT3_PWM_STOP_ON_KILL	When '1', the kill/stop event stops the counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	CNT3_PWM_SYNC_KILL	When '1', the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). When '0' the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present (asynchronous kill). In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. In aynchronous kill mode, STOP_EDGE should be RISING_EDGE. This field has a function in PWM and PWM_DT modes only. Default Value: 0
1	CNT3_AUTO_RELOAD_PERIOD	When '1', the hardware automatically updates the PERIOD register during a terminal count with an active switch event. Default Value: 0
0	CNT3_AUTO_RELOAD_CC	When '1', the hardware automatically updates the CC register during a terminal count with an active switch event. Default Value: 0

15.1.44 TCPWM_CNT3_STATUS

Counter status register

Address: 0x400501c4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							CNT3_DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CNT3_GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	CNT3_RUNNING	None [30:24]						

Bits	Name	Description
31	CNT3_RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	CNT3_GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	CNT3_DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

15.1.45 TCPWM_CNT3_COUNTER

Counter count register

Address: 0x400501c8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT3_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT3_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT3_COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

15.1.46 TCPWM_CNT3_CC

Counter compare/capture register

Address: 0x400501cC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT3_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT3_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT3_CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

15.1.47 TCPWM_CNT3_CC_BUFF

Counter buffered compare/capture register

Address: 0x400501d0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT3_CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT3_CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT3_CC	Additional buffer for counter CC register. Default Value: 65535

15.1.48 TCPWM_CNT3_PERIOD

Counter period register

Address: 0x400501d4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT3_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT3_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT3_PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

15.1.49 TCPWM_CNT3_PERIOD_BUFF

Counter buffered period register

Address: 0x400501d8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CNT3_PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CNT3_PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT3_PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

15.1.50 TCPWM_CNT3_TR_CTRL0

Counter trigger control register 0

Address: 0x400501e0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CNT3_COUNT_SEL [7:4]				CNT3_CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	CNT3_STOP_SEL [15:12]				CNT3_RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				CNT3_START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	CNT3_START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	CNT3_STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	CNT3_RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	CNT3_COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

15.1.50 TCPWM_CNT3_TR_CTRL0 (continued)

3 : 0	CNT3_CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

15.1.51 TCPWM_CNT3_TR_CTRL1

Counter trigger control register 1

Address: 0x400501e4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CNT3_STOP_EDGE [7:6]		CNT3_RELOAD_EDGE [5:4]		CNT3_COUNT_EDGE [3:2]		CNT3_CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						CNT3_START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	CNT3_START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	CNT3_STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

15.1.51 TCPWM_CNT3_TR_CTRL1 (continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	CNT3_RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	CNT3_COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CNT3_CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

15.1.52 TCPWM_CNT3_TR_CTRL2

Counter trigger control register 2

Address: 0x400501e8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		CNT3_UNDERFLOW_MODE [5:4]		CNT3_OVERFLOW_MODE [3:2]		CNT3_CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	CNT3_UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	CNT3_OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

15.1.52 TCPWM_CNT3_TR_CTRL2 (continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CNT3_CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

15.1.53 TCPWM_CNT3_INTR

Interrupt request register.

Address: 0x400501f0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CNT3_CC_MATCH	CNT3_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT3_CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	CNT3_TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

15.1.54 TCPWM_CNT3_INTR_SET

Interrupt set request register.

Address: 0x400501f4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CNT3_CC_MATCH	CNT3_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT3_CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	CNT3_TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

15.1.55 TCPWM_CNT3_INTR_MASK

Interrupt mask register.

Address: 0x400501f8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CNT3_CC_MATCH	CNT3_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT3_CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	CNT3_TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

15.1.56 TCPWM_CNT3_INTR_MASKED

Interrupt masked request register

Address: 0x400501fC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CNT3_CC_MATCH	CNT3_TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CNT3_CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	CNT3_TC	Logical and of corresponding request and mask bits. Default Value: 0

16 Universal Digital Block Registers

This section discusses the Universal Digital Block (UDB) registers. It lists all the registers in mapping tables, in address order.

16.1 Register Details

Register Name	Address
UDB_INT_CFG	0x400F8000

16.1.1 UDB_INT_CFG

UDB Subsystem Interrupt Configuration

Address: 0x400F8000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UDB_INT_MODE_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	UDB_INT_MODE_CFG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UDB_INT_MODE_CFG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UDB_INT_MODE_CFG [31:24]							

Bits	Name	Description
31 : 0	UDB_INT_MODE_CFG	Interrupt Mode; bit position corresponds to interrupt Default Value: 0 **0x0: LEVEL:** Level **0x1: PULSE:** Pulse

17 UDB Array Bank Control Registers

This section discusses the UDB Array Bank Control (BCTL) registers. It lists all the registers in mapping tables, in address order.

17.1 Register Details

Register Name	Address
UDB_BCTL_DRV	0x400F6000
UDB_BCTL_MDCLK_EN	0x400F6001
UDB_BCTL_MBCLK_EN	0x400F6002
UDB_BCTL_BOTSEL_L	0x400F6008
UDB_BCTL_BOTSEL_U	0x400F6009
UDB_BCTL_TOPSEL_L	0x400F600A
UDB_BCTL_TOPSEL_U	0x400F600B
UDB_BCTL_QCLK_EN	0x400F6010

17.1.1 UDB_BCTL_DRV

Master Digital Clock Drive Register

Address: 0x400F6000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BCTL0_DRV [7:0]							

Bits	Name	Description
7 : 0	BCTL0_DRV	Master digital clock drive enable for the digital clock that matches the index. Default Value: 0 **0x0: DISABLE:** Enabled drive from array bottom, top drive enabled. **0x1: ENABLE:** Disabled drive from array bottom, top drive disabled.

17.1.2 UDB_BCTL_MDCLK_EN

Master Digital Clock Enable Register

Address: 0x400F6001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BCTL0_DCEN [7:0]							

Bits	Name	Description
7 : 0	BCTL0_DCEN	Master digital clock enable for the digital clock that matches the index. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

17.1.3 UDB_BCTL_MBCLK_EN

Master Digital Clock Enable Register

Address: 0x400F6002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							BCTL0_BCEN

Bits	Name	Description
0	BCTL0_BCEN	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

17.1.4 UDB_BCTL_BOTSEL_L

Lower Nibble Bottom Digital Clock Select Register

Address: 0x400F6008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	BCTL0_CLK_SEL3 [7:6]		BCTL0_CLK_SEL2 [5:4]		BCTL0_CLK_SEL1 [3:2]		BCTL0_CLK_SEL0 [1:0]	

Bits	Name	Description
7 : 6	BCTL0_CLK_SEL3	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	BCTL0_CLK_SEL2	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	BCTL0_CLK_SEL1	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	BCTL0_CLK_SEL0	Clock selection control for digital clock Default Value: 0

17.1.4 UDB_BCTL_BOTSEL_L (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

17.1.5 UDB_BCTL_BOTSEL_U

Upper Nibble Bottom Digital Clock Select Register

Address: 0x400F6009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	BCTL0_CLK_SEL7 [7:6]		BCTL0_CLK_SEL6 [5:4]		BCTL0_CLK_SEL5 [3:2]		BCTL0_CLK_SEL4 [1:0]	

Bits	Name	Description
7 : 6	BCTL0_CLK_SEL7	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	BCTL0_CLK_SEL6	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	BCTL0_CLK_SEL5	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	BCTL0_CLK_SEL4	Clock selection control for digital clock Default Value: 0

17.1.5 UDB_BCTL_BOTSEL_U (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

17.1.6 UDB_BCTL_TOPSEL_L

Lower Nibble Top Digital Clock Select Register

Address: 0x400F600A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	BCTL0_CLK_SEL3 [7:6]		BCTL0_CLK_SEL2 [5:4]		BCTL0_CLK_SEL1 [3:2]		BCTL0_CLK_SEL0 [1:0]	

Bits	Name	Description
7 : 6	BCTL0_CLK_SEL3	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	BCTL0_CLK_SEL2	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	BCTL0_CLK_SEL1	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	BCTL0_CLK_SEL0	Clock selection control for digital clock Default Value: 0

17.1.6 UDB_BCTL_TOPSEL_L (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

17.1.7 UDB_BCTL_TOPSEL_U

Upper Nibble Top Digital Clock Select Register

Address: 0x400F600B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	BCTL0_CLK_SEL7 [7:6]		BCTL0_CLK_SEL6 [5:4]		BCTL0_CLK_SEL5 [3:2]		BCTL0_CLK_SEL4 [1:0]	

Bits	Name	Description
7 : 6	BCTL0_CLK_SEL7	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	BCTL0_CLK_SEL6	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	BCTL0_CLK_SEL5	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	BCTL0_CLK_SEL4	Clock selection control for digital clock Default Value: 0

17.1.7 UDB_BCTL_TOPSEL_U (continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

17.1.8 UDB_BCTL_QCLK_EN

Quadrant Digital Clock Enable Registers

Address: 0x400F6010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BCTL0_DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	BCTL0_SLEEP_TEST	BCTL0_NC0	BCTL0_WR_CFG_OPT	BCTL0_GLB_DSI_WR	BCTL0_DISABLE_ROUTE	BCTL0_GCH_WR_HI	BCTL0_GCH_WR_LO	BCTL0_BCEN_Q

Bits	Name	Description
15	BCTL0_SLEEP_TEST	Reserved Default Value: 0
14	BCTL0_NC0	Spare register bit Default Value: 0
13	BCTL0_WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.
12	BCTL0_GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.

17.1.8 UDB_BCTL_QCLK_EN (continued)

11	BCTL0_DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0 **0x0: DISABLE:** The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	BCTL0_GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	BCTL0_GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCTL0_BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	BCTL0_DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

18 UDB Digital System Interconnect Registers

This section discusses the UDB Digital System Interconnect (DSI) registers. It lists all the registers in mapping tables, in address order.

18.1 Register Details

Register Name	Address
UDB_DSI_HC	0x400F4000
UDB_DSI_HV_L	0x400F4080
UDB_DSI_HS	0x400F4090
UDB_DSI_HV_R	0x400F40A8
UDB_DSI_DSIINP	0x400F40C0
UDB_DSI_DSIOUTP	0x400F40CC
UDB_DSI_DSIOUTT	0x400F40D4
UDB_DSI_VS	0x400F40E0

18.1.1 UDB_DSI_HC

DSI HC Tile Configuration

Address: 0x400F4000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI_HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	DSI_HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

18.1.2 UDB_DSI_HV_L

DSI HV Tile Configuration; Left

Address: 0x400F4080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI_HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	DSI_HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

18.1.3 UDB_DSI_HS

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI_HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	DSI_HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

18.1.4 UDB_DSI_HV_R

DSI HV Tile Configuration; Right

Address: 0x400F40A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI_HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	DSI_HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

18.1.5 UDB_DSI_DSIINP

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F40C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSI_PI_BOT [7:4]				DSI_PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	DSI_PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	DSI_PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

18.1.6 UDB_DSI_DSIOUTP

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F40CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSI_PI_BOT [7:4]				DSI_PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	DSI_PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	DSI_PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

18.1.7 UDB_DSI_DSIOUTT

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F40D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSI_PI_BOT [7:4]				DSI_PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	DSI_PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	DSI_PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

18.1.8 UDB_DSI_VS

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F40E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DSI_VS_BOT [7:4]				DSI_VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	DSI_VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	DSI_VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

19 UDB Port Adapter Registers

This section discusses the UDB Port Adapter registers. It lists all the registers in mapping tables, in address order.

19.1 Register Details

Register Name	Address
UDB_PA_CFG0	0x400F5000
UDB_PA_CFG1	0x400F5001
UDB_PA_CFG2	0x400F5002
UDB_PA_CFG3	0x400F5003
UDB_PA_CFG4	0x400F5004
UDB_PA_CFG5	0x400F5005
UDB_PA_CFG6	0x400F5006
UDB_PA_CFG7	0x400F5007
UDB_PA_CFG8	0x400F5008
UDB_PA_CFG9	0x400F5009
UDB_PA_CFG10	0x400F500A
UDB_PA_CFG11	0x400F500B
UDB_PA_CFG12	0x400F500C
UDB_PA_CFG13	0x400F500D
UDB_PA_CFG14	0x400F500E

19.1.1 UDB_PA_CFG0

PA Data In Clock Control Register

Address: 0x400F5000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	PA_NC [7:6]		PA_CLKIN_INV	PA_CLKIN_EN_INV	PA_CLKIN_EN_MODE [3:2]		PA_CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	PA_NC	Spare register bits Default Value: 0
5	PA_CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	PA_CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	PA_CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	PA_CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5]

19.1.1 UDB_PA_CFG0 (continued)

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

19.1.2 UDB_PA_CFG1

PA Data Out Clock Control Register

Address: 0x400F5001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	PA_NC [7:6]		PA_CLKOUT_INV	PA_CLKOUT_EN_INV	PA_CLKOUT_EN_MODE [3:2]		PA_CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	PA_NC	Spare register bits Default Value: 0
5	PA_CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	PA_CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	PA_CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	PA_CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5]

19.1.2 UDB_PA_CFG1 (continued)

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

19.1.3 UDB_PA_CFG2

PA Clock Select Register

Address: 0x400F5002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PA_CLKOUT_SEL [7:4]				PA_CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	PA_CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	PA_CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

19.1.3 UDB_PA_CFG2 (continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

19.1.4 UDB_PA_CFG3

PA Reset Select Register

Address: 0x400F5003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	PA_NC7	PA_RES_OUT_INV	PA_RES_OUT_SEL [5:4]		PA_NC0	PA_RES_IN_INV	PA_RES_IN_SEL [1:0]	

Bits	Name	Description
7	PA_NC7	Spare register bit Default Value: 0
6	PA_RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	PA_RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	PA_NC0	Spare register bit Default Value: 0
2	PA_RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	PA_RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

19.1.4 UDB_PA_CFG3 (continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

19.1.5 UDB_PA_CFG4

PA Reset Enable Register

Address: 0x400F5004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	PA_NC7654 [7:3]					PA_RES_OE_EN	PA_RES_OUT_EN	PA_RES_IN_EN

Bits	Name	Description
7 : 3	PA_NC7654	Spare register bits Default Value: 0
2	PA_RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	PA_RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	PA_RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

19.1.6 UDB_PA_CFG5

PA Reset Pin Select Register

Address: 0x400F5005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	PA_NC7654 [7:3]					None [2:1]		PA_PIN_SEL

Bits	Name	Description
7 : 3	PA_NC7654	Spare register bits Default Value: 0
0	PA_PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

19.1.7 UDB_PA_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_IN_SYNC3 [7:6]		PA_IN_SYNC2 [5:4]		PA_IN_SYNC1 [3:2]		PA_IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	PA_IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	PA_IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	PA_IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	PA_IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

19.1.7 UDB_PA_CFG6 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

19.1.8 UDB_PA_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_IN_SYNC7 [7:6]		PA_IN_SYNC6 [5:4]		PA_IN_SYNC5 [3:2]		PA_IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	PA_IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	PA_IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	PA_IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	PA_IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

19.1.8 UDB_PA_CFG7 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

19.1.9 UDB_PA_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_OUT_SYNC3 [7:6]		PA_OUT_SYNC2 [5:4]		PA_OUT_SYNC1 [3:2]		PA_OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	PA_OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	PA_OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	PA_OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	PA_OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

19.1.9 UDB_PA_CFG8 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

19.1.10 UDB_PA_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_OUT_SYNC7 [7:6]		PA_OUT_SYNC6 [5:4]		PA_OUT_SYNC5 [3:2]		PA_OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	PA_OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	PA_OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	PA_OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	PA_OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

19.1.10 UDB_PA_CFG9 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

19.1.11 UDB_PA_CFG10

PA Output Data Select Register - Low

Address: 0x400F500A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_DATA_SEL3 [7:6]		PA_DATA_SEL2 [5:4]		PA_DATA_SEL1 [3:2]		PA_DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	PA_DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	PA_DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	PA_DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	PA_DATA_SEL0	Data selection for PA output 0 Default Value: 0

19.1.11 UDB_PA_CFG10 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

19.1.12 UDB_PA_CFG11

PA Output Data Select Register - High

Address: 0x400F500B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_DATA_SEL7 [7:6]		PA_DATA_SEL6 [5:4]		PA_DATA_SEL5 [3:2]		PA_DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	PA_DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	PA_DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	PA_DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	PA_DATA_SEL4	Data selection for PA output 4 Default Value: 0

19.1.12 UDB_PA_CFG11 (continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

19.1.13 UDB_PA_CFG12

PA OE Select Register - Low

Address: 0x400F500C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_OE_SEL3 [7:6]		PA_OE_SEL2 [5:4]		PA_OE_SEL1 [3:2]		PA_OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	PA_OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	PA_OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	PA_OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	PA_OE_SEL0	Data selection for PA oe 0 Default Value: 0

19.1.13 UDB_PA_CFG12 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

19.1.14 UDB_PA_CFG13

PA OE Select Register - High

Address: 0x400F500D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_OE_SEL7 [7:6]		PA_OE_SEL6 [5:4]		PA_OE_SEL5 [3:2]		PA_OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	PA_OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	PA_OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	PA_OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	PA_OE_SEL4	Data selection for PA oe 4 Default Value: 0

19.1.14 UDB_PA_CFG13 (continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

19.1.15 UDB_PA_CFG14

PA OE Sync Register

Address: 0x400F500E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PA_OE_SYNC3 [7:6]		PA_OE_SYNC2 [5:4]		PA_OE_SYNC1 [3:2]		PA_OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	PA_OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	PA_OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	PA_OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	PA_OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

19.1.15 UDB_PA_CFG14 (continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

20 UDB Routing Registers

This section discusses the UDB Routing registers. It lists all the registers in mapping tables, in address order.

20.1 Register Details

Register Name	Address
UDB_P_ROUTE_HC	0x400F3100
UDB_P_ROUTE_HV_L	0x400F3180
UDB_P_ROUTE_HS	0x400F3190
UDB_P_ROUTE_HV_R	0x400F31A8
UDB_P_ROUTE_PLD0IN	0x400F31C0
UDB_P_ROUTE_PLD1IN	0x400F31CA
UDB_P_ROUTE_DPIN0	0x400F31D0
UDB_P_ROUTE_DPIN1	0x400F31D2
UDB_P_ROUTE_SCIN	0x400F31D6
UDB_P_ROUTE_SCIOIN	0x400F31D8
UDB_P_ROUTE_RCIN	0x400F31DE
UDB_P_ROUTE_VS	0x400F31E0

20.1.1 UDB_P_ROUTE_HC

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ROUTE_HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	ROUTE_HC_BYTE	RAM configuration bytes for channel Default Value: X

20.1.2 UDB_P_ROUTE_HV_L

UDB Channel HV Tile Configuration; Left

Address: 0x400F3180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ROUTE_HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	ROUTE_HV_BYTE	RAM configuration bytes for channel Default Value: X

20.1.3 UDB_P_ROUTE_HS

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ROUTE_HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	ROUTE_HS_BYTE	RAM configuration bytes for channel Default Value: X

20.1.4 UDB_P_ROUTE_HV_R

UDB Channel HV Tile Configuration; Right

Address: 0x400F31A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ROUTE_HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	ROUTE_HV_BYTE	RAM configuration bytes for channel Default Value: X

20.1.5 UDB_P_ROUTE_PLD0IN

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ROUTE_PI_BOT [7:4]				ROUTE_PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	ROUTE_PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	ROUTE_PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

20.1.6 UDB_P_ROUTE_PLD1IN

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ROUTE_PI_BOT [7:4]				ROUTE_PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	ROUTE_PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	ROUTE_PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

20.1.7 UDB_P_ROUTE_DPIN0

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F31D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ROUTE_PI_BOT [7:4]				ROUTE_PI_TOP [3:0]			

Bits	Name	Description
7 : 4	ROUTE_PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	ROUTE_PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

20.1.8 UDB_P_ROUTE_DPIN1

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F31D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		None	
HW Access	None		R		R		None	
Name	None [7:6]		ROUTE_PI_BOT2 [5:4]		ROUTE_PI_TOP2 [3:2]		None [1:0]	

Bits	Name	Description
5 : 4	ROUTE_PI_BOT2	RAM configuration bits (2) for BOTTOM UDB port interface configuration Default Value: X
3 : 2	ROUTE_PI_TOP2	RAM configuration bits (2) for TOP UDB port interface configuration Default Value: X

20.1.9 UDB_P_ROUTE_SCIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input Control

Address: 0x400F31D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ROUTE_PI_BOT [7:4]				ROUTE_PI_TOP [3:0]			

Bits	Name	Description
7 : 4	ROUTE_PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	ROUTE_PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

20.1.10 UDB_P_ROUTE_SCIOIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input / Output Control

Address: 0x400F31D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ROUTE_PI_BOT [7:4]				ROUTE_PI_TOP [3:0]			

Bits	Name	Description
7 : 4	ROUTE_PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	ROUTE_PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

20.1.11 UDB_P_ROUTE_RCIN

UDB Channel PI Tile Configuration; Reset and Clock Blocks Input Control

Address: 0x400F31DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ROUTE_PI_BOT [7:4]				ROUTE_PI_TOP [3:0]			

Bits	Name	Description
7 : 4	ROUTE_PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	ROUTE_PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

20.1.12 UDB_P_ROUTE_VS

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ROUTE_VS_BOT [7:4]				ROUTE_VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	ROUTE_VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	ROUTE_VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

21 UDB 8-bit Working Registers

This section discusses the UDB 8-bit Working registers. It lists all the registers in mapping tables, in address order.

21.1 Register Details

Register Name	Address
UDB_W8_A0	0x400F0000
UDB_W8_A1	0x400F0010
UDB_W8_D0	0x400F0020
UDB_W8_D1	0x400F0030
UDB_W8_F0	0x400F0040
UDB_W8_F1	0x400F0050
UDB_W8_ST	0x400F0060
UDB_W8_CTL	0x400F0070
UDB_W8_MSK	0x400F0080
UDB_W8_ACTL	0x400F0090
UDB_W8_MC	0x400F00A0

21.1.1 UDB_W8_A0

Accumulator 0

Address: 0x400F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W8_A0 [7:0]							

Bits	Name	Description
7 : 0	W8_A0	Accumulator 0 Default Value: 0

21.1.2 UDB_W8_A1

Accumulator 1

Address: 0x400F0010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W8_A1 [7:0]							

Bits	Name	Description
7 : 0	W8_A1	Accumulator 1 Default Value: 0

21.1.3 UDB_W8_D0

Data 0

Address: 0x400F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W8_D0 [7:0]							

Bits	Name	Description
7 : 0	W8_D0	Data 0 Default Value: 0

21.1.4 UDB_W8_D1

Data 1

Address: 0x400F0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W8_D1 [7:0]							

Bits	Name	Description
7 : 0	W8_D1	Data 1 Default Value: 0

21.1.5 UDB_W8_F0

FIFO 0

Address: 0x400F0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W8_F0 [7:0]							

Bits	Name	Description
7 : 0	W8_F0	Fifo 0 Default Value: X

21.1.6 UDB_W8_F1

FIFO 1

Address: 0x400F0050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W8_F1 [7:0]							

Bits	Name	Description
7 : 0	W8_F1	Fifo 1 Default Value: X

21.1.7 UDB_W8_ST

Status Register

Address: 0x400F0060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	W8_ST [7:0]							

Bits	Name	Description
7 : 0	W8_ST	Status register Default Value: 0

21.1.8 UDB_W8_CTL

Control Register

Address: 0x400F0070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	W8_CTL [7:0]							

Bits	Name	Description
7 : 0	W8_CTL	Control register Default Value: 0

21.1.9 UDB_W8_MSK

Interrupt Mask

Address: 0x400F0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	W8_MSK [6:0]						

Bits	Name	Description
6 : 0	W8_MSK	Interrupt Mask Register Default Value: 0

21.1.10 UDB_W8_ACTL

Auxiliary Control

Address: 0x400F0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		W8_CNT_START	W8_INT_EN	W8_FIFO1_LVL	W8_FIFO0_LVL	W8_FIFO1_CLR	W8_FIFO0_CLR

Bits	Name	Description
5	W8_CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	W8_INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	W8_FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	W8_FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	W8_FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	W8_FIFO0_CLR	FIFO clear Default Value: 0

21.1.10 UDB_W8_ACTL (continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

21.1.11 UDB_W8_MC

PLD Macrocell reading

Address: 0x400F00A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	W8_PLD1_MC [7:4]				W8_PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	W8_PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	W8_PLD0_MC	Read Macrocell 0 Default Value: 0

22 UDB 16-bit Concatenated Working Registers

This section discusses the UDB 16-bit Concatenated Working registers. It lists all the registers in mapping tables, in address order.

22.1 Register Details

Register Name	Address
UDB_CAT16_A	0x400F1000
UDB_CAT16_D	0x400F1040
UDB_CAT16_F	0x400F1080
UDB_CAT16_CTL_ST	0x400F10C0
UDB_CAT16_ACTL_MSK	0x400F1100
UDB_CAT16_MC	0x400F1140

22.1.1 UDB_CAT16_A

Accumulator Registers {A1,A0}

Address: 0x400F1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CAT16_A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CAT16_A1 [15:8]							

Bits	Name	Description
15 : 8	CAT16_A1	Accumulator 1 Register Default Value: 0
7 : 0	CAT16_A0	Accumulator 0 Register Default Value: 0

22.1.2 UDB_CAT16_D

Data Registers {D1,D0}

Address: 0x400F1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CAT16_D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CAT16_D1 [15:8]							

Bits	Name	Description
15 : 8	CAT16_D1	Data 1 Register Default Value: 0
7 : 0	CAT16_D0	Data 0 Register Default Value: 0

22.1.3 UDB_CAT16_F

FIFOs {F1,F0}

Address: 0x400F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CAT16_F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CAT16_F1 [15:8]							

Bits	Name	Description
15 : 8	CAT16_F1	FIFO 1 Default Value: X
7 : 0	CAT16_F0	FIFO 0 Default Value: X

22.1.4 UDB_CAT16_CTL_ST

Status and Control Registers {CTL,ST}

Address: 0x400F10C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CAT16_ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CAT16_CTL [15:8]							

Bits	Name	Description
15 : 8	CAT16_CTL	Control Register Default Value: 0
7 : 0	CAT16_ST	Status Register Default Value: 0

22.1.5 UDB_CAT16_ACTL_MSK

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CAT16_MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CAT16_CNT_START	CAT16_INT_EN	CAT16_FIFO1_LVL	CAT16_FIFO0_LVL	CAT16_FIFO1_CLR	CAT16_FIFO0_CLR

Bits	Name	Description
13	CAT16_CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	CAT16_INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	CAT16_FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	CAT16_FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	CAT16_FIFO1_CLR	FIFO clear Default Value: 0

22.1.5 UDB_CAT16_ACTL_MSK (continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	CAT16_FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	CAT16_MSK	Interrupt Mask Register Default Value: 0

22.1.6 UDB_CAT16_MC

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	CAT16_PLD1_MC [7:4]				CAT16_PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	CAT16_PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	CAT16_PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

23 UDB 16-bit Working Registers

This section discusses the UDB 16-bit Working registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

23.1 Register Details

Register Name	Address
UDB_W16_A0	0x400F1000
UDB_W16_A1	0x400F1020
UDB_W16_D0	0x400F1040
UDB_W16_D1	0x400F1060
UDB_W16_F0	0x400F1080
UDB_W16_F1	0x400F10A0
UDB_W16_ST	0x400F10C0
UDB_W16_CTL	0x400F10E0
UDB_W16_MSK	0x400F1100
UDB_W16_ACTL	0x400F1120
UDB_W16_MC	0x400F1140

23.1.1 UDB_W16_A0

Accumulator 0

Address: 0x400F1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W16_A0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W16_A0_MS [15:8]							

Bits	Name	Description
15 : 8	W16_A0_MS	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	W16_A0_LS	Accumulator 0 for UDB[n] Default Value: 0

23.1.2 UDB_W16_A1

Accumulator 1

Address: 0x400F1020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W16_A1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W16_A1_MS [15:8]							

Bits	Name	Description
15 : 8	W16_A1_MS	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	W16_A1_LS	Accumulator 1 for UDB[n] Default Value: 0

23.1.3 UDB_W16_D0

Data 0

Address: 0x400F1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W16_D0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W16_D0_MS [15:8]							

Bits	Name	Description
15 : 8	W16_D0_MS	Data 0 for UDB[n+1] Default Value: 0
7 : 0	W16_D0_LS	Data 0 for UDB[n] Default Value: 0

23.1.4 UDB_W16_D1

Data 1

Address: 0x400F1060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W16_D1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W16_D1_MS [15:8]							

Bits	Name	Description
15 : 8	W16_D1_MS	Data 1 for UDB[n+1] Default Value: 0
7 : 0	W16_D1_LS	Data 1 for UDB[n] Default Value: 0

23.1.5 UDB_W16_F0

FIFO 0

Address: 0x400F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W16_F0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W16_F0_MS [15:8]							

Bits	Name	Description
15 : 8	W16_F0_MS	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	W16_F0_LS	Fifo 0 for UDB[n] Default Value: X

23.1.6 UDB_W16_F1

FIFO 1

Address: 0x400F10A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W16_F1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W16_F1_MS [15:8]							

Bits	Name	Description
15 : 8	W16_F1_MS	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	W16_F1_LS	Fifo 1 for UDB[n] Default Value: X

23.1.7 UDB_W16_ST

Status Register

Address: 0x400F10C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	W16_ST_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	W16_ST_MS [15:8]							

Bits	Name	Description
15 : 8	W16_ST_MS	Status register for UDB[n+1] Default Value: 0
7 : 0	W16_ST_LS	Status register for UDB[n] Default Value: 0

23.1.8 UDB_W16_CTL

Control Register

Address: 0x400F10E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	W16_CTL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	W16_CTL_MS [15:8]							

Bits	Name	Description
15 : 8	W16_CTL_MS	Control register for UDB[n+1] Default Value: 0
7 : 0	W16_CTL_LS	Control register for UDB[n] Default Value: 0

23.1.9 UDB_W16_MSK

Interrupt Mask

Address: 0x400F1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	W16_MSK_LS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	W16_MSK_MS [14:8]						

Bits	Name	Description
14 : 8	W16_MSK_MS	Interrupt Mask Register Default Value: 0
6 : 0	W16_MSK_LS	Interrupt Mask Register Default Value: 0

23.1.10 UDB_W16_ACTL

Auxiliary Control

Address: 0x400F1120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		W16_CNT_START_LS	W16_INT_EN_LS	W16_FIFO1_LVL_LS	W16_FIFO0_LVL_LS	W16_FIFO1_CLR_LS	W16_FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		W16_CNT_START_MS	W16_INT_EN_MS	W16_FIFO1_LVL_MS	W16_FIFO0_LVL_MS	W16_FIFO1_CLR_MS	W16_FIFO0_CLR_MS

Bits	Name	Description
13	W16_CNT_START_MS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	W16_INT_EN_MS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	W16_FIFO1_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	W16_FIFO0_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

23.1.10 UDB_W16_ACTL (continued)

9	W16_FIFO1_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	W16_FIFO0_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	W16_CNT_START_LS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	W16_INT_EN_LS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	W16_FIFO1_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	W16_FIFO0_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	W16_FIFO1_CLR_LS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	W16_FIFO0_CLR_LS	FIFO clear Default Value: 0

23.1.10 UDB_W16_ACTL (continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

23.1.11 UDB_W16_MC

PLD Macrocell reading

Address: 0x400F1140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	W16_PLD1_MC_LS [7:4]				W16_PLD0_MC_LS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	W16_PLD1_MC_MS [15:12]				W16_PLD0_MC_MS [11:8]			

Bits	Name	Description
15 : 12	W16_PLD1_MC_MS	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	W16_PLD0_MC_MS	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	W16_PLD1_MC_LS	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	W16_PLD0_MC_LS	Read Macrocell 0 for UDB[n] Default Value: 0

24 UDB 32-bit Working Registers

This section discusses the UDB 32-bit Working registers. It lists all the registers in mapping tables, in address order.

24.1 Register Details

Register Name	Address
UDB_W32_A0	0x400F2000
UDB_W32_A1	0x400F2040
UDB_W32_D0	0x400F2080
UDB_W32_D1	0x400F20C0
UDB_W32_F0	0x400F2100
UDB_W32_F1	0x400F2140
UDB_W32_ST	0x400F2180
UDB_W32_CTL	0x400F21C0
UDB_W32_MSK	0x400F2200
UDB_W32_ACTL	0x400F2240
UDB_W32_MC	0x400F2280

24.1.1 UDB_W32_A0

Accumulator 0

Address: 0x400F2000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W32_A0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W32_A0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	W32_A0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	W32_A0_3 [31:24]							

Bits	Name	Description
31 : 24	W32_A0_3	Accumulator 0 for UDB[n+3] Default Value: 0
23 : 16	W32_A0_2	Accumulator 0 for UDB[n+2] Default Value: 0
15 : 8	W32_A0_1	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	W32_A0_0	Accumulator 0 for UDB[n] Default Value: 0

24.1.2 UDB_W32_A1

Accumulator 1

Address: 0x400F2040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W32_A1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W32_A1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	W32_A1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	W32_A1_3 [31:24]							

Bits	Name	Description
31 : 24	W32_A1_3	Accumulator 1 for UDB[n+3] Default Value: 0
23 : 16	W32_A1_2	Accumulator 1 for UDB[n+2] Default Value: 0
15 : 8	W32_A1_1	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	W32_A1_0	Accumulator 1 for UDB[n] Default Value: 0

24.1.3 UDB_W32_D0

Data 0

Address: 0x400F2080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W32_D0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W32_D0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	W32_D0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	W32_D0_3 [31:24]							

Bits	Name	Description
31 : 24	W32_D0_3	Data 0 for UDB[n+3] Default Value: 0
23 : 16	W32_D0_2	Data 0 for UDB[n+2] Default Value: 0
15 : 8	W32_D0_1	Data 0 for UDB[n+1] Default Value: 0
7 : 0	W32_D0_0	Data 0 for UDB[n] Default Value: 0

24.1.4 UDB_W32_D1

Data 1

Address: 0x400F20C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W32_D1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W32_D1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	W32_D1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	W32_D1_3 [31:24]							

Bits	Name	Description
31 : 24	W32_D1_3	Data 1 for UDB[n+3] Default Value: 0
23 : 16	W32_D1_2	Data 1 for UDB[n+2] Default Value: 0
15 : 8	W32_D1_1	Data 1 for UDB[n+1] Default Value: 0
7 : 0	W32_D1_0	Data 1 for UDB[n] Default Value: 0

24.1.5 UDB_W32_F0

FIFO 0

Address: 0x400F2100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W32_F0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W32_F0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	W32_F0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	W32_F0_3 [31:24]							

Bits	Name	Description
31 : 24	W32_F0_3	Fifo 0 for UDB[n+3] Default Value: X
23 : 16	W32_F0_2	Fifo 0 for UDB[n+2] Default Value: X
15 : 8	W32_F0_1	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	W32_F0_0	Fifo 0 for UDB[n] Default Value: X

24.1.6 UDB_W32_F1

FIFO 1

Address: 0x400F2140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	W32_F1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	W32_F1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	W32_F1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	W32_F1_3 [31:24]							

Bits	Name	Description
31 : 24	W32_F1_3	Fifo 1 for UDB[n+3] Default Value: X
23 : 16	W32_F1_2	Fifo 1 for UDB[n+2] Default Value: X
15 : 8	W32_F1_1	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	W32_F1_0	Fifo 1 for UDB[n] Default Value: X

24.1.7 UDB_W32_ST

Status Register

Address: 0x400F2180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	W32_ST_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	W32_ST_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	W32_ST_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	W32_ST_3 [31:24]							

Bits	Name	Description
31 : 24	W32_ST_3	Status register for UDB[n+3] Default Value: 0
23 : 16	W32_ST_2	Status register for UDB[n+2] Default Value: 0
15 : 8	W32_ST_1	Status register for UDB[n+1] Default Value: 0
7 : 0	W32_ST_0	Status register for UDB[n] Default Value: 0

24.1.8 UDB_W32_CTL

Control Register

Address: 0x400F21C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	W32_CTL_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	W32_CTL_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	W32_CTL_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	W32_CTL_3 [31:24]							

Bits	Name	Description
31 : 24	W32_CTL_3	Control register for UDB[n+3] Default Value: 0
23 : 16	W32_CTL_2	Control register for UDB[n+2] Default Value: 0
15 : 8	W32_CTL_1	Control register for UDB[n+1] Default Value: 0
7 : 0	W32_CTL_0	Control register for UDB[n] Default Value: 0

24.1.9 UDB_W32_MSK

Interrupt Mask

Address: 0x400F2200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	W32_MSK_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	W32_MSK_1 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	W32_MSK_2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	W32_MSK_3 [30:24]						

Bits	Name	Description
30 : 24	W32_MSK_3	Interrupt Mask Register Default Value: 0
22 : 16	W32_MSK_2	Interrupt Mask Register Default Value: 0
14 : 8	W32_MSK_1	Interrupt Mask Register Default Value: 0
6 : 0	W32_MSK_0	Interrupt Mask Register Default Value: 0

24.1.10 UDB_W32_ACTL

Auxiliary Control

Address: 0x400F2240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		W32_CNT_START_0	W32_INT_EN_0	W32_FIFO1_LVL_0	W32_FIFO0_LVL_0	W32_FIFO1_CLR_0	W32_FIFO0_CLR_0

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		W32_CNT_START_1	W32_INT_EN_1	W32_FIFO1_LVL_1	W32_FIFO0_LVL_1	W32_FIFO1_CLR_1	W32_FIFO0_CLR_1

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [23:22]		W32_CNT_START_2	W32_INT_EN_2	W32_FIFO1_LVL_2	W32_FIFO0_LVL_2	W32_FIFO1_CLR_2	W32_FIFO0_CLR_2

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		W32_CNT_START_3	W32_INT_EN_3	W32_FIFO1_LVL_3	W32_FIFO0_LVL_3	W32_FIFO1_CLR_3	W32_FIFO0_CLR_3

Bits	Name	Description
29	W32_CNT_START_3	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
28	W32_INT_EN_3	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled

24.1.10 UDB_W32_ACTL (continued)

27	W32_FIFO1_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
26	W32_FIFO0_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
25	W32_FIFO1_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
24	W32_FIFO0_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
21	W32_CNT_START_2	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
20	W32_INT_EN_2	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
19	W32_FIFO1_LVL_2	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
18	W32_FIFO0_LVL_2	FIFO fill status level control Default Value: 0

24.1.10 UDB_W32_ACTL (continued)

		0x0: NORMAL: input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
17	W32_FIFO1_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
16	W32_FIFO0_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
13	W32_CNT_START_1	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	W32_INT_EN_1	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	W32_FIFO1_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	W32_FIFO0_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	W32_FIFO1_CLR_1	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation

24.1.10 UDB_W32_ACTL (continued)

		0x1: CLEAR: Clear FIFO state
8	W32_FIFO0_CLR_1	FIFO clear Default Value: 0
		0x0: NORMAL: Normal FIFO operation
		0x1: CLEAR: Clear FIFO state
5	W32_CNT_START_0	Control Register Counter Enable Default Value: 0
		0x0: DISABLE: Counter disabled
		0x1: ENABLE: Counter enabled
4	W32_INT_EN_0	enable interrupt Default Value: 0
		0x0: DISABLE: Interrupt disabled
		0x1: ENABLE: Interrupt enabled
3	W32_FIFO1_LVL_0	FIFO fill status level control Default Value: 0
		0x0: NORMAL: input mode: FIFO not full; output mode: FIFO not empty
		0x1: MID: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	W32_FIFO0_LVL_0	FIFO fill status level control Default Value: 0
		0x0: NORMAL: input mode: FIFO not full; output mode: FIFO not empty
		0x1: MID: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	W32_FIFO1_CLR_0	FIFO clear Default Value: 0
		0x0: NORMAL: Normal FIFO operation
		0x1: CLEAR: Clear FIFO state
0	W32_FIFO0_CLR_0	FIFO clear Default Value: 0
		0x0: NORMAL: Normal FIFO operation
		0x1: CLEAR: Clear FIFO state

24.1.11 UDB_W32_MC

PLD Macrocell reading

Address: 0x400F2280

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	W32_PLD1_MC_0 [7:4]				W32_PLD0_MC_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	W32_PLD1_MC_1 [15:12]				W32_PLD0_MC_1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	W32_PLD1_MC_2 [23:20]				W32_PLD0_MC_2 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	RW				RW			
Name	W32_PLD1_MC_3 [31:28]				W32_PLD0_MC_3 [27:24]			

Bits	Name	Description
31 : 28	W32_PLD1_MC_3	Read Macrocell 1 for UDB[n+3] Default Value: 0
27 : 24	W32_PLD0_MC_3	Read Macrocell 0 for UDB[n+3] Default Value: 0
23 : 20	W32_PLD1_MC_2	Read Macrocell 1 for UDB[n+2] Default Value: 0
19 : 16	W32_PLD0_MC_2	Read Macrocell 0 for UDB[n+2] Default Value: 0
15 : 12	W32_PLD1_MC_1	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	W32_PLD0_MC_1	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	W32_PLD1_MC_0	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	W32_PLD0_MC_0	Read Macrocell 0 for UDB[n] Default Value: 0

25 UDB Interface Registers

This section discusses the UDB Interface registers. It lists all the registers in mapping tables, in address order.

25.1 Register Details

Register Name	Address
UDB_UDBIF_BANK_CTL	0x400F7000
UDB_UDBIF_WAIT_CFG	0x400F7001
UDB_UDBIF_INT_CLK_CTL	0x400F701C

25.1.1 UDB_UDBIF_BANK_CTL

Bank Control

Address: 0x400F7000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW	RW	RW	RW	RW
HW Access	R	None		R	R	R	R	R
Name	UDBIF_GLBL_WR	None [6:5]		UDBIF_PIPE	UDBIF_LOCK	UDBIF_BANK_EN	UDBIF_ROUTE_EN	UDBIF_DIS_COR

Bits	Name	Description
7	UDBIF_GLBL_WR	UDB Array Global Writing Option Default Value: 0 **0x0: DISABLE:** Global Writes disabled **0x1: ENABLE:** Global Writes enabled
4	UDBIF_PIPE	Pipelining Control Default Value: 0 **0x0: BYPASS:** Pipelining bypassed **0x1: PIPELINED:** Pipelining enabled
3	UDBIF_LOCK	UDB Array Configuration Locking Default Value: 0 **0x0: MUTABLE:** UDB Array configuration is writable **0x1: LOCKED:** UDB Array configuration is locked
2	UDBIF_BANK_EN	Enable Bank Default Value: 0 **0x0: DISABLE:** Bank disabled **0x1: ENABLE:** Bank enabled
1	UDBIF_ROUTE_EN	Enable Routing Default Value: 0 **0x0: DISABLE:** Routing disabled **0x1: ENABLE:** Routing enabled
0	UDBIF_DIS_COR	Selection of Clear-On-Read Default Value: 0

25.1.1 UDB_UDBIF_BANK_CTL (continued)

0x0: NORMAL:
Clear-On-Read enabled

0x1: DISABLE:
Clear-On-Read disabled

25.1.2 UDB_UDBIF_WAIT_CFG

Wait States Configuration

Address: 0x400F7001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	UDBIF_WR_WRK_WAIT [7:6]		UDBIF_RD_WRK_WAIT [5:4]		UDBIF_WR_CFG_WAIT [3:2]		UDBIF_RD_CFG_WAIT [1:0]	

Bits	Name	Description
7 : 6	UDBIF_WR_WRK_WAIT	Write Work Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
5 : 4	UDBIF_RD_WRK_WAIT	Read Work Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
3 : 2	UDBIF_WR_CFG_WAIT	Write Configuration Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
1 : 0	UDBIF_RD_CFG_WAIT	Read Configuration Wait States Default Value: 0

25.1.2 UDB_UDBIF_WAIT_CFG (continued)

0x0: FIVE_WAITS:
5 wait states

0x1: FOUR_WAITS:
4 wait states

0x2: THREE_WAITS:
3 wait states

0x3: ONE_WAIT:
1 wait state

25.1.3 UDB_UDBIF_INT_CLK_CTL

Interrupt Synchronizer Clock Control

Address: 0x400F701C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							UDBIF_EN_HFCLK

Bits	Name	Description
0	UDBIF_EN_HFCLK	This bit enables the interrupt synchronizer in the UDB interface. It needs to be set whenever UDB/DSI interrupts are used. Disabling the interrupt synchronizer saves power in Active/Sleep mode. Default Value: 0

26 UDB Single Configuration Registers

This section discusses the UDB Single Configuration registers. It lists all the registers in mapping tables, in address order.

26.1 Register Details

Register Name	Address
UDB_P_U_PLD_IT	0x400F3000
UDB_P_U_PLD_ORT	0x400F3030
UDB_P_U_PLD_MC_CFG_CEN_CONST	0x400F3038
UDB_P_U_PLD_MC_CFG_XORFB	0x400F303A
UDB_P_U_PLD_MC_SET_RESET	0x400F303C
UDB_P_U_PLD_MC_CFG_BYPASS	0x400F303E
UDB_P_U_CFG0	0x400F3040
UDB_P_U_CFG1	0x400F3041
UDB_P_U_CFG2	0x400F3042
UDB_P_U_CFG3	0x400F3043
UDB_P_U_CFG4	0x400F3044
UDB_P_U_CFG5	0x400F3045
UDB_P_U_CFG6	0x400F3046
UDB_P_U_CFG7	0x400F3047
UDB_P_U_CFG8	0x400F3048
UDB_P_U_CFG9	0x400F3049
UDB_P_U_CFG10	0x400F304A
UDB_P_U_CFG11	0x400F304B
UDB_P_U_CFG12	0x400F304C
UDB_P_U_CFG13	0x400F304D
UDB_P_U_CFG14	0x400F304E
UDB_P_U_CFG15	0x400F304F
UDB_P_U_CFG16	0x400F3050
UDB_P_U_CFG17	0x400F3051
UDB_P_U_CFG18	0x400F3052
UDB_P_U_CFG19	0x400F3053
UDB_P_U_CFG20	0x400F3054

Register Name	Address
UDB_P_U_CFG21	0x400F3055
UDB_P_U_CFG22	0x400F3056
UDB_P_U_CFG23	0x400F3057
UDB_P_U_CFG24	0x400F3058
UDB_P_U_CFG25	0x400F3059
UDB_P_U_CFG26	0x400F305A
UDB_P_U_CFG27	0x400F305B
UDB_P_U_CFG28	0x400F305C
UDB_P_U_CFG29	0x400F305D
UDB_P_U_CFG30	0x400F305E
UDB_P_U_CFG31	0x400F305F
UDB_P_U_DCFG	0x400F3060

26.1.1 UDB_P_U_PLD_IT

PLD Input Terms

Address: 0x400F3000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD0_ITxC_7	U_PLD0_ITxC_6	U_PLD0_ITxC_5	U_PLD0_ITxC_4	U_PLD0_ITxC_3	U_PLD0_ITxC_2	U_PLD0_ITxC_1	U_PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD1_ITxC_7	U_PLD1_ITxC_6	U_PLD1_ITxC_5	U_PLD1_ITxC_4	U_PLD1_ITxC_3	U_PLD1_ITxC_2	U_PLD1_ITxC_1	U_PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD0_ITxT_7	U_PLD0_ITxT_6	U_PLD0_ITxT_5	U_PLD0_ITxT_4	U_PLD0_ITxT_3	U_PLD0_ITxT_2	U_PLD0_ITxT_1	U_PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD1_ITxT_7	U_PLD1_ITxT_6	U_PLD1_ITxT_5	U_PLD1_ITxT_4	U_PLD1_ITxT_3	U_PLD1_ITxT_2	U_PLD1_ITxT_1	U_PLD1_ITxT_0

Bits	Name	Description
31	U_PLD1_ITxT_7	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
30	U_PLD1_ITxT_6	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
29	U_PLD1_ITxT_5	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
28	U_PLD1_ITxT_4	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X

26.1.1 UDB_P_U_PLD_IT (continued)

27	U_PLD1_ITxT_3	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
26	U_PLD1_ITxT_2	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
25	U_PLD1_ITxT_1	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
24	U_PLD1_ITxT_0	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
23	U_PLD0_ITxT_7	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
22	U_PLD0_ITxT_6	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
21	U_PLD0_ITxT_5	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
20	U_PLD0_ITxT_4	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
19	U_PLD0_ITxT_3	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
18	U_PLD0_ITxT_2	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
17	U_PLD0_ITxT_1	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
16	U_PLD0_ITxT_0	True input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
15	U_PLD1_ITxC_7	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
14	U_PLD1_ITxC_6	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
13	U_PLD1_ITxC_5	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
12	U_PLD1_ITxC_4	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X

26.1.1 UDB_P_U_PLD_IT (continued)

11	U_PLD1_ITxC_3	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
10	U_PLD1_ITxC_2	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
9	U_PLD1_ITxC_1	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
8	U_PLD1_ITxC_0	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
7	U_PLD0_ITxC_7	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
6	U_PLD0_ITxC_6	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
5	U_PLD0_ITxC_5	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
4	U_PLD0_ITxC_4	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
3	U_PLD0_ITxC_3	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
2	U_PLD0_ITxC_2	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
1	U_PLD0_ITxC_1	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
0	U_PLD0_ITxC_0	Complement input term. Bit position corresponds to product term. (ITx denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X

26.1.2 UDB_P_U_PLD_ORT

PLD OR Terms

Address: 0x400F3030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD0_ORT_PTx_7	U_PLD0_ORT_PTx_6	U_PLD0_ORT_PTx_5	U_PLD0_ORT_PTx_4	U_PLD0_ORT_PTx_3	U_PLD0_ORT_PTx_2	U_PLD0_ORT_PTx_1	U_PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD1_ORT_PTx_7	U_PLD1_ORT_PTx_6	U_PLD1_ORT_PTx_5	U_PLD1_ORT_PTx_4	U_PLD1_ORT_PTx_3	U_PLD1_ORT_PTx_2	U_PLD1_ORT_PTx_1	U_PLD1_ORT_PTx_0

Bits	Name	Description
15	U_PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
14	U_PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
13	U_PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
12	U_PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
11	U_PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
10	U_PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
9	U_PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
8	U_PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
7	U_PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X

26.1.2 UDB_P_U_PLD_ORT (continued)

6	U_PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
5	U_PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
4	U_PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
3	U_PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
2	U_PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
1	U_PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X
0	U_PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term.(x denotes input number of the PLD, where "x" varies from 0 to 12) Default Value: X

26.1.3 UDB_P_U_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F3038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD0_MC3_DFF_C	U_PLD0_MC3_CEN	U_PLD0_MC2_DFF_C	U_PLD0_MC2_CEN	U_PLD0_MC1_DFF_C	U_PLD0_MC1_CEN	U_PLD0_MC0_DFF_C	U_PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD1_MC3_DFF_C	U_PLD1_MC3_CEN	U_PLD1_MC2_DFF_C	U_PLD1_MC2_CEN	U_PLD1_MC1_DFF_C	U_PLD1_MC1_CEN	U_PLD1_MC0_DFF_C	U_PLD1_MC0_CEN

Bits	Name	Description
15	U_PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	U_PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	U_PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	U_PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

26.1.3 UDB_P_U_PLD_MC_CFG_CEN_CONST (continued)

11	U_PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	U_PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	U_PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	U_PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	U_PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	U_PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	U_PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	U_PLD0_MC2_CEN	Carry enable Default Value: X

26.1.3 UDB_P_U_PLD_MC_CFG_CEN_CONST (continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	U_PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	U_PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	U_PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	U_PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

26.1.4 UDB_P_U_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F303A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	U_PLD0_MC3_XORFB [7:6]		U_PLD0_MC2_XORFB [5:4]		U_PLD0_MC1_XORFB [3:2]		U_PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	U_PLD1_MC3_XORFB [15:14]		U_PLD1_MC2_XORFB [13:12]		U_PLD1_MC1_XORFB [11:10]		U_PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	U_PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	U_PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	U_PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF

26.1.4 UDB_P_U_PLD_MC_CFG_XORFB (continued)

		0x1: CARRY: Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
9 : 8	U_PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
7 : 6	U_PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
5 : 4	U_PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
3 : 2	U_PLD0_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high

26.1.4 UDB_P_U_PLD_MC_CFG_XORFB (continued)

		0x3: TFF_L: TFF on low
1 : 0	U_PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

26.1.5 UDB_P_U_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F303C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD0_MC3_RESET_SEL	U_PLD0_MC3_SET_SEL	U_PLD0_MC2_RESET_SEL	U_PLD0_MC2_SET_SEL	U_PLD0_MC1_RESET_SEL	U_PLD0_MC1_SET_SEL	U_PLD0_MC0_RESET_SEL	U_PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_PLD1_MC3_RESET_SEL	U_PLD1_MC3_SET_SEL	U_PLD1_MC2_RESET_SEL	U_PLD1_MC2_SET_SEL	U_PLD1_MC1_RESET_SEL	U_PLD1_MC1_SET_SEL	U_PLD1_MC0_RESET_SEL	U_PLD1_MC0_SET_SEL

Bits	Name	Description
15	U_PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	U_PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	U_PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	U_PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

26.1.5 UDB_P_U_PLD_MC_SET_RESET (continued)

11	U_PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	U_PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	U_PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	U_PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	U_PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	U_PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	U_PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	U_PLD0_MC2_SET_SEL	Set select enable Default Value: X

26.1.5 UDB_P_U_PLD_MC_SET_RESET (continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	U_PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	U_PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	U_PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	U_PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

26.1.6 UDB_P_U_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F303E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_NC7	U_PLD0_MC3_BYPASS	U_NC5	U_PLD0_MC2_BYPASS	U_NC3	U_PLD0_MC1_BYPASS	U_NC1	U_PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_NC15	U_PLD1_MC3_BYPASS	U_NC13	U_PLD1_MC2_BYPASS	U_NC11	U_PLD1_MC1_BYPASS	U_NC9	U_PLD1_MC0_BYPASS

Bits	Name	Description
15	U_NC15	Spare register bit Default Value: X
14	U_PLD1_MC3_BYPASS	Bypass selection Default Value: X
		0x0: REGISTER: Registered output
		0x1: COMBINATIONAL: Combinational output
13	U_NC13	Spare register bit Default Value: X
12	U_PLD1_MC2_BYPASS	Bypass selection Default Value: X
		0x0: REGISTER: Registered output
		0x1: COMBINATIONAL: Combinational output
11	U_NC11	Spare register bit Default Value: X
10	U_PLD1_MC1_BYPASS	Bypass selection Default Value: X
		0x0: REGISTER: Registered output
		0x1: COMBINATIONAL: Combinational output

26.1.6 UDB_P_U_PLD_MC_CFG_BYPASS (continued)

9	U_NC9	Spare register bit Default Value: X
8	U_PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	U_NC7	Spare register bit Default Value: X
6	U_PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	U_NC5	Spare register bit Default Value: X
4	U_PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	U_NC3	Spare register bit Default Value: X
2	U_PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	U_NC1	Spare register bit Default Value: X
0	U_PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

26.1.7 UDB_P_U_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F3040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	U_RAD1 [6:4]			None	U_RAD0 [2:0]		

Bits	Name	Description
6 : 4	U_RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	U_RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

26.1.7 UDB_P_U_CFG0 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

26.1.8 UDB_P_U_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F3041

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	U_DP_RTE_BYPASS4	U_DP_RTE_BYPASS3	U_DP_RTE_BYPASS2	U_DP_RTE_BYPASS1	U_DP_RTE_BYPASS0	U_RAD2 [2:0]		

Bits	Name	Description
7	U_DP_RTE_BYPASS4	DP_In bypass ctl Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	U_DP_RTE_BYPASS3	DP_In bypass ctl Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	U_DP_RTE_BYPASS2	DP_In bypass ctl Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	U_DP_RTE_BYPASS1	DP_In bypass ctl Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	U_DP_RTE_BYPASS0	DP_In bypass ctl Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass
2 : 0	U_RAD2	Datapath Permutable Input Mux Default Value: 0

26.1.8 UDB_P_U_CFG1 (continued)

0x0: OFF:
Input off

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

26.1.9 UDB_P_U_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F3042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	U_NC7	U_F1_LD [6:4]			U_DP_RTE_BYPASS5	U_F0_LD [2:0]		

Bits	Name	Description
7	U_NC7	Spare register bit Default Value: 0
6 : 4	U_F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	U_DP_RTE_BYPASS5	DP_In bypass ctl Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	U_F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0]

26.1.9 UDB_P_U_CFG2 (continued)

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

26.1.10 UDB_P_U_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F3043

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	U_D1_LD [6:4]			None	U_D0_LD [2:0]		

Bits	Name	Description
6 : 4	U_D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	U_D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

26.1.10 UDB_P_U_CFG3 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

26.1.11 UDB_P_U_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F3044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	U_CI_MUX [6:4]			None	U_SI_MUX [2:0]		

Bits	Name	Description
6 : 4	U_CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	U_SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

26.1.11 UDB_P_U_CFG4 (continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

26.1.12 UDB_P_U_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F3045

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	U_OUT1 [7:4]				U_OUT0 [3:0]			

Bits	Name	Description
7 : 4	U_OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

26.1.12 UDB_P_U_CFG5 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	U_OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

26.1.13 UDB_P_U_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F3046

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	U_OUT3 [7:4]				U_OUT2 [3:0]			

Bits	Name	Description
7 : 4	U_OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

26.1.13 UDB_P_U_CFG6 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	U_OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

26.1.14 UDB_P_U_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F3047

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	U_OUT5 [7:4]				U_OUT4 [3:0]			

Bits	Name	Description
7 : 4	U_OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

26.1.14 UDB_P_U_CFG7 (continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	U_OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

26.1.15 UDB_P_U_CFG8

Datapath Output Synchronization Option

Address: 0x400F3048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	U_NC7	U_NC6	U_OUT_SYNC [5:0]					

Bits	Name	Description
7	U_NC7	Spare register bit Default Value: 0
6	U_NC6	Spare register bit Default Value: 0
5 : 0	U_OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

26.1.16 UDB_P_U_CFG9

Datapath ALU Mask

Address: 0x400F3049

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	U_AMASK [7:0]							

Bits	Name	Description
7 : 0	U_AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

26.1.17 UDB_P_U_CFG10

Datapath Compare 0 Mask

Address: 0x400F304A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	U_CMASK0 [7:0]							

Bits	Name	Description
7 : 0	U_CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

26.1.18 UDB_P_U_CFG11

Datapath Compare 1 Mask

Address: 0x400F304B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	U_CMASK0 [7:0]							

Bits	Name	Description
7 : 0	U_CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

26.1.19 UDB_P_U_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F304C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	U_CMASK1_EN	U_CMASK0_EN	U_AMASK_EN	U_DEF_SI	U_SI_SELB [3:2]		U_SI_SELA [1:0]	

Bits	Name	Description
7	U_CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	U_CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	U_AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	U_DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	U_SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input

26.1.19 UDB_P_U_CFG12 (continued)

		0x3: CHAIN: Shift in is chained from the previous datapath
1 : 0	U_SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

26.1.20 UDB_P_U_CFG13

Datapath carry in and compare configuration

Address: 0x400F304D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	U_CMP_SELB [7:6]		U_CMP_SELA [5:4]		U_CI_SELB [3:2]		U_CI_SELA [1:0]	

Bits	Name	Description
7 : 6	U_CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	U_CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	U_CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	U_CI_SELA	Datapath carry in source select Default Value: 0

26.1.20 UDB_P_U_CFG13 (continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

26.1.21 UDB_P_U_CFG14

Datapath chaining and MSB configuration

Address: 0x400F304E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	U_MSB_EN	U_MSB_SEL [6:4]			U_CHAIN_CMSB	U_CHAIN_FB	U_CHAIN1	U_CHAIN0

Bits	Name	Description
7	U_MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	U_MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	U_CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath
2	U_CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0

26.1.21 UDB_P_U_CFG14 (continued)

		0x0: DISABLE: CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	U_CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	U_CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

26.1.22 UDB_P_U_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F304F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	U_PI_SEL	U_SHIFT_SEL	U_PI_DYN	U_MSB_SI	U_F1_INSEL [3:2]		U_F0_INSEL [1:0]	

Bits	Name	Description
7	U_PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	U_SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	U_PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	U_MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	U_F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

26.1.22 UDB_P_U_CFG15 (continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	U_F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

26.1.23 UDB_P_U_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F3050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	U_F1_CK_INV	U_F0_CK_INV	U_FIFO_FAST	U_FIFO_CAP	U_FIFO_EDGE	U_FIFO_ASYNC	U_EXT_CRCPRS	U_WRK16_CONCAT

Bits	Name	Description
7	U_F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	U_F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	U_FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	U_FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	U_FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

26.1.23 UDB_P_U_CFG16 (continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	U_FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	U_EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	U_WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

26.1.24 UDB_P_U_CFG17

Datapath FIFO control

Address: 0x400F3051

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			U_FIFO_ADD_SYNC	U_NC3	U_NC2	U_F1_DYN	U_F0_DYN

Bits	Name	Description
4	U_FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	U_NC3	Spare register bit Default Value: 0
2	U_NC2	Spare register bit Default Value: 0
1	U_F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	U_F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

26.1.25 UDB_P_U_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F3052

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	U_CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	U_CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

26.1.26 UDB_P_U_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F3053

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	U_CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	U_CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

26.1.27 UDB_P_U_CFG20

Status Register input mode selection

Address: 0x400F3054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	U_STAT_MD [7:0]							

Bits	Name	Description
7 : 0	U_STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

26.1.28 UDB_P_U_CFG21

Spare register bits

Address: 0x400F3055

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						U_NC1	U_NC0

Bits	Name	Description
1	U_NC1	Spare register bit Default Value: 0
0	U_NC0	Spare register bit Default Value: 0

26.1.29 UDB_P_U_CFG22

SC block configuration control

Address: 0x400F3056

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			U_SC_EXT_RES	U_SC_SYNC_MD	U_SC_INT_MD	U_SC_OUT_CTL [1:0]	

Bits	Name	Description
4	U_SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. In Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	U_SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	U_SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	U_SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

26.1.29 UDB_P_U_CFG22 (continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

26.1.30 UDB_P_U_CFG23

Counter Control

Address: 0x400F3057

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	U_ALT_CNT	U_ROUTE_EN	U_ROUTE_LD	U_CNT_EN_SEL [3:2]		U_CNT_LD_SEL [1:0]	

Bits	Name	Description
6	U_ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	U_ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	U_ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	U_CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	U_CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

26.1.30 UDB_P_U_CFG23 (continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

26.1.31 UDB_P_U_CFG24

PLD0 Clock and Reset control

Address: 0x400F3058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	U_RC_RES_SEL1	U_RC_RES_SEL0_OR_FRES	U_RC_INV	U_RC_EN_INV	U_RC_EN_MODE [3:2]		U_RC_EN_SEL [1:0]	

Bits	Name	Description
7	U_RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing Default Value: 0
6	U_RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} s Default Value: 0
5	U_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	U_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	U_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive

26.1.31 UDB_P_U_CFG24 (continued)

1 : 0	U_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

26.1.32 UDB_P_U_CFG25

PLD1 Clock and Reset control

Address: 0x400F3059

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	U_RC_RES_SEL1	U_RC_RES_SEL0_OR_FRES	U_RC_INV	U_RC_EN_INV	U_RC_EN_MODE [3:2]		U_RC_EN_SEL [1:0]	

Bits	Name	Description
7	U_RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing Default Value: 0
6	U_RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} s Default Value: 0
5	U_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	U_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	U_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive

26.1.32 UDB_P_U_CFG25 (continued)

1 : 0	U_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

26.1.33 UDB_P_U_CFG26

Datapath Clock and Reset control

Address: 0x400F305A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	U_RC_RES_SEL1	U_RC_RES_SEL0_OR_FRES	U_RC_INV	U_RC_EN_INV	U_RC_EN_MODE [3:2]		U_RC_EN_SEL [1:0]	

Bits	Name	Description
7	U_RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing Default Value: 0
6	U_RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} s Default Value: 0
5	U_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	U_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	U_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive

26.1.33 UDB_P_U_CFG26 (continued)

1 : 0	U_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

26.1.34 UDB_P_U_CFG27

Status/Control Clock and Reset control

Address: 0x400F305B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	U_RC_RES_SEL1	U_RC_RES_SEL0_OR_FRES	U_RC_INV	U_RC_EN_INV	U_RC_EN_MODE [3:2]		U_RC_EN_SEL [1:0]	

Bits	Name	Description
7	U_RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing Default Value: 0
6	U_RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} s Default Value: 0
5	U_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	U_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	U_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive

26.1.34 UDB_P_U_CFG27 (continued)

1 : 0	U_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

26.1.35 UDB_P_U_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F305C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	U_PLD1_CK_SEL [7:4]				U_PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	U_PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	U_PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

26.1.35 UDB_P_U_CFG28 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

26.1.36 UDB_P_U_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F305D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	U_SC_CK_SEL [7:4]				U_DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	U_SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	U_DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

26.1.36 UDB_P_U_CFG29 (continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

26.1.37 UDB_P_U_CFG30

Reset control

Address: 0x400F305E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	U_SC_RES_POL	U_DP_RES_POL	None	U_GUDB_WR	U_EN_RES_CNTCTL	U_RES_POL	U_RES_SEL [1:0]	

Bits	Name	Description
7	U_SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	U_DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	U_GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	U_EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the r Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register
2	U_RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0

26.1.37 UDB_P_U_CFG30 (continued)

		0x0: NEGATED: Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	U_RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

26.1.38 UDB_P_U_CFG31

Reset control

Address: 0x400F305F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	U_PLD1_RES_POL	U_PLD0_RES_POL	U_EXT_CK_SEL [5:4]		U_EN_RES_DP	U_EN_RES_STAT	U_EXT_SYNC	U_ALT_RES

Bits	Name	Description
7	U_PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	U_PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available in the PLD block for both PLDs, therefore this bit contr Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	U_EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	U_EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

26.1.38 UDB_P_U_CFG31 (continued)

2	U_EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	U_EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	U_ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs.; Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control it's individual routed reset.

26.1.39 UDB_P_U_DCFG

Dynamic Configuration RAM

Address: 0x400F3060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	U_A0_WR_SRC [7:6]		U_A1_WR_SRC [5:4]		U_CFB_EN	U_CI_SEL	U_SI_SEL	U_CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	U_FUNC [15:13]			U_SRC_A	U_SRC_B [11:10]		U_SHIFT [9:8]	

Bits	Name	Description
15 : 13	U_FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	U_SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	U_SRC_B	Dynamic ALU source B selection Default Value: X

26.1.39 UDB_P_U_DCFG (continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	U_SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	U_A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	U_A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	U_CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

26.1.39 UDB_P_U_DCFG (continued)

2	U_CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	U_SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	U_CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

Revision History

Revision History

Document Title: PSoC 4100/4200 Family PSoC® 4 Registers TRM (Technical Reference Manual) Document Number: 001-85847				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	3971396	04/17/2013	OWEN	New TRM
*A	4035068	06/23/2013	OWEN	Added Registers
*B	5272449	05/18/2016	NIDH	Update Template. Reorganized TRM Chapters. Added CSD config, IDAC and counter registers. Added all instances of SCB, TCPWM, and GPIO_PRT registers