nRF52832

Rev 1

Errata

v1.9

NORDIC® SEMICONDUCTOR

Contents

1 nRF52832 Rev 1 Errata

This Errata document contains anomalies for the nRF52832 chip, revision Rev 1 (QFAA-Bx0, QFAB-Bx0, CIAA-Bx0).

The document indicates which anomalies are fixed, inherited, or new compared to revision Engineering C.

2 Change log

See the following list for an overview of changes from previous versions of this document.

Version	Date	Change
nRF52832 Rev 1 v1.9	31.01.2019	• Added: No. 204. “Switching beween TX and RX causes unwanted emissions” • Added: No. 210. “Bits in GPIO LATCH register are incorrectly set to 1”
nRF52832 Rev 1 v1.8	23.03.2018	• Updated: No. 89. “Static 400 µA current while using GPIOTE” • Updated: No. 107. “Immediate address match for access addresses containing MSBs 0x00” • Updated: No. 143. “False CRC failures on specific addresses” • Added: No. 192. “LFRC frequency offset after calibration” • Added: No. 194. “STOP task does not switch off all resources” • Added: No. 196. “PSEL acquires GPIOs regardless of ENABLE” • Added: No. 201. “EVENTS_HFCLKSTARTED might be generated twice”
nRF52832 Rev 1 v1.7	13.11.2017	• Added: No. 173. “Writes to LATCH register take several CPU cycles to take effect” • Added: No. 176. “Flash erase through CTRL-AP fails due to watchdog time-out” • Added: No. 178. “END event firing too early” • Added: No. 179. “COMPARE event is generated twice from a single RTC compare match” • Added: No. 181. “Invalid value in FICR for double-size NFCID1 ” • Added: No. 183. “False SEQEND[0] and SEQEND[1] events”
nRF52832 Rev 1 v1.6	12.07.2017	• Updated: No. 12. “Reference ladder is not correctly calibrated” • Updated: No. 66. “Linearity specification not met with default settings” • Updated: No. 79. “ A false EVENTS_FIELDDETECTED event occurs after the field is lost” • Added: No. 102. “PAYLOAD/END events delayed or not triggered after ADDRESS” • Added: No. 106. “Higher CRC error rates for some access addresses” • Added: No. 107. “Immediate address match for access addresses containing MSBs 0x00” • Added: No. 143. “False CRC failures on specific addresses” • Added: No. 149. “First clock pulse after clock stretching may be too long or too short” • Added: No. 155. “IN event may occur more than once on input edge” • Added: No. 156. “Some CLR tasks give unintentional behavior” • Added: No. 163. “Code and RAM size fields do not match chip specification”

Version	Date	Change
nRF52832 Rev 1 v1.5	21.04.2017	• Updated: No. 136. “Bits in RESETREAS are set when they should not be” • Added: No. 146. “LFRC frequency deviation” • Added: No. 150. “EVENT_STARTED does not fire”
nRF52832 Rev 1 v1.4	12.01.2017	• Updated the attachment of No. 109. “DMA access transfers might be corrupted”
nRF52832 Rev 1 v1.3	16.12.2016	• Added: No. 101. “Sleep current increases after soft reset” • Added: No. 109. “DMA access transfers might be corrupted” • Added: No. 113. “Single-ended mode with external reference is not functional” • Added: No. 132. “The LFRC oscillator might not start” • Added: No. 136. “Bits in RESETREAS are set when they should not be” • Added: No. 138. “Spurious emission on GPIO exceeds limits in radiated tests” • Added: No. 141. “HFCLK not stopped when entering SENSE mode”
nRF52832 Rev 1 v1.2	28.09.2016	• Added: No. 108. “RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode”
nRF52832 Rev 1 v1.1	05.07.2016	• Added: No. 84. “ISOURCE not functional” • Added: No. 86. “Triggering START task after offset calibration may write a sample to RAM” • Added: No. 87. “Unexpected wake from System ON Idle when using FPU” • Added: No. 88. “Increased current consumption when configured to pause in System ON idle” • Added: No. 89. “Static 400 µA current while using GPIOTE” • Added: No. 91. “ Radio performance using CSP package version” • Added: No. 97. “High current consumption in System ON Idle mode”

Version	Date	Change
nRF52832 Rev 1 v1.0	17.02.2016	• Added: No. 12. “Reference ladder is not correctly calibrated” • Added: No. 15. “RAM[x].POWERSET/CLR read as zero” • Added: No. 20. “Register values are invalid” • Added: No. 31. “Calibration values are not correctly loaded from FICR at reset” • Added: No. 36. “Some registers are not reset when expected” • Added: No. 51. “Aligned stereo slave mode does not work” • Added: No. 54. “Wrong LRCK polarity in Aligned mode” • Added: No. 55. “RXPTRUPD and TXPTRUPD events asserted after STOP” • Added: No. 58. “An additional byte is clocked out when RXD.MAXCNT = 1” • Added: No. 64. “Only full bytes can be received or transmitted, but supports 4-bit frame transmit” • Added: No. 66. “Linearity specification not met with default settings” • Added: No. 67. “Some events cannot be used with the PPI” • Added: No. 68. “EVENTS_HFCLKSTARTED can be generated before HFCLK is stable” • Added: No. 72. “TASKS_ACTIVATE cannot be used with the PPI” • Added: No. 74. “Started events fires prematurely” • Added: No. 75. “Increased current consumption” • Added: No. 76. “READY event is set sooner than it should” • Added: No. 77. “RC oscillator is not calibrated when first started” • Added: No. 78. “High current consumption when using timer STOP task only” • Added: No. 79. “ A false EVENTS_FIELDDETECTED event occurs after the field is lost” • Added: No. 81. “PIN_CNF is not retained when in debug interface mode” • Added: No. 83. “STOPPED event occurs twice if the STOP task is triggered during a transaction”

3 New and inherited anomalies

The following anomalies are present in revision Rev 1 of the nRF52832 chip.

ID	Module	Description	New in Rev 1	Inherited from Engineering C
12	COMP	Reference ladder is not correctly calibrated		X
15	POWER	RAM[x].POWERSET/CLR read as zero		X
20	RTC	Register values are invalid		X
31	CLOCK	Calibration values are not correctly loaded from FICR at reset		X
36	CLOCK	Some registers are not reset when expected		X
51	I2S	Aligned stereo slave mode does not work		X
54	I2S	Wrong LRCK polarity in Aligned mode		X
55	I2S	RXPTRUPD and TXPTRUPD events asserted after STOP		X
58	SPIM	An additional byte is clocked out when RXD.MAXCNT = 1		X
64	NFCT	Only full bytes can be received or transmitted, but supports 4-bit frame transmit		X
66	TEMP	Linearity specification not met with default settings		X
67	NFCT,PPI	Some events cannot be used with the PPI		X
68	CLOCK	EVENTS_HFCLKSTARTED can be generated before HFCLK is stable		X
72	NFCT,PPI	TASKS_ACTIVATE cannot be used with the PPI		X
74	SAADC	Started events fires prematurely		X
75	MWU	Increased current consumption		X
76	LPCOMP	READY event is set sooner than it should		X
77	CLOCK	RC oscillator is not calibrated when first started		X
78	TIMER	High current consumption when using timer STOP task only		X
79	NFCT	A false EVENTS_FIELDDETECTED event occurs after the field is lost		X
81	GPIO	PIN_CNF is not retained when in debug interface mode		X
83	TWIS	STOPPED event occurs twice if the STOP task is triggered during a transaction		X
84	COMP	ISOURCE not functional		X

ID	Module	Description	New in Rev 1	Inherited from Engineering C
86	SAADC	Triggering START task after offset calibration may write a sample to RAM		X
87	CPU	Unexpected wake from System ON Idle when using FPU		X
88	WDT	Increased current consumption when configured to pause in System ON idle		X
89	GPIOTE	Static 400 µA current while using GPIOTE		X
91	RADIO	Radio performance using CSP package version		X
97	GPIOTE	High current consumption in System ON Idle mode		X
101	CLOCK	Sleep current increases after soft reset		X
102	RADIO	PAYLOAD/END events delayed or not triggered after ADDRESS		X
106	RADIO	Higher CRC error rates for some access addresses		X
107	RADIO	Immediate address match for access addresses containing MSBs 0x00		X
108	RAM	RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode		X
109	DMA	DMA access transfers might be corrupted		X
113	COMP	Single-ended mode with external reference is not functional		X
132	CLOCK	The LFRC oscillator might not start		X
136	System	Bits in RESETREAS are set when they should not be		X
138	RADIO	Spurious emission on GPIO exceeds limits in radiated tests		X
141	NFCT	HFCLK not stopped when entering SENSE mode		X
143	RADIO	False CRC failures on specific addresses		X
146	CLOCK	LFRC frequency deviation		X
149	TWIM	First clock pulse after clock stretching may be too long or too short		X
150	SAADC	EVENT_STARTED does not fire		X
155	GPIOTE	IN event may occur more than once on input edge		X
156	GPIOTE	Some CLR tasks give unintentional behavior		X
163	FICR	Code and RAM size fields do not match chip specification	X	
173	GPIO	Writes to LATCH register take several CPU cycles to take effect		X
176	System	Flash erase through CTRL-AP fails due to watchdog time-out		X

ID	Module	Description	New in Rev 1	Inherited from Engineering C
178	SAADC	END event firing too early		X
179	RTC	COMPARE event is generated twice from a single RTC compare match		X
181	NFCT	Invalid value in FICR for double-size NFCID1	X	
183	PWM	False SEQEND[0] and SEQEND[1] events		X
192	CLOCK	LFRC frequency offset after calibration		X
194	I2S	STOP task does not switch off all resources		X
196	I2S	PSEL acquires GPIOs regardless of ENABLE		X
201	CLOCK	EVENTS_HFCLKSTARTED might be generated twice		X
204	RADIO	Switching beween TX and RX causes unwanted emissions		X
210	GPIO	Bits in GPIO LATCH register are incorrectly set to 1	X	

Table 1: New and inherited anomalies

3.1 [12] COMP: Reference ladder is not correctly calibrated

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

COMP does not compare correctly.

Conditions

Always.

Consequences

COMP module is unusable.

Workaround

Execute the following code before enabling the COMP module:

```
*(volatile uint32_t *)0x40013540 = (*(volatile uint32_t *)0x10000324 & 0x00001F00) >> 8;
```

This workaround is included in MDK version 8.12.0 and later.

3.2 [15] POWER: RAM[x].POWERSET/CLR read as zero

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

RAM[x].POWERSET and RAM[x].POWERCLR read as zero, even though the RAM is on.

Conditions

Always.

Consequences

Not possible to read the RAM state using RAM[x].POWERSET and RAM[x].POWERCLR registers. Write works as it should.

Workaround

Use RAM[x].POWER to read the state of the RAM.

3.3 [20] RTC: Register values are invalid

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

RTC registers will not contain the correct/expected value if read.

Conditions

The RTC has been idle.

Consequences

RTC configuration cannot be determined by reading RTC registers.

Workaround

Execute the below code before you use RTC.

```
NRF_CLOCK->EVENTS_LFCLKSTARTED  = 0;
NRF_CLOCK->TASKS_LFCLKSTART     = 1;
while (NRF_CLOCK->EVENTS_LFCLKSTARTED == 0) {}
NRF_RTC0->TASKS_STOP = 0;
```

3.4 [31] CLOCK: Calibration values are not correctly loaded from FICR at reset

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

RCOSC32KICALLENGTH is initialized with the wrong FICR value.

Conditions

Always.

Consequences

RCOSC32KICALLENGTH default value is wrong.

Workaround

Execute the following code after reset:

```
*(volatile uint32_t *)0x4000053C = ((*(volatile uint32_t *)0x10000244) & 0x0000E000) >>
13;
```

This code is already present in the latest system_nrf52.c file.

3.5 [36] CLOCK: Some registers are not reset when expected

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

After watchdog timeout reset, CPU lockup reset, soft reset, or pin reset, the following CLOCK peripheral registers are not reset:

- CLOCK->EVENTS_DONE
- CLOCK->EVENTS_CTTO
- CLOCK->CTIV

Conditions

After watchdog timeout reset, CPU Lockup reset, soft reset, and pin reset.

Consequences

Register reset values might be incorrect. It may cause undesired interrupts in case of enabling interrupts without clearing the DONE or CTTO events.

Workaround

Clear affected registers after reset. This workaround has already been added into system_nrf52.c file. This workaround has already been added into system_nrf52840.c file present in MDK 8.11.0 or later.

3.6 [51] I2S: Aligned stereo slave mode does not work

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Sample values for the left channel are transmitted twice (for both channels within a frame), sample values for the right channel are lost.

Conditions

CONFIG.MODE = SLAVE, CONFIG.CHANNELS = STEREO, CONFIG.FORMAT = ALIGNED.

Consequences

Aligned format cannot be used for stereo transmission in Slave mode.

Workaround

None.

3.7 [54] I2S: Wrong LRCK polarity in Aligned mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

In Aligned mode, left and right samples are swapped.

Conditions

CONFIG.FORMAT = ALIGNED

Consequences

Left and right audio channels are swapped.

Workaround

Swap left and right samples in memory.

3.8 [55] I2S: RXPTRUPD and TXPTRUPD events asserted after STOP

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The RXPTRUPD event is generated when the STOP task is triggered, even though reception (RX) is disabled. Similarly, the TXPTRUPD event is generated when the STOP task is triggered, even though transmission (TX) is disabled.

Conditions

A previous transfer has been performed with RX/TX enabled, respectively.

Consequences

The indication that RXTXD.MAXCNT words were received/transmitted is false.

Workaround

Ignore the RXPTRUPD and TXPTRUPD events after triggering the STOP task. Clear these events before starting the next transfer.

3.9 [58] SPIM: An additional byte is clocked out when RXD.MAXCNT = 1

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

SPIM clocks out additional byte.

Conditions

RXD.MAXCNT = 1

TXD.MAXCNT <= 1

Consequences

Additional byte is redundant.

Workaround

Use the SPI module (deprecated but still available) or use the following workaround with SPIM:

```
/**
 * @brief Work-around for transmitting 1 byte with SPIM.
 *
 * @param spim: The SPIM instance that is in use.
 * @param ppi_channel: An unused PPI channel that will be used by the workaround.
 * @param gpiote_channel: An unused GPIOTE channel that will be used by the workaround.
 *
 * @warning Must not be used when transmitting multiple bytes.
 * @warning After this workaround is used, the user must reset the PPI channel and the
 GPIOTE channel before attempting to transmit multiple bytes.
 */
void setup_workaround_for_ftpan_58(NRF_SPIM_Type * spim, uint32_t ppi_channel, uint32_t
 gpiote_channel)
{
    // Create an event when SCK toggles.
    NRF_GPIOTE->CONFIG[gpiote_channel] = (
        GPIOTE_CONFIG_MODE_Event <<
        GPIOTE_CONFIG_MODE_Pos
        ) | (
        spim->PSEL.SCK <<
        GPIOTE_CONFIG_PSEL_Pos
        ) | (
        GPIOTE_CONFIG_POLARITY_Toggle <<
        GPIOTE_CONFIG_POLARITY_Pos
        );

    // Stop the spim instance when SCK toggles.
    NRF_PPI->CH[ppi_channel].EEP = (uint32_t)&NRF_GPIOTE->EVENTS_IN[gpiote_channel];
    NRF_PPI->CH[ppi_channel].TEP = (uint32_t)&spim->TASKS_STOP;
    NRF_PPI->CHENSET = 1U << ppi_channel;

    // The spim instance cannot be stopped mid-byte, so it will finish
    // transmitting the first byte and then stop. Effectively ensuring
    // that only 1 byte is transmitted.
}
```

3.10 [64] NFCT: Only full bytes can be received or transmitted, but supports 4-bit frame transmit

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Data bits are not transmitted, or appear to not be received, if the Frame length is not a multiple of 8 bits (i.e. Frame includes data bits).

Conditions

Frame length is not a multiple of 8 bits (bytes only). Exception: 4-bit frame transmit supported.

Consequences

Partial bytes cannot be transferred:

- TXD.AMOUNT.TXDATABITS must be 0
- RXD.AMOUNT.RXDATABITS must be 0

Workaround

None

3.11 [66] TEMP: Linearity specification not met with default settings

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

TEMP module provides non-linear temperature readings over the specified temperature range.

Conditions

Always.

Consequences

TEMP module returns out of spec temperature readings.

Workaround

Execute the following code after reset:

```
NRF_TEMP->A0 = NRF_FICR->TEMP.A0;
NRF_TEMP->A1 = NRF_FICR->TEMP.A1;
NRF_TEMP->A2 = NRF_FICR->TEMP.A2;
NRF_TEMP->A3 = NRF_FICR->TEMP.A3;
NRF_TEMP->A4 = NRF_FICR->TEMP.A4;
NRF_TEMP->A5 = NRF_FICR->TEMP.A5;
NRF_TEMP->B0 = NRF_FICR->TEMP.B0;
NRF_TEMP->B1 = NRF_FICR->TEMP.B1;
NRF_TEMP->B2 = NRF_FICR->TEMP.B2;
NRF_TEMP->B3 = NRF_FICR->TEMP.B3;
NRF_TEMP->B4 = NRF_FICR->TEMP.B4;
NRF_TEMP->B5 = NRF_FICR->TEMP.B5;
NRF_TEMP->T0 = NRF_FICR->TEMP.T0;
NRF_TEMP->T1 = NRF_FICR->TEMP.T1;
NRF_TEMP->T2 = NRF_FICR->TEMP.T2;
NRF_TEMP->T3 = NRF_FICR->TEMP.T3;
NRF_TEMP->T4 = NRF_FICR->TEMP.T4;
```

This code is already present in the latest system_nrf52.c file and in the system_nrf52840.c file released in MDK 8.12.0.

3.12 [67] NFCT,PPI: Some events cannot be used with the PPI

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The following NFCT events do not trigger tasks when used with the PPI:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Conditions

PPI is used to trigger peripheral tasks using the NFCT events.

Consequences

The PPI cannot be used to trigger tasks using the following NFCT events:

- EVENTS_AUTOCOLRESSTARTED
- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Workaround

The EVENTS_AUTOCOLRESSTARTED cannot be used with the PPI.

Subtract an offset of 0x04 while configuring the PPI event end points for the following NFCT events:

- EVENTS_COLLISION
- EVENTS_SELECTED
- EVENTS_STARTED

Examples:

```
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_COLLISION) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_SELECTED) - 0x04;
NRF_PPI->CH[x].EEP = ((uint32_t) &NRF_NFCT->EVENTS_STARTED) - 0x04;
```

3.13 [68] CLOCK: EVENTS_HFCLKSTARTED can be generated before HFCLK is stable

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

EVENTS_HFCLKSTARTED may come before HFXO is started.

Conditions

When using a 32 MHz crystal with start-up longer than 400 µs.

Consequences

Performance of radio and peripheral requiring HFXO will be degraded until the crystal is stable.

Workaround

32 MHz crystal oscillator startup time must be verified by the user. If the worst-case startup time is shorter than 400 µs, no workaround is required. If the startup time can be longer than 400 µs, the software must ensure, using a timer, that the crystal has had enough time to start up before using peripherals that require the HFXO. The Radio requires the HFXO to be stable before use. The ADC, TIMERs, and TEMP sensor for example can use the HFXO as a reference for improved accuracy.

3.14 [72] NFCT,PPI: TASKS_ACTIVATE cannot be used with the PPI

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The NFCT peripheral does not get activated when the PPI is configured to trigger TASKS_ACTIVATE on any event.

Conditions

Always

Consequences

The TASKS_ACTIVATE cannot be used with the PPI.

Workaround

None

3.15 [74] SAADC: Started events fires prematurely

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

False EVENTS_STARTED

Conditions

TACQ <= 5 µs

Consequences

The EVENTS_STARTED can come when not expected

Workaround

The module must be fully configured before it is enabled, and the TACQ configuration must be the last configuration set before ENABLE.

3.16 [75] MWU: Increased current consumption

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Increased current consumption in System ON IDLE.

Conditions

When MWU is enabled.

Consequences

Increased current consumption in System ON IDLE.

Workaround

Do not use MWU or disable MWU before WFE/WFI, enable it on IRQ.

3.17 [76] LPCOMP: READY event is set sooner than it should

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

May receive unexpected events and wakeups from LPCOMP.

Conditions

LPCOMP is configured to send an event or to wake up the chip. LPCOMP.TASKS_START task is set and LPCOMP.EVENTS_READY event has been received.

Consequences

Unpredictable system behavior caused by falsely triggered events and wakeups.

Workaround

Use the following configuration sequence.

1. Configure the LPCOMP to send an event or wake up the chip, but do not enable any PPI channels or IRQ to be triggered from the LPCOMP events.
2. Trigger the LPCOMP.TASKS_START task and wait for the LPCOMP.EVENTS_READY event.
3. After receiving the LPCOMP.EVENTS_READY event wait for 115 µs.
4. After 115 µs, clear the LPCOMP.EVENTS_DOWN, LPCOMP.EVENTS_UP, and LPCOMP.EVENTS_CROSS events. LPCOMP is now ready to be used.

3.18 [77] CLOCK: RC oscillator is not calibrated when first started

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The LFCLK RC oscillator frequency can have a frequency error of up to -25 to +40% after reset. A +/- 2% error is stated in the Product Specification.

Conditions

Always.

Consequences

The LFCLK RC oscillator frequency is inaccurate.

Workaround

Calibrate the LFCLK RC oscillator before its first use after a reset.

3.19 [78] TIMER: High current consumption when using timer STOP task only

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Increased current consumption when the timer has been running and the STOP task is used to stop it.

Conditions

The timer has been running (after triggering a START task) and then it is stopped using a STOP task only.

Consequences

Increased current consumption.

Workaround

Use the SHUTDOWN task after the STOP task or instead of the STOP task.

3.20 [79] NFCT: A false EVENTS_FIELDDETECTED event occurs after the field is lost

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

A false EVENTS_FIELDDETECTED event occurs.

Conditions

The task TASK_SENSE is triggered within 270 µs of the event EVENTS_FIELDLOST.

Consequences

EVENTS_FIELDDETECTED will occur after a field is lost. (SHORT between eventfieldlost and taskSense should not be used since a false fieldDetected event will occur from using the task.)

Workaround

- Wait 170 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE for temperatures ≥ 0°C.
- Wait 270 µs after an EVENTS_FIELDLOST event before triggering TASK_SENSE for temperatures < 0°C.

Important: This anomaly was changed compared to the original publication.

3.21 [81] GPIO: PIN_CNF is not retained when in debug interface mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

GPIO pin configuration is reset on wakeup from System OFF.

Conditions

The system is in debug interface mode.

Consequences

GPIO state unreliable until PIN_CNF is reconfigured.

3.22 [83] TWIS: STOPPED event occurs twice if the STOP task is triggered during a transaction

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

STOPPED event is set after clearing it.

Conditions

The STOP task is triggered during a transaction.

Consequences

STOPPED event occurs twice: When the STOP task is fired and when the master issues a stop condition on the bus. This could provoke an extra interrupt or a failure in the TWIS driver.

Workaround

The last STOPPED event must be accounted for in software.

3.23 [84] COMP: ISOURCE not functional

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The programmable current source (ISOURCE) has too high varation. Variance over temp is >20 times specified nominal value

Conditions

Always.

Consequences

Inaccurate current source.

Workaround

None.

3.24 [86] SAADC: Triggering START task after offset calibration may write a sample to RAM

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The first sample in the result buffer is incorrect, and will be present although the SAMPLE task has never been issued.

Conditions

The START task is triggered after performing calibration (through the CALIBRATEOFFSET task).

Consequences

Incorrect sample data in the result buffer.

Workaround

Calibration should follow the pattern STOP -> STOPPED -> CALIBRATEOFFSET -> CALIBRATEDONE -> STOP -> STOPPED -> START.

3.25 [87] CPU: Unexpected wake from System ON Idle when using FPU

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The CPU is unexpectedly awoken from System ON Idle.

Conditions

The FPU has been used.

Consequences

The CPU is awoken from System ON Idle.

Workaround

The FPU can generate pending interrupts just like other peripherals, but unlike other peripherals there are no INTENSET, INTENCLR registers for enabling or disabling interrupts at the peripheral level. In order to prevent unexpected wake-up from System ON Idle, add this code before entering sleep:

```
#if (__FPU_USED == 1)
 _set_FPSCR(_get_FPSCR() & ~(0x0000009F));
 (void) __get_FPSCR();
 NVIC_ClearPendingIRQ(FPU_IRQn);
#endif
 __WFE();
```

3.26 [88] WDT: Increased current consumption when configured to pause in System ON idle

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Using the mode where watchdog is paused in CPU Idle, the current consumption jumps from 3 µA to 400 µA.

Conditions

When we enable WDT with the CONFIG option to pause when CPU sleeps:

```
NRF_WDT->CONFIG = (WDT_CONFIG_SLEEP_Pause<<WDT_CONFIG_SLEEP_Pos);
```

Consequences

Reduced battery life.

Workaround

Do not enter System ON IDLE within 125 µs after reloading the watchdog.

3.27 [89] GPIOTE: Static 400 µA current while using GPIOTE

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Static current consumption between 400 µA and 450 µA when using SPIM or TWIM in combination with GPIOTE.

Conditions

- GPIOTE is configured in event mode
- TWIM/SPIM utilizes EasyDMA

Consequences

Current consumption higher than specified.

Workaround

Turn the TWIM/SPIM off and back on after it has been disabled. To do so, write 0 followed by 1 to the POWER register (address 0xFFC) of the TWIM/SPIM that must be disabled:

- If TWIM0 or SPIM0 is used:

```
*(volatile uint32_t *)0x40003FFC = 0;
*(volatile uint32_t *)0x40003FFC;
*(volatile uint32_t *)0x40003FFC = 1;
```

- If TWIM1 or SPIM1 is used:

```
*(volatile uint32_t *)0x40004FFC = 0;
*(volatile uint32_t *)0x40004FFC;
*(volatile uint32_t *)0x40004FFC = 1;
```

- If SPIM2 is used:

```
*(volatile uint32_t *)0x40023FFC = 0;
*(volatile uint32_t *)0x40023FFC;
*(volatile uint32_t *)0x40023FFC = 1;
```

Reconfiguration of TWIM/SPIM is required before next usage.

3.28 [91] RADIO: Radio performance using CSP package version

This anomaly applies to IC Rev. Rev 1, build codes CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

WLCSP package has reduced receiver sensitivity compared to QFN packages in LDO and DCDC regulator modes.

Conditions

- Average Sensitivity over all channels degraded in LDO mode by 2 dB.
- Average Sensitivity over all channels degraded in DCDC mode by 4 dB.

Consequences

Reduced receiver sensitivity.

Workaround

None.

3.29 [97] GPIOTE: High current consumption in System ON Idle mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

High current consumption (<20 µA) in System ON Idle mode.

Conditions

GPIOTE used with one or more channels in input mode.

Consequences

Higher current consumption.

Workaround

Use Port event to detect transitions on inputs instead of GPIOTE input mode.

3.30 [101] CLOCK: Sleep current increases after soft reset

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Sleep current with LFXO active is 0.5 µA higher than expected.

Conditions

Low frequency crystal oscillator is active, due to use of RTC or WDT, and a soft-reset is issued or a CPU lock-up reset occurs.

Consequences

Increased sleep current.

Workaround

None.

3.31 [102] RADIO: PAYLOAD/END events delayed or not triggered after ADDRESS

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

After the ADDRESS event, the PAYLOAD/END events might not trigger until another packet is received with the same access address. The frequency at which this occurs is low (<0.1% of packets).

Conditions

BLE and Nordic proprietary radio mode. Radio receive mode.

Consequences

The radio remains in receive mode until the next packet is received. Both packets are lost.

Workaround

Use one of the following workarounds:

- Use SoftDevice s132_nrf52_4.0.2 or later and the ESB and Gazell libraries of SDK v14.0.0 or later.

  These implementations prevent the radio from remaining in receive mode when a packet is not received.

- Apply the following code before triggering the RXEN task:

```
 *(volatile uint32_t *) 0x40001774 = ((*(volatile uint32_t *) 0x40001774) & 0xfffffffe)
| 0x01000000;
```

  This code will reduce sensitivity with 3 dB.

3.32 [106] RADIO: Higher CRC error rates for some access addresses

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Payload in RX is corrupted.

Conditions

BLE and Nordic proprietary radio mode. 4 and 5 byte addresses. 1 in 1600 (<0.07%) randomly generated BLE addresses and 1 in 1200 (<0.09%) randomly generated proprietary addresses are affected.

Consequences

The radio reports up to 30% CRC error rate for packets being received when affected access addresses are used. For BLE, new access addresses are generated on each connection so the symptom is rare and not persistent.

Workaround

Use one of the following workarounds:

- Use SoftDevice s132_nrf52_4.0.2 or later and the ESB and Gazell libraries of SDK v14.0.0 or later to avoid higher CRC error rate.

  The S132 SoftDevice detects when affected access addresses are being used in a connection and applies the following workaround resulting in 3 dB reduced sensitivity for approximately 0.1% of connections. The ESB and Gazell libraries apply the following workaround for all addresses.
- Apply the following code before triggering the RXEN task:

```
*(volatile uint32_t *) 0x40001774 = ((*(volatile uint32_t *) 0x40001774) & 0xfffffffe) |
0x01000000;
```

  This code will reduce sensitivity with 3 dB.

3.33 [107] RADIO: Immediate address match for access addresses containing MSBs 0x00

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Loss of connection.

Conditions

1 Mbit/s and 2 Mbit/s Nordic proprietary radio mode and Bluetooth Low Energy radio mode using 4 and 5 byte addresses with certain combinations of 0 in the access address. BLE addresses are not affected.

Consequences

100% packet error rate.

Workaround

Either use the ESB and Gazell libraries of SDK v14.0.0 or later, or avoid using access addresses in the following pattern (where X is don't care):

```
ADDRLEN=5
BASE0    =  0x0000XXXX, PREFIX0 = 0xXXXXXX00
BASE1    =  0x0000XXXX, PREFIX0 = 0xXXXX00XX
BASE1    =  0x0000XXXX, PREFIX0 = 0xXX00XXXX
BASE1    =  0x0000XXXX, PREFIX0 = 0x00XXXXXX
BASE1    =  0x0000XXXX, PREFIX1 = 0xXXXXXX00
BASE1    =  0x0000XXXX, PREFIX1 = 0xXXXX00XX
BASE1    =  0x0000XXXX, PREFIX1 = 0xXX00XXXX
BASE1    =  0x0000XXXX, PREFIX1 = 0x00XXXXXX

ADDRLEN=4
BASE0    =  0x00XXXXXX, PREFIX0 = 0xXXXXXX00
BASE1    =  0x00XXXXXX, PREFIX0 = 0xXXXX00XX
BASE1    =  0x00XXXXXX, PREFIX0 = 0xXX00XXXX
BASE1    =  0x00XXXXXX, PREFIX0 = 0x00XXXXXX
BASE1    =  0x00XXXXXX, PREFIX1 = 0xXXXXXX00
BASE1    =  0x00XXXXXX, PREFIX1 = 0xXXXX00XX
BASE1    =  0x00XXXXXX, PREFIX1 = 0xXX00XXXX
BASE1    =  0x00XXXXXX, PREFIX1 = 0x00XXXXXX
```

3.34 [108] RAM: RAM content cannot be trusted upon waking up from System ON Idle or System OFF mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

RAM not correctly retained.

Conditions

System ON Idle mode or System OFF is used with parts or all RAM retained.

Consequences

RAM not correctly retained.

Workaround

Apply the following code after any reset:

```
*(volatile uint32_t *)0x40000EE4 = (*(volatile uint32_t *)0x10000258 & 0x0000004F);
```

This workaround is implemented in MDK version 8.9.0 and newer version. This workaround increases the I_RAM current per 4 KB section from 20nA to 30nA.

3.35 [109] DMA: DMA access transfers might be corrupted

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The first byte sent out by the peripheral is sometimes wrong.

Conditions

System enters IDLE and stops the 64 MHz clock at the same time as the peripheral that is using DMA is started. This problem affects the peripherals PWM, SPIS, SPIM, TWIS, UARTE, and TWIM.

Consequences

Wrong data sent to external device.

Workaround

Workarounds will be incorporated into SDK v13.0.0. See the following document for a description of the workarounds:

nRF52832 Errata Attachment Anomaly 109 Addendum

3.36 [113] COMP: Single-ended mode with external reference is not functional

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

COMP output is not correct.

Conditions

COMP is used in single-ended mode with external reference.

Consequences

COMP cannot be used in this mode.

Workaround

None.

3.37 [132] CLOCK: The LFRC oscillator might not start

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The LFRC oscillator does not start and the LFCLKSTARTED event is not triggered.

Conditions

The LFRC oscillator is started in the window [66 µs, 138 µs] after the LFRC oscillator has stopped.

Consequences

The LFRC oscillator might become non-functional until it is reset.

Workaround

Delay starting the LFRC oscillator if it was last stopped [66 µs, 138 µs] ago.

3.38 [136] System: Bits in RESETREAS are set when they should not be

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

After pin reset, RESETREAS bits other than RESETPIN might also be set.

Conditions

A pin reset has triggered.

Consequences

If the firmware evaluates RESETREAS, it might take the wrong action.

Workaround

When RESETREAS shows a pin reset (RESETPIN), ignore other reset reason bits.

Important: RESETREAS bits must be cleared between resets.

Apply the following code after any reset:

```
if (NRF_POWER->RESETREAS & POWER_RESETREAS_RESETPIN_Msk){
    NRF_POWER->RESETREAS =  ~POWER_RESETREAS_RESETPIN_Msk;
}
```

This workaround is implemented in MDK version 8.13.0 and later.

3.39 [138] RADIO: Spurious emission on GPIO exceeds limits in radiated tests

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Spurious emission in RX mode can exceed ETSI limits.

Conditions

Using the Nordic Development Kit or a product built from reference schematic using GPIO P0.25 and P0.26.

Consequences

Product does not conform to ETSI requirements.

Workaround

Use the updated reference schematics and reference layout, version 1.1 or later, available from Reference layout nRF52832.

3.40 [141] NFCT: HFCLK not stopped when entering SENSE mode

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Higher current consumption than specified in SENSE mode.

Conditions

Going from active mode to SENSE mode.

Consequences

Higher current consumption in SENSE mode than specified.

Workaround

Power cycle the NFCT using the POWER register, then issue the SENSE task to enter SENSE mode.

3.41 [143] RADIO: False CRC failures on specific addresses

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

100% CRC failure rate even if the payload is received correctly.

Conditions

1 Mbit/s and 2 Mbit/s Nordic proprietary radio mode and Bluetooth Low Energy. `CRCCNF.SKIPADDR = 0`. CRC calculation includes the address field.

Logical address 0 and logical address 1 to 7 have the same BASE address MSBs configured.

```
ADDRLEN=5
BASE0 = 0xAAAAXXXX
BASE1 = 0xAAAAXXXX
ADDRLENLEN=4
BASE0 = 0xAAXXXXXX
BASE1 = 0xAAXXXXXX
```

AND logical address 0 and one of the logical addresses 1 to 7 have the same PREFIX value configured.

The issue is present regardless of which logical address is enabled in RXADDRESSES.

Consequences

If receiving on logical address 0, the address is reconstructed incorrectly for CRC calculation, resulting in CRCSTATUS.CRCError being returned. However, the received payload bytes are correct. Packet error rate 100 percent. RXMATCH shows the wrong logical address.

Workaround

Use one of the following workarounds:

- Use the ESB and Gazell libraries of SDK v14.0.0 or later.

  This implementation applies the following workaround.
- Set bit 16 in RXADDRESSES to 1.

- Apply the following code before triggering the RXEN task:

```
*(volatile uint32_t *) 0x40001774 = ((*(volatile uint32_t *) 0x40001774) & 0xfffffffe)
| 0x01000000;
```

  This code will reduce sensitivity with 3 dB.

3.42 [146] CLOCK: LFRC frequency deviation

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

The frequency tolerance (fTOL_CAL_LFRC) of the LFRC oscillator is exceeding 250 ppm.

Conditions

Always.

Consequences

Timers using LFRC are not as precise as described in the specification.

Workaround

Account for a frequency tolerance of 500 ppm when using the LFRC oscillator.

3.43 [149] TWIM: First clock pulse after clock stretching may be too long or too short

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

When the TWI slave exits a clock stretching state, the first clock pulse from the master is too long or too short.

The following deviations from the normal clock pulse length can occur:

400 kHz

- Minimum: 0.7 µs
- Maximum: 3.0 µs

100 kHz

- Minimum: 0.7 µs
- Maximum: 11.0 µs

Conditions

TWI slave uses clock stretching.

Consequences

The slave may give an error condition due to a too long or too short clock pulse or the pulse may be lost. This depends on the slave clock stretching behavior.

Workaround

None.

3.44 [150] SAADC: EVENT_STARTED does not fire

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

EVENT_STARTED does not fire.

Conditions

ADC started (TASKS_START) with PPI task. Any channel configured to TACQ <= 5 µs.

Consequences

ADC cannot be started (TASKS_START) with PPI if TACQ <= 5 µs.

Workaround

Use TAQC > 5 µs when starting ADC from PPI.

3.45 [155] GPIOTE: IN event may occur more than once on input edge

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

IN event occurs more than once on an input edge.

Conditions

Input signal edges are closer together than 1.3 µs or >= 750 kHz for a periodic signal.

Consequences

Tasks connected through PPI or SHORTS to this event might be triggered twice.

Workaround

Apply the following code when any GPIOTE channel is configured to generate an IN event on edges that can occur within 1.3 µs of each other:

```
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 1;
```

Important: A clock is kept on by the workaround and must be reverted to avoid higher current consumption when GPIOTE is not in use, using the following code:

```
*(volatile uint32_t *)(NRF_GPIOTE_BASE + 0x600 + (4 * GPIOTE_CH_USED)) = 0;
```

3.46 [156] GPIOTE: Some CLR tasks give unintentional behavior

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

One of the following:

- Current consumption is high when entering IDLE.
- Latency for detection changes on inputs connected to GPIOTE channels becoming longer that expected.

Conditions

Using the following tasks:

Address	GPIOTE task
0x060	TASK_CLR[0]
0x064	TASK_CLR[1]
0x068	TASK_CLR[2]
0x06C	TASK_CLR[3]
0x070	TASK_CLR[4]
0x074	TASK_CLR[5]
0x078	TASK_CLR[6]
0x07C	TASK_CLR[7]

Consequences

High current consumption or too long time from external event to internal triggering of PPI event and/or IRQ from GPIOTE.

Using TASK_CLR[*n*] for even values of *n* has the side effect of setting the system in constant latency mode (see POWER->TASKS_CONSTLAT). Using TASK_CLR[*n*] for odd values of *n* has the side effect of setting the system in low power mode (see POWER->TASKS_LOWPOWER).

Workaround

To set the system back in the mode it was before using the TASK_CLR[*n*], triggering of tasks with even *n* must be followed by triggering any of the TASK_CLR with odd *n* and vice versa.

3.47 [163] FICR: Code and RAM size fields do not match chip specification

This anomaly applies to IC Rev. Rev 1, build codes QFAB-Bx0.

Symptoms

FICR values CODESIZE and INFO.RAM does not contain correct values.

Conditions

Always.

Consequences

None.

Workaround

None.

3.48 [173] GPIO: Writes to LATCH register take several CPU cycles to take effect

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

A bit in the LATCH register reads '1' even after clearing it by writing '1'.

Conditions

Reading the LATCH register right after writing to it.

Consequences

Old value of the LATCH register is read.

Workaround

Have at least 3 CPU cycles of delay between the write and the subsequent read to the LATCH register. This can be achieved by having 3 dummy reads to the LATCH register.

3.49 [176] System: Flash erase through CTRL-AP fails due to watchdog time-out

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Full flash erase through CTRL-AP is not successful.

Conditions

WDT is enabled.

Consequences

Flash is not erased. If the device has a WDT time-out less than 1 ms and is readback-protected through UICR.APPROTECT, there is a risk of permanently preventing the erasing of the flash.

Workaround

Try again.

3.50 [178] SAADC: END event firing too early

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

False END events.

Conditions

Offset calibration is run with TACQ < 10 µs before sampling is started.

Consequences

The END event can occur earlier than expected. Data is not ready.

Workaround

Apply one of the following workarounds:

- Run offset calibration with TACQ >=10 µs.
- Apply STOP task after calibration, before sampling. CALIBRATEOFFSET -> CALIBRATEDONE -> STOP -> STOPPED -> START.

3.51 [179] RTC: COMPARE event is generated twice from a single RTC compare match

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Tasks connected to RTC COMPARE event through PPI are triggered twice per compare match.

Conditions

RTC registers are being accessed by CPU while RTC is running.

Consequences

Tasks connected to RTC COMPARE event through PPI are triggered more often than expected.

Workaround

Do not access the RTC registers, including the COMPARE event register, from CPU while waiting for the RTC COMPARE event. Note that CPU interrupt from this event can still be enabled.

3.52 [181] NFCT: Invalid value in FICR for double-size NFCID1

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

Symptoms

NFC not communicating with the peer device.

Conditions

Using NFCID1 values from FICR and using double-size ID. FICR address 0x454 NFC.TAGHEADER1.UD4 is equal to 0x88.

Consequences

NFC does not communicate reliably with the peer device.

Workaround

Do not use 0x88 value in NFCID1.

3.53 [183] PWM: False SEQEND[0] and SEQEND[1] events

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

False SEQEND[0] and SEQEND[1] events are being generated.

Conditions

Any of the LOOPSDONE_SEQSTARTn shortcuts are enabled. LOOP register is non-zero and sequence 1 is one value long.

Consequences

SEQEND[0] and SEQEND[1] events might falsely trigger other tasks if these are routed through the PPI.

Workaround

Avoid using the LOOPSDONE_SEQSTARTn shortcuts, when LOOP register is non-zero and sequence 1 is one value long.

3.54 [192] CLOCK: LFRC frequency offset after calibration

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

LFRC oscillator frequency is wrong after calibration, exceeding 500 ppm.

Conditions

On some devices, when entering System ON Idle while calibration is ongoing.

Consequences

After calibration, LFRC has a frequency offset that is outside specification.

Workaround

Apply the following code before starting the RCOSC32K calibration:

```
*(volatile uint32_t *)0x40000C34 = 0x00000002;
```

Apply the following code after the RCOSC32K calibration is finished:

```
*(volatile uint32_t *)0x40000C34 = 0x00000000;
```

This workaround is included in SDK v15.0.0 and SoftDevices S140, S132, and S112 v6.0.0.

3.55 [194] I2S: STOP task does not switch off all resources

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Current consumption too high (~900 µA) after using the STOP task.

Conditions

I2S was running and was stopped by triggering the STOP task.

Consequences

Current consumption higher than specified.

Workaround

Apply the following code after the STOP task:

```
*((volatile uint32_t *)0x40025038) = 1;
*((volatile uint32_t *)0x4002503C) = 1;
```

3.56 [196] I2S: PSEL acquires GPIOs regardless of ENABLE

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

I2S controls GPIO even when I2S is not enabled.

Conditions

When using I2S->PSEL to configure GPIO.

Consequences

GPIO selected for I2S cannot be used for any other peripheral.

Workaround

Do not rely on the pins selected in I2S->PSEL registers being free when I2S->ENABLE is set to DISABLE.

Only set the CONNECT bit in the I2S->PSEL registers to CONNECTED immediately before enabling I2S. When disabling I2S, set the CONNECT bit in the I2S->PSEL registers to DISCONNECTED.

3.57 [201] CLOCK: EVENTS_HFCLKSTARTED might be generated twice

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

EVENTS_HFCLKSTARTED might occur twice, and HFCLKSTAT might be wrong.

Conditions

When running HFCLK with crystal.

Consequences

HFCLKSTAT might be wrong when reading it after HFCLK is started.

Workaround

Disregard HFCLKSTAT and EVENT_HFCLKSTARTED after first EVENT_HFCLKSTARTED.

This workaround is included in nRF5 SDK v15.0.0 and SoftDevices S140, S132, and S112 v6.0.0.

3.58 [204] RADIO: Switching beween TX and RX causes unwanted emissions

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

It was inherited from the previous IC revision Engineering C.

Symptoms

Unwanted emissions when switching from TX to RX.

Conditions

Switching from TX to RX without using DISABLE.

Consequences

Unwanted emissions on the channel used for RX.

Workaround

Always use DISABLE when switching from TX to RX.

3.59 [210] GPIO: Bits in GPIO LATCH register are incorrectly set to 1

This anomaly applies to IC Rev. Rev 1, build codes QFAA-Bx0, QFAB-Bx0, CIAA-Bx0.

Symptoms

The GPIO.LATCH[n] register is unexpectedly set to 1 (Latched).

Conditions

Set GPIO.PIN_CNF[n].SENSE at low level (3) at the same time as PIN_CNF[n].INPUT is set to Connect (0).

Consequences

The GPIO.LATCH[n] register is set to 1 (Latched). This could have side effects, depending on how the chip is configured to use this LATCH register.

Workaround

Always configure PIN_CNF[n].INPUT before PIN_CNF[n].SENSE.