megawin
make you win

MG32F103xx

MCU based on high-performance 32-bit ARMCortex™-M3 core, up to 128KBFlash space and 28KBSRAM, 1 full-speed USB, 7 timers, 12-bit ADC, 11 communication interfaces

Features

ÿ High-performance 32-bit ARM Cortex™-M3 core
- ÿ Up to 72MHz system frequency ÿ Built-in dedicated instruction and data cache
- ÿ Single-cycle 32-bit hardware multiplier and hardware divide
- ÿ AHB, APB1 and APB2 clocks are independent of each other stand

ÿ Storage space
- ÿ 96 or 128K bytes Flash
- ÿ 28K bytes SRAM

ÿ Power supply
- ÿ Dual power domains: main power VDD2.0V~3.6V, backup power Battery power supply VBAT1.8V~3.6V
- ÿ Power-on reset and configurable voltage detection module

ÿ Clock
- ÿ Support 4~16MHz crystal oscillator
- ÿ Built-in 8MHz RC oscillator with calibration
- ÿ Built-in 48MHz RC oscillator with calibration
- ÿ Embedded 32KHz watchdog oscillator
- ÿ PLL clock
- ÿ External LSE: 32.768KHz crystal oscillator

ÿ Power management
- ÿ Three power saving modes: sleep mode, stop mode, Standby mode
- ÿ Dynamic power consumption: ~160uA/MHz@3.3V
- ÿ Stop standby power consumption: ~18.5uA@3.3V
- ÿ Standby standby power consumption: ~4.5uA@3.3V ÿ VBAT RTC power consumption: ~1.1uA@3.3V ÿ When main When the power supply is powered down, 84 Byte-sized backup register

ÿ Operating temperature range
- ÿ Industrial grade (-40°C~+85°C)

ÿ 12-bit SAR ADC converter
- ÿ Maximum converter frequency: 1Msps ÿ Supports up to 16 channels
- ÿ Support a variety of automatic continuous conversion, scan conversion
- ÿ Temperature sensor connected to AD converter 16 channels

ÿ Voltage comparator
- ÿ 2 independent voltage comparators
- ÿ The positive and negative ends of each comparator support 4 outputs. input channel, a total of 16 independent channels

ÿ LED driver module
- ÿ Can drive 56 LEDs or 8 seven-segment numbers at the same time Code tube

ÿ General-purpose input and output IO
- ÿ The 64-pin product has 51 GPIO pins, 48 pins Pin products have 37 GPIO pins
- ÿ All GPIO pins can be configured as external interrupt input

ÿ Debug interface
- ÿ Serial Single Wire Debug (SWD) ÿ 7 timers/counters
- ÿ 3 basic timers/counters and 1 enhanced timer timer/counter
- ÿ 20-bit PWM timer (enhanced timer Channels 1~3 support dead-time complementary output)
- ÿ Enhanced timer/counter supports edge counting, gate Control count, quadrature count, trigger count, symbol count number
- ÿ Independent watchdog timer and window watchdog timer ÿ 24-bit SystemTick timer ÿ 11 communication interfaces

- ÿ 2 I2C interfaces, support Smbus protocol
- ÿ 3 UART interfaces ÿ 3 SPI interfaces, 1 QSPI interface
- ÿ 1 I2S interface
- ÿ 1 USB 2.0 full-speed device interface

ÿ Two multi-channel DMA controllers supporting Timers, ADC, SPIs, I2Cs, UARTs and other peripherals trigger ÿ RTC clock counter, record the year, month, day, hour, minute and second

ÿ CRC calculation module

ÿ RNG module

ÿ ECOPACK® package

Table of contents

Chapter 1 Introduction

1.1 Overview

The MG32F103 series uses a high-performance ARM®Cortex™-M3 32-bit RISC core, with a maximum operating frequency of 72MHz, built-in up to 128KB FLASH, 28KB SRAM, 1 enhanced timer, 3 general-purpose timers, and two watchdogs WWDG and IWDG, 3 SPI serial synchronous communication interfaces, 1 QSPI serial synchronous communication interface, 2 I2C serial communication interfaces, 3 UART serial asynchronous communication interfaces, 1 I2S audio interface, 1 USB2.0 Full Speed communication interface, 1 12-bit SAR analog-to-digital converter, 1 LED driver module, 2 voltage comparators, real-time clock module RTC.

1.2 Main Features

- Voltage operating range
  - Dual power domains: main power VDD 2.0V ÿ 3.6V, backup battery power VBAT 1.8V ÿ 3.6V
  - When the main power is lost, the RTC module can continue to operate on VBAT power
  - When the main power is powered off, the VBAT power supply provides a backup register with a capacity of 84Bytes
- Power management
  - Three power saving modes: Sleep Mode, Stop Mode, Standby Mode
  - Dynamic power consumption: ÿ 160uA/MHz@3.3V
  - Stop standby power consumption: ÿ 18.5uA@3.3V
  - Standby power consumption: ÿ 4.5uA@3.3V
  - VBAT RTC power consumption: ÿ 1.1uA@3.3V
- range of working temperature
  - Industrial Grade (-40°C ÿ +85°C)
- reset
  - External pin reset
  - Power on reset
  - software reset
  - Watchdog (IWDT and WWDT) timer reset

– Low power mode reset

• Low Voltage Detection (PVD)

– 8-level detection threshold adjustable

– Rising edge/falling edge can be configured

• Clock unit

– External HSE: Support 4 ÿ 16MHz crystal oscillator, typical 8MHz crystal oscillator

– External LSE: 32.768KHz crystal oscillator

– Embedded factory-trimmed 8MHz RC oscillator (MHSI)

–**Built-** in 48MHz RC oscillator with calibration (FHSI)

– Embedded 32KHz watchdog oscillator (LSI)

– PLL clock

• High-performance 32-bit ARM CPU core

– ARM Cortex™-M3 processor up to 72MHz

– Built-in dedicated instruction and data cache

– Support frequency configurable

– Nestable Vectored Interrupt Controller (NVIC)

– Single-cycle 32-bit hardware multiplier

– 24-bit System Tick Timer

• Flash memory

– 96KB ÿ 128KB Flash

• SRAM memory

– 28KB SRAM

• 12-bit SAR ADC converter

– Supports up to 16 channels

– Maximum converter frequency: 1Msps

– Support automatic continuous conversion, scan conversion

– Support software and hardware AD conversion trigger mode

– Temperature sensor connected to AD converter independent channel 16

• Voltage Comparator

– 2 independent voltage comparators

– Each comparator supports 4 input channels on the positive and negative sides, for a total of 16 independent channels

• Debug interface

- Serial Single Wire Debug (SWD)
- Cortex-M3 Measurement Tracking Macrocell (ITM)

• Communication Interface

- 3 UART ports
- 3 SPI interfaces, 1 QSPI interface
- 2 I2C interfaces, support Smbus protocol
- 1 USB2.0 Full Speed device port
- 1 I2S interface

• Timer/Counter

- 3 basic timers/counters and 1 enhanced timer/counter
- 20-bit PWM timer (channels 1 to 3 of the enhanced timer support complementary dead-time outputs)
- Enhanced timer/counter supports edge count, gate count, AB phase quadrature count, trigger count, symbol count
- Can generate ADC trigger events

• General purpose input and output IO

- 51 GPIO pins for 64-pin products and 37 GPIO pins for 48-pin products
- All GPIO pins can be configured as external interrupt inputs
- Provides up to 16mA drive current

• Multi-channel DMA controller, supports various peripheral triggers such as Timers, ADC, SPIs, I2Cs, UARTs, etc.

• CRC calculation module, supports multiple 8/16/32-bit CRC algorithms.

• RNG module for generating random numbers

• LED driver module, can drive 56 LEDs or 8 seven-segment digital tubes at the same time

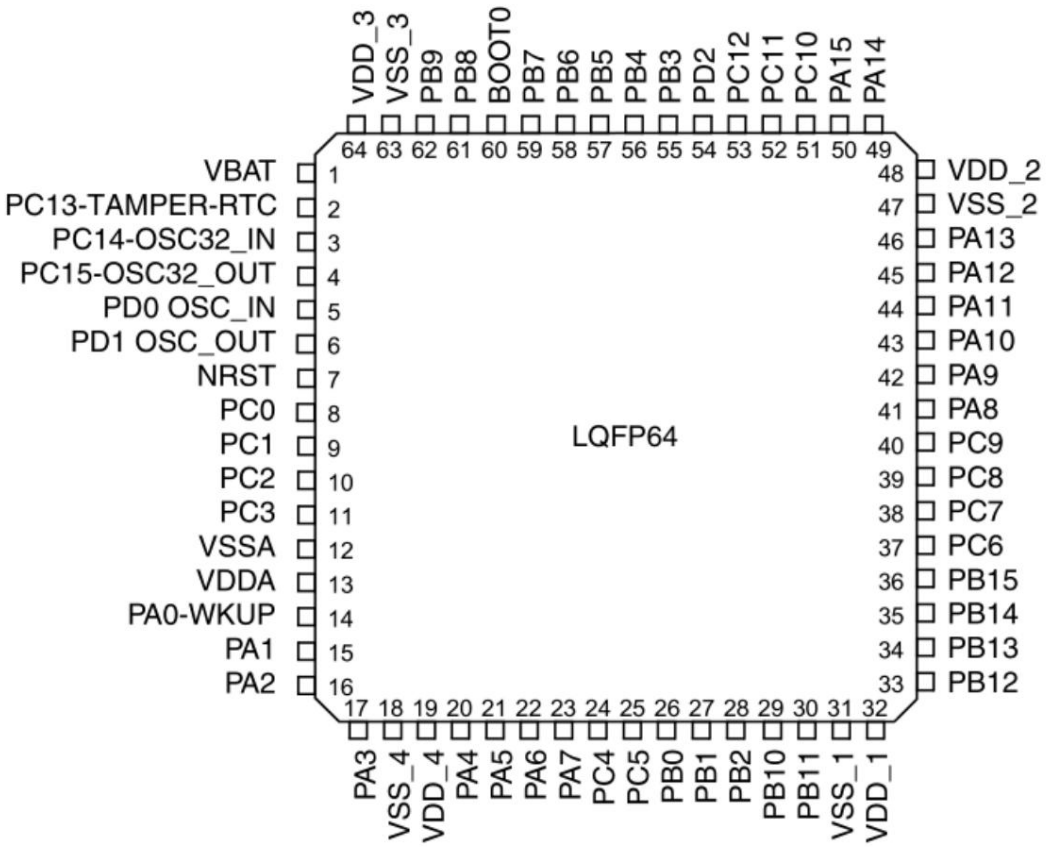
• RTC clock counter, cooperate with software to record year, month, day, hour, minute and second

• Support secondary development of user programs

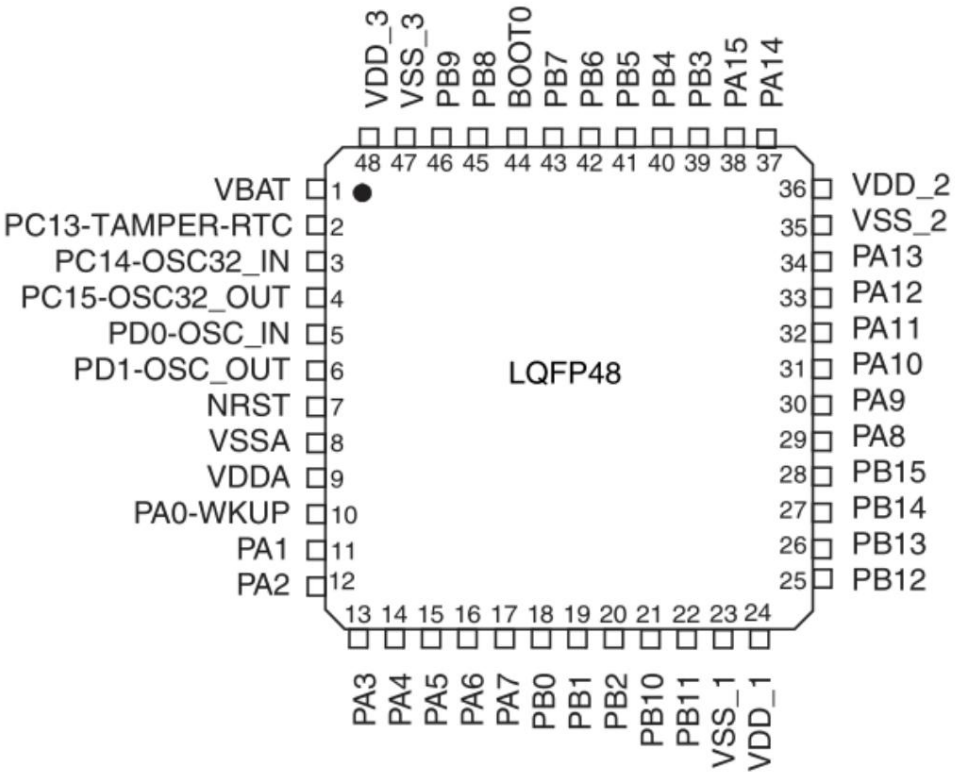
• Support LQFP64, LQFP48 packages

Chapter 2 Package Pins

2.1 LQFP64 Package



2.2 LQFP48 Package



2.3 Pin Function Description

Table 2.1: Pin Function Description

Pin No.		Pin Name	Type	Main Function	Alternate Function	Analog Function
1	1	VBAT	S	VBAT		
2	2	PC13	I/O	PC13	TAMPER/RTC	
3	3	PC14	I/O	PC14		OSC32_IN
4	4	PC15	I/O	PC15		OSC32_OUT
5	5	PD0	I/O	PD0		OSC_IN
6	6	PD1	I/O	PD1		OSC_OUT
7	7	NRST	I/O	NRST		
-	8	PC0	I/O	PC0	I2S_WS/SPIM2_NSS0/SPIS2_NSS	ADC_IN10
-	9	PC1	I/O	PC1	I2S_SCLK/SPIM2_SCK/SPIS2_SCK	ADC_IN11
-	10	PC2	I/O	PC2	I2S_SD0/SPIM2_MI/SPIS2_SO	ADC_IN12
-	11	PC3	I/O	PC3	I2S_SD1/SPIM2_MO/SPIS2_SI	ADC_IN13
8	12	VSSA	S	VSSA		
9	13	VDDA	S	VDDA		
10	14	PA0	I/O	PA0/WKUP	TIM2_CH1_ETR/UART2_CTS/WKUP	ADC_IN0
11	15	PA1	I/O	PA1	TIM2_CH2/UART2_RTS	ADC_IN1
12	16	PA2	I/O	PA2	TIM2_CH3/UART2_TX	ADC_IN2
13	17	PA3	I/O	PA3	TIM2_CH4/UART2_RX	ADC_IN3
-	18	VSS_4	S	VSS_4		
-	19	VDD_4	S	VDD_4		
14	20	PA4	I/O	PA4	QSPI_NSS0/SPIS1_NSS/UART2_CK	ADC_IN4
15	21	PA5	I/O	PA5	QSPI_SCK/SPIS1_SCK	ADC_IN5
16	22	PA6	I/O	PA6	TIM1_BKIN/TIM3_CH1/QSPI_MI_IO1/SPIS1_SO	ADC_IN6
17	23	PA7	I/O	PA7	TIM1_CH1N/TIM3_CH2/QSPI_MO_IO0/SPIS1_SI	ADC_IN7
-	24	PC4	I/O	PC4	TRACECK	ADC_IN14
-	25	PC5	I/O	PC5	SPIM2_NSS2/TRACED0	ADC_IN15
18	26	PB0	I/O	PB0	TIM1_CH2N/TIM3_CH3/I2S_MCLK/QSPI_IO2	ADC_IN8
19	27	PB1	I/O	PB1	TIM1_CH3N/TIM3_CH4/QSPI_IO3	ADC_IN9
20	28	PB2	I/O	PB2/BOOT1		
21	29	PB10	I/O	PB10	TIM2_CH3/TIM4_CH1/I2C2_SCL/QSPI_NSS2/UART3_TX	
22	30	PB11	I/O	PB11	TIM2_CH4/I2C2_SDA/SPIM2_NSS1/UART3_RX	
23	31	VSS_1	S	VSS_1		
24	32	VDD_1	S	VDD_1		
25	33	PB12	I/O	PB12	TIM1_BKIN/I2S_WS/LED4/SPIM2_NSS0/SPIS2_NSS/UART3_CK	
26	34	PB13	I/O	PB13	TIM1_CH1N/I2S_SCLK/LED5/SPIM2_SCK/SPIS2_SCK/UART3_CTS	
27	35	PB14	I/O	PB14	TIM1_CH2N/LED6/SPIM2_MI/SPIS2_SO/UART3_RTS	
28	36	PB15	I/O	PB15	TIM1_CH3N/LED7/SPIM2_MO/SPIS2_SI/I2S_SD0	
-	37	PC6	I/O	PC6	TIM3_CH1/I2S_MCLK/LED0	
-	38	PC7	I/O	PC7	TIM3_CH2/I2S_MCLK/LED1	
-	39	PC8	I/O	PC8	TIM3_CH3/LED2	
-	40	PC9	I/O	PC9	TIM3_CH4/LED3/TRACED1	

Pin No.		Pin Name	Type	Main Function	Alternate Function	Analog Function
29	41	PA8	I/O	PA8	TIM1_CH1/LED0/UART1_CK/MCO	CMPA_P0
30	42	PA9	I/O	PA9	TIM1_CH2/LED1/UART1_TX	CMPA_N0
31	43	PA10	I/O	PA10	TIM1_CH3/LED2/UART1_RX	
32	44	PA11	I/O	ISOCLK	TIM1_CH4/LED3/UART1_CTS	USBDM
33	45	PA12	I/O	ISODIO	TIM1_ETR/UART1_RTS	USBDP
34	46	PA13	I/O	SWDIO	QSPI_NSS1	CMPA_P3
35	47	VSS_2	S	VSS_2		
36	48	VDD_2	S	VDD_2		
37	49	PA14	I/O	SWDCLK	QSPI_NSS2	CMPA_N3
38	50	PA15	I/O	PA15	TIM2_CH1_ETR/I2S_WS/I2C1_SMBAI/QSPI_NSS0/SPIS1_NSS	CMPB_P3
-	51	PC10	I/O	PC10	LED4/UART3_TX/TRACED2	CMPB_P1
-	52	PC11	I/O	PC11	LED5/UART3_RX/TRACED3	CMPB_P2
-	53	PC12	I/O	PC12	TIM4_ETR/LED6/UART3_CK	CMPB_N0
-	54	PD2	I/O	PD2	TIM3_ETR/LED7	CMPB_P0
39	55	PB3	I/O	PB3	SWO/TIM2_CH2/I2S_SCLK/QSPI_SCK/SPIS1_SCK	CMPB_N3
40	56	PB4	I/O	PB4	TIM3_CH1/QSPI_MI_IO1/SPIS1_SO	CMPA_P1
41	57	PB5	I/O	PB5	TIM3_CH2/I2S_SD1/I2C1_SMBAI/QSPI_MO_IO0/SPIS1_SI	CMPA_P2
42	58	PB6	I/O	PB6	TIM4_CH1/I2C1_SCL/QSPI_NSS1/UART1_TX	CMPA_N1
43	59	PB7	I/O	PB7	TIM4_CH2/I2C1_SDA/SPIM2_NSS1/UART1_RX	CMPA_N2
44	60	BOOT0	I	BOOT0		
45	61	PB8	I/O	PB8	TIM4_CH3/I2C1_SCL/SPIM2_NSS2/UART1_CTS	CMPB_N1
46	62	PB9	I/O	PB9	TIM4_CH4/I2C1_SDA/UART1_RTS	CMPB_N2
47	63	VSS_3	S	VSS_3		
48	64	VDD_3	S	VDD_3		

MG32F103xx GPIO function selection:

Table 2.2: Pin Function Selection

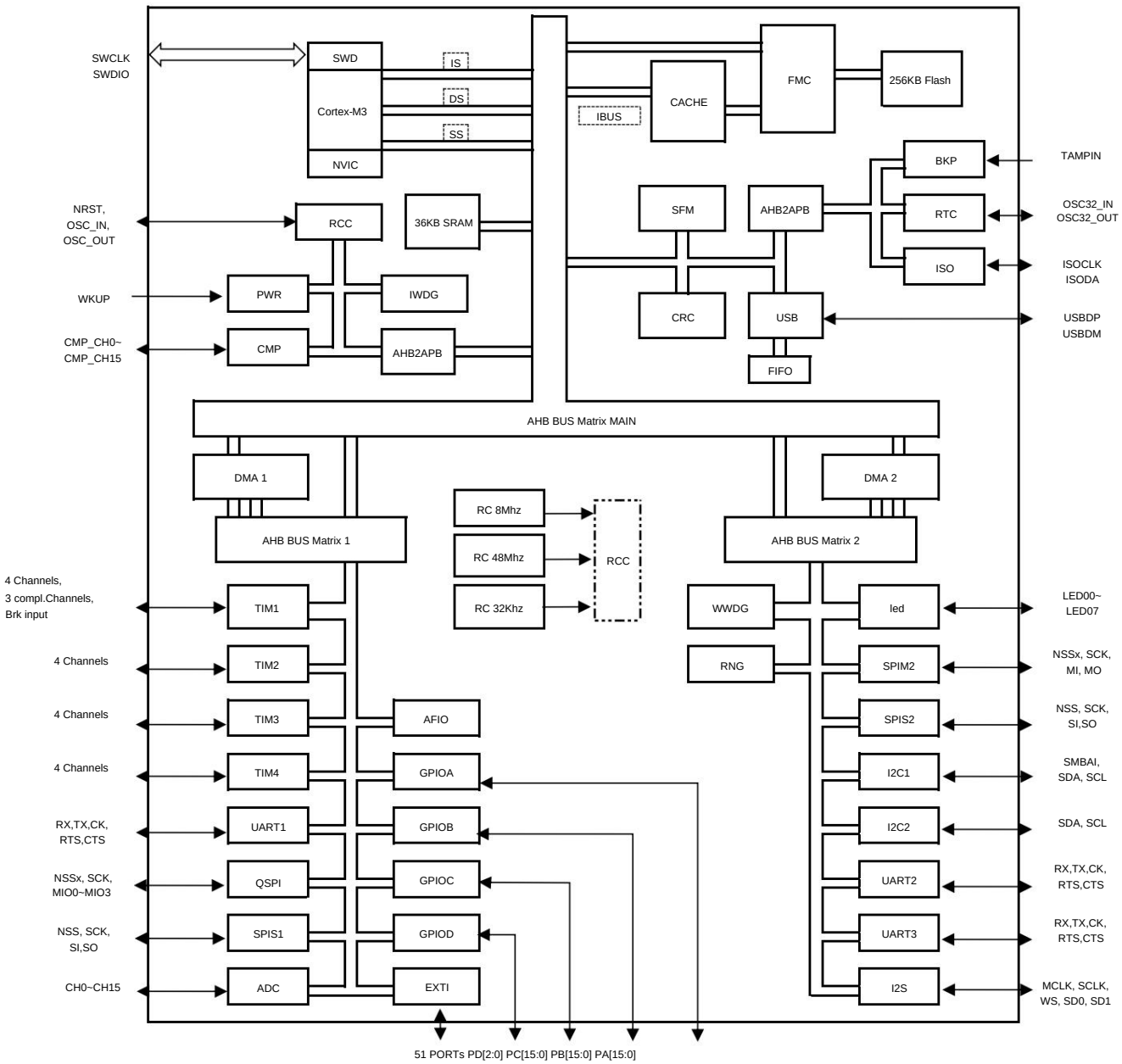
AFR[3:0]		0	1	2	3	4	5	6	7
PORT A	PA0	WKUP	TIM2_CH1_ETR						UART2_CTS
	PA1		TIM2_CH2						UART2_RTS
	PA2		TIM2_CH3						UART2_TX
	PA3		TIM2_CH4						UART2_RX
	PA4						QSPI_NSS0	SPIS1_NSS	UART2_CK
	PA5						QSPI_SCK	SPIS1_SCK	
	PA6		TIM1_BKIN	TIM3_CH1			QSPI_MI_IO1	SPIS1_SO	
	PA7		TIM1_CH1N	TIM3_CH2			QSPI_MO_IO0	SPIS1_SI	
	PA8	MCO	TIM1_CH1			LED0			UART1_CK
	PA9		TIM1_CH2			LED1			UART1_TX
	PA10		TIM1_CH3			LED2			UART1_RX
	PA11		TIM1_CH4			LED3			UART1_CTS
	PA12		TIM1_ETR						UART1_RTS
	PA13	SWD_DIO					QSPI_NSS1		
	PA14	SWD_CLK					QSPI_NSS2		
	PA15		TIM2_CH1_ETR		I2S_WS	I2C1_SMBAI	QSPI_NSS0	SPIS1_NSS	
PORT B	PB0		TIM1_CH2N	TIM3_CH3	I2S_MCLK		QSPI_IO2		
	PB1		TIM1_CH3N	TIM3_CH4			QSPI_IO3		
	PB2	BOOT1							
	PB3	SWO	TIM2_CH2		I2S_SCLK		QSPI_SCK	SPIS1_SCK	
	PB4			TIM3_CH1			QSPI_MI_IO1	SPIS1_SO	
	PB5			TIM3_CH2	I2S_SD1	I2C1_SMBAI	QSPI_MO_IO0	SPIS1_SI	
	PB6			TIM4_CH1		I2C1_SCL	QSPI_NSS1		UART1_TX
	PB7			TIM4_CH2		I2C1_SDA	SPIM2_NSS1		UART1_RX
	PB8			TIM4_CH3		I2C1_SCL	SPIM2_NSS2		UART1_CTS
	PB9			TIM4_CH4		I2C1_SDA			UART1_RTS
	PB10		TIM2_CH3	TIM4_CH1		I2C2_SCL	QSPI_NSS2		UART3_TX
	PB11		TIM2_CH4			I2C2_SDA	SPIM2_NSS1		UART3_RX
	PB12		TIM1_BKIN		I2S_WS	LED4	SPIM2_NSS0	SPIS2_NSS	UART3_CK
	PB13		TIM1_CH1N		I2S_SCLK	LED5	SPIM2_SCK	SPIS2_SCK	UART3_CTS
	PB14		TIM1_CH2N			LED6	SPIM2_MI	SPIS2_SO	UART3_RTS
	PB15		TIM1_CH3N		I2S_SD0	LED7	SPIM2_MO	SPIS2_SI	
PORT C	PC0				I2S_WS		SPIM2_NSS0	SPIS2_NSS	
	PC1				I2S_SCLK		SPIM2_SCK	SPIS2_SCK	
	PC2				I2S_SD0		SPIM2_MI	SPIS2_SO	
	PC3				I2S_SD1		SPIM2_MO	SPIS2_SI	
	PC4	TRACECK							
	PC5	TRACED0					SPIM2_NSS2		
	PC6			TIM3_CH1	I2S_MCLK	LED0			
	PC7			TIM3_CH2	I2S_MCLK	LED1			
	PC8			TIM3_CH3		LED2			
	PC9	TRACED1		TIM3_CH4		LED3			
	PC10	TRACED2				LED4			UART3_TX
	PC11	TRACED3				LED5			UART3_RX

AFR[3:0]		0	1	2	3	4	5	6	7
	PC12			TIM4_ETR		LED6			UART3_CK
	PC13	TAMPER_RTC							
	PC14	OSC32_IN							
	PC15	OSC32_OUT							
PORT D	PD0	OSC_IN							
	PD1	OSC_OUT							
	PD2			TIM3_ETR		LED7			

Chapter 3 System Block Diagram

The following figure is the system block diagram of MG32F103xx series products:

Figure 3.1: MG32F103xx System Block Diagram



Chapter 4 System Description

4.1 Overview

The table below shows the MG32F103xx series product features and peripheral counts.

Table 4.1: MG32F103xx device features and peripheral function numbers

Peripheral functions		MG32F103Cx		MG32F103RBT6
Flash memory (KB)		96	128	128
SRAM(KB)		28	28	28
counter	Universal	3	3	3
	advanced	1	1	1
	QSPI(Master)	1	1	1
	SPIM	1	1	1
	SPIS	2	2	2
	I2C _	2	2	2
	UART	3	3	3
	USB	1	1	1
	I2S _	0	1	1
Number of GPIOs		37	37	51
ADC	Number of 12-bit converters	1	1	1
	Number of channels	10	10	16
comparator	quantity	2	2	2
	Number of channels	12	12	16
CPU frequency		72MHz		
Operating Voltage		2.0V ÿ 3.6V		
Operating temperature		Industrial temperature: -40°C ÿ +85°C Junction temperature: -40°C ÿ +125°C		
package		LQFP48		LQFP64

4.2 ARM Cortex™-M3 core

The Cortex™ M3 processor is a 32-bit configurable multi-stage pipelined RISC processor with embedded AMBA-Lite interface and nested vectored interrupts Controller (NVIC), is a low-cost, high-performance MCU platform. With optional hardware debug function, Thumb-2 instruction can be executed order and compatible with other Cortex-M series. The MG32F103xx series has a built-in Cortex™-M3 core, so it is compatible with all

ARM tools and software are compatible.

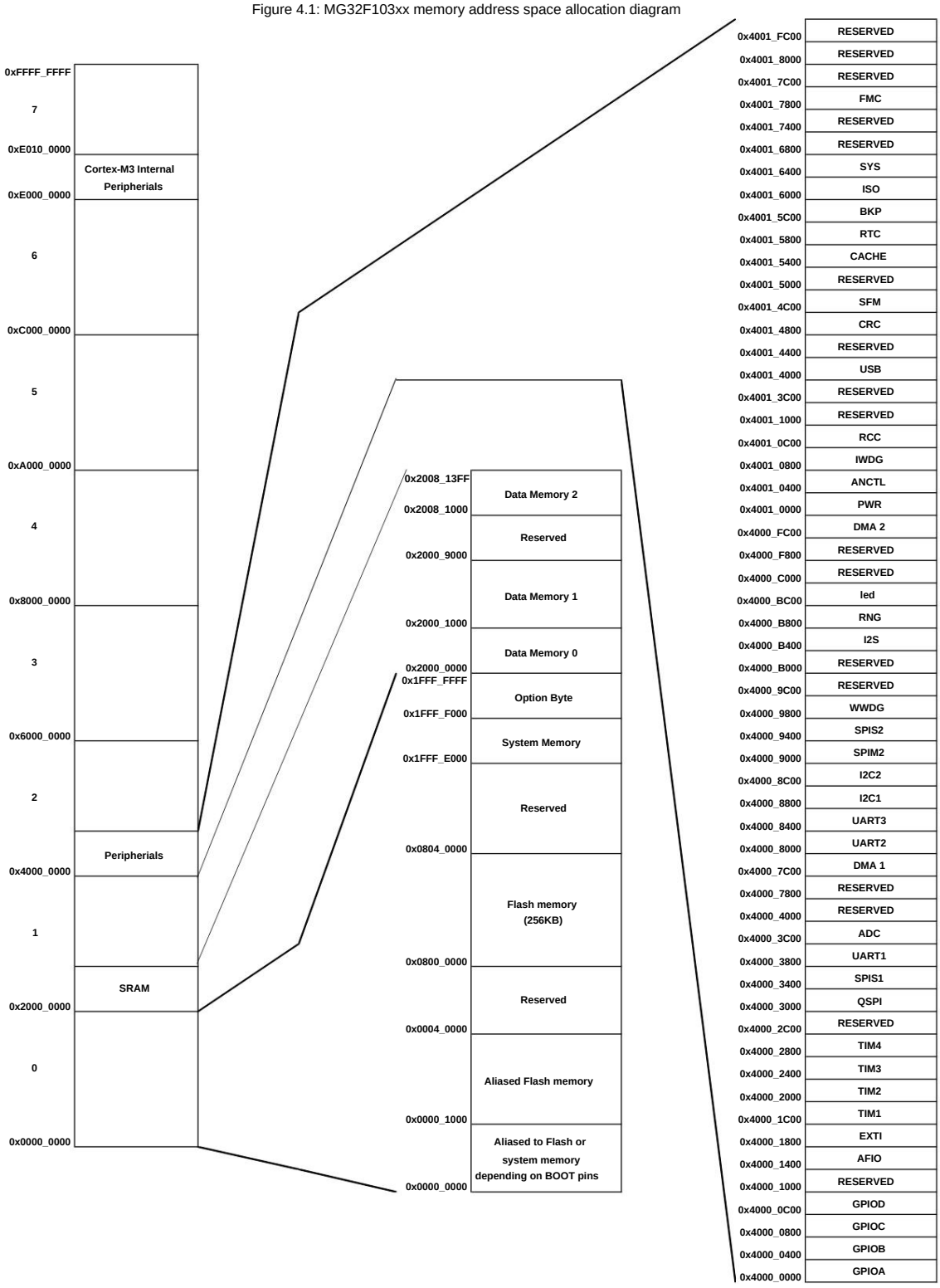
4.3 Memory mapping

MG32F103xx memory address space supports 4GB size. Divided into: Boot area, Flash memory area, SRAM area, system own peripheral area, APB peripheral area and AHB peripheral area. The system's own peripheral area is reserved for the M3 core.

The AHB peripheral area occupies a 64KB space and can support up to 64 peripherals. The APB peripheral area is a 64KB space, and each APB peripheral is allocated 1KB space. All control registers in the APB peripheral area are written and read using word address addressing, and the user cannot access the high-order byte or low-order byte of the register independently.

The boot area has a 4KB space for storing boot programs and ISP functions. Both Flash and SRAM data buses use 32-bit operation. The following figure is the allocation diagram of MG32F103xx memory address space:

Figure 4.1: MG32F103xx memory address space allocation diagram



4.4 System reset

The following events can trigger a system reset:

- Power on reset (POR)

- External pin reset signal (low level)
- Watchdog Timeout Reset (IWDG and WWDG)
- Software reset
- Low power mode reset

A reset can be caused by any reset source, and the internal MHSI is activated and remains active as long as the operating voltage is at a usable level. When the external reset is deasserted, the oscillator is running and the flash controller is initialized.

4.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex™-M3 core. It allows the CPU to respond to interrupts in the shortest possible time. The main features are: • Short interrupt latency.

- Handling system exceptions and peripheral interrupts.
- Supports 43 interrupt vectors.
- Four programmable interrupt response priority levels.
- Generate a software interrupt.
- Configurable non-maskable interrupt sources (NMI).

4.6 EXTI

The external interrupt/event controller contains 19 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured for its trigger event (rising or falling or both edges) and can be individually masked. Having a pending register maintains the status of all interrupt requests.

4.7 Clock

The selection of the system clock is made at startup, the internal 8MHz RC oscillator (MHSI) is selected as the default CPU clock at reset, and then the external 4 ~ 16MHz clock (HSE), the internal 48Mhz RC oscillator (FHSI) or the frequency obtained by dividing the output of the PLL. When the external clock fails, it will be isolated and the corresponding interrupt will be generated. Has multiple prescalers for configuring AHB,
Frequency of APB1 and APB2 regions. The highest frequency of AHB, APB1 and APB2 area can reach 72MHz, and the configuration frequency of AHB, APB1 and APB2 can be independent of each other.

4.8 Boot Mode

At startup, the bootstrap pins are used to select one of three bootstrap modes:

- Bootstrapping from user flash
- Bootstrapping from system memory
- Bootstrapping from internal SRAM

4.9 Power supply scheme

- VDD = 2.0ÿ3.6V: VDD pin powers I/O pins and internal LDO
- VDDA = 2.4ÿ3.6V: supply power for ADC analog part.
- VBAT = 1.8~3.6V: When VDD is turned off, the internal power switching circuit will use VBAT for RTC, external 32kHz oscillator and Backup registers are powered.

Note: The voltages of VDD and VDDA need to be the same, it is recommended to use the same power supply to power VDD and VDDA.

4.10 DMAC

Two general-purpose DMAC controllers, each with 3 channels and up to 16 sets of hardware handshake interfaces (16 sets of DMAC0, 12 sets of DMAC1, a total of 28 sets of hardware handshake interfaces), manage various types of memory to Memory, device-to-memory, and memory-to-device data transfers. There is also an arbiter inside each DMAC to coordinate the priority of each DMA request.

The hardware handshake interface can be configured individually for each channel, or the software handshake interface can trigger each channel; the transmission length, transmission source address and destination address can be individually set by software. DMAC can be used for major peripherals: SPI, I2C, I2S, UART, timers TIMx and ADC.

4.11 RTC Clock and Backup Register

The RTC and backup registers are powered by a switch, which selects VDD when VDD is active, otherwise it is powered by VBAT pin. Backup registers can be used to hold user application data. This register is not reset by system or power reset sources. It is also not reset when waking up from standby mode. A real-time clock has a set of continuously running counters that can provide calendar clock functionality with appropriate software, as well as alarm interrupts and periodic interrupts. The drive clock for the RTC can be a 32.768kHz oscillator using an external crystal, an internal low power RC oscillator. The typical frequency of the internal low power RC oscillator is 32kHz. In order to compensate for the deviation of the natural crystal, the clock of the RTC can be calibrated by outputting a 512Hz signal. The RTC has a 32-bit programmable counter that uses a compare register for long-term measurements. There is a 20-bit prescaler for the time base clock, which by default produces a 1 second long time base when the clock is 32.768kHz.

4.12 Independent Watchdog

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 32kHz RC oscillator. Because this RC oscillator is independent of the main clock, it can be Operates in stop and standby modes. It can be used as a watchdog to reset the entire system in the event of a problem, or as a free timer to provide timeout management for applications. By selecting bytes

The watchdog can be configured as software or hardware to start the watchdog. In debug mode, the counters can be frozen.

4.13 Window Watchdog

The windowed watchdog has a 7-bit down-counter that can be set to free-run. It can be used as a watchdog in the event of a problem reset the entire system. It is driven by the master clock and has an early warning interrupt function. In debug mode, the counters can be frozen.

4.14 System Tick

This timer is dedicated to the operating system and can also be used as a standard down counter. It has the following properties.

- 24-bit down counter
- Reload function
- Can generate a maskable interrupt when the counter is 0
- 1/8 of the CPU clock frequency

4.15 General purpose timer

Each timer has a 20-bit auto-load up/down counter, a 16-bit prescaler and 4 independent channels. Each channel can be used for input capture, output compare, PWM, and single-pulse mode outputs, providing up to 16 input capture, output compare, or PWM channels in the largest package configuration. They can also work with advanced control timers through the timer link function, providing synchronization or event linking capabilities. In debug mode, the counter can be frozen. Any standard timer can be used to generate the PWM output. Each timer has an independent DMA request mechanism.

4.16 Advanced Timer

The Advanced Control Timer (TIM1) can be viewed as a three-phase PWM generator assigned to 6 channels, or as a complete general-purpose timer. Four independent channels can be used for: •

Input capture

- Output compare
- Generate PWM (edge or center-aligned mode)
- Single pulse output
- Complementary PWM outputs with programmable dead-time insertion

When configured as a 20-bit standard timer, it has the same functionality as the TIMx timer. When configured as a 20-bit PWM generator, it has full modulation capability (0 ÿ 100%). In debug mode, the counter can be frozen. Many functions are the same as the standard TIM timer, internal

The structure is also the same, so the advanced control timer can cooperate with the TIM timer through the timer link function to provide synchronization or event link function.

4.17 I2C bus

Up to 2 I2C bus interfaces, capable of working in multi-master and slave modes, supporting standard (<= 100Kb/s), fast (<= 400Kb/s) and high-speed (<= 3.4M b/s) modes, and supporting SMBus bus. The I2C interface supports 7-bit or 10-bit addressing, and supports dual-slave addressing in 7-bit slave mode. Built-in hardware CRC generator/checker. They can use DMA operations.

4.18 I2S bus

It has a built-in I2S bus interface, supports multiple audio transmission protocols, works in master control mode, and supports dual-channel input and output. provide master time clock (MCLK) and serial clock (SCLK) and frame clock (WS) and serial data (SD0/SD1).

4.19 UART

Built-in 3 universal synchronous/asynchronous transceivers (UART1, UART2 and UART3), these 3 interfaces provide asynchronous communication and support infrared transmission. The communication rate of UART1, UART2 and UART3 interface can reach 6MBit/s, the interface has hardware CTS and RTS signal management, all interfaces can use DMA operation.

4.20 SPI

Up to 3 SPI interfaces, and 1 QSPI interface. The communication rate in master mode can reach 24MBit/s, and the communication rate in slave mode Up to 18MBit/s. Supports multiple frame size configurations, which can be configured to 4/8/16/32 bits per

frame. All SPI interfaces can use DMA operations.

4.21 USB

A full-speed USB-compatible device controller is embedded, following the full-speed USB device standard, and the endpoints can be configured by software, with standby/resume functions. The USB dedicated 48MHz clock is generated by dividing the system clock.

4.22 GPIO

Each GPIO pin can be configured by software as an output (push-pull or open-circuit), input (with or without pull-up or pull-down), or other peripheral function port. Most GPIO pins are shared with digital or analog peripherals. All GPIO pins have high current passing capability. If desired, the peripheral functions of the I/O pins can be locked by a specific operation to avoid accidental writes to the I/O registers.

4.23 ADCs

Embedded 1 12-bit analog/digital converter (ADC), 1Msps conversion rate, supports 16 external AD channel sampling conversion, can be realized One-shot or scan conversion. In sweep mode, conversion on a selected set of analog inputs occurs automatically.

The ADC can operate using DMA. The analog watchdog function allows very precise monitoring of one, multiple or all selected channels, and will generate an interrupt when the monitored signal exceeds a preset threshold. Events generated by standard timers (TIMx) and advanced control timers (TIM1) can be internally cascaded to the ADC's start trigger and injection trigger, respectively, and the application program can synchronize AD conversion with the clock.

The ADC requires an independent power supply VDDA with a power supply range of 2.4V to 3.6V. The ADC measurement range is between 0V and VDDA. The embedded temperature sensor is internally connected to the input channel of ADC_IN16 to convert the sensor output to a digital value.

4.24 Comparator

Two analog input comparators are embedded, and the positive and negative inputs of each analog input comparator support 4 input channels, and a total of 16 external input channels are supported for comparison.

4.25 RNG

Random number generator, support to generate 8, 16, 32 bit random number sequence.

4.26 LED Driver

The built-in LED driver module can drive up to 56 LEDs or 8 seven-segment digital tubes at the same time.

4.27 CRC calculation unit

An independent CRC hardware calculation unit is integrated inside, which supports a variety of 8/16/32-bit CRC algorithms and provides the ability to accelerate processing.

4.28 Memory and Programming

It integrates 32KB ÿ 256KB Flash program memory space, 4KB system memory space, and up to 36KByte SRAM. In-system programming (ISP) programming mode is supported. The user can call the ISP function through the bootloader interface.

4.29 Power Monitor

The power-on reset (POR)/power-down reset (PDR) circuit is integrated inside, which is always in working state to ensure that the system works when the power supply exceeds 2V. When VDD is below the POR/PDR threshold, the device is placed in reset without using an external reset circuit. There is also a Programmable Voltage Monitor (PVD) in the device that monitors the VDD supply and compares it to the threshold VP VD when VDD is below or/and above the threshold VP VD

An interrupt will be generated and the interrupt handler can issue a warning message or put the microcontroller into safe mode. The PVD function needs to be enabled through program enable.

4.30 Low Power Mode

The MG32F103xx supports various power control functions. During normal processor operating mode, power and clocking of selected peripherals can be optimized , thereby reducing system power consumption. In addition, the processor has three special low-power modes: sleep mode, shutdown mode, and standby mode.

4.30.1 Sleep Mode

In sleep mode, the clock to the ARM Cortex™-M3 core is turned off and all instruction execution is suspended until the system is restarted or woken up by an interrupt. For a peripheral, its clock is now controlled by a register and can generate an interrupt to wake up the processor to restart executing instructions. Sleep mode can reduce system dynamic power consumption by processor, memory and internal bus. The state and registers of the processor, peripheral registers, memory data, and the logic state of the pins remain unchanged during sleep mode.

4.30.2 Stop Mode

Shutdown mode achieves the lowest power consumption without losing SRAM and register contents. In stop mode, all internal clocks are shut down and the RC oscillators for HSI and HSE are shut down. The microcontroller can be woken up from the shutdown mode by any signal configured as EXTI. The EXTI signal can be one of 16 external I/O ports, PVD output, RTC alarm clock or USB wakeup signal.

4.30.3 Standby Mode

The lowest power consumption can be achieved in standby mode. The internal LDO is turned off, so the power supply of all internal 1.2v parts is cut off; the RC oscillators of HSI and HSE are also turned off; after entering standby mode, the contents of SRAM and registers will disappear, but the contents of backup registers are still retained, and the standby circuit still work. The conditions for exiting from standby mode are: an external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, or the RTC's alarm has expired.

4.31 SWD debug port

Embedded ARM's SWJ-DP interface, which is a serial single-wire debugging interface, can realize the connection of serial single-wire debugging interface.

Chapter 5 Electrical Specifications

5.1 Absolute Maximum Ratings

Maximum ratings are only short-term pressure values. And it is not advisable for the chip to operate at this value or any other condition beyond this recommended value. Exceeding the following maximum ratings may cause permanent damage to the chip. Exposure to maximum ratings for extended periods of time may affect the chip's reliability table.

5.1.1 Limiting voltage characteristics

Table 5.1: Limiting voltage characteristics

symbol	describe	Min	Max	Unit
VDD-VSS	Input voltage on external main supply voltage	-0.5	3.6	V
Vin	(including VDDA and VDD) pins	V SS ÿ 0.3	V DD + 0.5	V
|ÿV DDx|	Voltage difference between different supply pins	-	50	mV
|V SSx ÿ V SS|	Voltage difference between different ground pins	-	50	mV

5.1.2 Limiting current characteristics

Table 5.2: Limiting current characteristics

symbol	describe	Maximum	unit
IV DD	Total current through VDD/VDDA power lines (supply	60	mA
IV SS	current) Total current through VSS ground (sink	60	mA
IIO	current) Output sink current on any I/O and control pins	16	mA
	Output Sourcing Current on Any I/O and Control Pins	-16	mA
IINJ(P IN)	Injection current on pin	± 5	mA
ÿIINJ(P IN)	Injection current on pin	± 25	mA

Note 1: All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power system within the allowable range traditionally.

Note 2: Back-injected current can interfere with the analog performance of the device.

Note 3: When VIN >VDD, there is a forward injection current; when VIN < VSS, there is a reverse injection current, the injection current is absolutely The specified range cannot be exceeded.

Note 4: When several I/O ports have injection current at the same time, the maximum value of ÿIINJ(P IN) is the instant absolute difference between the forward injection current and the reverse injection current. The sum of the pair values.

5.1.3 Extreme temperature characteristics

Table 5.3: Extreme temperature characteristics

symbol	describe	parameter value	unit
TST G	Storage temperature range	ÿ45 ÿ +150	°C
TJ	Maximum Junction Temperature	100	

5.2 Operating parameters

5.2.1 Recommended operating conditions

Table 5.4: Recommended operating conditions

symbol	describe	Min	Max	Unit
fHCLK	Internal AHB clock frequency	-	72	MHz
fP CLK1	Internal APB1 clock frequency	-	72	
fP CLK2	Internal APB2 clock frequency	-	72	
VDD	Standard working voltage	2	3.6	V
VDDA	Analog working voltage	2	3.6	V
VBAT	Spare part working voltage	1.8	3.6	V
T	Operating temperature	-40	85	°C

Note: When the ADC is working, the working range of *VDDA* is *2.4Vÿ3.6V.*

5.2.2 Reset and Low Voltage Detection

Table 5.5: Power-on Reset Characteristics

symbol	parameter	Condition	Min	Typ	Max	Units
Tdelay	RSTN setup time	-	-	40	-	us
VP OR/PDR	reset threshold	rising edge	-	1.92	-	V
		falling edge	-	1.88	-	V

Table 5.6: PVD characteristics

symbol	parameter	Condition	Min	Typ	Max	Units
VP VD	The detection level of the programmable voltage detector selects the rising edge	PLS[2:0] = 000	-	2.25	-	V
		PLS[2:0] = 001	-	2.35	-	
		PLS[2:0] = 010	-	2.45	-	
		PLS[2:0] = 011	-	2.55	-	
		PLS[2:0] = 100	-	2.65	-	
		PLS[2:0] = 101	-	2.75	-	
		PLS[2:0] = 110	-	2.85	-	
		PLS[2:0] = 111	-	2.95	-	
	The detection level of the programmable voltage detector selects the falling edge	PLS[2:0] = 000	-	2.14	-	
		PLS[2:0] = 001	-	2.24	-	
		PLS[2:0] = 010	-	2.34	-	
		PLS[2:0] = 011	-	2.44	-	
		PLS[2:0] = 100	-	2.54	-	
		PLS[2:0] = 101	-	2.64	-	
		PLS[2:0] = 110	-	2.74	-	
		PLS[2:0] = 111	-	2.84	-	

5.2.3 Operating current characteristics

Table 5.7: Operating current characteristics

model	condition	VDD TA@25°C			unit
		2.0V	2.5V	3.6V	
Run Mode1	HCLK=72MHz, execute instruction from FLASH, APB clock enable	12.43	12.92	12.3 mA	
	HCLK=72MHz, execute instruction from FLASH, APB clock is disabled	8.0	8.22	7.73 mA	
	HCLK=48MHz(FHSI), execute instruction from FLASH, APB clock enable	9.83	9.55	10.04 mA	
	HCLK=48MHz(FHSI), execute instruction from FLASH, APB clock disable	6.96	6.41	6.89 mA	
	HCLK=8MHz(HSE), execute instruction from FLASH, APB clock enable	3.35	2.78	3.41 mA	
	HCLK=8MHz(HSE), execute instruction from FLASH, APB clock is disabled	2.84	2.37	2.87 mA	
	HCLK=8MHz(MHSI), execute instruction from FLASH, APB clock enable	3.11	2.54	2.79 mA	
	HCLK=8MHz(MHSI), execute instruction from FLASH, APB clock disable	2.54	1.91	2.28 mA	
Sleep Mode	HCLK=72MHz, APB clock disabled	3.23	2.79	3.04 mA	
	HCLK=8MHz(MHSI), APB clock disabled	1.68	0.93	1.12 mA	
Stop Mode	LDO working at full speed, HSE/HSI/LSE off	240	264	296uA	
	LDO low power state, HSE/HSI/LSE off	15.98	17.34	20.8uA	
Standby Mode	LSI and IWDG work	4.29	4.52	5.14 uA	
VBAT Mode	RTC and LSE clock operation	0.78	1.05	1.25 uA	

Note *1: Cache is* turned on.

Note *2:* When the voltage is lower than *2.5V* , the internal boost circuit works, which will increase the current by *ÿ1mA* .

Note *3:* When the *ADC* operates in *12* -bit mode, the current will increase by *ÿ0.8mA* .

5.2.4 External Clock Characteristics

Table 5.8: External high-speed clock characteristics

symbol	parameter	Condition	Min	Typ	Max	Units
fHSEext	Clock frequency	-	-	8	16MHz	
VHSEH	Input pin high	-	0.7VDD	-	VDD	V
VHSEL	input pin low	-	VSS	-	0.3VDD	V
TW(HSE)	Active high/low time	-	16	-	-	ns
Tr(HSE)	Rise/Fall Time	-	-	-	5	ns
Tf(HSE)	Rise/Fall Time	-	-	-	5	ns
Cin(HSE)	Input capacitive reactance	-	-	5	-	pF
DuCy(HSE)	duty cycle	-	45	-	55%	

Note: Based on design simulation and laboratory test results, not a product test item.

Table 5.9: External low-speed clock characteristics

symbol	parameter	Condition	Min	Typ	Max	Units
fLSEext	Clock frequency	-	-	32.768	-	KHz
VLSEH	input pin high	-	0.7VDD	-	VDD	V
VLSEL	input pin low	-	VSS	-	0.3VDD	V
TW(LSE)	Active high/low time	-	450	-	-	ns
Tr(LSE)	Rise/Fall Time	-	-	-	50	ns
Tf(LSE)	Rise/Fall Time	-	-	-	50	ns
Cin(LSE)	Input capacitive reactance	-	-	5	-	pF
DuCy(LSE)	duty cycle	-	30	-	70%	
TSU(LSE)	Start Time	VDD is stable	-	2	-	s

Note: Based on design simulation and laboratory test results, not a product test item.

5.2.5 Internal Clock Characteristics

Table 5.10: Internal Fast Clock 0 Features

symbol	parameter	condition	Min	Typ	Max	Units
fMHSI	Clock frequency	-	-	8	-	MHz
DuCy(MHSI)	duty cycle	-	45	-	55%	
ACC (MHSI)	Oscillator Accuracy	TA=-40 to 85°C	TBD	-	TBD	%
		TA=0 to 85°C	TBD	-	TBD	%
		TA=25°C	TBD	-	TBD	%
TSU(MHSI)	Oscillator start-up time	V SS ÿ V in ÿ V DD 1		-	2	us
IDD(MHSI)	Oscillator power consumption	-	-	25	-	uA

Table 5.11: Internal Fast Clock 1 Features

symbol	parameter	condition	Min	Typ	Max	Units
fFHSI	Clock frequency	-	-	48	-	MHz
DuCy(FHSI)	duty cycle	-	45	-	55%	
ACC (FHSI)	Oscillator Accuracy	TA=-40 to 85°C	TBD	-	TBD	%
		TA=0 to 85°C	TBD	-	TBD	%
		TA=25°C	TBD	-	TBD	%
TSU (FHSI)	Oscillator start-up time	V SS ÿ V in ÿ V DD 200		-	500	ns
IDD(FHSI)	Oscillator power consumption	-	-	55	-	uA

Table 5.12: Internal Slow Clock Characteristics

symbol	parameter	condition	Min	Typ	Max	Units
fLSI	Clock frequency	-	20	-	40KHz	
TSU (LSI)	Oscillator start-up time	-	-	-	85	us
IDD(LSI)	Oscillator power consumption	-	-	250	-	nA

Note: Based on design simulation and laboratory test results, not a product test item.

5.2.6 PLL characteristics

Table 5.13: PLL characteristics

symbol	parameter	condition	Min	Typ	Max	Units
fP LLIN	Input Clock Frequency	-	1	8	16MHz	
	Input Clock Duty Cycle	-	40	-	60%	
fP LLOUT	output clock frequency	-	-	72	- MHz	
TLOCK	Phase lock time	-	-	-	200	us
Jitter	Cyclic jitter	-	-	-	300	ps

Note: Based on design simulation and laboratory test results, not a product test item.

5.2.7 Memory Features

Table 5.14: Memory characteristics

symbol	parameter	Min	Typ	Max	Units
TP ROG	page write time	-	2.1	-	ms
TERASE	Page Erase Time	-	6.4	-	ms
	Chip Erase Time	-	25.6	-	ms
IDDP ROG	page write current	-	-	2 mA	
IDDERASE	Page/Chip Erase Current	-	-	1.5mA	
IDDREAD	Read current@48MHz	-	-	4.7 mA	
	Read current@24MHz	-	-	2.5mA	
NEND	Erase and write life	100	-	- thousand times	
tRET	data retention time	10	-	-	year

5.2.8 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU), the chip is strength tested to determine its electrical susceptibility using specific measurement methods surface performance.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse after a one second interval) was applied to all pins of all samples of the same size as The number of power supply pins on the chip is related (3 pieces × (n+1) power supply pins). This test complies with JESD22-A114/C101.

Electrostatic Latch

To evaluate latching performance, 2 complementary static latching tests were performed on 6 samples:

- For each power supply pin, supply a supply voltage that exceeds the limit.
- Inject current on each input, output and configurable I/O pin.

This test complies with the ANSI/ESDA/JEDEC standard for latching of integrated circuits.

Table 5.15: ESD characteristics

symbol	parameter	condition	Maximum unit	
VESD(HBM)	Electrostatic Discharge Voltage (Human Body Model)	TA = +25 ÿC, compliant JEDEC JS-001-2017	4000	V
VESD(CDM)	Electrostatic Discharge Voltage (Charging Device Model)	TA = +25 ÿC, compliant JEDEC JS-002-2018	500	V
ILU	Static latch class (Latch-up current)	TA = +25 ÿC, compliant JEDEC 2016	200	mA

5.2.9 EFT Characteristics

Table 5.16: EFT characteristics

symbol	standard	Voltage	level
EFT to IO	(IEC61000-4-4)	2KV	Class: 4
EFT to Power	(IEC61000-4-4)	4KV	Class: 4

software advice

The software process must include the control of the program running away, such as:

- Corrupted program counter.
- Unexpected reset.
- Critical data is corrupted (control registers, etc...)

Enhancing the driving ability of IO can improve the ability to EFT.

During the EET test, a voltage exceeding the application requirements can be directly applied to the chip. When an unexpected action is detected, the software Parts need to be hardened to prevent unrecoverable errors.

5.2.10 IO pin characteristics

Table 5.17: IO pin DC characteristics

symbol	parameter	condition	Min	Typ	Max	Units
VIH	input high level	-	0.65VDD	-		VDD+0.5V
VIL	input low level	-	-0.5	-		0.3VDD V
Vhys	Schmitt Trigger Voltage Hysteresis	-	5%VDD	-		V
ilkg	Input leakage current	V SS ÿ V in ÿ V DD	-		-	±1 uA
Rpu	Weak pull-up equivalent resistance	Vin=VSS	30	40	50	kÿ
Rpd	Weak pull-down equivalent resistance	Vin=VDD	30	40	50	kÿ
CIO	I/O pin capacitance	-	-	5	-	pF

Note: Based on design simulation and laboratory test results, not a product test item.

Table 5.18: IO pin AC characteristics

speed	symbol	parameter	condition	Min	Max	Unit
x0	fmax(IO)out	maximum frequency	CL=50pF,VDD=2V to 3.6V	-	10MHz	
	tf(IO)out	high to low output time		-	125	ns
	tr(IO)out	low to high output time		-	125	ns
x1	fmax(IO)out	maximum frequency	CL=50pF,VDD=2V to 3.6V	-	50MHz	
	tf(IO)out	high to low output time		-	25	ns
	tr(IO)out	low to high output time		-	25	ns

Note: Based on design simulation and laboratory test results, not a product test item.

5.2.11 TIM counting characteristics

Table 5.19: TIM counting characteristics

symbol	condition	minimum	maximum value	unit
Tres(T IM)	Timer Resolution Units	1	-	TT IMxCLK
FEXT	External frequency for channel 1 to channel 4	0	TT IMxCLK/2	MHz
RESTIM	Timer resolution	-	20	bit
Tcounter	when the internal clock source is period 1 of the 16-bit counter		65536	TT IMxCLK
TMAX_COUNT	maximum count	1	1048576×1048576	TT IMxCLK

Note *1: TTIMxCLK = 72MHz*

5.2.12 CMP Features

Table 5.20: CMP characteristics

symbol	parameter	Min	Typ	Max	Units
Vin	Input voltage	0.6	-	VDD-0.3V	
VHY ST	Hysteresis	-	2	5mV	
VOF F	offset voltage	-	5	15mV	
TP GD	propagation delay	-	-	200nS	
Iq	Working current average	-	-	8.5uA	

5.2.13 ADC Characteristics

Table 5.21: ADC characteristics

symbol	parameter	condition	Min	Typ	Max	Units
VDDA	ADC power supply	-	2.4	-	3.6V	
fs	Sampling Rate	-	0.05	-	1 MHz	
fT RIG	External trigger frequency	fADC =14MHz	-	-	823KHz	
VAIN	Conversion voltage range	-	0	-	VDDA V	
RAIN	External input impedance	-	-	-	200ÿ	
CAIN	external capacitor	-	-	TBD	-	pF
Ilkg	analog pin negative input leakage current	-	-	-	10uA	
RADC	sampling switch impedance	-	-	-	1.4	kÿ
CADC	Internal sample and hold capacitor	-	-	15.5	-	pF

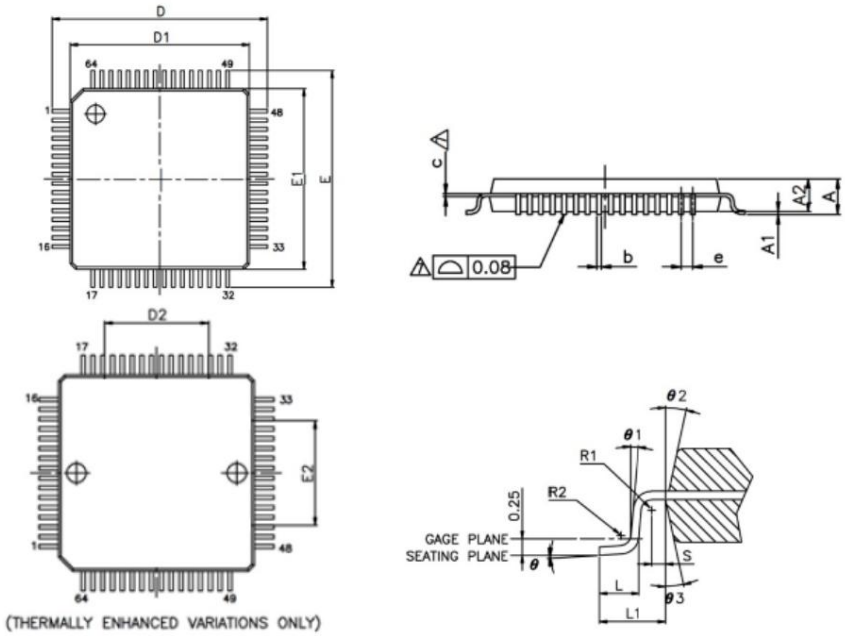
Table 5.22: ADC conversion time

symbol	parameter	condition	Min	Typ	Max	Units
TAD	ADC clock period	-	62.5	-	-	ns
TCONV	Conversion time	12-bit	-	13TAD	-	ns
FCONV	Slew rate	12-bit	-	-	940 KSPS	
TSAMP	sampling time	12-bit	3TAD	-	-	ns
tDIS	discharge time	-	-	0.5TAD	-	ns
tDP U	Power up time	-	-	-	20	us

Chapter 6 Package Dimensions

6.1 LQFP64 10X10mm

Figure 6.1: LQFP64 10X10mm, 0.5mm pitch and recommended package



Note 1: Schematic diagrams are not drawn to scale

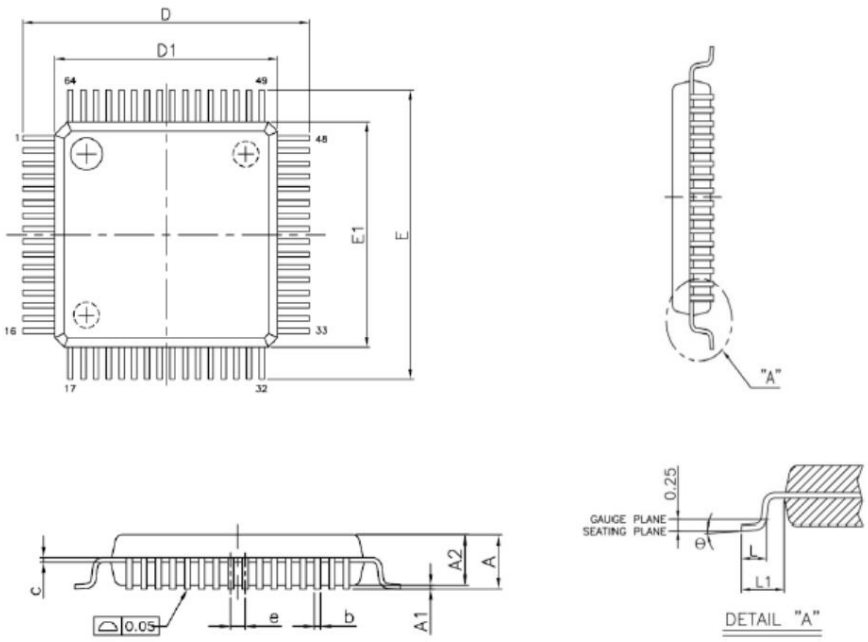
Figure 6.2: LQFP64 10X10mm, 64 pin package parameters

Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.062
A1	0.05	---	0.15	0.001	---	0.005
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09	---	0.20	0.003	---	0.007
D	11.75	12.00	12.25	0.462	0.472	0.482
D1	9.90	10.00	10.10	0.389	0.393	0.397
E	11.75	12.00	12.25	0.462	0.472	0.482
E1	9.90	10.00	10.10	0.389	0.393	0.397
e	0.50 BSC			0.019 BSC		
L	0.45	0.6	0.75	0.017	0.023	0.029
L1	1.00 REF			0.039 REF.		
S	0.20 REF			0.007 REF.		
θ	3.5° REF			0.137 REF.		
θ1	5.0° REF			0.196 REF.		
θ2	12° REF			0.472 REF.		
θ3	12° REF			0.472 REF.		
R1	0.16 REF			0.006 REF.		
R2	0.15 REF			0.005 REF.		

	E2		D2	
PAD SIZE	Min.	Max.	Min.	Max.
165*16E	3.99	4.19	3.99	4.19
210*21E	4.27	5.33	4.27	5.33
260*26E	5.28	6.60	5.28	6.60

6.2 LQFP64 7X7mm

Figure 6.3: LQFP64 7X7mm, 0.4mm pitch and package parameters



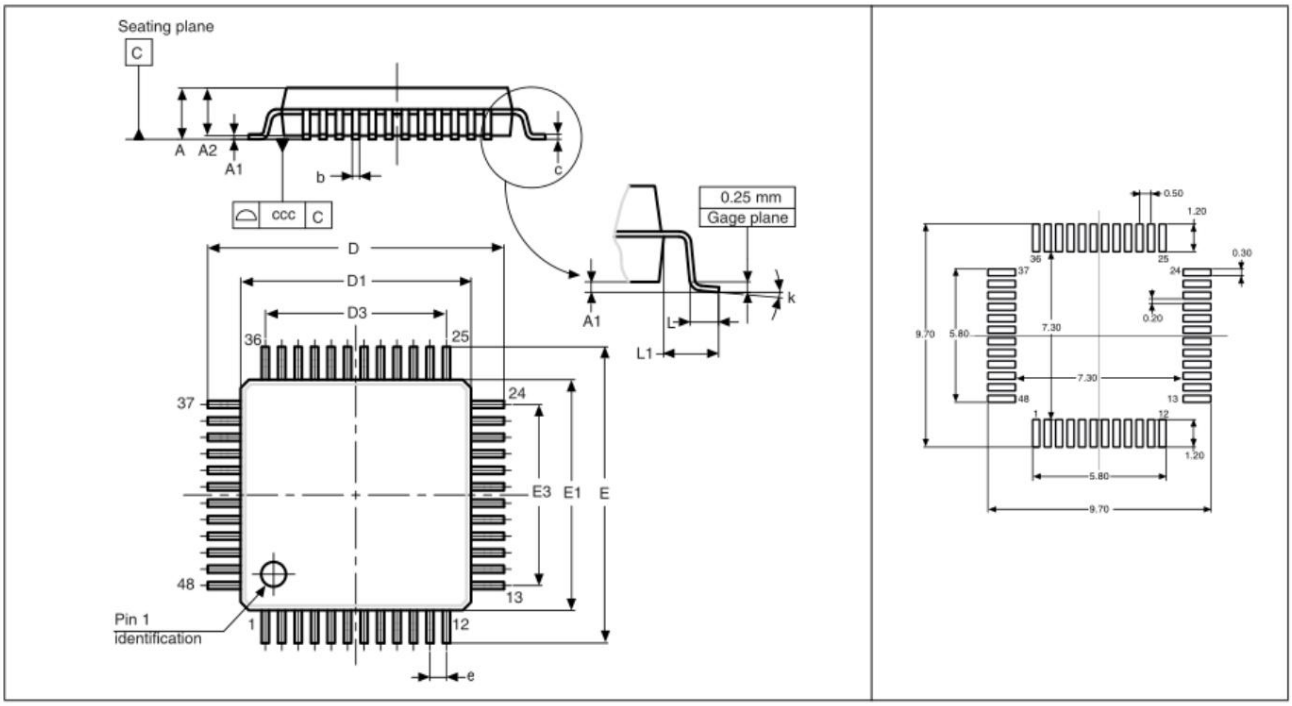
Note 1: Schematic diagrams are not drawn to scale

Figure 6.4: LQFP64 7X7mm, 64 pin package parameters

Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09	---	0.20	0.004	---	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

6.3 LQFP48 7X7mm

Figure 6.5: LQFP48 7X7mm, 0.5mm pitch and package parameters



Note 1: Schematic diagrams are not drawn

to scale Note 2: Dimensions are in millimeters

Figure 6.6: LQFP48 7X7mm, 48 pin package parameters

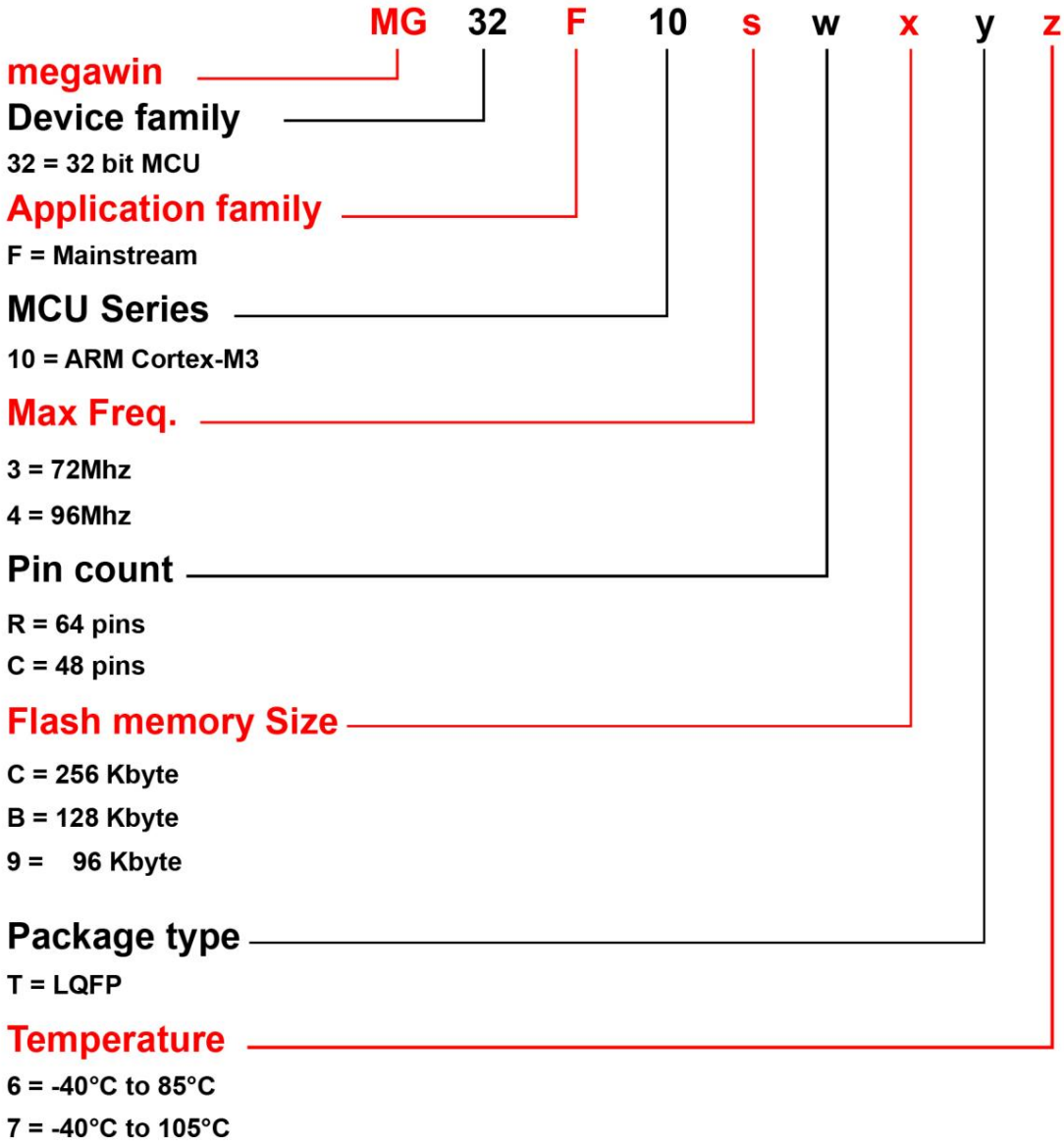
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

Chapter 7 Product Selection Table

Nb Segment LCD pins	8	8	8
USB	1	1	1
UART	3	3	3
I2C	2	2	2
I2S	1	1	1
SPI(S)	0	1	1
SPI(M)	2	2	2
Quad SPI (M)	1	1	1
Nb COMP Channels	1	1	1
Nb COMP			
Nb ADC Channels			
Nb ADC 10/12 bit Cell	-	-	-
Nb Motor Control Timer	1	1	1
Nb Timer (20bit)	1	1	1
Vmax			
Vmin			
IONb			
Package Name			
Ram (Kbytes)			
Flash (Kbytes)			
Core			
Frequency (MHz)			
Commercial Product Code			

Chapter VIII Product Code Information

Figure 8.1: MG32F103xx Product Code Information Sheet



Chapter IX Revised Version

Revision	Date	Author	Modify
01.01	20211124	zy.yao	Add LQFP64 7X7mm
01.00	20211013	zy.yao	Draft version