Cypress Product Roadmaps

Corporate Presentation

Q4 2018

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Cypress Roadmap: Module Solutions

Cypress Bluetooth Module Portfolio

Features ↑

Cost

CYBLE-416045-02 Q418
EZ-BLE Creator BT 5.0
PSoC 6 BLE
1MB Flash, 2Mbps BLE, 36 GPIOs
14 x 18.5 x 2.00 mm SMT

CYBT-413034-02
EZ-BT WICED BT 5.0 Dual Mode
CYW20719
1MB Flash, 2Mbps BLE
12 x 16.3 x 1.70 mm SMT
Mesh

CYBT-213043-02 Q119
EZ-BT WICED BT 5.0 Dual Mode
CYW20819
256KB Flash, 2Mbps BLE
12 x 16.3 x 1.70 mm SMT
Mesh

CYBT-343026-01
EZ-BT WICED BT 5.0 Dual Mode
CYW20706
512KB SFlash, 11 GPIOs, XR
12 x 15.5 x 1.95 mm SMT
Mesh EZ-S

CYBLE-x120xx-0x
EZ-BLE Creator BT 4.1/4.2
PSoC 4 BLE
128/256KB Flash, 23 GPIOs
14 x 19 x 2.00 mm SMT
EZ-S

CYBLE-0130xx-00
EZ-BLE WICED BT 4.1
CYW20737
128KB/0KB SFlash, 16/18 GPIOs
14 x 19 x 2.25 mm SMT
EZ-S

Size

CYBT-423028-02
EZ-BT WICED BT 5.0 Dual Mode
CYW20719
1MB Flash, 2Mbps BLE
11 x 11 x 1.70 mm SMT
Mesh

CYBT-353027-02
EZ-BT WICED BT 5.0 Dual Mode
CYW20707
512KB SFlash[5], XR
9 x 9 x 1.75 mm SMT
Mesh EZ-S

CYBLE-x140xx-0x
EZ-BLE Creator BT 4.1/4.2
PSoC 4 BLE, 128/256KB Flash,
Opamp, CMP, 4 UDBs, 25 GPIOs
11 x 11 x 1.70 mm SMT
EZ-S

CYBLE-x220xx-0x
EZ-BLE Creator BT 4.1/4.2
PSoC 4 BLE
128/256KB Flash, 16 GPIOs
10 x 10 x 1.80 mm SMT
EZ-S

External Antenna

CYBT-333032-02 Q119
EZ-BT WICED BT 5.0 Dual Mode
CYW20706
512KB SFlash, LMA[3], XR
Ext. Antenna via RF Pad
12 x 12 x 1.95 mm SMT
Mesh

CYBT-333047-02 Q119
EZ-BT WICED BT 5.0 Dual Mode
CYW20706
512KB SFlash, LMA, XR
Ext. Antenna via u.FL
12 x 12 x 1.95 mm SMT
Mesh

CYBLE-202007-01
EZ-BLE Creator BT 4.2
PSoC 4 BLE, 256 KB Flash, PA/LNA,
XR , Ext. Antenna via u.FL, 19 GPIOs
15 x 23 x 2.05 mm SMT
EZ-S

CYBLE-202013-11
EZ-BLE Creator BT 4.2
PSoC 4 BLE,
256 KB Flash, PA/LNA, NS[8], NC[9], XR,
Ext. Antenna via RF Pad, 19 GPIOs
15 x 23 x 1.55 mm SMT
EZ-S

XR[1]

CYBT-483039-02
EZ-BT WICED BT 5.0 Dual Mode
CYW20719
1MB Flash, 2Mbps BLE, PA/LNA[4] , XR
12.75 x 18.59 x 1.80 mm SMT
Mesh

CYBLE-212006-01
EZ-BLE Creator BT 4.2
PSoC 4 BLE
256 KB Flash, PA/LNA, XR
PCB Antenna, 19 GPIOs
15 x 23 x 2.00 mm SMT
EZ-S

CYBT-343052-02 Q219
EZ-BT WICED BT 5.0 Dual Mode
CYW20735
512KB SFlash, 11 GPIOs, XR,
Analog MIC interface
12 x 15.5 x 1.95 mm SMT
Mesh

XT[2]/XR

CYBT-343151-02 Q119
EZ-BT WICED BT 5.0 Dual Mode
CYW20706
512KB SFlash, 11 GPIOs, XR
12 x 15.5 x 1.95 mm SMT
Mesh

CYBLE-22411x-0x
EZ-BLE Creator BT 4.1/4.2
PSoC4-BLE,
256 KB Flash, PA/LNA, XR
Opamp, CMP[6], 4 UDB[7], 25 GPIOs
9.5 x 15.4 x 1.80 mm SMT
EZ-S

EZ-BLE/BT modules are pre-programmed with Cypress' EZ-Serial Firmware Platform

EZ-BLE Creator Standard Features:
CapSense, 1MSPS ADC, LCD Driver,
4 TCPWM[10], DAC, 2SCB[11]

EZ-BT/BLE WICED Standard Features:
Simultaneous Master/Slave,
ADC, PWM, UART

[1] Extended range power
[2] Extended temperature
[3] Limited modular approval
[4] Power amplifier/Low-noise amplifier
[5] Serial flash
[6] Comparator
[7] Universal digital block
[8] No shield
[9] No certifications
[10] Timer/counter/pulse-width modulator
[11] Serial communication block

Mesh Bluetooth SIG Mesh Qualified
EZ-S Pre-programmed with EZ-Serial Firmware

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

EZ-BLE™ Creator Modules CYBLE-x220xx-0x

Space-Optimized Bluetooth Low-Energy (BLE) Modules

Applications

Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, KC[2], MIC[3], and ISED[4]
- **Small Footprint**
  - 10 mm x 10 mm x 1.8 mm, 21/22-pad SMT with 16 GPIOs
- **Bluetooth Smart Connectivity with BLE 4.1 and 4.2**
  - 2.4-GHz BLE radio and baseband
  - -91-dBm Rx sensitivity, +3-dBm Tx output power
- **1.3-µA Deep Sleep, 150-nA Hibernate, 60-nA Stop Power Modes**
- **Highly Integrated Solution**
  - Two crystals, chip antenna, passives, shield
  - 128KB and 256KB flash sizes
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-x220xx-EVAL Evaluation Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense®, buttons, GPIOs, over-the-air (OTA)

Availability

Sampling (4.1/128KB, 4.1/256KB, 4.2): Now

Production (4.1/128KB, 4.1/256KB, 4.2): Now

EZ-BLE Creator Module Family: CYBLE-x220xx-0x

Collateral

Datasheets

CYBLE-022001-00 Datasheet

CYBLE-222005-00 Datasheet

CYBLE-222014-01 (BT 4.2) Datasheet

BLE Silicon Datasheet

App Notes/Evaluation Kit User Guides

Getting Started With EZ-BLE™ Module (AN96841)

PSoC Creator

PSoC Programmer

CySmart[7] Windows Host Emulation Tool

CySmart iOS and Android Apps

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Korea certification
[3] Ministry of Internal Affairs and Communications (Japan)
[4] Innovation, Science and Economic Development Canada
[5] Serial wire debug communication protocol
[6] VREF only available on 256KB module
[7] A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

EZ-BLE Creator Modules CYBLE-x140xx-0x

BLE Modules Designed to Maximize System Integration with Integrated Analog Functionality

Applications

Sports and fitness monitors, medical devices, wearable, electronics, home automation solutions, and game controllers

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, KC[2], MIC[3], and ISED[4]
- **Small Footprint**
  - 11 mm x 11 mm x 1.8 mm, 32-SMT, 25 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2**
- **Highly Integrated Solution**
  - Two crystals, trace antenna, passives, shield
  - 128KB and 256KB flash sizes, with over-the-air (OTA) firmware upgrades
  - Preprogrammed with EZ-Serial firmware
- **Programmable Analog Blocks**
  - Four opamps and one 12-bit, 1-Msps SAR[5] ADC
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Four configurable TCPWM[6] blocks: 16-bit timer, counter, or PWM
  - Two configurable serial communication blocks for I^2C/SPI/UART
- **1.3-µA Deep Sleep, 150-nA Hibernate, 60-nA Stop Power Modes**
- **CYBLE-x140xx-EVAL Kit for Fast Evaluation and Development**

Availability

Sampling (4.1/128KB, 4.1/256KB, 4.2): Now

Production (4.1/128KB, 4.1/256KB, 4.2): Now

EZ-BLE Creator Module Family: CYBLE-x140xx-0x

Collateral

Datasheets

CYBLE-014008-00 Datasheet
CYBLE-214009-00 Datasheet
CYBLE-214015-01 (BT 4.2) Datasheet
BLE Silicon Datasheet

App Notes/Evaluation Kit User Guides

Getting Started With EZ-BLE™ Module (AN96841)
PSoC Creator
PSoC Programmer
CySmart[8] Windows Host Emulation Tool
CySmart iOS and Android Apps

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Korea Certification
[3] Ministry of Internal Affairs and Communications (Japan)
[4] Innovation, Science and Economic Development Canada
[5] Successive approximation register
[6] Timer/counter/pulse-width modulator
[7] Serial wire debug communication protocol
[8] A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

EZ-BLE Creator Modules CYBLE-x120xx-xx

Cost-Optimized Bluetooth Low-Energy (BLE) Modules

Applications

Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1] (CYBLE-012011-00/CYBLE-212019-00), FCC, CE, KC[2], MIC[3], and ISED[4]
- **Small Footprint**
  - 14.5 mm x 19.2 mm x 2.0 mm, 31-pad SMT with 23 GPIO
- **Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2**
  - 2.4-GHz BLE radio and baseband
  - -91-dBm Rx sensitivity, +3-dBm Tx output power
- **Power Modes**
  - 1.3-µA Deep Sleep, 150-nA Hibernate, and 60-nA Stop
- **Highly Integrated Solution**
  - Two crystals, trace antenna, passives, shield[5]
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-x120xx-EVAL Adapter Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

Availability

Sampling (4.1/128KB, 4.1/256KB, 4.2): Now

Production (4.1/128KB, 4.1/256KB, 4.2): Now

EZ-BLE Creator Module Family: CYBLE-x120xx-xx

Collateral

Datasheets

CYBLE-012011-00 Datasheet
CYBLE-212019-00 Datasheet
CYBLE-212020-01 (BT 4.2) Datasheet
BLE Silicon Datasheet

App Notes/Evaluation Kit User Guides

Getting Started With EZ-BLE™ Module (AN96841)
PSoC Creator
PSoC Programmer
CySmart[7] Windows Host Emulation Tool
CySmart iOS and Android Apps

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Korea Certification
[3] Ministry of Internal Affairs and Communications (Japan)
[4] Innovation, Science and Economic Development Canada
[5] CYBLE-0120012-10 does not include metal shield
[6] Serial wire debug communication protocol
[7] A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

EZ-BLE Creator XR[1] Modules CYBLE-2x20xx-x1

Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting External Antenna

Applications

BLE connectivity, lighting, industrial, and medical

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[2], FCC, CE, MIC[3], KC[4], and ISED[5]
- **Small Footprint**
  - 15.0 mm x 23.0 mm x 2.0 mm, 30-pad SMT with 19 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.2**
  - 2.4-GHz BLE radio and baseband
- **Industrial Temperature Range**
  - Operating temperature range from -40°C to +85°C
- **Long Range**
  - +7.5-dBm Tx output power, 400 meters line-of-sight range
  - -93-dBm Rx sensitivity
- **Highly Integrated Solution**
  - Two crystals, trace antenna (optional), power amplifier, passives
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-2x20xx-EVAL Adapter Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

Availability

Sampling: Now
Production: Now

EZ-BLE Creator Module Family: CYBLE-2x20xx-x1

Collateral

Datasheets

CYBLE-2x20xx-x1 (BT 4.2) Datasheet
BLE Silicon Datasheet

App Notes/Evaluation Kit User Guides

Getting Started With EZ-BLE™ Module (AN96841)
PSoC Creator
PSoC Programmer
CySmart[7] Windows Host Emulation Tool
CySmart iOS and Android Apps

[1] Extended range
[2] Bluetooth Special Interest Group Qualification Design ID
[3] Ministry of Internal Affairs and Communications (Japan)
[4] Korea Certification
[5] Innovation, Science and Economic Development Canada
[6] Serial wire debug communication protocol
[7] A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

EZ-BLE Creator XT/XR[1] Modules CYBLE-22411x-0x

Long-Range Bluetooth Low-Energy (BLE) Modules Supporting Extended Temperatures

Applications

Connectivity, lighting, industrial, and medical

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[2], FCC, CE, MIC[3], KC[4], and ISED[5]
- **Small Footprint**
  - 9.5 mm x 15.4 mm x 1.8 mm, 32-pad SMT with 25 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2**
  - 2.4-GHz BLE radio and baseband
- **Extended Industrial Temperature Range**
  - Operating temperature range from -40°C to +105°C
- **Long Range**
  - +9.5-dBm Tx output power, 400 meters line-of-sight range
  - -95-dBm Rx sensitivity
- **Highly Integrated Solution**
  - Two crystals, trace antenna, power amplifier, passives, shield
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-22411x-EVAL Adapter Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

Availability

Sampling (4.1/128KB, 4.2/256KB): Now

Production (4.1/128KB, 4.2/256KB): Now

EZ-BLE Creator Module Family: CYBLE-22411x-0x

Collateral

Datasheet

CYBLE-224110-00 Datasheet

BLE Silicon Datasheet

CYBLE-224116-01 (BT 4.2) Datasheet

App Notes/Evaluation Kit User Guides

Getting Started With EZ-BLE™ Module (AN96841)

PSoC Creator

PSoC Programmer

CySmart[7] Windows Host Emulation Tool

CySmart iOS and Android Apps

[1] Extended temperature/extended range
[2] Bluetooth Special Interest Group Qualification Design ID
[3] Ministry of Internal Affairs and Communications (Japan)
[4] Korea Certification
[5] Innovation, Science and Economic Development Canada
[6] Serial wire debug communication protocol
[7] A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

EZ-BLE Creator Modules CYBLE-416045-02

Ultra-Low-Power Bluetooth Low-Energy (BLE) Module

Applications

BLE connectivity, lighting, industrial, and medical

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 14.0 mm x 18.5 mm x 2.0 mm, 43-pad SMT with 36 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 5.0**
  - 2.4-GHz BLE radio and baseband
  - +4.0-dBm Tx output power, -95-dBm Rx sensitivity
- **Industrial Temperature Range**
  - Operating temperature range from -40°C to +85°C
- **Power Modes**
  - 5.7-mA TX (0 dBm) and 6.7-mA RX (2 Mbps) current with 3.3-V battery and internal SIMO Buck converter
  - Deep Sleep mode current with 64K SRAM retention is 7 µA with 3.3-V external supply and internal buck
  - On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, <1 µA quiescent current
- **Highly Integrated Solution**
  - One crystal, trace antenna, passives

Availability

Sampling: Now

Production: Q4 2018

EZ-BLE Creator Module Family: CYBLE-416045-02

Collateral

Datasheets

CYBLE-416045-02 Datasheet

BLE Silicon, PSoC 6 MCU: PSoC 63 with BLE Datasheet

App Notes/Evaluation Kit User Guides

Getting Started With EZ-BLE™ Module (AN96841)

PSoC Creator

PSoC Programmer

CySmart[6] Windows Host Emulation Tool

CySmart iOS and Android Apps

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada
[4] Serial wire debug communication protocol
[5] A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

EZ-BLE WICED Modules CYBLE-0130xx-00

Cost-Optimized Bluetooth Low-Energy (BLE) WICED Modules

Applications

Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 14.5 mm x 19.2 mm x 2.0 mm, 31-pad SMT with 16/18 GPIO
- **Bluetooth Smart Connectivity with Bluetooth 4.1**
  - 2.4-GHz BLE radio and baseband
  - -93-dBm Rx sensitivity, +4-dBm Tx output power
- **Highly Integrated Solution**
  - One crystal, 128KB flash (CYBLE-013025-00), PCB antenna, shield
  - Simultaneous multiple Master and Slave (1M, 3S)
  - Security engine
  - Secure over-the-air (OTA) firmware upgrade (CYBLE-013025-00)
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-013025-EVAL Arduino Evaluation Board**

Availability

Sampling: Now
Production: Now

EZ-BLE WICED Module Family: CYBLE-0130xx-00

Collateral

Datasheets

CYBLE-0130xx-00 Datasheet

Evaluation Kit User Guide

CYBLE-013025-EVAL Evaluation Board
WICED SMART SDK（Software)
WICED SMART SDK 2.x (Quick Start Guide)

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BT WICED Module CYBT-343026-01

Cost-Optimized Bluetooth Smart Ready WICED Modules

Applications

Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/I^{2}S audio interface with wideband speech support
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

Availability

Sampling: Now
Production: Now

EZ-BT WICED Module Family: CYBLE-343026-01

Collateral

Datasheets

CYBT-343026-01 Datasheet

Evaluation Kit User Guide

CYBT-343026-EVAL Evaluation Board

WICED Studio

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BT WICED Module CYBT-3330xx-02

Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting External Antenna

Applications

Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/I^{2}S audio interface with wideband speech support
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

Availability

Sampling: Now
Production: Q1 2019

EZ-BT WICED Module Family: CYBT-3330xx-02

Collateral

Datasheets

CYBT-333032-01 Datasheet

CYBT-333047-01 Datasheet

Evaluation Kit User Guide

CYBT-343047-EVAL Evaluation Board

WICED Studio

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BT WICED Module CYBT-343151-02

Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting Extended Temperatures

Applications

Connectivity, lighting, industrial, and medical

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
  - Drop-in compatible with CYBT-343026-01
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- **Extended Industrial Temperature Range**
  - Operating temperature range from -40°C to +105°C
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/I²S audio interface with wideband speech support
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

Availability

Sampling: Now

Production: Q1 2019

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BT WICED Module Family: CYBLE-343151-02

Collateral

Datasheets

CYBT-343151-02 Datasheet

Evaluation Kit User Guide

CYBT-343026-EVAL Evaluation Board

WICED Studio

EZ-BT WICED Module CYBT-353027-02

Size-Optimized Bluetooth 5.0 WICED Module

Applications

Bluetooth speaker, POS, medical, industrial, PC accessories, toys, and smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 9 mm x 9 mm x 1.75 mm, 19-pad SMT with 8 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx sensitivity, +9-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/I^{2}S audio interface with wideband speech support
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q3 2018)

Availability

Sampling: Now
Production: Now

EZ-BT WICED Module Family: CYBLE-353027-02

Collateral

Datasheets

CYBT-353027-02 Datasheet

Evaluation Kit User Guide

CYBT-353027-EVAL Board

WICED Studio

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BT WICED Module CYBT-423028-02

Ultra-Low-Power Size-Optimized Bluetooth 5.0 WICED Module

Applications

Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 11 mm x 11 mm x 1.70 mm, 28-pad SMT with 17 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 1MB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/I²S audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q3 2018)

Availability

Sampling: Now
Production: Now

EZ-BT WICED Module Family: CYBLE-423028-02

Collateral

Datasheets

CYBT-423028-02 Datasheet

Evaluation Kit User Guide

CYBT-423028-EVAL Board

WICED Studio

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BT WICED Module CYBT-413034-02

Ultra-Low-Power Cost-Optimized Bluetooth 5.0 WICED Module

Applications

Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 12 mm x 16.3 mm x 1.70 mm, 30-pad SMT with 17 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 1MB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/I²S audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2018)

Availability

Sampling: Now
Production: Now

EZ-BT WICED Module Family: CYBLE-413034-02

Collateral

Datasheets

CYBT-413034-02 Datasheet

Evaluation Kit User Guide

CYBT-413034-EVAL Board

WICED Studio

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BT WICED Module CYBT-483039-02

Ultra-Long Range Bluetooth 5.0 WICED Module

Applications

Bluetooth audio, mesh, sensor hubs, and industrial

Features

- **Qualification and Certification**
  - Bluetooth SIG QDID[1], FCC, CE, MIC[2], and ISED[3]
- **Small Footprint**
  - 12.75 mm x 18.59 mm x 1.8 mm, 34-pad SMT with 15 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BLE Tx output power up to 20 dBm for U.S. (FCC)
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 1MB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/I²S audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2018)

Availability

Sampling: Now
Production: Now

EZ-BT WICED Module Family: CYBLE-483039-02

Collateral

Datasheets

CYBT-483039-02 Datasheet

Evaluation Kit User Guide

CYBT-483039-EVAL Board

WICED Studio

[1] Bluetooth Special Interest Group Qualification Design ID
[2] Ministry of Internal Affairs and Communications (Japan)
[3] Innovation, Science and Economic Development Canada

EZ-BLE/EZ-BT Module Product Selector Guide

EZ-BLE Module Part Numbering Decoder

CY BT – X X X X XX – N X

Bluetooth Version:	0 = Bluetooth 4.1, 1 = Bluetooth 4.2, 2 = Bluetooth 5.0
Integration Type:	0 = Full Integration with Shield, 1 = No Shield
Device Identification #:	Unique sequential product number for each module
Temperature Range:	0 = Industrial, 1 = Extended Industrial
EZ-BT Module Type:	2/4 = PSoC 4 Module, 3 = WICED Module, 6 = PSoC 6 Module
Antenna Type:	0 – No Antenna, Standard Range 1 – PCB Antenna, Standard Range 2 – Chip Antenna, Standard Range 3 – No Antenna, Long Range (internal PA) 4 – PCB Antenna, Long Range (internal PA) 5 – Chip Antenna, Long Range (internal PA) 6 – No Antenna, Long Range (external PA/LNA) 7 – PCB Antenna, Long Range (external PA/LNA) 8 – Chip Antenna, Long Range (external PA/LNA)
Flash Size:	0 = 128KB, 2 = 256KB, 3 = 512KB, 4 = 1024KB
Marketing Code:	BLE = BLE Only Product, BT = Dual-Mode BT/LE Product
Company ID:	CY = Cypress

MCU Portfolio Roadmap

MCU Portfolio Public

8-Bit	32-Bit Arm® Cortex®-M0/M0+	32-Bit Arm Cortex-M3	32-Bit Arm Cortex-M4/M33(future)
High Analog Integration	8-/16-Bit Replacement	Mid-Range Performance	Ultra-Low-Power High Performance

Analog and Digital Integration

PSoC is a brand of Cypress MCUs for the broad-based embedded market that delivers an Arm Cortex-M CPU (PSoC 4+) with unique software-defined peripherals and CapSense capacitive sensing

FM is a portfolio of high-performance Arm Cortex-M-based MCUs for industrial and consumer applications

PSoC 3
8051 CPU
67 MHz, 64KB Flash
Up to 19 PAB, 30 PDB, 72 I/Os

PSoC 1
M8C CPU
24 MHz, 32KB Flash
16 PAB, 16 PDB, 64 I/Os

8FX
8-bit RISC MCU
16 MHz, 32–50KB Flash

PSoC 4
Cortex-M0/M0+
48 MHz, 256KB Flash
Up to 13 PAB, 20 PDB, 98 I/Os

FM0+ MCUs
Cortex®-M0+
40 MHz, 512KB Flash, 102 I/Os

PSoC 5LP
Cortex-M3
80 MHz, 256KB Flash
20 PAB, 30 PDB, 72 I/Os

FM3 MCUs
Cortex-M3
144 MHz, 1.5MB Flash, 154 I/Os

PSoC 6
150 MHz Cortex-M4, 100 MHz Cortex-M0+, 2MB Flash
7 PAB, 56 PDB, 104 I/Os

FM4 MCUs
Cortex-M4
200 MHz, 2MB Flash, 190 I/Os

[1] A programmable analog block that is configured using PSoC software to create analog front ends, signal conditioning circuits with opamps and filters
[2] A programmable digital block that is configured using PSoC software to implement custom digital peripherals and glue logic

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

PSoC 6 MCU Portfolio

Ultra-Low-Power | Flexibility | Hardware-Based Security and Root of Trust

Performance and Integration

PSoC 60 Line General-Purpose MCU Series	PSoC 61 Line Ultra-Low-Power and High-Performance MCU Series	PSoC 62 Line Ultra-Low-Power, Dual-Core, and High-Performance MCU Series	PSoC 63 Line High-Integration Wired/Wireless Connectivity MCU Series
NEW, Q119 **CY8C60xA** Arm Cortex-M4 2MB/1MB CMP, ADC, SCB, FS-USB, QSPI, SDHC, DAC	NEW, Q119 **CY8C61xA** Arm Cortex-M4 2MB/1MB CMP, ADC, SCB DAC, QSPI, FS-USB, SDHC, DC-DC	NEW, Q119 **CY8C62xA** Arm Cortex-M4 & Arm Cortex-M0+ 2MB/1MB[1] CMP, ADC, SCB[2], DAC QSPI[3], FS-USB[4], SDHC[5], DC-DC	**CY8C63xA** Arm Cortex-M4 & Arm Cortex-M0+ 2MB/1MB CMP, ADC, SCB, DAC, QSPI, UDB[6], MIPI[7], SDHC, CAN[8], BT/BLE, DC-DC
CY8C60x7 Arm Cortex-M4 1MB/288KB CMP, ADC, SCB, FS-USB, QSPI, DAC	**CY8C61x7** Arm Cortex-M4 1MB/288KB CMP, Opamp, ADC, SCB DAC, QSPI, UDB, FS-USB DC-DC	**CY8C62x7** Arm Cortex-M4 & Arm Cortex-M0+ 1MB/288KB CMP, Opamp, ADC, SCB, DAC, QSPI, UDB, FS-USB, DC-DC	**CY8C63x7** Arm Cortex-M4 & Arm Cortex-M0+ 1MB/288KB CMP, Opamp, ADC, SCB DAC, QSPI, UDB, BLE, DC-DC
NEW, Q219 **CY8C60x5** Arm Cortex-M4 512KB/160KB CMP, ADC, SCB, FS-USB, QSPI, SDHC, DAC, CAN	NEW, Q219 **CY8C61x5** Arm Cortex-M4 512KB/160KB CMP, Opamp, ADC, SCB DAC, QSPI, UDB, FS-USB CAN, SDHC	NEW, Q219 **CY8C62x5** Arm Cortex-M4 & Arm Cortex-M0+ 512KB/160KB CMP, Opamp, ADC, SCB, DAC, QSPI, UDB, FS-USB, CAN[6], DC-DC, SDHC	**CY8C63x5** Arm Cortex-M4 & Arm Cortex-M0+ 512KB/160KB, 1.71–3.6V CMP, Opamp , ADC, SCB DAC, QSPI, UDB, BLE, DC-DC

[1] Flash KB/SRAM KB
[2] Serial communication block (UART, SPI, I²C)
[3] Quad-SPI
[4] Full-Speed USB
[5] Secure Digital Host Controller
[6] Universal digital block – programmable logic
[7] Mobile Industry Processor Interface
[8] Controller Area Network

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

Roadmap

PSoC® 5LP Portfolio

Arm® Cortex®-M3 | CapSense® | DMA | LCD | RTC | TCPWM

CPU Speed and Flash ↑

Programmable Digital PSoC 5200	Intelligent Analog PSoC 5400	Performance Analog PSoC 5600	Precision Analog PSoC 5800
Analog: 1x ADC[1], 1x DAC[2], 2x CMP[3], 0.9% V_{REF} Interfaces: USB, FF[4] I²C	Analog: 1x ADC, 2x DAC, 4x CMP, 2x Opamps, 2x SC/CT PAB[5], 0.9% V_{REF} Interfaces: USB, FF I²C	Analog: 2x ADC, 4x DAC, 4x CMP, 4x Opamps, DFB[6], 4x SC/CT PAB, 0.9% V_{REF} Interfaces: USB, FF I²C, CAN[7]	Analog: 2x/3x ADC, 4x DAC, 4x CMP, 4x Opamps, DFB, 4x SC/CT PAB, 0.1% V_{REF} Interfaces: USB, FF I²C, CAN
CY8C5288 80 MHz, 256K/64K/2K[8] 12b SAR ADC 24x UDB[9], 99-CSP[10]	**CY8C5488** 80 MHz, 256K/64K/2K 12b SAR ADC 24x UDB, 99-CSP	**CY8C5688** 80 MHz, 256K/64K/2K 2x 12b SAR ADC 24x UDB, 99-CSP	**CY8C5888** 80 MHz, 256K/64K/2K 20b ΔΣ ADC[11], 2x 12b SAR ADC 24x UDB[9], 99-CSP
CY8C5268 67 MHz, 256K/64K/2K 12b SAR ADC 24x UDB	**CY8C5468** 67 MHz, 256K/64K/2K 12b SAR ADC 24x UDB	**CY8C5668** 67 MHz, 256K/64K/2K 12b ΔΣ ADC, 12b SAR/2x 12b SAR ADC 24x UDB	**CY8C5868** 67 MHz, 256K/64K/2K 20b ΔΣ ADC, 2x 12b SAR ADC 24x UDB
CY8C5267 67 MHz, 128K/32K/2K 12b SAR ADC 24x UDB	**CY8C5467** 67 MHz, 128K/32K/2K 12b SAR ADC 24x UDB	**CY8C5667** 67 MHz, 128K/32K/2K 12b ΔΣ ADC, 12b SAR/2x 12b SAR ADC 24x UDB	**CY8C5867** 67 MHz, 128K/32K/2K 20b ΔΣ ADC, 12b SAR ADC 24x UDB
CY8C5266 67 MHz, 64K/16K/2K 12b SAR ADC 20x UDB	**CY8C5466** 67 MHz, 64K/16K/2K 12b SAR ADC 20x UDB	**CY8C5666** 67 MHz, 64K/16K/2K 12b ΔΣ ADC, 12b SAR ADC 20x UDB	**CY8C5866** 67 MHz, 64K/16K/2K 20b ΔΣ ADC, 12b SAR ADC 20x UDB
CY8C5265 67 MHz, 32K/8K/2K 12b SAR ADC 20x UDB	**CY8C5465** 67 MHz, 32K/8K/2K 12b SAR ADC 20x UDB		

[1] Analog-to-digital converter
[2] Digital-to-analog converter
[3] Comparator
[4] Fixed function
[5] Switched capacitor/continuous time programmable analog block
[6] Digital filter block
[7] Controller area network
[8] Flash KB/SRAM KB/EEPROM KB
[9] Universal digital block
[10] Chip-scale package
[11] Delta-Sigma ADC

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

PSoC® 4 Portfolio

Flexibility | CapSense® | Ease-of-Use

Performance and Integration

BL = BLE-Series S = S-Series M = M-Series L = L-Series

PSoC MCU PSoC 4000

- **CY8C4045-S** 48-MHz M0+, 32K/4K CMP, ADC, SCB IDAC, Smart I/O
- **CY8C4024-S** 24-MHz M0+, 16K/2K CMP, ADC, SCB IDAC, Smart I/O
- **CY8C4014** 16-MHz M0, 16K/2K CMP, I²C, IDAC

Intelligent Analog PSoC 4100

- **CY8C4128-S** 24-MHz M0+, 256K/32K[1] CMP[2], Opamp, ADC[3] SCB[4], IDAC[5], Smart I/O[6] ECO
- **CY8C4147-S** 48-MHz M0+,128K/16K CMP, Opamp, ADC SCB, IDAC, Smart I/O ECO
- **CY8C4127-S** 24-MHz M0+, 128K/16K CMP, Opamp, ADC SCB, IDAC, Smart I/O ECO
- **CY8C4127-M** 24-MHz M0, 128K/16K CMP, Opamp, ADC, SCB IDAC
- **CY8C4126-M** 24-MHz M0, 64K/8K CMP, Opamp, ADC, SCB IDAC
- **CY8C4125** 24-MHz M0, 32K/4K CMP, Opamp, ADC, SCB IDAC
- **CY8C4124** 24-MHz M0, 16K/4K CMP, Opamp, ADC, SCB IDAC
- **CY8C4148-S** 48-MHz M0+, 256K/32K CMP, Opamp, ADC SCB, IDAC, Smart I/O ECO
- **CY8C4128-BL** 24-MHz M0, 256K/32K CMP, Opamp, ADC, SCB IDAC, BLE[7]
- **CY8C4127-BL** 24-MHz M0, 128K/16K CMP, Opamp, ADC, SCB IDAC, BLE
- **CY8C4146-S** 48-MHz M0+, 64K/8K CMP, Opamp, ADC, SCB IDAC, Smart I/O
- NEW **CY8C41xx-PS** 48-MHz M0+, 32K/4K CMP, Opamp, ADC SCB, VDAC, Smart I/O
- **CY8C4125-S** 24-MHz M0+, 32K/4K CMP, Opamp, ADC, SCB IDAC, Smart I/O
- **CY8C4124-S** 24-MHz M0+, 16K/4K CMP, Opamp, ADC, SCB IDAC, Smart I/O

Programmable Digital PSoC 4200

- **CY8C4247-M** 48-MHz M0, 128K/16K, CMP, Opamp, ADC, SCB IDAC, UDB[8], CAN[9]
- **CY8C4246-M** 48-MHz M0, 64K/8K, CMP, Opamp, ADC, SCB IDAC, UDB
- **CY8C4246-DS** 48-MHz M0, 64K/8K CMP, SCB UDB, Smart I/O
- **CY8C4245-DS** 48-MHz M0, 32K/4K CMP, SCB UDB, Smart I/O
- **CY8C4245** 48-MHz M0, 32K/4K CMP, Opamp, ADC, SCB IDAC, UDB
- **CY8C4244** 48-MHz M0, 16K/4K, CMP, Opamp, ADC, SCB IDAC, UDB
- **CY8C4248-BL** 48-MHz M0, 256K/32K CMP, Opamp, ADC, SCB IDAC, BLE, UDB
- **CY8C4247-BL** 48-MHz M0, 128K/16K CMP, Opamp, ADC, SCB IDAC, BLE, UDB
- **CY8C4248-L** 48-MHz M0, 256K/32K CMP, Opamp, ADC, SCB IDAC, UDB, CAN, USB
- **CY8C4247-L** 48-MHz M0, 128K/16K CMP, Opamp, ADC, SCB IDAC, UDB, CAN, USB
- **CY8C4246-L** 48-MHz M0, 64K/8K CMP, Opamp, ADC, SCB IDAC, UDB, CAN, USB

Analog Coprocessor PSoC 4A00

- **CY8C4Axx** 48-MHz M0+, 32K/4K CMP, Opamp, UAB[10] ADC, SCB, VDAC Smart I/O

Inductive Sensing PSoC 4700

- **CY8C47XX Inductive Sensing** 48-MHz M0+, 32K/4K CMP, Opamp, UAB[10] ADC, SCB, VDAC Smart I/O

[1] Flash KB/SRAM KB
[2] Comparator
[3] Analog-to-digital converter
[4] Serial communication block
[5] Current-output DAC
[6] Embedded programmable digital logic in the I/O subsystem
[7] Bluetooth Low Energy
[8] Universal digital block
[9] Controller area network
[10] Universal analog block

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

FM4® and FM0+® MCU Portfolio

Arm® Cortex®-M4 and Arm Cortex-M0+

Ultra-Low-Power 8-Bit/16-Bit Replacement	High Performance

Flash

S6E2D-Series
160 MHz, 540 CoreMark®, 2.7–3.6 V
2M/36K[1], 512KB Video RAM
120/176 Pins

S6E2C-Series
200 MHz, 675 CoreMark, 2.7–5.5 V
2M/256K, 144/176/216 Pins

MB9BFx6xM/N/R-Series
160 MHz, 540 CoreMark, 2.7–5.5 V
1M/128K, 32KB Work Flash[2]
80/100/120 Pins

S6E2G-Series
180 MHz, 608 CoreMark, 2.7–5.5 V
1M/192K, 144/176 Pins

S6E2H-Series
160 MHz, 540 CoreMark, 2.7–5.5 V
512K/64K, 32KB Work Flash
80/100/120 Pins

S6E1C-Series
40 MHz, 1.7–3.6 V
128K/16K, 26/32/48/64 Pins, 40 µA/MHz[3]

MB9BFx6xK/L-Series
160 MHz, 540 CoreMark, 2.7–5.5 V
512K/64K, 32KB Work Flash
48/64 Pins

S6E1A-Series
40 MHz, 2.7–5.5 V
88K/6K, 32/48 Pins, 70 µA/MHz

CPU Speed

[1] Flash KB/SRAM KB
[2] Independent flash memory available to store data or additional firmware
[3] Active power consumption

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

FM3® MCU Portfolio

Arm® Cortex®-M3

Midrange Performance

MB9BFx2xS/T-Series
60 MHz, 2.7–5.5 V
1.5M/192K[1], 64KB Work Flash[2]
144/176 Pins

MB9BFx1xS/T-Series
144 MHz, 2.7–5.5 V,
1M/128K, 144/176 Pins

MB9BFx1xN/R-Series
144 MHz, 2.7–5.5 V
512K/64K, 32KB Work Flash,
100/120 Pins

MB9AFx2xK/L-Series
40 MHz, 2.7–5.5 V
512K/32K, 80/100 Pins

MB9AFx5xM/N/R-Series
40 MHz, 1.7–3.6 V
512K/64K, 32KB Work Flash
80/100/120 Pins

MB9AFx4xL/M/N-Series
40 MHz, 1.7–3.6 V
256K/32K, 32KB Work Flash
64/80/100 Pins

MB9AFx3xK/L-Series
20 MHz, 1.8–5.5 V
128K/8K, 48/64 Pins

MB9AFx1xL/M/N-Series
40 MHz, 2.7–5.5 V
256K/32K, 64/80/100 Pins

MB9BFx2xK/L/M-Series
72 MHz, 2.7–5.5 V
256K/32K, 32KB Work Flash
48/64/80 Pins

MB9AFxAxL/M/N-Series
20 MHz, 1.8–5.5 V
128K/16K, 64/80/100 Pins

MB9AFx1xK-Series
40 MHz, 2.7–5.5 V
128K/16K, 32KB Work Flash
48 Pins

MB9AFx2xK/L-Series
40 MHz, 2.7–5.5 V
64K/4K, 48/64 Pins

MB9BF121J-Series
72 MHz, 2.7–5.5 V
64K/8K, 32 Pins

Flash

CPU Speed

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

[1] Flash KB/SRAM KB
[2] Independent flash memory available to store data or additional firmware

PSoC® 3 Portfolio

8051 CPU | CapSense® | DMA | LCD | RTC | TCPWM

CPU Speed and Flash ↑

Programmable Digital PSoC 3200	Intelligent Analog PSoC 3400	Performance Analog PSoC 3600	Precision Analog PSoC 3800
Analog: ΔΣ ADC[1], 1x DAC[2], 2x CMP[3], 0.9% V_{REF} Interfaces: FF[4] I²C	Analog: ΔΣ ADC, 2x DAC, 4x CMP, 2x Opamps, 2x SC/CT PAB[5], 0.9% V_{REF} Interfaces: FF I²C	Analog: ΔΣ ADC, 2x/4x DAC, 0x/2x/4x CMP, 0x/2x/4x Opamps, 0x/2x/4x SC/CT PAB, 0.1% V_{REF} Interfaces: USB, FF I²C	Analog: ΔΣ ADC, 2x/4x DAC, 0x/2x/4x CMP, 0x/2x/4x Opamps, 0x/2x/4x SC/CT PAB, 0.1% V_{REF} Interfaces: USB, FF I²C
		CY8C3666 67 MHz, 64K/8K/2K[6] 0x/1x DFB[7], 12b ADC 20x/24x UDB[8], CAN[9]	**CY8C3866** 67 MHz, 64K/8K/2K DFB, 20b ADC 20x/24x UDB, CAN, 72-CSP[10]
		CY8C3665 67 MHz, 32K/4-8K/1K 0x/1x DFB, 12b ADC 16x/20x UDB, 72-CSP	**CY8C3865** 67 MHz, 32K/4-8K/1K 0x/1x DFB, 20b ADC 16x/20x UDB
CY8C3246 50 MHz, 64K/8K/2K 12b ADC 24x UDB, USB, 72-CSP	**CY8C3446** 50 MHz, 64K/8K/2K 12b ADC 24x UDB, USB, CAN		
CY8C3245 50 MHz, 32K/4K/1K 12b ADC 20x UDB, USB, 72-CSP	**CY8C3445** 50 MHz, 32K/4K/1K 12b ADC 20x UDB, USB		
CY8C3244 50 MHz, 16K/2K/0.5K 12b ADC 16x UDB	**CY8C3444** 50 MHz, 16K/2K/0.5K 12b ADC 16x UDB		

[1] Delta-Sigma analog-to-digital converter
[2] Digital-to-analog converter
[3] Comparator
[4] Fixed function
[5] Switched capacitor/continuous time programmable analog block
[6] Flash KB/SRAM KB/EEPROM KB
[7] Digital filter block
[8] Universal digital block
[9] Controller area network
[10] Chip-scale package

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

PSoC® 1 Portfolio

M8C CPU | 24 MHz

Flash

PSoC MCU	Programmable Digital	Intelligent Analog	Performance Analog
			CY8C29xxx 32K/2K[1], 64 GPIOs[2] CapSense®, 16x PDB[3], 4x CMP[4] 1x14-bit ΔΣ[5] ADC, 12x SC/CT PAB[6]
CY8C24x93 32K/2K, 36 GPIOs 2x CMP, 1x10-bit Incremental ADC			**CY8C27xxx** 32K/2K, 44 GPIOs CapSense, 8x PDB, 4x CMP 1x14-bit ΔΣ ADC, 12x SC/CT PAB
		CY8C24x94 16K/1K, 56 GPIOs CapSense, 4x PDB, 2x CMP 2x14-bit SAR[7] ADC, 6x SC/CT PAB	**CY8C28xxx** 16K/1K, 44 GPIOs CapSense, 12x PDB, 4x CMP 4x14-bit ΔΣ ADC, 16x SC/CT PAB
		CY8C2xx45 16K/1K, 38 GPIOs CapSense, 8x PDB, 4x CMP 1x10-bit SAR ADC, 6x SC/CT PAB	
	CY8C21x34 8K/0.5K , 28 GPIOs CapSense, 4x PDB , 2x CMP 1x10-bit Single-Slope ADC, 4x SC/CT PAB		
	CY8C23x33 8K/0.25K, 26 GPIOs CapSense, 4x PDB, 1x CMP 1x 8-bit SAR ADC, 4x SC/CT PAB		
	CY8C21x23 4K/0.25K, 16 GPIOs 4x PDB, 2x CMP 1x10-bit Single-Slope ADC, 4x SC/CT PAB	**CY8C24x23** 4K/0.25K, 24 GPIOs CapSense, 4x PDB, 2x CMP 1x14-bit ΔΣ ADC, 6x SC/CT PAB	

[1] Flash KB/SRAM KB
[2] General purpose input/output pins
[3] Programmable digital block
[4] Comparator
[5] Delta-Sigma ADC
[6] Switched capacitor/continuous time programmable analog block
[7] Successive approximation register ADC

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

8FX® MCU Portfolio

8-Bit RISC CPU

CPU Speed and Flash

8-/16-Pin	20-Pin	24-Pin	32-Pin	48-/52-Pin	64-Pin	80-Pin
					MB95810K 16 MHz, 2.8–5.5 V 56/2/4[1]	**MB95710M** 16 MHz, 1.8–5.5 V 56/2/4
				MB95690K 16 MHz, 2.8–5.5 V 56/2/4	**MB95770M** 16 MHz, 1.8–5.5 V 56/2/4	
		MB95650L 16 MHz, 1.8–5.5 V 32/1/4	**MB95630H** 16 MHz, 2.4–5.5 V 32/1/4			**MB95610H** 16 MHz, 2.4–5.5 V 32/1/4
MB95580H 16 MHz, 2.4–5.5 V 16/0.5/4	**MB95560H** 16 MHz, 2.4–5.5 V 16/0.5/4					
MB95570H 16 MHz, 2.4–5.5 V 16/0.5/4						

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

[1] Flash KB/SRAM KB/work flash KB; work flash is independent flash memory available to store data or additional firmware

CapSense® Portfolio

	CapSense Express™		CapSense Plus™	
	Configurable Controllers[1]		Programmable Controllers[2]	
Performance	**CY8CMBR3106S** 11 Buttons, 2 Sliders Proximity, Liquid Tolerance SmartSense_EMCplus™[3]	**CY8CMBR3116** 16 Buttons, 8 LEDs Proximity, Liquid Tolerance SmartSense_EMCplus		
	CY8CMBR3108 8 Buttons, 4 LEDs Proximity, Liquid Tolerance SmartSense_EMCplus	**CY8CMBR3110** 10 Buttons, 5 LEDs Proximity, Liquid Tolerance SmartSense_EMCplus		**CY8C20xx7** 31 Buttons, 6 Sliders 16, 32KB Flash Proximity, Liquid Tolerance SmartSense™ Auto-tuning
	CY8CMBR3102 2 Buttons, Proximity SmartSense_EMCplus	**CY8CMBR2110** 10 Buttons, 10 LEDs SmartSense Auto-tuning		**CY8C20xx6A/S** 33 Buttons, 6 Sliders 16, 32KB Flash, 2KB SRAM SmartSense Auto-tuning
		CY8CMBR2016 16 Buttons SmartSense Auto-tuning	**CY8C20xx6H** 25 Buttons, 5 Sliders 8, 16KB Flash SmartSense Auto-tuning Haptics	**CY8C21x34/B** 24 Buttons, 4 Sliders 8KB Flash Proximity, Liquid Tolerance SmartSense Auto-tuning
	CY8CMBR2044 4 Buttons, 4 LEDs SmartSense Auto-tuning	**CY8CMBR2010** 10 Buttons, 10 LEDs SmartSense Auto-tuning		**CY8C20x36A** 33 Buttons, 6 Sliders 8KB Flash SmartSense Auto-tuning
	CY8CMBR3002 2 Buttons, 2 LEDs SmartSense_EMCplus	**CY8C201xx** 10 Buttons, 5 LEDs 2 Sliders	**CY8C20x34** 25 Buttons, 6 Sliders 8KB Flash	

Integration

[1] Standard products that are configured for target applications with a graphical user interface
[2] Microcontroller-based products that can be freely programmed to implement additional functions
[3] SmartSense Electromagnetic Compatible = SmartSense Auto-tuning + high noise immunity

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

PSoC® 4000S-Series

PSoC 4 MCU Entry Line

Applications

Consumer devices (wearable, mobile, personal care) and small home appliances (coffee machine, juicer)

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - 32KB flash (maximum)
  - 4KB SRAM
  - Real-time clock capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 10-bit, 46.8-ksps single-slope ADC[1]
  - Two low-power comparators (CMPs)
  - One CapSense® block that supports low-power operation and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
- **Packages**
  - 25-ball WLCSP, 24-pin QFN, 32-pin QFN, 48-pin TQFP
- **I/O Subsystem**
  - Up to 36 GPIOs, including 16 Smart I/Os[2]

PSoC® 4 One-Chip Solution

Collateral

Datasheet: PSoC 4000S

Availability

Production: Now

[1] A simple ADC used to measure slow-moving signals
[2] Embedded programmable digital logic in the I/O subsystem

PSoC® 4100S-Series

PSoC 4 MCU Base Line

Applications

Home appliances (washing machine, dishwasher) and industrial applications

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 64KB flash
  - 8KB SRAM
  - Real-time clock capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps SAR ADC
  - One 10-bit, 46.8-ksps single-slope ADC[1]
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
- **Packages**
  - 35-ball WLCSP, 32-pin QFN, 40-pin QFN, 48-pin TQFP
- **I/O Subsystem**
  - Up to 36 GPIOs, including 16 Smart I/Os[2]

Collateral

Datasheet: PSoC 4100S

PSoC® 4 One-Chip Solution

Availability

Production: Now

[1] A simple ADC used to measure slow-moving signals [2] Embedded programmable digital logic in the I/O subsystem

PSoC® 4100S Plus-Series

PSoC 4 MCU Base Line

Applications

Main control and user interface for home appliance, consumer, and industrial applications

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Up to 128KB flash and 16KB SRAM
  - External MHz oscillator (ECO) with PLL and 32-kHz watch crystal oscillator (WCO)
  - True random number generator (TRNG)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps SAR ADC
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I^2C, SPI, or UART
  - Segment LCD
- **One Controller Area Network (CAN) Controller**
- **Packages**
  - 44-pin TQFP, 64-pin LQFP (0.5-mm and 0.8-mm pitch)
- **I/O Subsystem**
  - Up to 57 GPIOs, including 24 Smart I/Os[1]

Collateral

Datasheet: PSoC 4100S Plus

[1] Embedded programmable digital logic in the I/O subsystem

PSoC® 4 One-Chip Solution

Availability

Production: Now

PSoC® 4100PS-Series

PSoC 4 MCU Base Line

Applications

Consumer products and industrial applications

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Up to 32KB flash, 4KB SRAM, RTC capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit/1-Msps SAR ADC
  - One 10-bit/11.6-ksps single-slope ADC[1]
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), transimpedance amplifiers (TIAs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 13-bit voltage output digital-to-analog converters (VDACs)
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Eight 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
- **Packages**
  - 28-pin SSOP, 45-ball WLCSP, 48-pin QFN, 48-pin TQFP
- **I/O Subsystem**
  - Up to 38 GPIOs, including 8 Smart I/Os[2]

Collateral

Datasheet: PSoC 4100PS

PSoC® 4 One-Chip Solution

Availability

Production: Now

[1] A simple ADC used to measure slow-moving signals

[2] Embedded programmable digital logic in the I/O subsystem

PSoC® 4200DS-Series

PSoC 4 MCU Programmable Line

Applications

Main system control with programmable communications, subsystem control with programmable digital functions, digital sensor hub, low-end field oriented control (FOC) motor control, CPLD SoC, and any other embedded control without ADC/DAC

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller
  - Up to 64KB flash, 8KB SRAM
- **Programmable Analog Blocks**
  - Two low-power comparators (CMPs)
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): customized digital functions for flexible designs
  - Four 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
  - One Smart I/O[1] supporting programmable digital logic in the I/O subsystem that works even in deep sleep mode
- **Packages**
  - 25-pin WLCSP, 28-pin SSOP, 24-pin QFN
- **I/O Subsystem**
  - Up to 25 GPIOs

PSoC® 4 One-Chip Solution

Collateral

Datasheet: PSoC 4200DS

Availability

Production: Now

[1] Embedded programmable digital logic in the I/O subsystem

PSoC® 4A00-Series

PSoC 4 Analog Coprocessor

Applications

Industrial sensors (photoelectric sensors, displacement sensors), instrumentation and measurement (photometers, pH meters), and consumer products (wearables, grooming products)

Features

- **Programmable Analog Blocks**
  - One universal analog block (UAB) configurable as a programmable analog filter, 14-bit Delta-Sigma ADC, or 13-bit voltage-output DAC (VDAC)
  - Four opamps, configurable as programmable gain amplifiers (PGAs), comparators (CMPs), transimpedance amplifiers (TIA), etc.
  - One 12-bit/1-Msps SAR ADC
  - One 10-bit/11.6-ksps single-slope ADC[1]
  - 38-channel analog multiplexer (AMUX)
  - One CapSense® block configurable as a capacitive-sensing controller, two 7-bit current-output DACs (IDACs), or two low-power CMPs
- **Signal Processing Engine**
  - 48-MHz Arm® Cortex®-M0+ with a DMA controller and watch crystal oscillator (WCO)
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) configurable as I^2C, SPI, or UART
- **Packages**
  - 28-pin SSOP, 45-pin CSP, 48-pin QFN, 48-pin TQFP
- **I/O Subsystem**
  - Up to 38 GPIOs

Collateral

Datasheet: CY8C4Axx Datasheet

PSoC® Analog Coprocessor

Availability

Production: Now

[1] A simple ADC used to measure slow-moving signals

PSoC® 4500 (NDA)

PSoC 4 Motor Control Line

Applications

Motor control and power factor correction (PFC) control in white goods
Industrial servo motor control

Features

- **MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Motor control accelerator
  - Up to 128KB flash and 24KB SRAM
  - External crystal oscillator with phase-locked loop (PLL)
- **Analog Blocks**
  - Two 12-bit SAR ADCs (1-Msps)
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
- **Digital Blocks and Communication Interfaces**
  - Eight timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs)
- **Packages**
  - 48-TQFP, 64-TQFP (0.5-mm and 0.8-mm pitch)
- **I/O Subsystem**
  - Up to 54 GPIOs, including 16 Smart I/Os

PSoC® 4500

Collateral

Datasheet: Contact Sales

Availability

Sampling: Q1 2019 **Production**: Q2 2019

PSoC® 4100S Plus 256K (NDA)

PSoC 4 MCU Base Line

Applications

Main control and user interface for home appliance, consumer, and industrial applications

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Up to 256KB flash and 32KB SRAM
  - External MHz oscillator (ECO) with PLL and 32-kHz watch crystal oscillator (WCO)
  - True random number generator (TRNG)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps SAR ADC
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - Two CapSense® blocks
  - Two 7-bit current-output digital-to-analog converters (IDACs)
- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
  - Segment LCD
- **One Controller Area Network (CAN) Controller**
- **Packages**
  - 64-pin TQFP and 100-pin TQFP
- **I/O Subsystem**
  - Up to 84 GPIOs, including 24 Smart I/Os[1]

Collateral

Datasheet: Contact Sales

PSoC® 4100S Plus 256K

Availability

Sampling: Q1 2019 **Production**: Q2 2019

[1] Embedded programmable digital logic in the I/O subsystem

PSoC® 4100BLE-Series

PSoC 4 MCU Base Line with BLE

Applications

Sports and fitness monitors, wearable electronics, medical devices, home automation solutions, game controllers, and sensor-based low-power systems for the Internet of Things (IoT)

Features

- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU
  - Up to 256KB flash and 32KB SRAM
- **Programmable Analog Front Ends (AFEs)**
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
- **CapSense® with SmartSense™ Auto-Tuning**
  - Industry's No. 1 capacitive-sensing solution with one Capacitive Sigma-Delta™ (CSD) controller with touchpad capability
- **Programmable Digital Logic**
  - Four 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) configurable I^2C master or slave, SPI master or slave, or UART
- **Packages**
  - 56-pin QFN and 68-pin CSP
- **Bluetooth Connectivity with Bluetooth 4.1 or Bluetooth 4.2**[1]
  - Royalty-free stack and GUI-based Component to configure profiles, 2.4-GHz BLE radio with integrated balun

Collateral

Datasheet: PSoC 4 BLE (CY8C4XX7 BLE)

[1] Bluetooth 4.2 is only available in the 256KB flash option device

PSoC® 4 BLE One-Chip Solution

Availability

Production: Now

PSoC® 4200BLE-Series

PSoC 4 MCU Programmable Line with BLE

Applications

Sports and fitness monitors, wearable electronics, medical devices, home automation solutions, game controllers, and sensor-based low-power systems for the Internet of Things (IoT)

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU
  - Up to 256KB flash and 32KB SRAM
- **Programmable Analog Front Ends (AFEs)**
  - Four opamps, configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
- **CapSense® with SmartSense™ Auto-Tuning**
  - Industry's No. 1 capacitive-sensing solution including one Capacitive Sigma-Delta™ (CSD) controller with touchpad capability
- **Programmable Digital Logic**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Four configurable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) configurable as I^2C master or slave, SPI master or slave, or UART
- **Packages**
  - 56-pin QFN and 68-pin CSP
- **Bluetooth Connectivity with Bluetooth 4.1 or Bluetooth 4.2**[1]
  - Royalty-free stack and GUI-based Component to configure profiles, 2.4-GHz BLE radio with integrated balun

Collateral

Datasheet: PSoC 4 BLE (CY8C4XX7 BLE)

[1] Bluetooth 4.2 is only available in the 256KB flash option device

PSoC® 4 BLE One-Chip Solution

Availability

Production: Now

PSoC® 4100M-Series

PSoC 4 MCU Base Line

Applications

User interface and host processor for home appliances, digital and analog sensor hubs, MCU, and discrete analog replacement

Features

- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 128KB flash and 16KB SRAM
- **CapSense® with SmartSense™ Auto-Tuning**
  - Cypress Capacitive Sigma-Delta™ (CSD) controller
  - CapSense supported on up to 55 pins
- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps, programmed as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)
- **Programmable Digital Blocks**
  - Eight programmable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I^2C master or slave, SPI master or slave, or UART
- **Packages**
  - 48-pin LQFP, 64-pin TQFP (0.8-mm pitch), 64-pin TQFP (0.5-mm pitch), and 68-pin QFN

PSoC® 4 One-Chip Solution

Collateral

Datasheet: PSoC 4 M-Series (CY8C4100)

Availability

Production: Now

PSoC® 4200M-Series

PSoC 4 MCU Programmable Line

Applications

User interface and host processor for home appliances, digital and analog sensor hubs, LED control and communication for lighting systems

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 128KB flash and 16KB SRAM
- **CapSense® with SmartSense™ Auto-Tuning**
  - One Cypress capacitive Sigma-Delta™ (CSD) controller
  - CapSense supported on up to 55 pins
- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps, programmed as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Eight programmable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I^2C master or slave, SPI master or slave, or UART
- **Two Controller Area Network (CAN) Controllers**
- **Packages**
  - 48-pin LQFP, 64-pin TQFP (0.8-mm pitch), 64-pin TQFP (0.5-mm pitch), and 68-pin QFN

Collateral

Datasheet: PSoC 4 M-Series (CY8C4200)

PSoC® 4 One-Chip Solution

Availability

Production: Now

PSoC® 4200L-Series

PSoC 4 MCU Programmable Line

Applications

User interface and host processor for home appliances, digital and analog sensor hub, MCU and discrete analog replacement, and LED control and communication for lighting systems

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 256KB flash and 32KB SRAM
  - Up to 98 GPIOs supporting analog and digital interfaces
- **CapSense® With SmartSense™ Auto-Tuning**
  - Two Cypress Capacitive Sigma-Delta™ (CSD) controllers
- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)
- **Programmable Digital Blocks**
  - Eight universal digital blocks (UDBs): custom digital peripherals
  - Eight configurable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I^2C master or slave, SPI master or slave, or UART
- **Full-Speed USB 2.0 Controller and Transceiver**
- **Two Controller Area Network (CAN) Controllers**
- **Packages**
  - 48-pin TQFP, 64-pin TQFP, 68-pin QFN, and 124-pin VFBGA

Collateral

Datasheet: PSoC 4 L-Series

PSoC® 4 One-Chip Solution

Availability

Production: Now

PSoC® 63 Line with Bluetooth Low Energy (BLE)

Applications

Wearables, portable medical, industrial IoT, and smart home

Features

- **MCU Subsystem**
  - Dual-core architecture: 150-MHz Arm® Cortex®-M4 and 100-MHz Arm Cortex-M0+
  - Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 1MB Flash, 288KB SRAM with a DMA controller
- **Analog Blocks**
  - Two opamps, two low-power comparators (CMPs), 12-bit SAR ADC (1-Msps)
  - 12-bit DAC, CapSense® capacitive-sensing block
- **Digital Blocks and Communication Interfaces**
  - Twelve universal digital blocks (UDBs): custom digital peripherals
  - Twenty-four 16-bit and eight 32-bit timer/counter/pulse-width modulator (TCPWM) blocks[1]
  - Eight serial communication blocks (SCBs)[2], deep sleep SCB
  - I²S and PDM-PCM[3] converter, SMIF[4]
- **Bluetooth Smart Connectivity**
  - Bluetooth Low Energy (BLE) 5.0 radio with 2-Mbps data throughput
- **Security Features**
  - Advanced cryptographic coprocessor (Crypto), true random number generator
  - One-time programmable eFuse[5] for secure key storage
  - Secure over-the-air (OTA) firmware update with read-while-write flash technology for firmware updates
- **I/O Subsystem**: Up to 78 GPIOs
- **Packages**: 104-M-WLCSP, 116-BGA

Collateral

Preliminary Datasheet: PSoC 6 Product Page

Availability

Sampling: Now **Production**: Now

[1] Configurable as a 8-bit, 16-bit timer, or 32-bit counter or PWM
[2] Configurable as a UART, SPI or I²C interface
[3] Digital microphone interface
[4] Serial memory interface for execute-in-place, encrypted Quad-SPI
[5] One-time programmable bits for secure key storage
[6] Single-precision floating-point unit

PSoC® 62 Line

Applications

IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

Features

- **MCU Subsystem**
  - Dual-core architecture: 150-MHz Arm® Cortex®-M4 and 100-MHz Arm Cortex-M0+
  - Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 1MB flash, 288KB SRAM with a DMA controller
- **Analog Blocks**
  - Two opamps, two low-power comparators (CMPs), 12-bit SAR ADC (1-Msps)
  - 12-bit DAC, CapSense® capacitive-sensing block
- **Digital Blocks and Communication Interfaces**
  - Twelve universal digital blocks (UDBs): custom digital peripherals
  - Twenty-four 16-bit and eight 32-bit timer/counter/pulse-width modulator (TCPWM) blocks[1]
  - Eight serial communication blocks (SCBs)[2], deep-sleep SCB
  - I²S and PDM-PCM[3] converter, SMIF[4]
  - USB 2.0 (host and device)
- **Security Features**
  - Advanced cryptographic coprocessor (Crypto)
  - True random number generator
  - One-time programmable eFuse[5] for secure key storage
  - Secure over-the-air (OTA) firmware update with read-while-write flash technology for firmware updates
- **I/O Subsystem**: Up to 104 GPIOs
- **Packages**: 124-BGA, 80-WLCSP

Collateral

Preliminary Datasheet: PSoC 6 Product Page

[1] Configurable as a 8-bit, 16-bit timer, or 32-bit counter or PWM
[2] Configurable as a UART, SPI or I²C interface
[3] Digital microphone interface
[4] Serial memory interface for execute-in-place, encrypted Quad-SPI

Availability

Sampling: Now **Production**: Now

[5] One-time programmable bits for secure key storage
[6] Single-precision floating-point unit

PSoC® 60 Line

Applications

Wearables, portable medical, smart home, and general embedded control

Features

- **MCU Subsystem**
  - 120-MHz Arm® Cortex®-M4
  - Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 512KB flash, 128KB SRAM with a DMA controller
- **Analog Blocks**
  - Two low-power comparators (CMPs), 12-bit SAR ADC (1-Msps)
- **Digital Blocks and Communication Interfaces**
  - Ten 16-bit and two 32-bit timer/counter/pulse-width modulator (TCPWM) blocks[1]
  - Five serial communication blocks (SCBs)[2], deep sleep SCB
  - One Secure Digital High Capacity (SDHC), two controller area networks (CANs)
- **I/O Subsystem**: Up to 76 GPIOs
- **Packages**: 100-LQFP

Collateral

Preliminary Datasheet: PSoC 6 Community

Availability

Sampling: Now **Production**: Now

[1] Configurable as a 8-bit, 16-bit timer, or 32-bit counter or PWM
[2] Configurable as a UART, SPI or I²C interface
[3] Single-precision floating-point unit

S6E1C-Series

FM0+ MCU Portfolio

Applications

Industrial, healthcare, sensor hubs, wearable electronics, and mobile, battery-powered devices

Features

- **Ultra-Low-Power MCU Subsystem**
  - Up to 40-MHz Arm® Cortex®-M0+ CPU, 40-µA/MHz active current with 1.65–3.6-V operating voltage
  - Low-power 1.2-µA RTC operating current
  - Up to 128KB flash and 16KB SRAM
  - Near-zero wait-state flash access at up to 40 MHz
  - Fast 540-µs startup from power-on reset and 40 µs from standby
- **Analog and Digital Subsystems**
  - Two base timers, dual timer, CRC, and watch counter
  - Six channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, LIN, USB, and I²S
  - Two HDMI-CEC[1] channels
  - Two Smart Card interface channels
  - 12-bit, 1-Msps ADC with a 24-channel multiplexer input
- **Packages**
  - 32-pin LQFP, 48-pin LQFP, 64-pin LQFP, 32-pin QFN, 48-pin QFN, 26-pin CSP (2.35-mm x 2.72-mm)

Collateral

Datasheet: S6E1C1-Series, S6E1C3-Series

Availability

Production: Now

[1] HDMI consumer electronics control signal
[2] Low-voltage detect
[3] Descriptor system transfer controller
[4] Watchdog timer

S6E2C-Series

FM4 MCU Portfolio

Applications

Motor control, factory automation, industrial, Internet of Things (IoT), and building management systems and automation

Features

- **High-Performance MCU Subsystem**
  - 675 CoreMark®, 200-MHz Arm® Cortex®-M4 CPU, 365-µA/MHz active current with 2.7–5.5-V operating voltage
  - Ultra-low-power 1.0-µA RTC operating current
  - Up to 2MB flash and 256KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications
- **Analog and Digital Subsystems**
  - Three multifunction timers (MFTs), nine programmable pulse generators (PPGs), sixteen base timers, four quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Sixteen channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I^2C, or LIN
  - Two USB interfaces, two controller area network (CAN), CAN with flexible data rate (CAN-FD), IEEE 1588 Ethernet[1], high-speed Quad-SPI (HS-QSPI), I^2S, and external bus interfaces
  - Three 12-bit/2-Msps ADCs with a 32-channel multiplexer input
  - Two 12-bit DACs
  - Built-in Cryptographic Assist hardware coprocessor for encryption
- **Packages**
  - 144-pin LQFP, 176-pin LQFP, 216-pin LQFP, 192-pin BGA

Collateral

Datasheet: S6E2CC-Series

S6E2C-Series

MCU Subsystem

- arm Cortex®-M4 200 MHz
- Flash (1MB to 2MB)
- SRAM (128KB to 256KB)
- MPU[2]
- LVD
- DMA
- DSTC[3]
- Internal Main Oscillator
- Clock Supervisor
- Serial Wire/ JTAG Debug

Advanced High-Performance Bus (AHB)

Digital Subsystem

- MFT x3
- PPG x9
- Base Timer x16
- Dual Timer
- QPRC x4
- RTC
- Watch Counter
- WDT
- CRC
- MFS x16
- USB x2 (Host + Device)
- CAN x2
- CAN-FD
- IEEE 1588 Ethernet
- SD Card
- HS-QSPI
- I^2S
- External Bus Interface
- Crypto Assist

Analog Subsystem

- 12-bit ADC x3
- 12-bit DAC x2

I/O Subsystem

Pin Relocation

- GPIO x8
- GPIO x16
- GPIO x11
- GPIO x15
- GPIO x15
- GPIO x16
- GPIO x15
- GPIO x15
- GPIO x4
- GPIO x8
- GPIO x16
- GPIO x16
- GPIO x16
- GPIO x3
- GPIO x3
- GPIO x13

Availability

Production: Now

[1] Ethernet communications solution that supports the Precision Time Protocol (PTP) standard

[2] Memory protection unit

[3] Descriptor system transfer controller

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S6E2G-Series

FM4 MCU Portfolio

Applications

Motor control, factory automation, industrial, Internet of Things (IoT), and building management systems and automation

Features

- **High-Performance MCU Subsystem**
  - 608 CoreMark®, 180-MHz Arm® Cortex®-M4 CPU, 244-µA/MHz active current with 2.7–5.5-V operating voltage
  - Up to 1MB flash and 192KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications
- **Analog and Digital Subsystems**
  - Two multifunction timers (MFTs), nine programmable pulse generators (PPGs), sixteen base timers, two quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Ten channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I^2C, or LIN
  - Two USB interfaces, controller area network (CAN), IEEE 1588 Ethernet[1], I^2S, two SD Card interfaces, and an external bus interface
  - Three 12-bit/2-Msps ADCs with a 32-channel multiplexer input
  - Built-in Cryptographic Assist hardware coprocessor for encryption
- **Packages**
  - 144-pin LQFP and 176-pin LQFP

Collateral

Datasheet: S6E2G-Series

S6E2G-Series

Availability

Production: Now

[1] Ethernet communications solution that supports the Precision Time Protocol (PTP) standard

[2] Memory protection unit

[3] Descriptor system transfer controller

S6E2H-Series

FM4 MCU Portfolio

Applications

Motor control, factory automation, industrial, IoT, DSLR lens MCU and home appliance

Features

- **High-Performance MCU Subsystem**
  - 540 CoreMark®, 160-MHz Arm® Cortex®-M4 CPU, 188-µA/MHz active current with 2.7–5.5-V operating voltage
  - Ultra-low power 1.3-µA RTC operating current
  - Up to 512KB flash and 64KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications
- **Analog and Digital Subsystems**
  - Three multifunction timers (MFTs), nine programmable pulse generators (PPGs), eight base timers, three quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Eight channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I^2C, or LIN
  - Two controller area network (CAN), SD Card, and external bus interfaces
  - Three 12-bit/2-Msps ADCs with a 24-channel multiplexer input
  - Two 12-bit DACs
- **Packages**
  - 80-pin LQFP, 100-pin LQFP, 120-pin LQFP, 121-pin BGA

Collateral

Datasheet: S6E2H-Series

Availability

Production: Now

[1] Memory protection unit
[2] Descriptor system transfer controller

MCU Development Kits

	PSoC Prototyping Kits	Bluetooth Low Energy (BLE) Pioneer Development Kit	PSoC 5LP Development Kit	FM4 S6E2H-Series Pioneer Kit	PSoC6 WiFi-BT Pioneer Kit	PSoC 6 BLE Pioneer Kit
Kit Number	CY8CKIT-049 or CY8CKIT-059	CY8CKIT-042-BLE	DEV-13229	FM4-176L-S6E2CC-ETH	CY8CKIT-062-WiFi-BT	CY8CKIT-062-BLE
Key Features	Ultra-low-cost prototyping Breadboard-compatible Serial wire debug (SWD) or bootload for program/debug	Arduino form factor compatible Access to all PSoC 4 BLE I/Os Full SWD program and debug	Arduino form factor compatible Access to all PSoC 5LP I/Os Full SWD program and debug	Arduino form factor compatible Full SWD program and debug	Arduino form factor compatible Full SWD program and debug	Arduino form factor compatible Full SWD program and debug
Price	$4–$10	$49	$55	$49	$99	$75

Learn more or buy a kit today at www.cypress.com/kits

MCU Packages

Package	LQFP	PDIP			QFN							SOIC			
Pins	48	8	20	28	16	24	32	40	48	56	68	8	16	20	28
PSoC 1		✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓
PSoC 3									✓		✓				
PSoC 4	✓				✓	✓	✓	✓	✓	✓	✓	✓	✓		
PSoC 5LP											✓				
CapSense					✓	✓	✓		✓			✓	✓		

Package	SSOP							TQFP				WLCSP			
Pins	8	16	20	24	28	32	48	44	48	64	100	25	30	32	35
PSoC 1	✓	✓	✓	✓	✓	✓	✓	✓			✓				
PSoC 3							✓				✓				
PSoC 4					✓			✓	✓	✓		✓		✓	✓
PSoC 5LP											✓				
CapSense			✓				✓						✓		

Package	WLCSP			Multi-Die WLCSP (M-WLCSP)	µBGA	
Pins	68	72	99	104	116	124
PSoC 1			✓			
PSoC 3		✓				
PSoC 4	✓					✓
PSoC 5LP						
PSoC 6				✓	✓	✓
CapSense						

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Additional MCU Packages

Package	SSOP				TSSOP			SDIP	QFN			LQFP			
Pins	8	16	20	24	16	20	24	32	32	48	64	32	48	52	64
8FX	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓
FM0+					✓				✓	✓		✓	✓	✓	✓
FM3									✓	✓		✓	✓	✓	✓
FM4										✓	✓		✓		✓

Package	LQFP						QFP	TQFP	BGA					WLCSP	
Pins	80	100	120	144	176	216	100	120	96	112	121	161	192	26	80
8FX	✓														
FM0+	✓	✓	✓						✓					✓	✓
FM3	✓	✓	✓	✓	✓				✓	✓			✓		
FM4	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓		

USB Portfolio

USB Portfolio

	Device	Hub	Bridge	Storage	Type-C
USB 3.1	**CYUSB301x** **FX3** 32-Bit Bus to USB 3.1 Gen 1 ARM9, 512KB RAM	**CYUSB33xx** **HX3** USB 3.1 Gen 1, Shared Link™[1] BC 1.2[2], Ghost Charge™[3]	**CYUSB306x** **CX3** CSI-2[4] to USB 3.1 Gen 1 4 CSI-2[4] Lanes, 1 Gbps/Lane	**CYUSB303x** **FX3S** 16-Bit Bus to USB 3.1 Gen 1 RAID[5], Dual SDXC[6]/eMMC[7]	**CYPD1xxx** **CCG1** USB Type-C Port Controller 1 PD Port, 5 Profiles, 100 W
	FX3Gen2 USB 3.1 Gen 2 Peripheral Controller **Contact Sales**	**CYUSB333x** **HX3C** 4 Ports: 1 Type-C, 3 Type-A USB PD, Billboard, BC1.2[2]	**CYUSB361x** **GX3** USB 3.1 Gen 1 to GigE Energy Efficient Ethernet	**CYUSB302x** **SD3** USB 3.1 Gen 1 SD Reader SDXC[6]/eMMC[7], RAID[5]	**CYPD2xxx** **CCG2** USB Type-C Cable Controller 1 PD Port, Termination, ESD
		NEW **CYUSB43xx** Q119 **HX3PD** USB 3.1 Gen 2 Type-C Hub 7 Ports, PD, Billboard, 10 Gbps			**CYPD3xxx** **CCG3** USB Type-C Port Controller 20-V, Crypto, Billboard
USB 2.0	**CY7C6801x/53** **FX2LP** 16-Bit Bus to USB 2.0 8051, 16KB RAM	**CY7C656x4** **HX2VL** 4 Ports 4 Transaction Translators	**CY7C6803x/3xx** **NX2LP/AT2LP** NAND Flash/PATA to USB 2.0 8051	**CYWB0x2xABS** **Arroyo™, Astoria™** 16-Bit Bus to USB 2.0 8051, Dual SD/eMMC[7]	**CYPD4xxx** **CCG4/CCG4M** USB Type-C Port Controller 2 PD Ports,128KB Flash, Mux
	CYUSB201x **FX2G2** 32-Bit Bus to USB 2.0 ARM9 512KB RAM	**CY7C656x1** **HX2LP** 4 Ports, Industrial Grade 1 Transaction Translator		**CYWB016xBB** **Bay™** HS USB OTG Dual SDXC[6]/eMMC[7]	**CYPD5xxx** **CCG5/CCG5C** USB Type-C Port Controller 2 PD Ports, V_{BUS} short protection
					NEW **CYPD612x** Q119 **CCG6** USB Type-C Port Controller 1 PD Port, Load S/W Cntrl, TBT
USB 1.1	**CY7C638xx/64215/643xx** **enCoRe™ II/III/V** M8C MCU, GPIOs SPI, Flash		**CY7C6521x** **USB-Serial** UART/SPI/I²C to USB 2 Channels, CapSense®	**SL811HS** FS USB Host/Device 256Byte RAM	NEW **CYPD612x** Q119 **CCG6F** USB Type-C Port Controller **Contact Sales**
	CY7C65210/7 **USB Billboard** ARM Cortex M0 1 or 2 UART/SPI/I²C channels		**CY7C65213** **USB-to-UART (Gen 2)** 3 Mbps, 8 GPIOs	**CY7C67300/200** **EZ-Host/EZ-OTG™** 4/2 Ports, FS USB OTG GPIOs	

Type-C

CYPD317x **CCG3PA** USB Type-C Port Controller 30V, PPS, QC4, 64KB Flash	
CYPDC118x **CCG3PA2** USB Type-C Port Controller 30V, PPS, QC4, 128KB Flash	
NEW **CYPD27xx** Q418 **CMG1** USB Type-C EMCA Controller PD 3.0, V_{BUS} short protection	
NEW **CYPAS1xx** Q119 **PAG1S** Secondary-side Controller **Contact Sales**	
NEW **CYPAP1xx** Q219 **PAG1P** Primary-side Start-up Controller **Contact Sales**	
CYAC1xxx **ACG1F** USB Type-C Port Controller **Contact Sales**	

Type-C products apply to any USB speed

[1] Simultaneous USB 2.0 and SuperSpeed traffic on the same port
[2] Battery Charging specification v1.2
[3] Enables USB charging without host connection
[4] Camera Serial Interface v2.0
[5] Redundant array of independent disks
[6] SD extended capacity
[7] Embedded Multimedia Card

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

EZ-PD CMG1

USB Type-C Passive EMCA Controller

Applications

USB-C EMCA

Features

- USB-C PD Controller, PD 3.0 Transceiver
- V_{BUS}-to-CC Short Protection
- V_{BUS}-to-V_{CONN} Short Protection
- Power from V_{CONN} range 3.0 to 5.5-V
- Termination Resistor R_A
- Supports R_A Weakening to Reduce Power Consumption
- Configurable 32-byte Storage for Configuration Over Type-C Interface
- Integrated oscillator eliminating the need for external clock
- Power Operation
  - 2.7-V to 5.5-V operation (V_{CONN} pin)
  - Active: 7.5 mA
  - Sleep: 1 mA
- System-Level ESD on CC, V_{CONN} Pins
  - ±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C
- Packages
  - 9-ball WLCSP (1.95 mm^2)
  - Supports industrial temperature range (-40°C to +85°C)

CMG1: USB Type-C Passive EMCA Controller

Collateral

Preliminary Datasheet: CMG1 Datasheet

Availability

Samples: Now **Production:** Q4 2018

CCG6

Single-Port USB Type-C and PD Port Controller

Applications

Thunderbolt / non- Thunderbolt Desktop, Notebook

Features

- **Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode and USB platforms**
- **V_{BUS} to CC/SBU short protection**
- **Integrated high-voltage 20V-regulator to power CCG6**
- **Integrated Analog Blocks**
  2x1 SBU analog mux, 2x2 USB analog mux
  Configurable V_{BUS} over-voltage protection and over-current protection
  High-side current sense[3] amplifier across 5mohms
  Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- **Integrated Digital Blocks**
  Two timers, counters and pulse-width modulators, 17x GPIOs
  Four SCBs[1] for configurable master/slave I2C, SPI or UART
- **ARM® Cortex®-M0 with MCU Subsystem and 128KB flash**
- **Power System**
  High-voltage (4 - 21.5 V, 26 V Max) V_{BUS} voltage inputs
  2x V_{CONN} FETs supporting up to 500 mA, Supports Dead Battery mode operation
- Integrated PFET gate drivers and Slew Rate Control
- VBUS Over Voltage Protection and Reverse Current Protection on provider path
- **Packages**
  96 BGA (6x6 mm)

Collateral

Preliminary Datasheet: Contact Sales

Availability

Sampling: Now Production: Q1 2019

[1] Serial communication block configurable as UART, SPI or I²C
[2] Analog feedback control circuit to regulate V_{BUS}
[3] Circuit to measure the current flowing on the V_{BUS}
[4] Timer/counter/pulse-width modulator block
[5] Termination resistors: R_P read as a DFP, R_D as a UFP

EZ-USB HX3PD

USB 3.1 Gen 2 Type-C Hub with Power Delivery

Applications

Notebook/tablet docking stations, monitor docks, multi-function USB Type-C peripherals

Features

- **USB 3.1 Gen 2-Compliant Hub Controller with Type-C and PD**
- **Upstream (US) ports:**
  - 10 Gbps; Type-A or Type-C plus PD (UFP)
- **Downstream (DS) ports:**
  - 7 ports: 5x 10 Gbps, 2x 480 Mbps
  - 3 Type-C ports: 1 PD port (DFP), 2 Type-C only
- **Integrated Type-C Transceivers and Dual-PHY for Type-C plug orientation correction**
  - Integrated termination resistors (R_P and R_D)[1]
  - Integrated USB Billboard Controller[2], USB Type-C Bridge Controller
  - Integrated V_{CONN} FETs and ADC for overvoltage and overcurrent protection
- **Charging Support**
  - USB PD, BC v1.2, Apple Charging Standard, QC 4.0, Samsung AFC
  - USB PD policy engine configures power profiles dynamically
- **Ghost Charge™:** Charging DS without US connection
- **Dock Management Controller for secured firmware download**
  - Firmware upgradable over USB
- **System-Level ESD on Configuration Channel (CC) Pins:** 8 kV Contact, 15 kV Air
- **Package:** 192-ball BGA (12 mm x 12 mm x 1 mm, 0.8-mm ball-pitch)

Collateral

Datasheet: HX3PD Datasheet
Kit: HX3PD Evaluation Kit

HX3PD: USB 3.1 Gen 1 Type-C PD Hub

Availability

Samples: Now **Production:** Q1 2019

[1] Termination resistors: R_P read as a DFP, R_D as a UFP [2] A USB Device controller that is used to implement the USB Billboard Device Class Informs the USB Host of the supported Alternate Modes as well as any failures [3] Transaction Translator

EZ-PD CCG2

USB Type-C and PD Port Controller

Applications

USB Type-C Electronically Marked Cabled Assembly (EMCA) and powered accessories

Features

- **32-bit MCU Subsystem**
  - 48-MHz ARM® Cortex® -M0 CPU with 32KB Flash and 4KB SRAM
- **Integrated Digital Blocks**
  - Integrated timer/counter/pulse-width modulators (TCPWMs)
  - Two SCBs[1] configurable to I²C, SPI or UART modes
- **Type-C Support**
  - Integrated transceiver, supporting one Type-C port
  - Integrated termination resistors (R_P, R_D, R_A)[2]
- **Power Delivery (PD) Support**
  - Standard power profiles
- **Low-Power Operation**
  - Two independent V_{CONN} rails with integrated isolation
  - Independent supply voltage pin for GPIO
  - 2.7–5.5-V operation; Sleep: 2.0 mA; Deep Sleep: 2.5 µA
- **System-Level ESD on CC and VDD Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 20-ball CSP (3.3 mm²) with 0.4-mm ball pitch, 14-pin DFN (2.5 x 3.5 mm) with 0.6-mm pin pitch and 24-pin QFN (4 mm²) with 0.55-mm pin pitch

Collateral

Datasheet: CCG2 Datasheet
Reference Design Kit: CCG2 RDK
Evaluation Kit: CCG3 EVK

CCG2: USB Type-C Port Controller With PD

Availability

Production: Now

[1] Serial communication block configurable as UART, SPI or I²C
[2] Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA

EZ-PD CCG3

USB Type-C and PD Port Controller

Applications

Accessories and power adapters

Features

- **One Type-C Port with Integrated Transceiver**
  - Alternate Modes[1], Crypto Engine[2] for USB Authentication[3]
- **Power Delivery (PD) Support for Standard Power Profiles**
- **Integrated Digital Blocks for V_{BUS} Power and MUX Interface**
  - 4 timers/counters/pulse-width modulators (TCPWM), 24x GPIOs
  - 4 serial communication blocks (SCBs) configurable as master/slave I²C, SPI or UART
  - USB Billboard Controller[4] with Billboard Device Class[5] support
- **Integrated Analog Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)**
  - 21.5-V OVP and OCP; 2:2 cross-bar switch
- **32-bit ARM® Cortex®-M0 CPU with MCU Subsystem**
  - 2x64KB Flash for fail-safe updates over CC, I²C or USB interfaces
- **Low-Power Operation**
  - 2x V_{BUS} Gate Drivers[6], for consumer and provider power paths
  - 2x high-voltage (5–21.5 V, 25 V, maximum) V_{BUS} voltage inputs
  - Sleep: 2.0 mA; Deep Sleep: 2.5 µA with wake-on-I²C or wake-on-CC
- **System-Level ESD on CC/V_{CONN}, V_{BUS}, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 42-ball (8.38 mm²) CSP, 40-pin (36 mm²) QFN and 32-pin (25 mm²) QFN

Collateral

Datasheet: CCG3 Datasheet

CCG3: USB Type-C Port Controller

Availability

Production: Now

[1] Mode of operation in which the data lines are repurposed to transmit non-USB data
[2] The encryption hardware and software required to implement USB Authentication
[3] A USB-IF specification that defines the authentication protocol for Type-C accessories
[4] A USB Device controller that informs the USB Host of the supported Alternate Modes
[5] A specification that defines the method for a USB Device to communicate the supported Alternate Modes
[6] Circuits to control the gates of external power Field-Effect Transistors (FETs) on V_{BUS} (5-20 V)
[7] Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA

EZ-PD CCG4/4M

Dual-Port USB Type-C and PD Port Controller

Applications

Notebooks, tablets, monitors, docking stations

Features

- **Integrated USB Type-C Transceivers Support Two Type-C Ports**
  - Integrated 2x 1-W V_{CONN} FETs and 2x FET control signals, per port programmable R_P[1] and removable R_P, and R_D[2] terminations
  - Supports dead battery mode operation
  - Integrated SuperSpeed USB/DisplayPort (DP) Mux (CCG4M)
- **Increased Flash Enables Fail-Safe Bootup**
  - Integrates 128KB Flash to store dual FW images for fail-safe boot
- **Integrated Digital Blocks for Inter-Chip Communications**
  - Four serial communication blocks (SCBs) master or slave configurable to I^2C, SPI or UART
  - SCBs interconnect CCG4 with embedded controller, two alternate muxes and Thunderbolt controller (optional)
- **Integrated Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)**
  - Four 8-bit SAR ADCs configurable for OVP and OCP
- **Low-Power Operation**
  - 2.7–V to 5.5-V operation and independent supply voltage for GPIO; Sleep: 2.0 mA; Deep Sleep: 2.5 µA with wake-on-I^2C or wake-on-configuration channel (CC)
- **System-Level ESD on CC Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **32-bit ARM® Cortex®-M0 CPU with MCU Subsystem**
  - 128KB Flash, upgradable over CC lines or I^2C interface
- **Packages**
  - 40-pin QFN, 96-ball BGA (CCG4M)

Collateral

Datasheet: CCG4 Datasheet

CCG4/4M: USB Type-C Port Controller

Availability

Production: Now

[1] Termination resistor read as a DFP
[2] Termination resistor read as a UFP

EZ-PD CCG3PA

USB Type-C and PD Port Controller

Applications

Power adapters, chargers, power banks

Features

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power CCG3PA
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART
- **Integrated Analog**
  - Configurable V_{BUS} overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier[1] with analog out for V_{BUS} control
  - Low side current sense[2] capable of detecting 100mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC[3])
- **32-bit ARM® Cortex®-M0 CPU with 64KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) V_{BUS} voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC
- **System-Level ESD on CC / V_{CONN}, V_{BUS}, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 24-QFN (16 mm²), 16-SOIC (60 mm²)

CCG3PA: USB Type-C Port Controller

Collateral

Datasheet: Contact Sales

Availability

Production: Now

[1] Analog feedback voltage control circuit to control V_{BUS}
[2] Circuit to measure the current flowing on the V_{BUS}
[3] Adaptive Fast Charging
[4] Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA

EZ-PD CCG3PA2

USB Type-C and PD Port Controller

Applications

Power adapters, chargers, power banks

Features

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART
- **Integrated Analog**
  - Configurable V_{BUS} overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier[1] with analog out for V_{BUS} control
  - Low side current sense[2] capable of detecting 100mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC[3])
- **32-bit ARM® Cortex®-M0 CPU with 128KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) V_{BUS} voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC
- **System-Level ESD on CC / V_{CONN}, V_{BUS}, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 32-QFN (25 mm²), 30-ball CSP (7.5 mm²)

CCG3PA2: USB Type-C Port Controller

Collateral

Datasheet: Contact Sales

Availability

Production: Now

[1] Analog feedback voltage control circuit to control V_{BUS}
[2] Circuit to measure the current flowing on the V_{BUS}
[3] Adaptive Fast Charging
[4] Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA

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EZ-PD CCG3PA2

USB Type-C and PD Port Controller

Applications

Power adapters, chargers, power banks

Features

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power CCG3PA
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I^2C, SPI or UART
- **Integrated Analog**
  - Configurable V_{BUS} overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier[1] with analog out for V_{BUS} control
  - Low side current sense[2] capable of detecting 100mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC[3])
- **32-bit ARM® Cortex®-M0 CPU with 64KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) V_{BUS} voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I^2C or CC
- **System-Level ESD on CC / V_{CONN}, V_{BUS}, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 32-QFN (25 mm^2), 30-ball CSP (7.5 mm^2)

CCG3PA: USB Type-C Port Controller

Collateral

Datasheet: Contact Sales

Availability

Production: Now

[1] Analog feedback voltage control circuit to control V_{BUS}
[2] Circuit to measure the current flowing on the V_{BUS}
[3] Adaptive Fast Charging
[4] Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA

EZ-PD CCG5

Dual-Port USB Type-C and PD Port Controller

Applications

Notebooks, docks, Thunderbolt devices

Features

- **Integrated Type-C Transceiver for Two Type-C USB PD 3.0-Compliant Ports**
  - Support for Thunderbolt, DisplayPort (DP), HDMI Alt Mode and USB platforms
  - USCI[1]-compliant Interface with WHQL[2]-certified driver
  - Support for UEFI[3] driver with Microsoft capsule firmware download
- **Integrated Analog**
  - Integrated high-voltage LDO and 4x V_{CONN} FETs supporting up to 500 mA
  - Integrated 2x2 USB analog switch; integrated SBU analog pass with high-voltage tolerance
  - Integrated 2x USB Charger Detect (BC 1.2, Apple Charging, QC 4.0 and Samsung AFC[4])
  - Integrated Type-C termination resistors (R_P, R_D R_{DB})[5]
  - 25-V tolerance on CC1/2 and SBU pins
- **ARM® Cortex®-M0 CPU with 128KB Flash and 12KB SRAM**
  - 4x serial communication blocks (SCB) - I²C, SPI or UART
  - Firmware upgradable over SWD/I²C interfaces
  - Supports Dead Battery mode operation
  - Overvoltage protection (OVP) with 2µs response time; integrated V_{BUS}/V_{CONN} overcurrent protection (OCP)
- **System-Level ESD on CC/V_{CONN}, V_{BUS}, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Discharge IEC61000-4-2 Level 4C
- **Packages**
  - 2-Port in 96-BGA (6 mm²), 1-Port in 40-QFN (6 mm²)

Collateral

Datasheet: Contact Sales

CCG5: USB Type-C Port Controller

Availability

Production: Now

[1] USB Type-C Connector System Software Interface
[2] Windows Hardware Quality Labs
[3] Unified Extensible Firmware Interface
[4] Adaptive Fast Charging
[5] Termination resistors: R_P read as a DFP, R_D as a UFP, R_{DB} as UFP in Dead-Battery scenario

EZ-USB FX3

USB 3.1 Gen 1 Peripheral Controller

Applications

Industrial cameras, medical and machine vision cameras, 3-D and 1080p full HD and 4K Ultra HD (UHD) cameras. document and fingerprint scanners, videoconferencing and data acquisition systems, video capture cards and HDMI converters, protocol and logic analyzers, USB test tools and software-designed radios (SDRs)

Features

- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz ARM® 926EJ Core**
  - 512KB of embedded SRAM for code space and buffers
- **32-bit, 100-MHz, flexible GPIF II Interface**
  - Other peripheral interfaces such as I^2C, I^2S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- **Flexible Clock Options**
- **Packages**
  - 121-ball BGA (10 mm^2), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral

Datasheet: FX3 Datasheet
Development Kit: FX3 SuperSpeed Explorer Kit
Software Development Kit: EZ-USB FX3 SDK

FX3: USB 3.1 Gen 1 Peripheral Controller

Availability

Production: Now

EZ-USB FX3S

USB 3.1 Gen 1 RAID[1]-on-Chip

Applications

Servers, routers, mobile storage, USB Flash drives, POS terminals, automatic teller machines (ATM), SDIO expanders and data logging devices

Features

- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz ARM® 926EJ Core**
  - 512KB of embedded SRAM for code space and buffers
- **32-bit, 100-MHz, Flexible GPIF II Interface**
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
- **Two SDXC[2], eMMC[3] 4,4, or SDIO 3.0 Interfaces**
  - Support RAID0 or RAID1 configurations
- **Flexible Clock Options**
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- **Packages**
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral

Datasheet: FX3S Datasheet
Kit: FX3S RAID[1]-on-Chip Boot Disk Kit
Software Development Kit: EZ-USB FX3 SDK

FX3S: RAID[1]-on-Chip

Availability

Production: Now

[1] Redundant array of independent disks
[2] SD extended capacity
[3] Embedded Multimedia Card

EZ-USB CX3

MIPI[1] CSI-2 to USB 3.1 Gen 1 Bridge

Applications

Industrial, medical and machine vision cameras, 1080p full HD and 4K Ultra HD (UHD) cameras, document scanners, fingerprint scanners, game consoles, videoconferencing systems, notebook PCs, tablets and image acquisition systems

Features

- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz ARM® 926EJ core**
  - 512KB of embedded SRAM for code space and buffers
- **Four-Lane MIPI[1] Camera Serial Interface v2.0 (CSI-2) Input**
  - Camera Control Interface (CCI) for image sensor configuration
  - Other peripheral interfaces such as I²C, UART, SPI and 12 GPIOs
- **Supports Industry-Standard Video Data Formats**
  - RAW8/10/12/14[2], YUV422/444[3], RGB888/666/565[4]
- **Supports Uncompressed Streaming Video**
  - 4K UHD at 15 fps, 1080p at 30 fps, 720p at 60 fps
- **Packages**
  - 121-ball BGA (10 x 10 x 1.7 mm)

Collateral

Datasheet: CX3 Datasheet
Reference Design Kit: CX3 Reference Design Kit
Software Development Kit: EZ-USB FX3 SDK

[1] Mobile Industry Processor Interface
[2] Video format for raw video data
[3] Video format for luminance and chrominance components
[4] Video format for red, green and blue pixel components

CX3: MIPI[1] CSI-2 to USB 3.1 Gen 1 Bridge

Availability

Production: Now

EZ-USB GX3

USB 3.1 Gen 1 to GigE[1] Bridge

Applications

USB dongles, docking stations and port replicators, network printers and security cameras, ultrabooks and home gateways, game consoles and portable media players, DVRs, IP set-top boxes and IP TVs and other embedded systems

Features

- **One-Chip USB 3.1 Gen 1 to 10/100/1000M GigE Bridge**
  - Integrates USB 3.1 Gen 1 PHY and GigE PHY
  - Integrates USB 3.1 Gen 1 Controller and GigE MAC[2]
  - Needs only a 25-MHz crystal to drive both USB and GigE1 PHY
- **IEEE 802.3az[3] Support for Low-Power Idle State**
  - Supports dynamic cable length and power adjustment
  - Offers multiple power management wake-on-LAN[4] features
- **Supports Optional EEPROM to Store USB Descriptors**
  - Integrates on-chip power-on-reset (POR) circuitry
- **Packages**
  - 68-QFN (8 x 8 x 0.85 mm)

Collateral

Datasheet: GX3 Datasheet
Reference Design Kit: GX3 Reference Design Kit
Software & Drivers: GX3 Drivers

GX3: USB 3.1 Gen 1 to GigE[1] Bridge

Availability

Production: Now

[1] Gigabit Ethernet
[2] Media access controller that provides the address to an Ethernet node
[3] A new-energy efficient Ethernet standard
[4] An Ethernet standard that allows a computer to be turned on by a network message

EZ-USB HX3

USB 3.1 Gen 1 Hub

Applications

Docking stations for notebook PCs and tablets, PC motherboards , servers, televisions and monitors, retail hub boxes, printers and scanners, set-top boxes, home gateways, routers and game consoles

Features

- **USB 3.1 Gen 1-Compliant Four-Port Hub Controller**
  - USB-IF certified (Test ID: 330000047)
  - WHQL certified for Windows 7, Window 8, Windows 8.1
- **Shared Link™**
  - Supports simultaneous USB 2.0 and USB SuperSpeed (SS) devices on the same port
- **Ghost Charge™**
  - Enables USB charging while the hub is disconnected from a USB Host
- **Charging Standard support**
  - USB-IF Battery Charging (BC) v1.2, Apple Charging Standard
  - Charging an OTG Host in an ACA-Dock
- **Programming of External EEPROM via USB**
- **Configurable USB SS and USB 2.0 PHY (drives 11" trace)**
- **Packages**
  - 68-QFN (8 x 8 x 1.0 mm), 88-QFN (10 x 10 x 1.0 mm), 100-BGA (6 x 6 x 1.0 mm)

Collateral

Datasheet:	HX3 Datasheet
Kit:	CY4609, CY4603, CY4613
Configuration Utility:	Blaster Plus[1]
App Notes:	HX3 Hardware Design Guide (AN91378)

[1] A Cypress GUI-based PC application for setting HX3 configuration parameters [2] Transaction translator

HX3: USB 3.1 Gen 1 Hub

Availability

Production: Now

EZ-USB HX3C

USB 3.1 Gen 1 Type-C PD Hub

Applications

USB Type-C charging hubs, adapters and accessories, docking stations for notebook PCs and tablets, televisions and monitors, PC motherboards and servers, set-top boxes, home gateways and routers

Features

- **USB 3.1 Gen 1-Compliant Hub Controller with Type-C and PD**
  - Upstream (US): Type-C, Downstream (DS): 1 Type-C and 2 Type-A ports
- **Integrated Type-C Transceivers, Supporting Two Type-C Ports**
  - Integrated termination resistors (R_P and R_D)[1]
  - Integrated USB Billboard Controller[2]
- **Charging Support**
  - USB PD, BC v1.2, Apple Charging Standard
  - PD policy engine configures power profiles dynamically
- **Ghost Charge™**
  - Charging DS without US connection
- **Firmware Upgradable Over USB**
- **System-Level ESD on Configuration Channel (CC) Pins**
  - 8 kV Contact, 15 kV Air
- **Configurable USB SS and USB 2.0 PHY (drives 11" trace)**
- **Packages**
  - 121-ball BGA (10 mm x 100 mm, 0.8 mm ball-pitch)

Collateral

Datasheet: HX3C Datasheet
Reference Design: HX3C Type-C Monitor/Dock Reference Design

HX3C: USB 3.1 Gen 1 Type-C PD Hub

Availability

Production: Now

[5] Termination resistors: R_P read as a DFP, R_D as a UFP

[2] A USB Device controller that is used to implement the USB Billboard Device Class Informs the USB Host of the supported Alternate Modes as well as any failures

[3] Transaction Translator

Cypress Roadmap: RAM Solutions (NDA)

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Nonvolatile RAM

F-RAM, nvSRAM

F-RAM™ Portfolio

Low Power | High Endurance

	LPC[1] F-RAM			Processor Companion	Parallel F-RAM	
512Kb–4Mb	**FM25V20A** **2Mb**; 2.0–3.6 V 40-MHz SPI; Ind[2]	**CY15B104Q** **4Mb;** 2.0–3.6 V 40-MHz SPI; Ind	**Excelon[3] F-RAM** **Up to 16Mb** **1.8V, 108-MHz QSPI[4]**		**FM22L16/LD16** **4Mb**; 2.7–3.6 V 55 ns; x8; Ind	
	CY15B102Q **2Mb;** 2.0–3.6 V 25-MHz SPI; Auto E[5]	**FM25V10/VN10** **1Mb**; 2.0–3.6 V 40-MHz SPI; Ind, Auto A[6]	**FM24V10/VN10** **1Mb**; 2.0–3.6 V 3.4-MHz I²C; Ind, Auto A		**FM28V102A** **1Mb;** 2.0–3.6 V 60 ns; x16; Ind	**FM28V202A** **2Mb;** 2.0–3.6 V 60 ns; x16; Ind
	FM25V05 **512Kb**; 2.0–3.6 V 40-MHz SPI; Ind, Auto A		**FM24V05** **512Kb**; 2.0–3.6 V 3.4-MHz I²C; Ind, Auto A		**CY15B101N** **1Mb;** 2.0–3.6 V 60 ns; x16; Auto A	**CY15B102N** **2Mb;** 2.0–3.6 V 60 ns; x16; Auto A
4Kb–256Kb	**FM25V02A/W256** **256Kb**; V02A: 2.0–3.6 V W256: 2.7–5.5 V 40-MHz SPI; Ind, Auto A		**FM24V02A/W256** **256Kb**; V02A: 2.0–3.6 V W256: 2.7–5.5 V 3.4-MHz I²C; Ind, Auto A	**FM33256** **256Kb**; 3.3V; 16-MHz SPI Ind; RTC[7]; Power Fail Watchdog; Counter	**FM28V020** **256Kb**; 2.0–3.6 V 70 ns; x8; Ind	**FM18W08** **256Kb**; 2.7–5.5 V 70 ns; x8; Ind
	FM25V01A **128Kb**; 2.0–3.6 V 40-MHz SPI; Ind, Auto A		**FM24V01A** **128Kb**; 2.0–3.6 V 3.4-MHz I²C; Ind, Auto A	**FM31256/31(L)278** **256Kb**; 3.3, 5.0V; 1-MHz I²C; Ind; RTC; Power Fail; Watchdog; Counter	**FM1808B** **256Kb**; 5.0 V 70 ns; x8; Ind	**FM16W08** **64Kb**; 2.7–5.5 V 70 ns; x8; Ind
	FM25640/CL64 **64Kb**; 3.3, 5.0 V 20-MHz SPI; Ind, Auto E		**FM24C64/CL64** **64Kb**; 3.3, 5.0 V 1-MHz I²C; Ind, Auto E	**FM3164/31(L)276** **64Kb**; 3.3, 5.0 V; 1-MHz I²C; Ind; RTC; Power Fail; Watchdog; Counter		
	FM25C160/L16 **16Kb**; 3.3, 5.0 V 20-MHz SPI; Ind, Auto E		**FM24C16/CL16** **16Kb**; 3.3, 5.0 V 1-MHz I²C; Ind, Auto A			
	FM25040/L04 **4Kb**; 3.3, 5.0 V 20-MHz SPI; Ind, Auto E		**FM24C04/CL04** **4Kb**; 3.3, 5.0 V 1-MHz I²C; Ind, Auto A			

[1] Low-pin-count
[2] Industrial grade -40°C to +85°C
[3] Ultra-Low-Energy
[4] Quad serial peripheral interface
[5] AEC-Q100 -40°C to +85°C
[6] AEC-Q100 -40°C to +125°C
[7] Real-time clock

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

nvSRAM Portfolio

High Density | High Speed

	Parallel nvSRAM				LPC[1] nvSRAM		
512Kb–16Mb	**CY14B116R/S** **16Mb**; 3.0 V 25, 45 ns; x32; Ind[2] RTC[3]	**CY14B116K/L** **16Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V116F/G** **16Mb**; 3.0, 1.8 V I/O 30 ns; ONFI[4] 1.0 x8, x16; Ind				
	CY14B104NA **4Mb**; 3.0 V 25, 45 ns; x16 Auto E[6]; RTC	**CY14B108K/L** **8Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14B108M/N** **8Mb**; 3.0 V 25, 45 ns; x16; Ind RTC	**CY14B116M/N** **16Mb**; 3.0 V 25, 45 ns; x16; Ind RTC			
	CY14B104K/LA **4Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V104LA** **4Mb**; 3.0, 1.8 V I/O 25, 45 ns; x8; Ind	**CY14B104M/NA** **4Mb**; 3.0 V 25, 45 ns; x16; Ind RTC	**CY14V104NA** **4Mb**; 3.0, 1.8 V I/O 25, 45 ns; x16; Ind	**CY14V101PS** **1Mb;** 3.0, 1.8 V I/O 108-MHz QSPI; Ind Ext. Ind[8]; RTC	**CY14V101QS** **1Mb;** 3.0, 1.8 V I/O 108-MHz QSPI; Ind Ext. Ind	**CY14B101I** **1Mb**; 3.0 V 3.4-MHz I²C; Ind RTC
	CY14B101KA/LA **1Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V101LA** **1Mb**; 3.0, 1.8 V I/O 25, 45 ns; x8; Ind	**CY14B101MA/NA** **1Mb**; 3.0 V 25, 45 ns; x16; Ind RTC	**CY14V101NA** **1Mb**; 3.0, 1.8 V I/O 25, 45 ns; x16; Ind	**CY14B101PA** **1Mb**; 3.0 V 40-MHz SPI; Ind RTC	**CY14B512P** **512Kb**; 3.0 V 40-MHz SPI; Ind RTC	**CY14B512I** **512Kb**; 3.0 V 3.4-MHz I²C; Ind RTC
64Kb–256Kb		**CY14B256KA/LA** **256Kb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V/U256LA** **256Kb**; 3.0, 1.8V I/O 35 ns; x8; Ind				
		CY14E256LA **256Kb**; 5.0 V 25, 45 ns; x8; Ind			**CY14B256PA** **256Kb**; 3.0 V 40-MHz SPI; Ind RTC		**CY14B256I** **256Kb**; 3.0 V 3.4-MHz I²C; Ind RTC
					CY14B064PA **64Kb**; 3.0 V 40-MHz SPI; Ind RTC		**CY14B064I** **64Kb**; 3.0 V 3.4-MHz I²C; Ind RTC

[1] Low-pin-count
[2] Industrial grade -40°C to +85°C
[3] Real-time clock
[4] Open NAND flash interface
[5] Error-correcting code
[6] AEC-Q100 -40°C to +125°C
[7] Quad serial peripheral interface
[8] Extended Industrial grade -40°C to +105°C
[9] Military grade -55°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

Nonvolatile RAM Roadmap

Product Family	Density	(ES) [EOL]
Serial Excelon F-RAM QSPI, SPI 1.71–1.89 V 1.8–3.6 V	4/8Mb 2Mb 16Mb	(Q1'18) (Q4'18) (Q2'19)
Serial F-RAM SPI, I^2C 3.3/5 V	4Kb–4Mb	
Processor Companion F-RAM I^2C 3.3/5 V	64Kb, 256Kb	
Parallel F-RAM x8, x16 3.3/5 V	64Kb–4Mb	
Parallel nvSRAM x8, x16 3 V, 5 V	64Kb–16Mb	
Serial nvSRAM I^2C, SPI, QSPI 3 V, 5 V	64Kb–1Mb	

Concept Samples Production EOL

2Mb-to-16Mb Excelon™ F-RAM Family

Applications

Medical devices, wearables, industrial control and automation, automotive

Features

- **Excelon-Ultra**
  - 4Mb
  - 108-MHz Single Data Rate (SDR)/54-MHz Double Data Rate (DDR) Quad SPI
  - Industrial temperature range: -40°C to +85°C
- **Excelon-Auto**
  - 2Mb Auto E, 4Mb Auto A
  - 50-MHz SPI
  - Automotive (AEC-Q100) temperature range grade A: -40°C to +85°C
  - Automotive (AEC-Q100) temperature range grade E: -40°C to +125°C
- **Common Features for Excelon-Ultra/Auto**
  - Operating voltage range: 1.71–1.89 V, 1.80–3.60 V
  - 100-trillion read/write cycle endurance
  - 100-year data retention

Collateral

Preliminary Datasheet: Contact Sales (Available Now)

Excelon F-RAM

Family Table

Density	Standby Current (Typ.)	Active Current (Typ.)	Packages
2Mb	1 µA	3 mA	SOIC (8)
4Mb	1 µA	3 mA	SOIC (8), GQFN (8)
8Mb	1 µA	3 mA	GQFN (8)
16Mb	1 µA	3 mA	SOIC (8), GQNF (8)

Availability

Samples: Now (2Mb Auto, 4Mb, 8Mb), Q2 2019 (2Mb, 16Mb)
Production: Q4 2018 (2Mb Auto, 4Mb, 8Mb), Q4 2019 (2Mb, 16Mb)

4Mb SPI Serial F-RAM™

Applications

Multifunction printers, industrial controls and automation, medical wearables[1], test and measurement equipment, smart meters

Features

- **High speed**
  - 40-MHz SPI interface
- **Nonvolatile**
  - 100-trillion read/write cycle endurance
  - 100-year data retention
- **Wide Operating Voltage**
  - Operating voltage range: 2.0–3.6 V
  - Low (8-µA) sleep current
- **Temperature Range**
  - Industrial temperature operation
- **Packages**
  - 8-pin TDFN, 8-pin SOIC

Collateral

Datasheet: CY15B104Q

[1] Compact electronic devices, such as watches or fitness monitors, used to collect, process, display and transmit sensor data

4Mb SPI Serial F-RAM

Availability

Samples: Now **Production:** Now

1Mb Quad SPI nvSRAM

Applications

Computing and networking, industrial automation, RAID storage

Features

- **High speed**
  - 108-MHz Quad SPI interface
- **Nonvolatile**
  - Unlimited write endurance
  - One million store cycles on power fail
  - Data retention of 20 years at 85°C
- **Operating Voltage**
  - Vcc: 3.0 V
  - I/O: 1.8 V
- **Features**
  - Low standby (280-µA) and sleep (10-µA) currents
  - Integrated, high-accuracy real-time clock (RTC)
- **Operating Temperatures**
  - Industrial temperature range: -40°C to +85°C
  - Extended Industrial temperature range: -40°C to +105°C
- **Packages**
  - 16-pin SOIC

Quad SPI nvSRAM

Collateral

Datasheet: CY14V101QS

Availability

Samples: Now **Production:** Now

[1] Crystal connections
[2] External capacitor connection
[3] Hardware store busy

F-RAM Packages

Family	Density	8-pin SOIC	8-pin DFN	8-pin EIAJ	14-pin SOIC	28-pin SOIC	28-pin TSOP I	32-pin TSOP I	44-pin TSOP II	48-ball FBGA	Wafer
SPI	4Kb	✓	✓								
	16Kb	✓	✓								
	64Kb	✓	✓								
	128Kb	✓									
	256Kb	✓	✓								
	512Kb	✓									
	1Mb	✓									
	2Mb		✓	✓							
	4Mb		✓	✓							
I²C	4Kb	✓									
	16Kb	✓	✓								
	64Kb	✓	✓								
	128Kb	✓									
	256Kb	✓									
	512Kb	✓									
	1Mb	✓									
Processor Companion	64Kb				✓						
	256Kb				✓						
Parallel	64Kb					✓					
	256Kb					✓	✓	✓			✓
	1Mb							✓	✓		✓
	2Mb								✓		✓
	4Mb								✓	✓	

nvSRAM Packages

Family	Density	8-pin SOIC	8-pin DFN	16-pin SOIC	28-pin SOIC	28-pin CDIP	28-pad LCC	32-pin SOIC	44-pin TSOP II	48-ball FBGA	48-pin SSOP	48-pin TSOP I	54-pin TSOPII	60-ball FBGA	165-ball FBGA	Wafer
Parallel	64Kb				✓	✓	✓									
	256Kb				✓	✓	✓	✓	✓	✓	✓					
	1Mb							✓	✓	✓	✓		✓			
	4Mb								✓	✓			✓			✓
	8Mb								✓	✓			✓			
	16Mb								✓			✓	✓	✓	✓	✓
SPI	64Kb	✓		✓												
	256Kb	✓	✓	✓												
	512Kb	✓		✓												
	1Mb	✓	✓	✓												
I²C	64Kb	✓		✓												
	256Kb			✓												
	512Kb			✓												
	1Mb	✓		✓												

Asynchronous SRAM

Low-Power (MoBL®), Fast, PowerSnooze™

CYPRESS
EMBEDDED IN TOMORROW™

Asynchronous SRAM Portfolio

High Density | Wide Voltage Range | Automotive A[1], E[2] | On-Chip ECC

Density	Fast SRAM			Low-Power SRAM (MoBL®[3])			PowerSnooze™[4]
	Non-ECC (≥90nm)		ECC (65nm)	Non-ECC (≥90nm)	ECC (65nm)	ECC (65nm) ULP[5]	ECC (65nm)
32Mb–64Mb	**CY7C107x** **32Mb**; 3.3 V 12 ns; x8, x16 Ind			**CY6218x** **64Mb**; 1.8, 3.0 V 55 ns; x16 Ind **CY6217x** **32Mb**; 1.8-5.0 V 55 ns; x16 Ind	**CY6218x** **64Mb**; 1.8, 3.0 V 45 ns; x16 Ind, Auto E **CY6217x** **32Mb**; 1.8, 3.0 V 45 ns; x16 Ind, Auto E	**CY6218x** **64Mb**; 3.0 V 45 ns; x16 Ind **CY6217x** **32Mb**; 3.0 V 45 ns; x16 Ind	
2Mb–16Mb	**CY7C106xGN** **16Mb**; 1.8, 3.3 V 10 ns; x8, x16, x32 Ind **CY7C105x** **8Mb**; 3.3 V 10 ns; x8, x16 Ind **CY7C1012** **12Mb**; 3.3 V 10 ns; x24 Ind **CY7C104x** **4Mb**; 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A, E **CY7C1034** **6Mb**; 3.3 V 10 ns; x24 Ind **CY7C1010/11** **2Mb**; 3.3 V 10 ns; x8, x16 Ind, Auto A, E **CY7C1024** **3Mb**; 3.3 V 10 ns; x24 Ind		**CY7C106xG/GE** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind, Auto E **CY7C105x** **8Mb**; 3.3, 5.0 V 10 ns; x8, x16 Ind, Auto E **CY7C104x** **4Mb**; 1.8-5.0 V 10 ns; x8, x16 Ind, Auto E	**CY6216x** **16Mb**;1.8, 3.0, 5.0 V 45 ns; x8, x16 Ind, Auto A **CY6215x** **8Mb**; 1.8, 3.0, 2.5-5V 45 ns; x8, x16 Ind, Auto A, E **CY6214x** **4Mb**; 1.8, 3.0, 2.5-5V 45 ns; x8, x16 Ind **CY6213x** **2Mb**; 1.8, 2.5-5.0 V 45 ns; x8, x16 Ind, Auto A, E	**CY6216x** **16Mb;** 1.8-5.0 V 45 ns; x8, x16, x32 Ind, Auto E **CY6216x** **8Mb;** 3.3, 5.0 V 45 ns; x8, x16, x32 Ind, Auto E **CY6214x** **4Mb**; 1.8-5.0 V 45 ns; x8, x16 Ind, Auto A, E	**CY6216x** **16Mb;** 3.0 V 45 ns; x8, x16, x32 Ind	**CY7S106x** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind **CY7S104x** **4Mb**; 1.8-5.0 V 10 ns; x8, x16 Ind
64Kb–1Mb	**CY7C1020** **512Kb**; 2.6, 3.3, 5.0 V 10 ns; x16 Ind, Auto E **CY7C1019/21/100x** **1Mb**; 2.6, 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A, E **CY7C19x/1399** **256Kb**; 3.3, 5.0 V 10 ns; x4, x8 Ind, Auto A			**CY6212x** **1Mb**; 2.5-5.0 V 45 ns; x8, x16 Ind, Auto A, E **CY62256** **256Kb**; 1.8, 3.0, 5V 55 ns, 70 ns; x8 Ind, Auto A, E			

[1] AEC-Q100 -40°C to +85°C
[2] AEC-Q100 -40°C to +125°C
[3] More Battery Life
[4] A Fast SRAM with a deep-sleep mode in addition to the conventional standby
[5] Ultra-Low-Power

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

Asynchronous SRAM Roadmap

Product Family	Density	(ES) [EOL]
MoBL SRAM ULP 65nm, ECC Parallel Asynchronous	16Mb 32Mb/64Mb	(Q3'20) (Q1'20)
MoBL SRAM 65nm, ECC Parallel Asynchronous	4Mb, 8Mb, 16Mb	
MoBL SRAM ≥ 90nm, Parallel Asynchronous	64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	
PowerSnooze SRAM 65nm, ECC Parallel Asynchronous	4Mb, 16Mb	
Fast SRAM 65nm, ECC Parallel Asynchronous	2Mb, 4Mb, 8Mb, 16Mb	
Fast SRAM ≥ 90nm Parallel Asynchronous	64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 3Mb, 6Mb, 8Mb, 12Mb, 32Mb, 64Mb	

Low-Power SRAM Family with ECC[1]

Applications

Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers and automotive

Features

- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Standby current: 8.7 µA for 4Mb
- **Features**
  - ECC[1] logic to detect and correct single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS[2]-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

Collateral

Datasheet: Asynchronous SRAM with ECC

SRAM with ECC

Family Table

Density	MPN	Standby Current (Maximum at 85°C)	Standby Current (Typical at 25°C)
4Mb	CY6214x	8.7 µA	3.5 µA
8Mb	CY6215x	16.0 µA	5.5 µA
16Mb	CY6216x	16.0 µA	5.5 µA

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Fast SRAM Family with PowerSnooze™[1]

Applications

Programmable logic controllers, handheld devices, multifunction printers, computation servers and automotive

Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Deep-sleep current: 15 µA for 4Mb
- **Features**
  - ECC[2] logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS[3]-Compliant Packages**
  - 48-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 36-pin and 44-pin SOJ

Collateral

Datasheet: Asynchronous SRAM with ECC

[1] A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode
[2] Error-correcting code
[3] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

SRAM with PowerSnooze

Family Table

Density	MPN	Access Time	Deep Sleep Current (Maximum at 85ºC)
4Mb	CY7S104x	10 ns	15 µA
16Mb	CY7S106x	10 ns	22 µA

Availability

Production: Now

Fast SRAM Family with ECC[1]

Applications

Switches and routers, IP phones, test equipment, computation servers, automotive, military and aerospace systems

Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS[2]-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

Collateral

Datasheet: Asynchronous SRAM with ECC

SRAM with ECC

Family Table

Density	MPN	Access Time	Operating Current (Maximum at 85°C)
4Mb	CY7C104x	10 ns	45 mA
8Mb	CY7C105X	10 ns	110 mA
16Mb	CY7C106x	10 ns	110 mA

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Asynchronous SRAM Packages

Family	Density	28-pin TSOP I	32-pin TSOP I	48-pin TSOP I	32-pin TSOP II	44-pin TSOP II	48-pin TSOP II	54-pin TSOP II	36-ball BGA	48-ball BGA	119-ball BGA	28-pin PDIP	28-pin SOJ	32-pin SOJ	36-pin SOJ	44-pin SOJ	32-pin SOIC	28-pin SNC	60-ball CSP	Wafer
Fast	256Kb	✓											✓							✓
	512Kb					✓										✓				
	1Mb		✓		✓	✓				✓			✓	✓		✓				✓
	2Mb					✓				✓					✓					
	3Mb										✓									
	4Mb					✓				✓					✓	✓				✓
	6Mb										✓									
	8Mb					✓				✓										
	12Mb										✓									
	16Mb			✓				✓		✓	✓									
	32Mb									✓										
Low-Power	256Kb	✓										✓						✓		
	1Mb		✓			✓				✓							✓			✓
	2Mb		✓		✓	✓			✓	✓							✓			✓
	4Mb		✓		✓	✓				✓							✓			✓
	8Mb			✓		✓				✓										✓
	16Mb									✓	✓								✓	✓
	32Mb						✓			✓										
	64Mb									✓										

Synchronous SRAM

Std Sync, NoBL®, QDR-II, DDR-II, QDR-IV

Synchronous SRAM Portfolio

High Random Transaction Rate (RTR)[1] | Low Latency | High Bandwidth

Standard Sync and NoBL®	Standard Sync and NoBL with ECC[2]	QDR®-II/ DDR-II	QDR-II+/ DDR-II+	QDR-II+X/ DDR-II+X	QDR-IV
RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes	RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes	RTR: 666 MT/s (max.) BW: 47.9 Gbps (max.) Latency: 1.5 Cycles CIO[3] and SIO[4]	RTR: 666 MT/s (max.) BW: 79.2 Gbps (max.) Latency: 2 or 2.5 Cycles CIO and SIO, ODT[5]	RTR: 900 MT/s (max.) BW: 91.1 Gbps (max.) Latency: 2.5 Cycles SIO, ODT	RTR: 2.1 GT/s (max.) BW: 153.5 Gbps (max.) Latency: 5 or 8 Cycles Dual-Port Bidirectional ODT
		CY7C161/2xKV18 **144Mb**; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4	**CY7Cx4/5/6/7xKV18** **144Mb**; 300–550 MHz 1.8 V; x18, x36 Burst 2, 4		**CY7C41xKV13** **144Mb**; 667–1,066 MHz 1.3 V; x18, x36 Burst 2
CY7C147/8xB **72Mb**; 133–250 MHz 2.5, 3.3 V; x18, x36		**CY7C151/2xKV18** **72Mb**; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4	**CY7Cx54/5/6/7KV18** **72Mb**; 250–550 MHz 1.8 V; x18, x36 RH[6]; Burst 2, 4	**CY7C156/7xXV18** **72Mb**; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4	**CY7C40xKV13** **72Mb**; 667–1,066 MHz 1.3 V; x18, x36 Burst 2
CY7C144/6xK **36Mb**; 133–250 MHz 2.5, 3.3 V; x36, x72	**CY7C144/6xKVE** **36Mb**; 133–250 MHz 2.5, 3.3 V; x18, x36	**CY7C141/2xKV18** **36Mb**; 250–333 MHz 1.8 V; x8, x9, x18, x36 Burst 2, 4	**CY7Cx24/5/6/7xKV18** **36Mb**; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4	**CY7C126/7x** **36Mb**; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4	
CY7C137/8xD/K **18Mb**; 100–250 MHz 3.3 V; x18, x32, x36	**CY7C137/8xKVE** **18Mb**; 100–250 MHz 2.5, 3.3 V; x18, x36	**CY7C131/2/9xKV18** **18Mb**; 250–333 MHz 1.8 V; x8, x18, x36 Burst 2, 4	**CY7Cx14/5/6/7xKV18** **18Mb**; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4		
CY7C135/6xC **9Mb**; 100–250 MHz 3.3 V; x18, x32, x36 Auto E[7]		**CY7C1911xKV18** **18Mb**; 250–333 MHz 1.8 V; x9 Burst 2, 4			
CY7C134/2xG **2–4Mb**; 100–250 MHz 3.3 V; x18, x32, x36					

Density ↑

Random Transaction Rate →

[1] Rate of truly random accesses to memory, expressed in transactions per second (MT/s, GT/s)
[2] Error-correcting code
[3] Common I/O
[4] Separate I/O
[5] On-die termination
[6] Radiation hardened, military grade
[7] AEC-Q100: -40°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

Synchronous SRAM Roadmap

Product Family	Density (Prod) [EOL]
QDR-IV SRAM 65nm, ECC 2.1 GT/s, 153.5 Gbps	72Mb, 144Mb
QDR-II+X SRAM 65nm, ECC 900 MT/s, 91.1 Gbps	36Mb, 72Mb
QDR-II+ SRAM 65nm, ECC 666 MT/s, 79.2 Gbps	18Mb, 36Mb, 72Mb[1], 144Mb
QDR-II SRAM 65nm 666 MT/s, 47.9 Gbps	18Mb, 36Mb, 72Mb, 144Mb
Standard Sync and NoBL® SRAM 65nm, ECC 250 MT/s, 18 Gbps	18Mb, 36Mb
Standard Sync and NoBL SRAM 65nm/90nm 250 MT/s, 18 Gbps	2Mb, 4Mb, 9Mb[2], 18Mb[3], 36Mb[3], 72Mb
Standard Sync and NoBL SRAM 90nm 250 MT/s, 18 Gbps	36Mb [LTS Q2'18]

[1] Radiation hardened, military grade
[2] AEC-Q100 -40°C to +125°C
[3] 65-nm

Concept | Samples | Production | EOL

Standard Synchronous SRAM With On-Chip ECC[1]

Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features

- **Speed**
  - Available in two modes[2]: Pipeline and Flow-Through
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options[3]
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral

Datasheets: 36M Sync SRAM, 18M Sync SRAM

Synchronous SRAM

Family Table

Option	Density	MPN	RTR	FIT/Mb[4]
Standard Sync with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1370/2K CY7C1440/2K	250 MT/s	<0.01
Standard Sync with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1371/3K CY7C1441/3K	133 MT/s	<0.01

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[3] Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
[4] The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

NoBL® SRAM With On-Chip ECC[1]

Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features

- **Speed**
  - Available in two modes[2]: Pipeline and Flow-Through
  - No Bus Latency™ (NoBL) architecture for balanced read and write
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral

Datasheets: 36M NoBL SRAM, 18M NoBL SRAM

NoBL SRAM

Family Table

Option	Density	MPN	RTR	FIT/Mb[3]
NoBL with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1380/2K CY7C1460/2K	250 MT/s	<0.01
NoBL with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1381/3K CY7C1461/3K	133 MT/s	<0.01

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[3] The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

QDR®-IV SRAM

Applications

Switches and routers, high-performance computing, military and aerospace systems, test and measurement

Features

- **Speed**
  - Available in two options: QDR-IV HP (RTR 1,334 MT/s) and QDR-IV XP (RTR 2,132 MT/s)
  - Two independent, bidirectional DDR[1] data ports
  - Bus widths: x18, x360.13
- **Features**
  - ECC[2] to reduce soft error rate to less than 0.01 FIT/Mb[3]
  - Bus inversion to reduce simultaneous switching I/O noise
  - On-die termination (ODT) to reduce board complexity
  - De-skew training[4] to improve signal-capture timing
  - I/O levels: 1.2–1.25 V (HSTL/SSTL), 1.1–1.2 V (POD[5])
- **Package**
  - 361-pin FCBGA[6]

Collateral

Datasheets: CY7C4122KV13/CY7C4142KV13
CY7C4121KV13/CY7C4141KV13
CY7C4022KV13/CY7C4042KV13
CY7C4021KV13/CY7C4041KV13

[1] Double Data Rate: Two data transfers per clock cycle
[2] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors
[3] Failures in Time per Megabit
[4] An iterative algorithm for assessing and eliminating the skew between multiple data signals
[5] Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up drive strength
[6] Flip-Chip Ball Grid Array

QDR-IV

Family Table

Option	Density	MPN	Maximum Frequency	RTR
QDR-IV HP	72Mb 144Mb	CY7C40x1KV13 CY7C41x1KV13	667 MHz	1,334 MT/s
QDR-IV XP	72Mb 144Mb	CY7C40x2KV13 CY7C41x2KV13	1,066 MHz	2,132 MT/s

Availability

Production: Now

Synchronous SRAM Packages

Family	Density	100-pin TQFP	119-ball BGA	165-ball BGA	209-ball BGA	361-ball BGA	Wafer
Std Sync	18Mb	✓		✓			
	36Mb			✓			
NoBL	2Mb	✓					
	4Mb	✓	✓				
	9Mb	✓	✓	✓			✓
	18Mb	✓	✓	✓			
	36Mb	✓		✓			✓
	72Mb	✓		✓	✓		✓
QDR	9Mb			✓			
	18Mb			✓			
	36Mb			✓			
	72Mb			✓		✓	
	144Mb			✓		✓	

Specialty Memory

Dual-Port SRAM, FIFO

Specialty Memory

Intelligent Memory | High Density | High Throughput

Density	Dual-Port SRAM		FIFO	
	Asynchronous	Synchronous	Asynchronous	Synchronous
2Mb–72Mb		**CYD02/9/18/36SxxV18** **2Mb, 9Mb, 18Mb, 36Mb**; 1.8 V 167 MHz, 200 MHz x18, x36, x72; Ind **CY7C083x/5x** **2Mb, 4Mb, 9Mb**; 3.3 V 100 MHz, 133 MHz, 167 MHz x18, x36, x72; Ind		**CYFB0072V**[1] **72Mb;** 1.8, 3.3 V 133 MHz x36; Ind **CYFX18V/36V/72V** **18Mb, 36Mb, 72Mb**; 1.8, 3.3 V 100 MHz, 133 MHz x9 to x36 Prog[2]; Ind
128Kb–1Mb	**CY7C02x/3x/5x** **512Kb, 1Mb**; 3.3, 5.0 V 12 ns, 15 ns, 20 ns, 25 ns x8, x16, x18, x36; Ind[3] **CY7C006/025/026** **128Kb, 256Kb**; 3.3, 5.0 V 15 ns, 20 ns, 25 ns, 55 ns x8, x16, x18; Ind	**CY7C09279/289/389/579** **512Kb, 1Mb**; 3.3 V 7, 9, 12 ns; 83 MHz, 100 MHz x8, x16, x18, x36; Ind **CY7C09269/369** **256Kb**; 3.3 V 9 ns, 12 ns x16, x18; Ind		**CY7C4275/85/91** **512Kb, 1Mb**; 3.3 V 67 MHz, 100 MHz x9, x18; Ind **CY7C4255/61/65** **128Kb, 256Kb**; 3.3, 5.0 V 67 MHz, 100 MHz x9, x18; Ind
2Kb–64Kb	**CY7C024/144** **64Kb**; 3.3, 5.0 V 15 ns, 20 ns, 25 ns, 55 ns x8, x16, x18; Ind **CY7C13x** **8Kb, 16Kb, 32Kb**; 5.0 V 15 ns, 25 ns, 55 ns x8; Ind	**CY7C09159/349** **64Kb**; 3.3 V 9 ns, 12 ns x9, x18; Comm[4]		

[1] Video Frame Buffer products
[2] Programmable Bus Width
[3] Industrial grade -40°C to +85°C
[4] Commercial grade 0°C to +85°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

Timing Solutions Portfolio

Clock Synthesizer Roadmap

	Product Family	Features	(Prod) [EOL]
High Performance	CY27430	4-PLL; Maximum Frequency: 700 MHz 12 Outputs; Diff[1] & SE[1]; PCIe 3.0; VCXO[2]; EMI[3]; 0.7-ps RMS Jitter[4] 1.8 V/2.5 V/3.3 V; Ind[5]; 48-QFN	
High Performance	CY27410	4-PLL; Maximum Frequency: 700 MHz 8 Outputs; Diff & SE; PCIe 3.0; VCXO; EMI; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; Auto A[6] S[7]; 48-QFN	
High Performance	CCY254x/CY251x	1-4 PLL; Maximum Frequency: 200 MHz 3-9 Outputs; I²C; EMI; Low Power[8] 100-ps CCJ[9]; Ind; 1.8 V/2.5 V/3.0 V/3.3 V 8-SOIC; 8/16/20-TSSOP; 24-QFN	
Standard Performance	CY229x/CY2238x	3-4 PLL; Maximum Frequency: 166 MHz 3-8 Outputs; CMOS; Low Power 200-ps PPJ[10]; VCXO; Ind; 3.3 V/5 V 8/16/20-SOIC; 16-TSSOP	
Standard Performance	CY2429x	1-PLL; Maximum Frequency: 200 MHz 2-5 Outputs; HCSL, CMOS; EMI 75-ps CCJ; PCIe 1.1; Ind; Auto A 3.3 V; 16-TSSOP; 32-QFN	
Standard Performance	CY2239x	3-4 PLL; Maximum Frequency: 400 MHz 5-8 Outputs; LVPECL, CMOS; I²C 400-ps PPJ; VCXO; 3.3 V Ind; Auto A E[11]; 16-TSSOP; 32-QFN	
Standard Performance	CY22800/801/CY2581x	1-PLL; Maximum Frequency: 200 MHz 1-3 Outputs; CMOS; EMI 110-ps CCJ; VCXO; Ind; 3.3 V; 8-SOIC; 8-TSSOP	
Standard Performance	CY22050/150	1-PLL; Maximum Frequency: 200 MHz 6 Outputs; CMOS; I²C 250-ps PPJ; Ind 2.5 V/3.3 V; 16-TSSOP	

[1] Differential and single-ended outputs
[2] Voltage-controlled crystal oscillation
[3] Electro Magnetic Interference reduction using Lexmark profile
[4] Integrated phase noise across 12-kHz to 20-MHz offset
[5] Industrial grade: -40°C to +85°C
[6] AEC-Q100: -40°C to +85°C
[7] AEC-Q100: -40°C to +105°C
[8] Power management options
[9] Cycle-to-cycle jitter
[10] Peak-to-peak period jitter
[11] AEC-Q100: -40°C to +125°C

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Oscillator Roadmap

	Product Family	Features	(Prod) [EOL]
High Performance	CY294x	1-PLL; Maximum Frequency: 2.1 GHz 1 Output; Diff[1] & SE[1]; 40/100 GbE; VCXO[2]; 0.11-ps RMS Jitter[3]; Ind[4]; 8-LCC (7 x 5, 5 x 3.2); 16-QFN	
High Performance	CY51x7	1-PLL; Maximum Frequency: 2.1 GHz 1 Output; Diff & SE; 40/100 GbE; VCXO; 0.11-ps RMS Jitter; Ind; 1.8 V/2.5 V/3.3 V; WAFER/DIE	
High Performance	CY2Xx (FleXO™)	1 PLL; Maximum Frequency: 690 MHz 1 Output; LVCMOS, LVDS, LVPECL Frequency Margining; 0.6-ps RMS Jitter; Ind; 6-LCC (7 x 5, 5 x 3.2); 8-TSSOP	
Standard Performance	CY25701	1-PLL; Maximum Frequency: 166 MHz 1 Output; CMOS; EMI[5]; 85-ps CCJ[6]; Ind; 3.3 V; 4-LCC (5 x 3.2)	
Standard Performance	CY2037/ 5037	1-PLL; Maximum Frequency: 133 MHz 1 Output; CMOS; 100-ps CCJ; Ind; 3.3 V/5.0 V; WAFER	
Standard Performance	CY5077	1-PLL; Maximum Frequency: 166 MHz 1 Output; CMOS; 75-ps CCJ; Ind; 1.8 V/2.5 V/3.0 V/3.3 V; WAFER	
Standard Performance	CY5057	1-PLL; Maximum Frequency: 170 MHz 1 Output; CMOS; EMI; <200-ps CCJ; Ind; 3.3 V/5.0 V; WAFER	

[1] Differential and single-ended outputs
[2] Voltage-controlled crystal oscillation
[3] Integrated phase noise across 12-kHz to 20-MHz offset
[4] Industrial grade: -40°C to +85°C
[5] Electromagnetic interference reduction using Lexmark profile
[6] Cycle-to-cycle jitter

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Clock Buffer Roadmap

	Product Family	Features	(Prod) [EOL]
High Performance	CY2DPx/CPx	Maximum Frequency: 1.5 GHz 2-10 Outputs; LVPECL; 2.5 V/3.3 V 0.11-ps Additive Jitter[1]; Ind[2] 8/20-TSSOP; 8-SOIC; 32-TQFP	
High Performance	CY2DMx/DLx	Maximum Frequency: 1.5 GHz 2-10 Outputs; LVDS, CML; 2.5 V/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 32-TQFP	
High Performance	CY230x/EP0x (Zero Delay)	Maximum Frequency: 220 MHz 2-9 Outputs; LVCMOS; 2.5 V/3.3 V/5 V 22-ps CCJ[3]; Ind; Auto A[4] 8/16-SOIC; 16-TSSOP; WAFER	
Standard Performance	CY230xNZ/ 2994x (Non-Zero Delay)	Maximum Frequency: 200 MHz 4-18 Outputs; LVCMOS 100-ps Op-Op Skew; Ind 2.5 V/3.3 V; 8-TSSOP, 16-SOIC	
Standard Performance	CY23FS04/08/FP12 (Zero Delay)	Maximum Frequency: 200 MHz 4-12 Outputs; LVCMOS; Fail Safe 200-ps CCJ; Ind; 2.5 V/3.3 V 16/28-SSOP	
Standard Performance	CY23S0x (Zero Delay)	Maximum Frequency: 133 MHz 5-9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind; 2.5 V/3.3 V; 8/16-SOIC; 16-TSSOP	
Standard Performance	CY7B99x (RoboClock™)	Maximum Frequency: 200 MHz; 8-13 Outputs Configurable Skew; 2.5 V/3.3 V/5.0 V 50-ps CCJ; Ind; 24-SOIC; 32-PLCC; 32/44/52,100-TQFP; 100-BGA	

[1] Additive RMS phase jitter
[2] Industrial grade: -40°C to +85°C
[3] Cycle-to-cycle jitter
[4] AEC-Q100: -40°C to +85°C

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Timing Solutions Portfolio

Programmable | High-Performance | EMI Reduction | Automotive

	Clock Synthesizers		Oscillators		Clock Buffers	
High Performance	**CY27410** 4-PLL; Max Freq: 700 MHz 12 Outputs; Diff[1] & SE[1]; PCIe 3.0 VCXO[2]; EMI[3]; 0.7-ps RMS Jitter[4] 1.8 V/2.5 V/3.3 V; Ind[5]; 48-QFN	**CY27430** 4-PLL; Max Freq: 700 MHz 8 Outputs; Diff & SE; PCIe 3.0 VCXO; EMI; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; Auto A[6] S[7]; 48-QFN	**CY2941x/2x** 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff & SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 8-LCC (7 x 5, 5 x 3.2)	**CY51x7** 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff & SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 1.8 V/2.5 V/3.3 V; WAFER/DIE	**CY2DPx/CPx** Max Freq: 1.5 GHz 2–10 Outputs; LVPECL; 2.5/3.3 V 0.11-ps Additive Jitter[8]; Ind 8/20-TSSOP; 8-SOIC; 32-TQFP	**CY2DMx/DLx** Max Freq: 1.5 GHz 2–10 Outputs; LVDS, CML; 2.5/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 32-TQFP
	CY29430 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff & SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 16-QFN		**CY2Xx (FleXO™)** Q320 1 PLL; Max Freq: 690 MHz 1 Output; LVCMOS, LVDS, LVPECL Freq Margining; 0.6-ps RMS Jitter Ind · 6-LCC (7x5, 5x3.2); 8-TSSOP			
Standard Performance	**CY254x/CY251x** 1–4 PLL; Max Freq: 200 MHz 3–9 Outputs; I²C; EMI; Low Power[9] 100-ps CCJ[10]; Ind; 1.8/2.5/3.0/3.3 V 8-SOIC; 8/16/20-TSSOP; 24-QFN	**CY229x/CY2238x** 3–4 PLL; Max Freq: 166 MHz 3–8 Outputs; CMOS; Low Power 200-ps PPJ[11]; VCXO; Ind; 3.3/5 V 8/16/20-SOIC; 16-TSSOP	**CY25701** 1-PLL; Max Freq: 166 MHz 1 Output; CMOS; EMI 85-ps CCJ; Ind 3.3 V; 4-LCC (5 x 3.2)	**CY2037/ 5037** 1-PLL; Max Freq: 133 MHz 1 Output; CMOS 100-ps CCJ; Ind 3.3/5.0 V; WAFER	**CY230x/EP0x (Zero Delay)** Max Freq: 220 MHz 2–9 Outputs; LVCMOS ; 2.5/3.3/5 V 22-ps CCJ; Ind[5]; Auto A 8/16-SOIC; 16-TSSOP; WAFER	**CY230xNZ/ 2994x (Non-Zero Delay)** Max Freq: 200 MHz 4–18 Outputs; LVCMOS 100-ps Op-Op Skew; Ind 2.5/3.3 V; 8-TSSOP, 16-SOIC
	CY2429x 1-PLL; Max Freq: 200 MHz 2-5 Outputs; HCSL, CMOS; EMI 75-ps CCJ; PCIe 1.1; Ind; Auto A 3.3 V; 16-TSSOP; 32-QFN	**CY2239x** 3–4 PLL; Max Freq: 400 MHz 5–8 Outputs; LVPECL, CMOS; I²C 400-ps PPJ; VCXO; 3.3 V Ind; Auto A E[12]; 16-TSSOP; 32-QFN	**CY5077** 1-PLLMax Freq: 166 MHz 1 Output; CMOS 75-ps CCJ; Ind 1.8/2.5/3.0/3.3 V; WAFER	**CY5057** 1-PLL; Max Freq: 170 MHz 1 Output; CMOS; EMI <200-ps CCJ; Ind 3.3/5.0 V; WAFER	**CY23FS04/08/FP12 (Zero Delay)** Max Freq: 200 MHz 4–12 Outputs; LVCMOS; Fail Safe 200-ps CCJ; Ind; 2.5/3.3 V 16/28-SSOP	**CY7B99x (RoboClock™)** Q319 Max Freq: 200 MHz; 8–13 Outputs Configurable Skew; 2.5/3.3/5.0 V 50-ps CCJ; Ind; 24-SOIC; 32-PLCC 32/44/52/100-TQFP; 100-BGA
	CY22800/801/CY2581x 1-PLL; Max Freq: 200 MHz 1-3 Outputs; CMOS; EMI 110-ps CCJ; VCXO; Ind 3.3 V; 8-SOIC; 8-TSSOP	**CY22050/150** 1-PLL; Max Freq: 200 MHz 6 Outputs; CMOS; I²C 250-ps PPJ; Ind[5] 2.5/3.3 V; 16-TSSOP			**CY23S0x (Zero Delay)** Max Freq: 133 MHz 5–9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind 2.5/3.3 V; 8,16-SOIC; 16-TSSOP	

[1] Differential and single-ended outputs
[2] Voltage-controlled crystal oscillation
[3] Electromagnetic interference reduction using Lexmark profile
[4] Integrated phase noise across 12-kHz to 20-MHz offset
[5] Industrial grade: -40°C to +85°C
[6] AEC-Q100: -40°C to +85°C
[7] AEC-Q100: -40°C to +105°C
[8] Additive RMS phase jitter
[9] Power management options
[10] Cycle-to-cycle jitter
[11] Peak-to-peak period jitter
[12] AEC-Q100: -40°C to +125°C

	Concept	Development	Sampling	Production	EOL
Status					
Availability			QQYY	QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

CY27410: High-Performance 4-PLL Clock Generator

Applications

Multifunction printers, digital TVs, Blu-ray recorders, home gateways, femtocells, routers and switches

Features

- **Twelve Outputs**
  - Eight configurable (differential or single-ended)
  - Four single-ended
- **Specifications**
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0 and 10 GbE
  - Industrial temperature grade
- **Additional Features**
  - Pin select and I^2C programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency Select option to choose from eight pre-programmed configurations
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- **RoHS-Compliant Package**
  - Available in a 7 mm x 7 mm 48-pin QFN package

Collateral

Datasheet: 4-PLL High-Performance Clock Generator (CY274X)

[1] Crystal input
[2] Crystal output
[3] Reference clock inputs
[4] Serial port
[5] Voltage input pin for VCFS
[6] Frequency select inputs

Four-PLL Spread-Spectrum Clock Generator

Availability

Production: Now

CY2941x/2x: High-Performance 1-PLL Programmable Oscillator

Applications

Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

Features

- **Outputs**
  - LVPECL[1], LVDS[2], HCSL[3] and CML[4] outputs
- **Specifications**
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter[5]: ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Pin select and I^{2}C programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40°C to +105°C)
- **RoHS-Compliant Packages**
  - Available in a 5 mm x 7 mm, 5 mm x 3.2 mm 8-pin LCC[9] package

Collateral

Datasheet: 1-PLL High-Performance Programmable Oscillator (CY2941x/2x)

High-Performance 1-PLL Programmable Oscillator

Availability

Production: Now

[1] Low-voltage positive emitter coupled logic
[2] Low-voltage differential signaling
[3] High-speed current steering logic
[4] Current mode logic
[5] The uncertainty of the clock rising and falling edge timing
[6] I^{2}C input
[7] Voltage input pin for VCFS
[8] Frequency select inputs
[9] Leadless ceramic chip carrier

CY29430: High-Performance 1-PLL Clock Synthesizer

Applications

Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

Features

- **Outputs**
  - LVPECL[1], LVDS[2], HCSL[3],CML[4] and LVCMOS outputs
- **Specifications**
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter[5]: ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Frequency Select option to choose from four pre-programmed configurations
  - Pin select and I^{2}C programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40°C to +105°C)
- **RoHS-Compliant Package**
  - Available in a 3 mm x 3 mm 16-pin QFN[9] package

Collateral

Datasheet: 1-PLL High-Performance Clock Synthesizer (CY29430)

High-Performance 1-PLL Clock Synthesizer

Availability

Production: Now

[1] Low-voltage positive emitter coupled logic
[2] Low-voltage differential signaling
[3] High-speed current steering logic
[4] Current mode logic
[5] The uncertainty of the clock rising and falling edge timing
[6] I^{2}C input
[7] Voltage input pin for VCFS
[8] Frequency select inputs
[9] Quad flat no-leads

Cypress Roadmap: Flash Memory (NDA)

NOR Flash Memory Family

NOR Flash Memory Family Decoder

S 25 H S 512 T

Technology:	J = 110-nm Floating Gate (FG)		N = 110-nm MirrorBit® (MB)	1 = 63-nm DRAM (DR)
	K = 90-nm FG		P = 90-nm MB	
	L = 65-nm FG		R, S = 65-nm MB	
	M = 50-nm FG		T = 45-nm MB	
Density:	008 = 8Mb	064 = 64Mb	512 = 512Mb	04G = 4Gb
	016 = 16Mb	128 = 128Mb	01G = 1Gb	
	032 = 32Mb	256 = 256Mb	02G = 2Gb	
Voltage:	D = 2.5 V	L = 3.0 V	S = 1.8 V	
Family:	A = Standard ADP (Address-Data Parallel)			
	C = Burst Mode ADP (Address-Data Parallel)			
	F = Serial			
	G = Page Mode			
	H = High-Performance Serial			
	J = Simultaneous Read/Write ADP (Address-Data Parallel)			
	K = HyperBus™			
	N = Burst Mode Simultaneous Read/Write ADM (Address-Data Multiplexed)			
	P = Page Mode Simultaneous Read/Write ADP (Address-Data Parallel)			
	V = Burst Mode Simultaneous Read/Write ADM (Address-Data Multiplexed)			
	W = Burst Mode Simultaneous Read/Write ADP (Address-Data Parallel)			
	X = Burst Mode Simultaneous Read/Write AADM (Address-Address-Data Multiplexed)			
Series:	25 = SPI	26 = HyperBus™	28 = Octal	
	29 = Parallel	70 = Stacked Die	79 = Dual Quad SPI	
Prefix:	S			

NOR Flash Memory Product Portfolio: New Products

Family	Interface	Sector Size	Series	Voltage	Densities	Lead	Tech	2018	2019	2020	2021	2022
Semper™ Flash	Quad SPI	Hybrid	S25HS-T S25HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45-nm MB					
	HyperBus™[1]		S26HS-T S26HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45-nm MB					
	Octal[1]		S28HS-T S28HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45-nm MB					
QSPI	QSPI	Hybrid	S25FS-S	1.8 V	64Mb–1Gb	-	65-nm MB					
			S25FL-S	3.0 V	128Mb–1Gb	-	65-nm MB					
		Uniform 4KB	S25FL-L	3.0 V	64–256Mb	-	65-nm FG					
Dual Quad SPI	QSPI	Hybrid	S79FS-S S79FL-S	1.8 V 3.0 V	256Mb–1Gb	-	65-nm MB					
HyperFlash	HyperBus	Hybrid	S26KS-S S26KL-S	3.0 V	128–512Mb	-	65-nm MB					
Parallel	Parallel	Hybrid	S29GL-T	3.0 V	512Mb–2Gb	-	45-nm MB					

[1] JEDEC xSPI Compliant

Concept | Samples | Production | EOL

x8 Serial Memory Roadmap

Product Family	Density	(Prod) [EOL]
S28HS-T[1] (1.8 V) S28HL-T[1] (3.0 V) Semper™ Flash with Octal Interface 45-nm MB[2]	4Gb[3] 2Gb[3] 1Gb 512Mb 256Mb	(TBD) (TBD) (Q4'19) (Q1'19) (Q2'20)
S26HS-T[1] (1.8 V) S26HL-T[1] (3.0 V) Semper Flash with HyperBus™ Interface 45-nm MB[2]	4Gb[3] 2Gb[3] 1Gb 512Mb 256Mb	(TBD) (TBD) (Q4'19) (Q1'19) (Q2'20)
S26KS-S (1.8 V) S26KL-S (3.0 V) HyperFlash 65-nm MB[2]	512Mb 256Mb 128Mb	
S79FS-S (1.8 V) Dual Quad SPI 65-nm MB[2]	1Gb[4] 512Mb[4] 256Mb[4]	 (TBD) (TBD)
S79FL-S (3.0 V) Dual Quad SPI 65-nm MB[2]	1Gb[4] 512Mb[4] 256Mb[4]	

[1] JEDEC xSPI Compliant
[2] Hybrid Sector
[3] Stacked Die
[4] S79 Series (stacked die)

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

x8 Serial Memory Portfolio

	Dual Quad SPI S79FL-S[1, 2] 65-nm MB, 3.0 V	HyperFlash S26KL-S[1] 65-nm MB, 3.0 V	Semper™ Flash[3] S26HL-T[1, 4] 45-nm MB, 3.0 V	Semper Flash[5] S28HL-T[1, 4] 45-nm MB, 3.0 V	Dual Quad SPI S79FS-S[1, 2] 65-nm MB, 1.8 V	HyperFlash S26KS-S[1] 65-nm MB, 1.8 V	Semper Flash[3] S26HS-T[1, 4] 45-nm MB, 1.8 V	Semper Flash[5] S28HS-T[1, 4] 45-nm MB, 1.8 V
	Density Initial Access/DDR Clock * Temperature Range	**Density (S79)** SDR Clock / DDR Clock * Temperature Range						
	All parts supported by Longevity Program unless noted							
≥256Mb			**4Gb[6]** 80 ns/166 MHz * I, A, V, B, M	**4Gb[6]** 80 ns/166 MHz * I, A, V, B, M			**4Gb[6]** 80 ns/200 MHz * I, A, V, B, M	**4Gb[6]** 80 ns/200 MHz * I, A, V, B, M
≥256Mb			**2Gb[6]** 80 ns/166 MHz * I, A, V, B, M	**2Gb[6]** 80 ns/166 MHz * I, A, V, B, M			**2Gb[6]** 80 ns/200 MHz * I, A, V, B, M	**2Gb[6]** 80 ns/200 MHz * I, A, V, B, M
≥256Mb	**1Gb** 133 MHz/80 MHz * I, A, V, B		Q219 **1Gb** Q419 80 ns/166 MHz * I, A, V, B, M	Q219 **1Gb** Q419 80 ns/166 MHz * I, A, V, B, M	**1Gb** 133 MHz/102 MHz * I, A, V, B		Q219 **1Gb** Q419 80 ns/200 MHz * I, A, V, B, M	Q219 **1Gb** Q419 80 ns/200 MHz * I, A, V, B, M
≥256Mb	**512Mb** 133 MHz/80 MHz * I, A, V, B	**512Mb** 96 ns/166 MHz * I, A, V, B, M	**512Mb** Q219 80 ns/166 MHz * I, A, V, B, M	**512Mb** Q219 80 ns/166 MHz * I, A, V, B, M	**512Mb** 133 MHz/80 MHz * I, A, V, B	**512Mb** 96 ns/166 MHz * I, A, V, B, M	**512Mb** Q119 80 ns/200 MHz * I, A, V, B, M	**512Mb** Q119 80 ns/200 MHz * I, A, V, B, M
≥256Mb	**256Mb** 133 MHz/80 MHz * I, A, V, B	**256Mb** 96 ns/166 MHz * I, A, V, B, M	Q419 **256Mb** Q220 80 ns/166 MHz * I, A, V, B, M	Q419 **256Mb** Q220 80 ns/166 MHz * I, A, V, B, M	**256Mb** 133 MHz/80 MHz * I, A, V, B	**256Mb** 96 ns/166 MHz * I, A, V, B, M	Q419 **256Mb** Q220 80 ns/200 MHz * I, A, V, B, M	Q419 **256Mb** Q220 80 ns/200 MHz * I, A, V, B, M
64–128Mb		**128Mb** 96 ns/166 MHz * I, A, V, B, M				**128Mb** 96 ns/166 MHz * I, A, V, B, M		

[1] Hybrid Sector
[2] S79 series (stacked die)
[3] With HyperBus™ Interface
[4] JEDEC xSPI Compliant
[5] With Octal Interface
[6] Stacked die

* I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

x4 Serial NOR Flash Memory Roadmap

Product Family	Density	(Prod) [EOL]
S25HS-T (1.8 V) S25HL-T (3.0 V) Semper™ Flash with Quad SPI 45-nm MB[1]	4Gb[4] 2Gb[4] 1Gb 512Mb 256Mb	(TBD) (Q219) (Q4'19) (Q1'19) (Q2'20)
S25FS-S (1.8 V) S25FL-S[2] (3.0 V) QSPI 65-nm MB[1]	1Gb[5] 512Mb 256Mb 128Mb[6] 64Mb[7]	
S25FL-L (3.0 V) QSPI 65-nm FG[3]	256Mb 128Mb 64Mb	
S25FL1-K (3.0 V) QSPI 90-nm FG[3]	64Mb 32Mb 16Mb	[Q3'19] [Q3'19] [Q3'19]

[1] Hybrid Sector
[2] VIO 1.8 V to 3.0 V
[3] Uniform Sector
[4] Stacked die
[5] S70 Series (stacked die)
[6] S25FL127S & S25FL128S
[7] FS-S only

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

x4 Serial NOR Flash Memory Portfolio

	QSPI S25FL-L[1] 65-nm FG, 3.0 V	QSPI S25FL-S[2] 65-nm MB, 3.0 V	Semper™ Flash[3] S25HL-T[2] 45-nm MB, 3.0 V	QSPI S25FS-S[2] 65-nm MB, 1.8 V	Semper Flash[3] S25HS-T[2] 45-nm MB, 1.8 V
≥256Mb	**Density** SDR Clock/DDR Clock * Temperature Range All parts supported by Longevity Program unless noted **256Mb** 133 MHz/66 MHz * I, A, V, B, M	**1Gb[5]** 133 MHz/80 MHz * I, A, V, B, M **512Mb** 133 MHz/80 MHz * I, A, V, B, M **256Mb** 133 MHz/80 MHz * I, A, V, B, M	**4Gb[4]** 166 MHz/102 MHz * I, A, V, B, M Q119 **2Gb[4]** Q219 166 MHz/102 MHz * I[8], A[8], V[8], B, M[8] Q418 **1Gb** Q219 166 MHz/102 MHz * I, A, V, B, M **512Mb** Q219 166 MHz/102 MHz * I, A, V, B, M Q419 **256Mb** Q220 166 MHz/102 MHz * I, A, V, B, M	**1Gb[5]** 133 MHz/80 MHz * I, A, V, B, N, M **512Mb** 133 MHz/80 MHz * I, A, V, B, N, M **256Mb** 133 MHz/80 MHz * I, A, V, B, M	**4Gb[4]** 166 MHz/102 MHz * I, A, V, B, M **2Gb[4]** 166 MHz/102 MHz * I, A, V, B, M Q418 **1Gb** Q319 166 MHz/102 MHz * I, A, V, B, M **512Mb** Q119 166 MHz/102 MHz * I, A, V, B, M Q419 **256Mb** Q220 166 MHz/102 MHz * I, A, V, B, M
64–128Mb	**128Mb** 133 MHz/66 MHz * I, A, V, B, M **64Mb** 108 MHz/54 MHz * I, A, V, B, M	**128Mb[6]** 133 MHz/80 MHz * I, A, V, B, M **128Mb[7]** 108 MHz/-- * I, A, V, B		**128Mb** 133 MHz/80 MHz * I, A, V, B, M **64Mb** 133 MHz/80 MHz * I, A, V, B, N, M	

[1] Uniform Sector
[2] Hybrid Sector
[3] With Quad SPI
[4] Stacked die
[5] S70 series (stacked die)
[6] S25FL128S 133-MHz SDR 80-MHz DDR
[7] S25FL127S 108-MHz SDR
[7] Contact Sales

* I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

Parallel NOR Flash Memory Roadmap

Product Family	Density	(Prod) [EOL]
S29GL-T[1] (3.0 V) 45-nm MB	2Gb[3] 1Gb 512Mb	
S29GL-S[1] (3.0 V) 65-nm MB	2Gb[3] 1Gb 512Mb 256Mb 128Mb 64Mb	
S29GL-P[1] (3.0 V) 90-nm MB	256Mb 128Mb	
S29GL-N[1] (3.0 V) 110-nm MB	64Mb 32Mb	
S29PL-J[1, 2] (3.0 V) 110-nm FG	128Mb 64Mb 32Mb	
S29JL-J[2] (3.0 V) 110-nm FG	64Mb 32Mb	
S29AL-J (3.0 V) 110-nm FG	16Mb 8Mb	
S29AS-J (1.8 V) 110-nm FG	16Mb	
S29AS-J (1.8 V) 110-nm FG	8Mb	[Q1'19]

[1] Supports Page Mode
[2] Supports simultaneous read/write operation
[3] S70 series (stacked die)

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Parallel NOR Flash Memory Portfolio

	S29AS-J 110-nm FG, 1.8 V	S29AL-J 110-nm FG, 3.0 V	S29JL-J[1] 110-nm FG, 3.0 V	S29PL-J[1, 2] 110-nm FG, 3.0 V	S29GL-N[2] 110-nm MB, 3.0 V	S29GL-P[2] 90-nm MB, 3.0 V	S29GL-S[2] 65-nm MB, 3.0 V	S29GL-T[2] 45-nm MB, 3.0 V
≥256Mb	**Density** Initial/Page Access * Temperature Range All parts supported by Longevity Program unless noted						**2Gb[3]** 110 ns/20 ns * I, A, V, B **1Gb** 100 ns/15 ns * I, A, V, B **512Mb** 100 ns/15 ns * I, A, V, B	**2Gb[3]** 110 ns/20 ns * I, A, V, B, N **1Gb** 100 ns/15 ns * I, A, V, B, N **512Mb** 100 ns/15 ns * I, A, V, B, N
						256Mb 90 ns/25 ns * I	**256Mb** 90 ns/15 ns * I, A, V, B	
64–128Mb				**128Mb** 60 ns/20 ns * I, A		**128Mb** 90 ns/25 ns * I	**128Mb** 90 ns/15 ns * I, A, V, B	
			64Mb 55 ns/-- * I, A	**64Mb** 55 ns/20 ns * I, A	**64Mb** 90 ns/25 ns * I, A		**64Mb** 70 ns/15 ns * I, A, B	
≤32Mb			**32Mb** 60 ns/-- * I, A	**32Mb** 55 ns/20 ns * I, A	**32Mb** 90 ns/25 ns * I, A			
	16Mb 70 ns/-- * I, A	**16Mb** 55 ns/-- * I, A, N, M						
	8Mb Q119 70 ns/-- * I, A	**8Mb** 55 ns/-- * I, A, N, M						

[1] Supports simultaneous read/write operation
[2] Supports Page Mode
[3] S70 series (stacked die)

* I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
N = Extended: -40°C to +125°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

Burst NOR Flash Memory Roadmap

Product Family	Density	(Prod) [EOL]	2018				2019				2020				2021				2022			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
S29WS-P[1] (1.8 V) 90-nm MB	512Mb 256Mb 128Mb																					
S29NS-P[2] (1.8 V) 90-nm MB	512Mb																					
S29VS-R[3] (1.8 V) 65-nm MB	256Mb 128Mb 64Mb																					
S29XS-R[2] (1.8 V) 65-nm MB	256Mb 128Mb 64Mb																					
S29CD-J[1] (1.8 V) 110-nm MB	32Mb 16Mb																					
S29CL-J[1] (3.0 V) 110-nm MB	32Mb 16Mb																					

[1] Address Data Parallel (ADP) Burst
[2] Address high, Address low, Data Multiplex (AADM) Burst
[3] Address Data Multiplex (ADM) Burst

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Burst NOR Flash Memory Portfolio

	S29CL-J[1] 110-nm FG, 3.0 V	S29CD-J[1] 110-nm FG, 2.5 V	S29XS-R[2] 65-nm MB, 1.8 V	S29VS-R[3] 65-nm MB, 1.8 V	S29NS-P[2] 90-nm MB, 1.8 V	S29WS-P[1] 90-nm MB, 1.8 V
≥256Mb	**Density** Initial Access/SDR Clock * Temp Range	All parts supported by Longevity Program unless noted	**256Mb** 80 ns/108 MHz * W, I	**256Mb** 80 ns/108 MHz * W, I	**512Mb** 80 ns/83 MHz * W	**512Mb** 80 ns/104 MHz * W **256Mb** 80 ns/104 MHz * W
64–128Mb			**128Mb** 80 ns/108 MHz * W, I **64Mb** 80 ns/108 MHz * W, I	**128Mb** 80 ns/108 MHz * W, I **64Mb** 80 ns/108 MHz * W, I		**128Mb** 80 ns/104 MHz * W
≤32Mb	**32Mb** 54 ns/75 MHz * I, A, N, M, H, T **16Mb** 54 ns/66 MHz * I, A, N, M, H, T	**32Mb** 54 ns/75 MHz * I, A, N, M, H, T **16Mb** 54 ns/66 MHz * I, A, N, M, H, T				

[1] Address Data Parallel (ADP) Burst
[2] Address high, Address low, Data Multiplex (AADM) Burst
[3] Address Data Multiplex (ADM) Burst

* W = Wireless: -25°C to +85°C
I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
N = Extended: -40°C to +125°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
T = Automotive, AEC-Q100 Grade 0: -40°C to +150°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

KGD NOR Flash Memory Portfolio[1]

	HyperFlash 3.0 V	HyperFlash 1.8 V	Quad SPI 3.0 V	Quad SPI 1.8 V	Parallel 3.0 V
	Density Initial Access/DDR Clock * Temperature Range		**Density** SDR Clock/DDR Clock * Temperature Range		**Density** Initial/Page Access * Temperature Range
≥256Mb	All parts supported by Longevity Program unless noted				
					GL-S 1Gb 100 ns/15 ns * I, V
	KL-S 512Mb 96 ns/100 MHz * I, V, N	**KS-S 512Mb** 96 ns/166 MHz * I, V, N	**FL-S 512Mb** 133 MHz/80 MHz * I, V		**GL-S 512Mb** 100 ns/15 ns * I, V
	KL-S 256Mb 96 ns/100 MHz * I, V, N	Q119 **KS-S 256Mb** Q319 96 ns /166 MHz * I, V, N	**FL-L 256Mb** 133 MHz/66 MHz * I, V, N	**FS-S 256Mb** 133 MHz/80 MHz * I, V	**GL-S 256Mb** 90 ns/15 ns * I, V
64–128Mb	**KL-S 128Mb** 96 ns/100 MHz * I, V, N	**KS-S 128Mb** Q418 96 ns/166 MHz * I, V, M	**FL-L 128Mb** 133 MHz/66 MHz * I, V, N	**FS-S 128Mb** 133 MHz/80 MHz * I, V	**GL-S 128Mb** 90 ns / 15 ns * I, V
			FL-L 64Mb 108 MHz/54 MHz * I, V, N	**FS-S 64Mb** 133 MHz/80 MHz * I, V, N	
<64Mb					**AL-J 16Mb** 55 ns/-- * I, V, N
					AL-J 8Mb 55 ns/-- * I, V, N

[1] Contact Sales for KGD datasheets

* I = Industrial: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
N = Extended: -40°C to +125°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

CYPRESS EMBEDDED IN TOMORROW™

NAND Flash Memory Family

NAND Flash Memory Family Decoder

S 34 M L 08G 2

Technology:	1 = 4x-nm	2 = 32-nm	3 = 16-nm
Density:	01G = 1Gb 02G = 2Gb	04G = 4Gb 08G = 8Gb	16G = 16Gb
Voltage:	L = 3.0 V	S = 1.8 V	
Family:	M = NAND (Address-Data Multiplexed) S = SecureNAND (Address-Data Multiplexed)		
Series:	34 = NAND		
Prefix:	S		

NAND Flash Memory Roadmap

Product Family	Density	(Prod) [EOL]
S34MS-2 (1.8 V) 32-nm SLC ONFI[1] 1.0	16Gb 8Gb 4Gb 2Gb 1Gb	
S34MS-1 (1.8 V) 4x-nm SLC ONFI[1] 1.0	4Gb 2Gb 1Gb	[Q4'20] [Q4'20] [Q4'20]
S34SL-2 (3.0 V) 32-nm SLC ONFI[1] 1.0	4Gb 2Gb 1Gb	
S34ML-3 (3.0 V) 16-nm SLC ONFI[1] 1.0	16Gb 8Gb 4Gb	(Q1'19) (Q1'19) (Q4'18)
S34ML-2 (3.0 V) 32-nm SLC ONFI[1] 1.0	16Gb 8Gb 4Gb 2Gb 1Gb	
S34ML-1 (3.0 V) 4x-nm SLC ONFI[1] 1.0	8Gb 4Gb 2Gb 1Gb	[Q4'20] [Q4'20] [Q4'20] [Q4'20]

[1] Open NAND Flash Interface

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

SLC NAND Flash Memory Portfolio

	S34ML-1[1] 4x-nm, 3.0 V SLC, ONFI 1.0[2]	S34ML-2[3] 32-nm, 3.0 V SLC, ONFI 1.0	S34ML-3[1] 16-nm, 3.0 V SLC, ONFI 1.0	S34SL-2[3, 4] 32-nm, 3.0 V SLC, ONFI 1.0	S34MS-1[1] 4x-nm, 1.8 V SLC, ONFI 1.0	S34MS-2[3] 32-nm, 1.8 V SLC, ONFI 1.0
8–16Gb	**Density; Bus Width** Interface Bandwidth * Temperature Range All parts supported by Longevity Program unless noted **8Gb; x8** Q420 40 MBps * I, A, V[5], B	**16Gb; x8** 40 MBps * I, A[5], V[5], B[5] **8Gb; x8** 40 MBps * I, A, V, B	**16Gb; x8** Q119 40 MBps * I, A, V, B **8Gb; x8** Q119 40 MBps * I, A, V, B			**16Gb; x8** 40 MBps * I, A[5], V[5], B[5] **8Gb; x8** 40 MBps * I, A, V, B
1–4Gb	**4Gb; x8/16** Q420 40 MBps * I, A, V , B **2Gb; x8/16** Q420 40 MBps * I, A, V, B **1Gb; x8** Q420 40 MBps * I, A, V, B	**4Gb; x8/16** 40 MBps * I, A, V, B **2Gb; x8/16** 40 MBps * I, A[5], V[5], B[5] **1Gb; x8/16** 40 MBps * I, A, V, B	**4Gb; x8** Q418 40 MBps * I, A, V, B	**4Gb; x8** 40 MBps * I, V **2Gb; x8** 40 MBps * I, V[5] **1Gb; x8** 40 MBps * I, V	**4Gb; x8** Q120 40 MBps * I, A[5], V, B **2Gb; x8/16** Q120 40 MBps * I, A[5], V, B **1Gb; x8/16** Q120 40 MBps * I, A[5], V, B	**4Gb; x8/16** 40 MBps * I, A, V, B **2Gb; x8/16** 40 MBps * I, A[5], V[5], B[5] **1Gb; x8/16** 40 MBps * I, A, V, B

[1] 1-bit error-correcting code (ECC)
[2] Open NAND Flash Interface
[3] 4-bit error-correcting code (ECC)
[4] SecureNAND™: Cypress' SLC NAND Flash Memory with full-capacity volatile and nonvolatile block protection
[5] Contact Sales

* I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

Flash and RAM Memory MCP

Flash and RAM Memory MCP Decoder

S 71 N S 512 R D

RAM Density:	A = 16Mb	B = 32Mb	C = 64Mb	D = 128Mb	E = 256Mb
Flash Technology:	N = 110-nm MirrorBit (MB)		P = 90-nm MB	R, S = 65-nm MB	T = 45-nm MB
Flash Density:	032 = 32Mb 064 = 64Mb	128 = 128Mb 256 = 256Mb	512 = 512Mb 01G = 1Gb		
Voltage:	L = 3.0 V	S = 1.8 V			
Family:	G = Page Mode H = High-Performance Serial K = HyperFlash N = Burst Mode Simultaneous Read / Write ADM (Address-Data Multiplexed) V = Burst Mode Simultaneous Read / Write ADM (Address-Data Multiplexed) W = Burst Mode Simultaneous Read / Write ADP (Address-Data Parallel) X = Burst Mode Simultaneous Read / Write AADM (Address-Address-Data Multiplexed)				
Series:	71, 98 = NOR Flash + pSRAM		72 = NOR Flash + DRAM		
Prefix:	S				

Flash and RAM Memory MCP Roadmap

Product Family Flash / RAM	Flash / RAM Density	(Prod) [EOL]
S71HS-T (1.8 V) 45-nm Semper™ Flash / HyperRAM™	1Gb/64Mb 512Mb/64Mb	(TBD) (TBD)
S71KS-S (1.8 V) 65-nm HyperFlash/ HyperRAM	512Mb/64Mb 256Mb/64Mb 128Mb/64Mb	 (TBD) (TBD)
S71HL-T (3.0 V) 45-nm Semper Flash / HyperRAM	1Gb/64Mb 512Mb/64Mb	(TBD) (TBD)
S71KL-S (3.0 V) 65-nm HyperFlash/ HyperRAM	512Mb/64Mb 256Mb/64Mb 128Mb/64Mb	 (TBD)
S98GL-N (3.0 V) 110-nm MB/pSRAM	64Mb/32Mb	
S72XS-R (1.8 V) 65-nm MB/DRAM	256Mb/256Mb	
S72VS-R (1.8 V) 65-nm MB/DRAM	256Mb/256Mb	
S71VS-R (1.8 V) 65-nm MB/pSRAM	256Mb/128Mb 256Mb/64Mb 128Mb/64Mb 128Mb/32Mb 64Mb/32Mb	
S71NS-P (1.8 V) 90-nm MB/pSRAM	512Mb/128Mb	
S71WS-P (1.8 V) 90-nm MB/pSRAM	256Mb/64Mb	

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Flash and RAM Memory MCP Portfolio

	S71WS-P[1] 90-nm MB, 1.8 V	S71NS-P[2] 90-nm MB, 1.8 V	S71VS-R[2] 65-nm MB, 1.8 V	S72VS-R[3] 65-nm MB, 1.8 V	S72XS-R[3] 65-nm MB, 1.8 V	S98GL-N[4] 110-nm MB, 3.0 V	S71KL-S[5] 65-nm MB, 3.0 V	S71HL-T[5] 45-nm MB, 3.0 V	S71KS-S[5] 65-nm MB, 1.8 V	S71HS-T[5] 45-nm MB, 1.8 V
≥256Mb	**Flash Density** **RAM Density** * Temperature Range	All parts supported by Longevity Program unless noted						**1Gb** **64Mb[8]** * I, A, V, B		**1Gb** **64Mb[8]** * I, A, V, B
≥256Mb		**512Mb** **128Mb** * W			**256Mb** **256Mb[6]** * I		**512Mb** **64Mb[8]** * I, A, V, B	**512Mb** **64Mb[8]** * I, A, V, B	**512Mb** **64Mb[8]** * I, A, V, B	**512Mb** **64Mb[8]** * I, A, V, B
≥256Mb			**256Mb** **128Mb** * W	**256Mb** **256Mb** * W	**256Mb** **256Mb[7]** * W, I					
≥256Mb	**256Mb** **64Mb** * W		**256Mb** **64Mb** * W				**256Mb** **64Mb[8]** * I, A, V, B		**256Mb** **64Mb[8]** * I, A, V, B	
64–128Mb			**128Mb** **64Mb** * W				**128Mb** **64Mb[8]** * I, A, V, B		**128Mb** **64Mb[8]** * I, A, V, B	
64–128Mb			**128Mb** **32Mb** * W							
64–128Mb			**64Mb** **32Mb** * W			**64Mb** **32Mb** * I				

[1] ADP (Address Data Parallel) Burst
[2] ADM (Address Data Multiplex) Burst
[3] AADM (Address High, Address Low, Data Multiplex) Burst
[4] Parallel, Page Mode
[5] HyperFlash
[6] DRAM Version 2
[7] DRAM Version 1
[8] HyperRAM™

* W = Wireless: -25°C to +85°C
I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

CYPRESS EMBEDDED IN TOMORROW™

x8 Serial Memory Packages

Family	Interface	Series	Density	Device	SOIC-16 300 mil	BGA24 8 x 8 mm/5 x 5 Ball	BGA24 8 x 6 mm/5 x 5 Ball	KGD
Semper™ Flash	HyperBus™	HS-T	256Mb	S28HS256T			CF	CF
			512Mb	S28HS512T			UD	CF
			1Gb	S28HS01GT		UD		CF
			2Gb	S28HS02GT		CF		
			4Gb	S28HS04GT		CF		
		HS-T	256Mb	S26HS256T			CF	CF
			512Mb	S26HS512T			UD	CF
			1Gb	S26HS01GT		UD		CF
			2Gb	S26HS02GT		CF		
			4Gb	S26HS04GT		CF		
		HL-T	256Mb	S28HL256T			CF	CF
			512Mb	S28HL512T			UD	CF
			1Gb	S28HL01GT		UD		CF
			2Gb	S28HL02GT		CF		
			4Gb	S28HL04GT		CF		
		HL-T	256Mb	S26HL256T			CF	CF
			512Mb	S26HL512T			UD	CF
			1Gb	S26HL01GT		UD		CF
			2Gb	S26HL02GT		CF		
			4Gb	S26HL04GT		CF		
HyperFlash		KS-S	128Mb	S26KS128S			✓	UD
			256Mb	S26KS256S			✓	CF
			512Mb	S26KS512S			✓	CF
		KL-S	128Mb	S26KL128S			✓	CF
			256Mb	S26KL256S			✓	CF
			512Mb	S26KL512S			✓	CF
QSPI	QSPI	FS-S Dual Quad	256Mb	S79FS256S			CF	
			512Mb	S79FS512S			CF	
			1Gb	S79FS01GS			✓	
		FL-S Dual Quad	256Mb	S79FL256S	✓			
			512Mb	S79FL512S	✓			
			1Gb	S79FL01GS			✓	

CF = Contact Factory
UD = Under Development

CYPRESS EMBEDDED IN TOMORROW™

x4 Serial NOR Flash Memory Packages

Family	Interface	Series	Density	Device	SOIC-8 150 mil	SOIC-8 208 mil	SOIC-16 300 mil	WSON 4 x 4 mm	WSON 6 x 5 mm	WSON 8 x 6 mm	BGA24 8 x 8 mm 5 x 5 Ball	BGA24 8 x 6 mm 5 x 5 Ball	BGA24 8 x 6 mm 4 x 6 Ball	KGD
Semper™ Flash	QSPI	HS-T	256Mb	S25HS256T			CF			CF		CF		CF
			512Mb	S25HS512T			UD			UD		UD		CF
			1Gb	S25HS01GT			UD				UD			CF
			2Gb	S25HS02GT							CF			
			4Gb	S25HS04GT							CF			
		HL-T	256Mb	S25HL256T			CF			CF		CF		CF
			512Mb	S25HL512T			UD			UD		UD		CF
			1Gb	S25HL01GT			UD				UD			CF
			2Gb	S25HL02GT							CF			
			4Gb	S25HL04GT							CF			
QSPI		FS-S	64Mb	S25FS064S		✓			✓			✓		✓
			128Mb	S25FS128S		✓	CF		✓	✓		✓	✓	CF
			256Mb	S25FS256S			✓			✓		✓	✓	✓
			512Mb	S25FS512S			✓			✓		✓	✓	CF
			1Gb	S70FS01GS			✓					✓		
		FL-S	128Mb	S25FL127S		✓	✓		✓			✓	✓	
			128Mb	S25FL128S			✓			✓		✓	✓	
			256Mb	S25FL256S			✓			✓		✓	✓	
			512Mb	S25FL512S			✓					✓	✓	✓
			1Gb	S70FL01GS			✓					✓		
		FL-L	64Mb	S25FL064L		✓	✓	✓	✓			✓	✓	CF
			128Mb	S25FL128L		✓	✓		✓			✓	✓	CF
			256Mb	S25FL256L			✓			✓		✓	✓	CF
		FL1-K	16Mb	S25FL116K	✓	✓			✓			✓	✓	✓
			32Mb	S25FL132K	✓	✓		✓	✓			✓	✓	✓
			64Mb	S25FL164K		✓	✓		✓			✓	✓	✓

CF = Contact Factory
UD = Under Development

CYPRESS EMBEDDED IN TOMORROW™

Parallel NOR Flash Memory Packages

Family	Density	Device	48-Ball FBGA (0.8-mm pitch)	48-Ball FBGA (0.5-mm pitch)	56-Ball BGA (0.8-mm pitch)	64-Ball BGA (0.8-mm pitch)	64-Ball Fortified BGA (1.0-mm pitch)	48-Pin TSOP	56-Pin TSOP	KGD
GL-T	512Mb	S29GL512T			✓		✓		✓	
	1Gb	S29GL01GT			✓		✓		✓	
	2Gb	S70GL02GT					✓			
GL-S	64Mb	S29GL064S	✓				✓	✓	✓	
	128Mb	S29GL128S			✓		✓		✓	✓
	256Mb	S29GL256S			✓		✓		✓	✓
	512Mb	S29GL512S			✓		✓		✓	✓
	1Gb	S29GL01GS					✓		✓	✓
	2Gb	S70GL02GS					✓			
GL-P	128Mb	S29GL128P					✓		✓	✓
	256Mb	S29GL256P					✓		✓	✓
GL-N	32Mb	S29GL032N	✓				✓	✓	✓	✓
	64Mb	S29GL064N	✓				✓	✓	✓	✓
PL-J	32Mb	S29PL032J	✓		✓					
	64Mb	S29PL064J	✓		✓					
	128Mb	S29PL127J				✓			✓	✓
JL-J	32Mb	S29JL032J	✓					✓		
	64Mb	S29JL064J	✓					✓		✓
AL-J	8Mb	S29AL008J	✓					✓		✓
	16Mb	S29AL016J	✓				✓	✓		✓
AS-J	8Mb	S29AS008J	✓					✓		✓
	16Mb	S29AS016J	✓	✓				✓		✓

CYPRESS EMBEDDED IN TOMORROW™

Burst NOR Flash Memory Packages

Family	Density	Device	44-Ball FBGA (0.5-mm pitch)	64-Ball BGA (0.5-mm pitch)	84-Ball Fortified BGA (0.8-mm pitch)	80-Ball FBGA (1.0-mm pitch)	80-Pin PQFP	KGD
WS-P	128Mb	S29WS128P			✓			
	256Mb	S29WS256P			✓			
	512Mb	S29WS512P			✓			
NS-P	512Mb	S29NS512P		✓				
VS-R	64Mb	S29VS064R	✓					
	128Mb	S29VS128R	✓					
	256Mb	S29VS256R	✓					
XS-R	64Mb	S29XS064R	✓					
	128Mb	S29XS128R	✓					
	256Mb	S29XS256R	✓					
CD-J	16Mb	S29CD016J				✓	✓	✓
	32Mb	S29CD032J				✓	✓	
CL-J	16Mb	S29CL016J				✓	✓	
	32Mb	S29CL032J				✓	✓	

CYPRESS EMBEDDED IN TOMORROW™

SLC NAND and Secure NAND Flash Memory Packages

Family	Density	Device	63-Ball BGA (0.8-mm pitch)	67-Ball BGA (0.8-mm pitch)	48-Pin TSOP
MS-2	1Gb	S34MS01G2	✓	✓	✓
	2Gb	S34MS02G2	✓	✓	✓
	4Gb	S34MS04G2	✓		✓
	8Gb	S34MS08G2	✓		
	16Gb	S34MS16G2	✓		
MS-1	1Gb	S34MS01G1	✓		
	2Gb	S34MS02G1	✓		✓
	4Gb	S34MS04G1	✓		✓
ML-3	4Gb	S34ML04G3	✓		✓
	8Gb	S34ML08G3	✓		✓
	16Gb	S34ML16G3	✓		✓
ML-2	1Gb	S34ML01G2	✓	✓	✓
	2Gb	S34ML02G2	✓	✓	✓
	4Gb	S34ML04G2	✓		✓
	8Gb	S34ML08G2	✓		✓
	16Gb	S34ML16G2	✓		✓
ML-1	1Gb	S34ML01G1	✓		✓
	2Gb	S34ML02G1	✓		✓
	4Gb	S34ML04G1	✓		✓
	8Gb	S34ML08G1	✓		✓
SL-2	1Gb	S34SL01G2	✓		
	2Gb	S34SL02G2	✓		
	4Gb	S34SL04G2	✓		

CYPRESS EMBEDDED IN TOMORROW™

Flash and RAM Memory MCP Packages

Family	Flash Density	RAM Density	BGA24 8 x 6 mm 5 x 5 Ball	56-Ball Very Thin FBGA (0.5-mm pitch)	56-Ball FBGA (0.8-mm pitch)	84-Ball FBGA (0.8-mm pitch)	130-Ball BGA (0.65-mm pitch)	133-Ball FBGA (0.5-mm pitch)
S71KS-S	128Mb	64Mb	✓					
	256Mb	64Mb	✓					
	512Mb	64Mb	✓					
S71KL-S	128Mb	64Mb	✓					
	256Mb	64Mb	✓					
	512Mb	64Mb	✓					
S98GL-N	64Mb	32Mb			✓			
S72XS-R	256Mb	256Mb						✓
S72VS-R	256Mb	256Mb						✓
S71VS-R	256Mb	128Mb		✓				
	256Mb	64Mb		✓				
	128Mb	64Mb		✓				
	128Mb	32Mb		✓				
	64Mb	32Mb		✓				
S71NS-P	512Mb	128Mb		✓				
S71WS-P	256Mb	64Mb				✓		

CYPRESS EMBEDDED IN TOMORROW™

Military Memory Portfolio

Military Memory Portfolio

Military Memory | Single-Event Latch-Up Immune

	Fast Async SRAM	Sync SRAM		Nonvolatile SRAM	F-RAM™	NOR Flash	
	ECC[1]	NoBL®[2], ECC	QDR®[3]II+/IV	Serial/Parallel I/O	Serial/Parallel I/O, ECC	Serial I/O, ECC	Parallel I/O, ECC
64Mb-1Gb			**CY7C41xKV13** **144Mb**; 667–1066 MHz, 1.3 V, x18/x36, Burst 2, M[4] **CYRS26xKV18** **144Mb**, 1.8 V, 450 MHz, x18/x36, Burst 2/4, M **CYPT154xAV18** **72Mb**, 1.8 V, 250 MHz, x18/x36; Burst 2/4, M			**S70/79FL-S** Q119 **1Gb**; 3.0 V, 133-MHz QSPI, Auto E, M **S25FL-S** Q418 **512Mb**; 3.0 V, 133-MHz QSPI, Auto E, M **S25FL-S** Q418 **128Mb/256Mb**; 3.0 V, 133-MHz QSPI, Auto E, M	**S29GL-S** Q119 **1Gb**; 3.0 V 130ns, x16, Auto E[5], M **S29GL-S** **128Mb-512Mb**; 3.0 V 130ns, x16, Auto E, M **S29GL-S** Q119 **64Mb**; 130 ns/15 ns, 3.0 V, x16, Auto E, M
1Mb-36Mb	**CY7S106x** **16Mb**, 1.8–5.0 V, 10 ns, x8/x16/x32, Auto E, M **CY7S105x** **8Mb**, 1.8–5.0 V, 10 ns, x8/x16/x32, Auto E, M **CY7S104x** **4Mb**, 1.8–5.0 V, 12 ns, x8/x16, Auto E, M	**CY7C144/6xK** **36Mb**, 133–250 MHz, 2.5 V/3.3 V, x18/x36, M **CY7C137/8xK** **18Mb**, 100–250 MHz, 2.5 V/3.3 V, x18/x36, M **CY7C136xK** **9Mb**, 100–250 MHz, 2.5 V/3.3 V, x18/x36, M		**CY14B116x** **16Mb**; 1.8–3.0 V, 25 ns/45 ns x8/x16/x32, M, RTC[6] **CY14B104x** **4Mb**, 1.8–3.0 V, 25 ns/45 ns x8/x16, Auto E, M **CY14B101x** **1Mb**, 1.8–3.0 V, 25 ns/45 ns x8/x16, SPI, Auto E, M, RTC	**CY15B102N** **2Mb**, 2.0–3.6 V, 60 ns, x16, Auto E, M **CY15B102Q** Q418 **2Mb**, 2.0–3.6 V, 40-MHz SPI, Auto E, M **FM25V10** **1Mb**; 2.0–3.6 V, 40-MHz SPI, Auto E, M		
64Kb-256Kb				**STK14CA8C** Q418 **1Mb**; 3.3 V/5.0 V, 35 ns, x8; QML-Q[7] **STK14C88C** Q418 **256Kb**; 3.0 V/5.0 V, 35 ns, x8; QML-Q			

[1] Error-correcting code
[2] No Bus Latency
[3] Quad Data Rate
[4] Military Temperature: −55°C to +125°C
[5] AEC-Q100 -40°C to +125°C
[6] Real-time clock
[7] Qualified Manufacturers List Level Q, per MIL-PRF-38535

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

CYPRESS EMBEDDED IN TOMORROW™

256Kb/1Mb Military nvSRAM

Applications

Military communication and real-time controls, avionics real-time controls and high-reliability data logging

Features

- **Fast Nonvolatile Memory**
  - Access time 35 ns
  - Available in parallel interface for 256Kb and 1Mb densities
  - Unlimited read/write endurance
  - One million store cycles on power fail
- **Specifications**
  - 100 years data retention at +85°C
  - Qualified Manufacturers List Level Q (QML-Q certified) per MIL-PRF-38535
  - Military temperature grade: -55°C to +125°C
- **Packages: Ceramic 32-pin DIP**

Collateral

Preliminary Datasheet: Contact Sales (Available Now)

STK14C88: 256Kb nvSRAM

Availability

Sampling:	Now
Production:	Q418

[1] External capacitor connection
[2] Hardware STORE busy

72Mb QDR®[1]-II+ SRAM

Applications

Payload processing and reconfigurable computing platforms

Features

- **High Performance Memory**
  - Maximum frequency of operation/throughput: 250 MHz/36 Gbps
  - Two independent unidirectional data ports for read and write enable concurrent transactions
  - Maximum throughput with double data rate (DDR) data ports
  - Output impedance matching input (ZQ): Matches the device outputs to system data bus impedance
  - Bit-interleaving to eliminate multi-bit errors
  - I/O signaling standards: 1.5–1.8 V (HSTL)
- **Specifications**
  - Burst sizes: 2 or 4
  - Bus-width configurations: x18 or x36
  - Military temperature grade: -55°C to +125°C
- **Controllers available for Altera/Xilinx/Microsemi FPGAs**
- **Package: 165-pin CCGA[2]**

Collateral

Datasheets: CYPT1542AV18/CYPT1544AV18
CYPT1543AV18/CYPT1545AV18

CYPT154XAV18: Military QDR®II+ SRAM

Availability

Sampling: Now
Production: Now

[1] Quad Data Rate: Four data transfers per clock cycle
[2] Ceramic column grid array package

QDR®-IV SRAM

Applications

Switches and routers, high-performance computing, test equipment, military and aerospace systems

Features

- **Highest Performance Memory**
  - Available in two options: High Performance (RTR 1334 MT/s) and Extreme Performance (RTR 2132 MT/s)
  - Two independent, bidirectional double data rate (DDR)[1] data ports
  - Error-correcting code (ECC) to detect and correct single-bit errors (<0.01 FIT/Mb[2])
  - On-die termination (ODT) to reduce board complexity
  - De-skew training[3] to improve signal-capture timing
- **Specifications**
  - I/O Levels: 1.2–1.25 V (HSTL/SSTL) and 1.1–1.2 V (POD[4])
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **RoHS[5]-Compliant Package**
- **Package: 361-ball flip-chip ball grid array (FCBGA)**

Collateral

Datasheets: CY7C4021KV13/CY7C4041KV13

Family Table

Option	Density	MPN	Maximum Frequency	RTR
QDR-IV HP	72Mb 144Mb	CY7C40x1KV13 CY7C41x1KV13	667 MHz	1,334 MT/s
QDR-IV XP	72Mb 144Mb	CY7C40x2KV13 CY7C41x2KV13	1,066 MHz	2,132 MT/s

QDR-IV

Availability

Production: Now

[1] Two data transfers per clock cycle
[2] The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data
[3] An iterative algorithm for assessing and eliminating the skew (differences in arrival times) between data signals
[4] Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up

Synchronous SRAM with On-Chip ECC

Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features

- **New Features**
  - Available in two modes[1]: Pipeline and Flow-Through
  - SCD and DCD deselect options[2]
  - Error-correcting code (ECC) to detect and correct single-bit errors
- **Specifications**
  - Voltage options: 2.5 V and 3.3 V
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **Packages: 165-ball BGA (w/ and w/o leaded balls) and 100-pin TQFP**

Collateral

Datasheets: CY7C135XKV33/CY7C136XKV33
CY7C137XKV33/CY7C138XKV33
CY7C144XKV33/CY7C146XKV33

Family Table

Option	Density	MPN	RTR	FIT/Mb[3]
Standard Sync with ECC Pipeline	9Mb 18Mb 36Mb	CY7C1360/2K CY7C1370/2K CY7C1440/2K	250 MT/s	<0.01
Standard Sync with ECC Flow-Through	9Mb 18Mb 36Mb	CY7C1361/3K CY7C1371/3K CY7C1441/3K	133 MT/s	<0.01

Synchronous SRAM with ECC

Availability

Production: Now

[1] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[2] Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
[3] The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data

Fast SRAM Family with PowerSnooze[1]

Applications

Programmable logic controller, handheld devices, multifunction printers, computation servers and automotive

Features

- **Error Detection and Correction**
  - Error-correcting code (ECC) logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Specifications**
  - Access time: 10 ns
  - Deep-sleep current: 15 µA for 4Mb
  - Bus-width configurations: x8, x16, and x32
  - Industrial and automotive temperature grades
  - Military temperature grade: -55°C to +125°C
- **Packages: 48-ball BGA (w/ and w/o leaded balls)**

Collateral

Datasheets: CY7S1049G/CY7C1049G
CY7S1059H/CY7C1059H
CY7S1069G/CY7C1069G

Family Table

Density	MPN	Access Time	Deep Sleep Current (maximum at 85ºC)
4Mb	CY7S104x	10 ns	15 µA
8Mb	CY7S105x	10 ns	22 µA
16Mb	CY7S106x	10 ns	22 µA

Fast SRAM with PowerSnooze

Availability

Sampling: Now
Production: Now

[1] A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode

16Mb Parallel nvSRAM

Applications

Industrial automation, programmable logic controllers. gaming machines, industrial data logging, telecom equipment, networking and storage

Features

- **Fast Nonvolatile Memory**
  - Access time (25 ns)
  - Optional real-time clock (RTC) functionality
  - Available in parallel and open NAND Flash Interface (ONFI) Version 1.0 interfaces
  - Unlimited read/write endurance
  - One million store cycles on power fail
- **Specifications**
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- **Packages: 44-pin TSOP, 54-pin TSOP, 165-ball BGA (w/ and w/o leaded balls)**

CY14B116: 16Mb nvSRAM

Collateral

Datasheet: CY14X116L/CY14X116N/CY14X116S

Availability

Sampling: Now
Production: Contact Sales

[1] Crystal connection input
[2] Crystal connection output
[3] Interrupt output/calibration/square wave
[4] External capacitor connection
[5] Hardware STORE busy

2Mb Military SPI F-RAM

Applications

Multifunction printers, industrial controls and automation, medical wearables, test and measurement equipment, smart meters, aerospace and defense applications, missiles and launchers

Features

- **Ultra-Low Power Memory**
  - 40-MHz SPI interface
  - 100-trillion read/write cycle endurance
- **Specifications**
  - Operating voltage range: 2.0–3.6 V
  - Low (20-µA) sleep current at +125°C
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- **Packages: 8-pin TDFN and 8-pin SOIC**

Collateral

Datasheet: CY15B102Q

CY15B102Q: 2Mb SPI F-RAM

Availability

Sampling: Now
Production: Q418

64Mb/128Mb/256Mb/512Mb/1Gb Parallel NOR Flash

Applications

Military systems boot memory
Avionics boot memory

Features

- **High-Reliability Boot Flash Memory**
  - 100 program[1]/sector erase[2] endurance cycles[3] at +125°C
  - >10 years data retention at +125°C
- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Initial access time: 120 ns
  - Page access time: 15 ns
  - Program time (512B): 0.4 ms (typical)
  - Sector erase time (128KB): 410 ms (typical)
  - Military temperature grade: -55°C to +125°C
- **Packages: 64-ball fortified[4] BGA (9 x 9 mm and 13 x 11 mm, w/ and w/o leaded balls)**

Collateral

Datasheet: S29GLXXXS (128M/256M/512M/1G)

S29GLXXXS: Parallel NOR Flash

Availability

Samples: Now
Production: Now (128Mb/256Mb/512Mb) / Q1'19 (1Gb) / Q1'19 (64Mb)

[1] The operation required to change a NOR Flash memory cell state from "1" to "0"
[2] The operation in which all the bytes in a sector of NOR Flash memory are erased simultaneously prior to programming
[3] The number of times a NOR Flash memory sector can be programmed or erased before it wears out
[4] Fortified BGA supports a 1-mm ball pitch
[5] Write protect input
[6] Ready/busy output

128Mb/256Mb/512Mb/1Gb SPI NOR Flash

Applications

Military systems boot memory
Avionics boot memory

Features

- **High-Reliability Boot Flash Memory**
  - 100 program[1]/sector erase[2] endurance cycles[3] at +125°C
  - >10 years data retention at +125°C
- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Single data rate (SDR)[4] clock rate: 104-MHz quad input/output (QIO)[5]
  - Double data rate (DDR)[6] clock rate: 80-MHz QIO
  - Program time (512B): 0.340 ms (typical)
  - Sector erase time (256KB): 520 ms (typical)
  - Military temperature grade: -55°C to +125°C
- **Packages: 24-ball BGA (6 x 8 mm, w/ and w/o leaded balls)**

Collateral

Datasheets: S25FL512S (512Mb)
S25FL128/256S (128Mb/256Mb)

S25/70/79FLXXXS: 512Mb QSPI NOR Flash

Availability

Sampling: Now
Production: Q418 (128/256/512Mb)/Q1'19 (1Gb)

[1] The operation required to change a NOR Flash memory cell state from "1" to "0"
[2] The operation in which all the bytes in a sector of NOR flash memory are erased simultaneously
[3] The number of times a NOR Flash memory sector can be programmed/erased before it wears out
[4] A mode of data transfer in which data is transferred once per clock cycle
[5] An interface that transfers addresses or data on four I/O's simultaneously
[6] A mode of data transfer in which data is transferred twice per clock cycle
[7] Signals used for standard Quad (x4) SPI interface. Refer to the S25FL512S datasheet for signal definitions in the x1 and x2 mode.
[8] RESET# is an optional signal available on 16-pin-SOIC and BGA packages

Aerospace Memory Portfolio

Aerospace Memory Portfolio

Radiation Hardened | Latch-up Immune | QML-V[1] Certified

	Fast Async SRAM		Sync SRAM	Nonvolatile NOR	FRAM	
	Non-ECC[2]	ECC[2]	QDR®-II+/IV	Serial I/O	Serial I/O	Parallel I/O
128Mb-512Mb			**CYRS4141x** **144Mb**; 1.2 V; 667 MHz x18, x36; Burst 2 **CYRS274x** **288Mb**; 1.8 V; 250 MHz x18, x36; Burst 2,4 Q219 **CYRS264x** **144Mb**; 1.8 V; 250 MHz x18, x36; Burst 2,4	Q418 Q219 **CYRS16B512** **512Mb**; 3.0 V DDR DQSPI; 133MHz Q418 Q219 **CYRS16B256** **256Mb**; 3.0 V DDR QSPI; 133MHz		
16Mb-72Mb		**CYRS108x** **64Mb**; 1.8-5.0 V 12 ns; x8, x16, x32 Q418 Q419 **CYRS106x** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32	**CYRS154x** **72Mb**; 1.8 V; 250 MHz x18, x36; Burst 2,4			
2Mb-4Mb	**CYRS104x** **4Mb**; 3.3 V 12 ns; x8	Q418 Q419 **CYRS104x** **4Mb**; 1.8-5.0 V 12 ns; x8, x16, x32			Q418 Q219 **CYRS15B102Q** **2Mb**; 2.0-3.6 V 40 MHz; SPI	**CYRS15x102** **2Mb**; 2.0-3.6 V 60 ns; x16

[1] Qualified Manufacturers List Level V, per military specification MIL-PRF-38535
[2] Error-correcting code

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

72Mb QDR®-II+ SRAM with RadStop™[1]

Applications

Payload processing and reconfigurable computing platforms

Features

- **Maximum frequency of operation/throughput: 250 MHz/36 Gbps**
- **Burst sizes: 2, 4**
- **Bus-width configurations: x18, x36**
- **Military temperature grade: –55°C to +125°C**
- **Two independent unidirectional data ports for read/write enable concurrent transactions**
- **Maximum throughput with double data rate (DDR) data ports**
- **Output impedance matching input (ZQ) matches the device outputs to system data bus impedance**
- **Bit-interleaving to eliminate multi-bit errors**
- **I/O signaling standards: 1.5 –1.8 V (HSTL)**
- **Controller available for Xilinx and Microsemi FPGAs**
- **Total ionizing dose: 300 Krad**
- **Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm sq/mg**
- **Heavy-ION single-event upset (SEU): 1.34E-07 (geosynchronous) error/bit-day**
- **QML-V[2]-qualified (DLAM[2] part number: 5962F11201/02VXA)**

Collateral

Cypress Datasheet: 72-Mbit SRAMs w/ RadStop™

DLAM Datasheet: 72-Mbit SRAMs w/ RadStop

CYRS154XAV18: Radiation Hard QDR-II+ SRAM

Availability

Non-Space-Qualified Prototypes (CYPT154x): Now

QML-V Space-Qualified Devices (CYRS154x): Now

[1] Cypress's proprietary design and process technology that increases radiation-resistance
[2] Qualified Manufacturers List Level V, per military specification MIL-PRF-38535
[3] Defense Logistics Agency Land and Maritime, Columbus, OH

4Mb Fast SRAM with RadStop™[1]

Applications

Payload processing, sensors and switches

Features

- **Access time: 10 ns (85°C), 12 ns (125°C)**
- **Bus-width configuration: x8**
- **Operating voltage: 3.3 V**
- **Military temperature grade: –55°C to +125°C**
- **Bit-interleaving to eliminate multi-bit errors**
- **Package: 36-pin ceramic flat pack (CFP)**
- **Total ionizing dose: 300 Krad**
- **Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm sq/mg**
- **Heavy-ION single-event upset (SEU): 5.0E-08 (geosynchronous) error/bit-day**
- **QML-V[2] qualified (DLAM[3] part number: 5962F1123501VXC)**

CYRS1049DV33: Radiation Hard 4M Fast Asynchronous SRAM

Collateral

Cypress Datasheet: 4-Mbit SRAM w/ RadStop™

DLAM6 Datasheet: 4-Mbit SRAM w/ RadStop

Availability

Non-Space-Qualified Prototypes (CYPT1049): Now

QML-V Space-Qualified Devices (CYRS1049): Now

[1] Proprietary Cypress design and process technology that increases radiation-resistance
[2] Qualified Manufacturers List Level V, per military specification MIL-PRF-38535
[3] Defense Logistics Agency Land and Maritime, Columbus, OH

Energy Harvesting PMIC Portfolio

Energy Harvesting PMIC[1] Portfolio

Series Solar Cell by Panasonic (AM-1801)

Single Solar Cell by Ningbo Hebe Solar (HSC125155)

TEG by Micropelt (TGP-651)

	Wearable Activity Monitor	Residential WSNs[2] for HVAC[3], Level of Light Emitted, Temperature, Humidity, Motion	Building WSNs for HVAC, Level of Light Emitted, Temperature, Humidity, Motion, BLE[4] Beacon[5]	Industrial WSNs for Infrastructure, Agriculture, Transportation, Factory Automation, Animal Monitoring	
	Indoor/Outdoor			Indoor	Outdoor
Light Series Solar Cell	**S6AE101A** Linear, Power Gating[6], Multiplexer[7], 10-pin QFN	**S6AE101A** Linear, Power Gating, Multiplexer, 10-pin QFN	**S6AE102A** Linear, Power Gating, Multiplexer, LDO[8], Comparator, 20-pin QFN	**S6AE103A** Linear, PowerGating, Multiplexer, LDO, Timer, Comparator, 24-pin QFN	
Light Single Solar Cell					**CY39C831** Boost DC/DC, MPPT[9], Li-ion Protection, 40-pin QFN
Heat Thermoelectric Generator (TEG)			**CY39C831** Boost DC/DC, MPPT, Li-ion Protection, 40-pin QFN		

Market Segment

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

[1] Power Management IC
[2] Wireless sensor nodes
[3] Heating, ventilation, air conditioning
[4] Bluetooth Low Energy
[5] A wireless device that transmits data (e.g., signal strength and ID) over a periodic radio signal from a known location
[6] Output power control circuit that controls power provided to the system load
[7] Power source switch circuit for primary battery or energy harvesting device
[8] Low dropout regulator
[9] Maximum power point tracking

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S6AE101A

Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications

Series solar cell energy harvesting[1] and wireless sensor nodes[2]

Features

- **Ultra-Low Power**
  - Enables 1 cm^2 minimum solar cell size for startup operation[3]
- **Input Voltage Range**
  - 2.0–5.5 V (series solar cell and primary battery)
- **1.1–5.2-V Output Voltage Range**
- **250-nA Quiescent Current[4]**
- **1.2-µW Startup Power**
- **Power Gating[5] Switch Circuit**
- **Storage Control Circuit**
- **Multiplexer[6] Circuit (battery vs. solar cell)**
- **Overvoltage Protection (OVP)**
- **Packages**
  - 3.0 mm x 3.0 mm 10-pin SON

Collateral

Datasheet: S6AE101A Datasheet

Development Kits: Solar-Powered IoT Device Kit

S6AE10xA Evaluation Board

S6AE101A: Solar-Optimized Energy Harvesting PMIC

Availability

Production: Now

[1] The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
[2] A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
[3] Estimate based on solar cell power = 2 µW/cm^2 at 100 lx
[4] Current consumed at no load condition
[5] Output power control circuit that controls power provided to the system load
[6] Power source switch circuit for primary battery and Energy Harvesting Device
[7] Voltage reference circuit for internal block

S6AE102A

Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications

Series solar cell energy harvesting[1] and wireless sensor nodes[2]

Features

- **Ultra-Low Power**
  - Enables 1 cm^2 minimum solar cell size for startup operation[3]
- **Input Voltage Range**
  - Series solar cell: 2.0–5.5 V (series solar cell and primary battery)
- **1.1–5.2-V Output Voltage Range**
- **280-nA Quiescent Current[4]**
- **1.2-µW Startup Power**
- **400-nA Low Quiescent Current Low Dropout Regulator (LDO)**
- **Dual-Channel Power Gating[5] Switch Circuit with Interrupt Request (IRQ) Control Function for Power Management**
- **Signal Output Circuit of Power Gating Switch Control**
- **Multiplexer[6] Circuit (battery vs. solar cell)**
- **Hybrid Storage Control Circuit[7] and Overvoltage Protection (OVP)**
- **Packages**
  - 4.0 mm x 4.0 mm 20-pin QFN

Collateral

Datasheet: S6AE102A Datasheet

Development Kits: S6AE10xA Evaluation Board, CYALKIT-E04

S6AE102A: Solar-Optimized Energy Harvesting PMIC

Availability

Production: Now

[1] The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
[2] A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
[3] Estimate based on solar cell power = 2 µW/cm^2 at 100 lx
[4] Current consumed at no load condition
[5] Output power control circuit that controls power provided to the system load
[6] Power source switch circuit for primary battery or series solar cell
[7] Uses a small and large capacitor to automatically store excess power for backup
[8] Voltage reference circuit for internal block

S6AE103A

Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications

Series solar cell energy harvesting[1] and wireless sensor nodes[2]

Features

- **Ultra-Low Power**
  - Enables 1 cm^2 minimum solar cell size for startup operation[3]
- **Input Voltage Range**
  - 2.0-5.5 V (series solar cell and primary battery)
- **1.1–5.2 V Output Voltage Range**
- **280 nA Quiescent Current[4]**
- **1.2 µW Startup Power**
- **400 nA Low Quiescent Current Low Dropout Regulator (LDO)**
- **30 nA Low Consumption Current CR Timer[5]**
- **20 nA General-Purpose Low Consumption Current Comparator**
- **Dual-Channel Power Gating[6] Switch Circuit with Interrupt Request (IRQ) Control Function for Power Management**
- **Signal Output Circuit of Power Gating Switch Control**
- **Multiplexer[7] Circuit (battery vs. solar cell)**
- **Hybrid Storage Control Circuit[8] and Overvoltage Protection (OVP)**
- **Packages**
  - 4.0 mm x 4.0 mm 20-pin QFN

Collateral

Datasheet: S6AE103A Datasheet

Development Kits: S6AE10xA Evaluation Board, CYALKIT-E04

S6AE103A: Solar-Optimized Energy Harvesting PMIC

Availability

Production: Now

[1] The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
[2] A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
[3] Estimate based on solar cell power = 2 µW/cm^2 at 100 lx
[4] Current consumed at no load condition
[6] Output power control circuit that controls power provided to the system load
[7] Power source switch circuit for primary battery or series solar cell
[8] Uses a small and large capacitor to automatically store excess power for backup
[9] Voltage reference circuit for internal block

CY39C831

General Purpose Energy Harvesting Power Management IC (PMIC)

Applications

Single solar cell energy harvesting[1], thermoelectric generator[2] energy harvesting and wireless sensor nodes[3]

Features

- **Ultra-Low-Voltage Startup Boost DC/DC Converter**
- **0.3–4.75-V Input Voltage Range**
- **0.35-V Startup Voltage**
- **Output Voltage (constant voltage mode only)**
  - 3.0 V, 3.3 V, 3.6 V, 4.1 V, 4.5 V and 5.0 V
- **32-µA Quiescent Current[4]**
- **Output Current**
  - 8 mA (V_{DD} = 0.6 V, V_{OUT} = 3.3 V) and 80 mA (V_{DD} = 3.0 V, V_{OUT} = 3.3 V)
- **200-mA Input Peak Current Limit**
- **Built-In Maximum Power Point Tracking (MPPT)[5] Function**
- **Built-In Li-ion Charge Function**
- **Input and Output Power Good Monitoring**
- **Package**
  - 6.0 mm x 6.0 mm 40-pin QFN

Collateral

Datasheet: CY39C831 Datasheet

Development Kits: CY39C831 Evaluation Board

CY39C811: General Purpose Energy Harvesting PMIC

Availability

Production: Now

[1] The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
[2] Power Generation Device using heat
[3] A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
[4] Current consumed at no load condition
[5] Maximum Power Point Tracking maximizes the Energy Harvest by adjusting current drawn from a solar panel
[6] Undervoltage lockout
[7] Band Gap Reference

Cypress Roadmap: Automotive Products

Cypress Automotive Roadmaps Slide Index

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Automotive TrueTouch® Roadmap

Automotive Portfolio: TrueTouch®

Active Touch Area	Gen6			Gen7
	Touchscreen			Next Generation
	Gestures, AMS[1] Thick Glove[2] or Thick Overlay	In-Cell[3], Gestures, AMS Thick Glove[6] or Thick/Curved Overlay	SLIM[4], Force Touch[5], Gestures, AMS Thick Glove or Thick/Curved Overlay	
	10 Finger, AutoArmor™[7], DualSense™[8], H_2O[9], Glove Touch[10], Grades: A[11] and S[12]			
> 12"	CYAT8168X 88 I/O, 100-Hz RR[13]	CYAT8268X 54 I/O, 100-Hz RR	CYAT8X68X 88 I/O, 100-Hz RR	CYAT8X7XX 98 I/O, 100 Hz-RR
> 12"	CYAT8168X 77/71 I/O[14], 120-Hz RR	CYAT8268X 46/39 I/O, 120-Hz RR	CYAT8X68X 77/71 I/O, 120-Hz RR	
7–12"	CYAT8168X 61 I/O, 120-Hz RR	CYAT8268X 31 I/O, 120-Hz RR	CYAT8X68X 61 I/O, 120-Hz RR	CYAT8X7XX 88/77/71 I/O, 100 Hz-RR
3–8"	CYAT8165X 48 I/O, 100-Hz RR	CYAT8268X 17 I/O, 120-Hz RR	CYAT8X65X 48 I/O, 100-Hz RR	
3–8"	CYAT816XX 36 I/O, 120-Hz RR		CYAT8X6XX 36 I/O, 100-Hz RR	

[1] Automatic Mode Switching
[2] 1-mm to 5-mm glove thickness (ski gloves)
[3] A type of sensor stack-up in which the RX sensor is inside the LCD module under the color-filter glass
[4] Single-Layer Independent Multi-Touch
[5] The ability of touchscreen to distinguish between different levels of force being applied on the touchscreen
[6] Less than 1-mm glove thickness (normal leather gloves)
[7] Enables compliance with chip-level emission, immunity and system-level specifications
[8] Self-Capacitance + Mutual-Capacitance
[9] Waterproofing and wet-finger tracking
[10] A feature that allows the detection of gloved fingers on a touch sensor
[11] AEC-Q100: -40°C to +85°C
[12] AEC-Q100: -40°C to +105°C
[13] Refresh rate
[14] Number of available I/Os depends on package selection

	Concept	Development	Sampling	Production
Industrial				
Automotive				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

Automotive Portfolio: TrueTouch® Software[1]

Software	MPN	PSoC® Designer™	TrueTouch® Host Emulator[2]	TrueTouch Driver for Android[3]	Manufacturing Test Kit[4]
Current Version		5.4 SP1	3.4.20	3.5	1.9.10
Gen 1	CY8CTMA120	Production			
	CY8CTMG120	Production			
Gen 3	CY8CTMA616		Production	TTDA 2.5.1 Production	Production
	CY8CTMA884		Production		Production
Gen 4	CY8CTMA460		Production	TTDA 2.5 Production	Production
	CY8CTMA461		Production		Production
	CY8CTMA768		Production		Production
	CY8CTMA1036		Production		Production
Gen 6	CYAT8165X-48		Production	Contact Sales	Production
	CYAT8168X-61		Production		Production
	CYAT8168X-71		Production		Production
	CYAT8168X-77		Production		Production
	CYAT8168X-88		Production		Production
Gen7	CYAT8X7XX		Production	Contact Sales	Production

Contact Cypress Sales for the latest TrueTouch software, drivers and tools

[1] PSoC Designer, TTHE and MTK releases are backward compatible. The latest version is recommended for new designs.
[2] TrueTouch Host Emulator (TTHE) is a front-end tool used to configure, tune, debug and demonstrate TrueTouch devices
[3] TrueTouch Driver for Android (TTDA) is the driver for Android that translates touch information into Linux/Android events
[4] TrueTouch Manufacturing Test Kit (MTK) enables customers and ITO partners to test touch panels that use Cypress TrueTouch controllers through the manufacturing flow

CYAT8168X

Automotive TrueTouch® Gen6 Family

Applications

Large touchscreen human machine interface (HMI) systems

Features

- **Advanced User Interface**
  - Waterproofing[1]: Works with water droplets, condensation, sweat and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
- **Proprietary Analog Front End[2] with AutoArmor™[3]**
  - True 5-V TX-Boost™ with Multi-Phase TX[4]
  - 54 Receive Channels to support ≥100-Hz refresh rates
  - DualSense™: Self[5]- and mutual[6]-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications
- **System Solutions**
  - Manufacturing test kits for production testing
- **Package**
  - 128-pin TQFP, 100-pin TQFP

Collateral

Datasheet and Design Guide: Contact Sales or automotive@cypress.com

Availability

Production: Now

[1] The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
[2] Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
[3] Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
[4] A scanning method used to drive multiple TX lines simultaneously
[5] The capacitance of a row or column line in a touchscreen sensor
[6] The capacitance between a row and a column in a touchscreen sensor
[7] Interrupt

CYAT8165X

Automotive TrueTouch® Gen6 Family

Applications

Small and medium touchscreen human machine interface (HMI) systems

Features

- **Advanced User Interface**
  - Waterproofing[1]: Works with water droplets, condensation, sweat and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
- **Proprietary Analog Front End[2] with AutoArmor™[3]**
  - True 5-V TX-Boost™ with Multi-Phase TX[4]
  - 17 Receive Channels to support ≥100-Hz refresh rates
  - DualSense™: Self[5]- and mutual[6]-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications
- **System Solutions**
  - Manufacturing test kits for production testing
- **Package**
  - 100-pin TQFP and 64-pin TQFP

Collateral

Datasheet and Design Guide: Contact Sales or automotive@cypress.com

Availability

Sampling: 64 TQFP (Now)

Production: 100 TQFP (Now), 64 TQFP (Q1 2019)

[1] The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
[2] Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
[3] Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
[4] A scanning method used to drive multiple TX lines simultaneously
[5] The capacitance of a row or column line in a touchscreen sensor
[6] The capacitance between a row and a column in a touchscreen sensor
[7] Interrupt

CYAT6165X

Automotive TrueTouch® Gen6 Family

Applications

Slider human machine interface (HMI) systems

Features

- **Advanced User Interface**
  - Waterproofing[1]: Works with water droplets, condensation, sweat and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
  - Typical refresh rate of 200 Hz
  - Low-power wake-up button: Typical power consumption of 50 µA
- **Proprietary Analog Front End[2] with AutoArmor™[3]**
  - True 5-V TX-Boost™ with Multi-Phase TX[4]
  - 17 Receive Channels to support ≥200-Hz refresh rates
  - DualSense™: Self[5]- and mutual[6]-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications
- **System Solutions**
  - Manufacturing test kits for production testing
- **Package**
  - 56-pin QFN wettable flank, 8 × 8 × 1 mm, 0.5-mm pin-pitch
  - 64-pin TQFP, 10 x 10 x 1.4 mm, 0.5-mm pin-pitch

Collateral

Datasheet and Design Guide: Contact Sales or automotive@cypress.com

Availability

Sampling: 64 TQFP (Now)

Production: 56 QFN (Now), 64 TQFP (Q1 2019)

[1] The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
[2] Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
[3] Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
[4] A scanning method used to drive multiple TX lines simultaneously
[5] The capacitance of a row or column line in a touchscreen sensor
[6] The capacitance between a row and a column in a touchscreen sensor
[7] Interrupt

CYAT817XX

Automotive TrueTouch® Gen7 Family

Applications

Integrated touchscreen human machine interface (HMI) systems with multimodal feedback

Features

- **Advanced User Interface**
  - 50-mm hover[1] performance and force touch[2] support
  - Supports low-power CapSense®[3] wake-up button
  - 4x timer/counter/pulse-width modulator (TCPWM) blocks for haptic feedback controls
  - 1x I²S block for acoustic feedback
  - Parallel reporting of touch data via SCB[4] or CAN blocks
  - Includes a Crypto block for optional data encryption
- **Proprietary Analog Front End[5] with AutoArmor™[6]**
  - True 5-V TX-Boost™ with multi-phase TX
  - 64 receive channels to support ≥100-Hz refresh rates
  - Multi-phase self-capacitance methodology aids in meeting EMI/EMC requirements without performance degradation
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), ESD (IEC 62132) and system-level (CISPR 25) specifications
- **Packages**
  - 128-pin TQFP, 100-pin TQFP

Collateral

Datasheet and Design Guide: Contact Sales or automotive@cypress.com

Availability

Production: Now

[1] A feature allowing the detection of fingers hovering over the touchscreen sensor
[2] The ability of a touchscreen sensor to distinguish between different levels of force being applied on the touchscreen
[3] Cypress' touch-sensing user interface solution. The industry's No. 1 solution in sales by 4x over No. 2 due to superior performance
[4] Serial communication block, configurable as SPI, I²C or UART
[6] Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
[6] Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements

Automotive TrueTouch Packages

Family	Package	QFN	TQFP		
	Pins	56	64	100	128
	Body Size (mm)	8 x 8	10 x 10	14 x 14	14 x 20
	Pitch (mm)	0.5	0.5	0.5	0.5
Gen 4	CY8CTMA460	✓[1]		✓	
	CY8CTMA461	✓[1]		✓	
	CY8CTMA768			✓	
	CY8CTMA1036			✓	
Gen 6	CYAT8165X-48			✓	
	CYAT8168X-61			✓	
	CYAT8168X-71			✓	
	CYAT8168X-77			✓	
	CYAT8168X-88				✓

[1] Wettable flanks package to allow automated optical inspection (AOI)

Automotive PSoC® Roadmap

Automotive PSoC and MCU Portfolio

8-Bit	32-Bit Arm® Cortex®-M0/M0+	32-Bit Arm Cortex®-M3	32-Bit Arm Cortex®-M4	32-Bit Arm Cortex®-M7
High Analog Integration	**Ultra-Low-Power 8-/16-Bit Replacement**	**Mid-Range Performance**	**High Performance**	**Next Generation**

Analog and Digital Integration

Programmable System-on-Chip (PSoC) is a brand of Cypress MCUs for the broad-base embedded market that delivers an Arm Cortex-M CPU (PSoC 4+) with unique software-defined peripherals and CapSense capacitive sensing

Flexible MCU (FM) is a portfolio of high-performance Arm® Cortex®-M-based MCUs for industrial and consumer applications

PSoC 7
Cortex®-M7
NDA Required, Contact Sales

PSoC 6 HMI
Cortex®-M4 and Cortex®-M0+
NDA Required, Contact Sales

PSoC 4
Cortex®-M0/M0+
48 MHz, 256KB Flash
Up to 13 PAB[1], 20 PDB[2], 98 I/Os

PSoC 5LP
Cortex®-M3
80 MHz, 256KB Flash
20 PAB, 30 PDB, 72 I/Os

FM4 MCUs
Cortex®-M4
200 MHz, 2MB Flash, 190 I/Os

PSoC 3
8051 CPU
67 MHz, 64KB Flash
Up to 19 PAB, 30 PDB, 72 I/Os

PSoC Analog Coprocessor CY8C4Axx
48 MHz, 32KB Flash
Up to 12 PAB, 11 PDB, 38 I/Os

FM3 MCUs
Cortex®-M3
144 MHz, 1.5MB Flash, 154 I/Os

PSoC 1
M8C CPU
24 MHz, 32KB Flash
16 PAB, 16 PDB, 64 I/Os

FM0+ MCUs
Cortex®-M0+
40 MHz, 512KB Flash, 102 I/Os

8FX
8-bit RISC MCU
16 MHz, 32–50KB Flash

[1] A programmable analog block that is configured using PSoC software to create analog front ends, signal conditioning circuits with opamps and filters
[2] A programmable digital block that is configured using PSoC software to implement custom digital peripherals and glue logic

	Concept	Development	Sampling	Production
Industrial				
Automotive				
Availability			QQYY	QQYY

Automotive Portfolio: PSoC® 1

M8C CPU | 24 MHz

Performance

PSoC MCU	Programmable Digital	Intelligent Analog	Performance Analog
			CY8C29x66 32K/2K[1], 44 GPIOs[2] 1x14-bit ΔΣ ADC[3] Grades: A[4] and E[5]
			CY8C27x43 32K/2K, 44 GPIOs CapSense®, 1x14-bit ΔΣ ADC
		CY8C24894 16K/1K, 56 GPIOs CapSense, 2x14-bit SAR ADC Grade: A	**CY8C28xxx** 16K/1K, 44 GPIOs CapSense, 4x14-bit ΔΣ ADC
		CY8C2xx45 16K/1K, 38 GPIOs CapSense, 1x10-bit SAR ADC Grades: A and E	
	CY8C21x34 8K/0.5K, 28 GPIOs CapSense, 1x10-bit ADC Grades: A and E	**CY8C24x23** 4K/0.25K, 24 GPIOs CapSense, 1x14-bit ΔΣ ADC Grades: A and E	
	CY8C23x33 8K/0.25K, 26 GPIOs CapSense, 1x 8-bit SAR ADC		
CY8C24x93 32K/2K, 36 GPIOs 1x10-bit ADC	**CY8C21x23** 4K/0.25K, 16 GPIOs 1x10-bit ADC		

[1] Flash KB/SRAM KB
[2] General-purpose input/output pins
[3] Analog-to-digital converter: Includes incremental, successive approximation register (SAR) or Delta-Sigma (ΔΣ) ADCs

[4] AEC-Q100: -40°C to +85°C
[5] AEC-Q100: -40°C to +125°C

	Concept	Development	Sampling	Production
Industrial				
Automotive				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

Automotive Portfolio: PSoC® 4

Flexibility | CapSense® | Ease-of-Use

PSoC MCU PSoC 4000	Intelligent Analog PSoC 4100				Programmable Digital PSoC 4200		Sense Anything PSoC 4700
	S = S-Series	M = M-Series	L = L-Series				
				CY8C4148-S 48-MHz M0+, 256K/32K[1] **NDA Contact Sales**		**CY8C4248-L** 48-MHz M0, 256K/32K CMP[2], Opamp, ADC SCB, IDAC[3], UDB[4], CAN[5] USB	
	CY8C4127-M 24-MHz M0, 128K/16K **NDA Contact Sales** Q119	**CY8C4127-S** 24-MHz M0+, 128K/16K **NDA Contact Sales** Q119	**CY8C4147-S** 48-MHz M0+, 128K/16K **NDA Contact Sales** Q119	**CY8C4147-S3** 48-MHz M0+, 128K/16K **NDA Contact Sales**	**CY8C4247-M** 48-MHz M0, 128K/16K **NDA Contact Sales** Q119	**CY8C4247-L** 48-MHz M0, 128K/16K CMP, Opamp, ADC SCB, IDAC, UDB, CAN USB	
	CY8C4126-M 24-MHz M0, 64K/8K **NDA Contact Sales** Q119	**CY8C4126-S** 24-MHz M0+, 64K/8K CMP, Opamp, ADC SCB, IDAC, Smart I/O Grades: A, S and E	**CY8C4146-S** 48-MHz M0+, 64K/8K CMP, Opamp, ADC SCB, IDAC, Smart I/O Grades: A, S and E		**CY8C4246-M** 48-MHz M0, 64K/8K **NDA Contact Sales** Q119	**CY8C4246-L** 48-MHz M0, 64K/8K CMP, Opamp, ADC SCB, IDAC, UDB, CAN USB	
CY8C4045-S 48-MHz M0+, 32K/4K CMP, ADC, SCB IDAC, Smart I/O Grades: A and S	**CY8C4125** 24-MHz M0, 32K/4K CMP, Opamp, ADC SCB, IDAC Grades: A[6] and S[7]	**CY8C4125-S** 24-MHz M0+, 32K/4K CMP, Opamp, ADC SCB, IDAC, Smart I/O Grades: A, S and E			**CY8C4245** 48-MHz M0, 32K/4K CMP, Opamp, ADC SCB, IDAC, UDB Grades: A and S		**CY8C47xx-S** 48-MHz M0+, 32K/4K **NDA Contact Sales** Q119
CY8C4024-S 24-MHz M0+, 16K/2K CMP, ADC, SCB IDAC, Smart I/O Grades: A and S	**CY8C4124** 24-MHz M0, 16K/4K CMP, Opamp, ADC SCB, IDAC Grades: A and S	**CY8C4124-S** 24-MHz M0+, 16K/2K CMP, Opamp, ADC SCB, IDAC, Smart I/O Grades: A, S and E			**CY8C4244** 48-MHz M0, 16K/4K CMP, Opamp, ADC SCB, IDAC, UDB Grades: A and S		
CY8C4014 16-MHz M0, 16K/2K CMP, I²C, IDAC Grades: A and S							

Flash

[1] Flash KB/SRAM KB
[2] Comparator
[3] Current-output DAC
[4] Universal digital block
[5] Controller area network
[6] AEC-Q100: -40°C to +85°C
[7] AEC-Q100: -40°C to +105°C

	Concept	Development	Sampling	Production
Industrial				
Automotive				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

Automotive Portfolio: PSoC® Software[1]

Software	PSoC Creator™[2]	PSoC Designer™[3]	PSoC Programmer[4]	EZ-Click™[5]
Current Version	4.2	5.4 SP1	3.27.3	2.0 SP2
PSoC 1		Production	Production	
PSoC 4	Production		Production	

Download the latest PSoC software version here

[1] All software and tool releases are backward compatible. The latest versions are recommended for new designs
[2] PSoC Creator is an Integrated Design Environment (IDE) that allows concurrent hardware and firmware design of PSoC 3 and PSoC 4 systems
[3] PSoC Designer is an IDE that enables firmware design using a library of precharacterized peripherals for PSoC 1 systems
[4] PSoC Programmer can be used with PSoC Designer and PSoC Creator to program and debug any design onto a PSoC device
[5] EZ-Click is a Windows® GUI-based tool that enables development of CapSense MBR solutions. It allows you to set up sensor configuration, apply global system properties, monitor real-time sensor output, and run production-line system diagnostics

PSoC® 4000S-Series

PSoC MCU

Applications

User interface for infotainment systems, user interface for heating, ventilation, air conditioning

Features

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 32KB Flash
  - 4KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 10-bit, 46.8-ksps single-slope analog-to-digital converter (ADC)[1]
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Two serial communication blocks (SCB) that are configurable as I²C, SPI, UART or LIN Slave
- **Packages**
  - 24-pin QFN and 28-pin SSOP
- **I/O Subsystem**
  - Up to 24 GPIOs, including 16 Smart I/Os[2]

Collateral

Datasheet: PSoC 4000S

Availability

Sampling: Now **Production:** Now

[1] A simple ADC used to measure slow-moving signals
[2] Embedded programmable digital logic in the I/O subsystem

PSoC® 4100S-Series

Intelligent Analog

Applications

User interface for heating, ventilation, air conditioning, MCU and discrete analog replacement

Features

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 64KB Flash
  - 8KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-ksps single-slope ADC[1]
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, UART or LIN Slave
- **Packages**
  - 28-pin SSOP and 40-pin QFN
- **I/O Subsystem**
  - Up to 34 GPIOs, including 16 Smart I/Os[2]

Collateral

Datasheet: PSoC 4100S

[1] A simple ADC used to measure slow-moving signals [2] Embedded programmable digital logic in the I/O subsystem

Availability

Sampling: Now **Production:** Now

PSoC® 4100S Plus-Series

Intelligent Analog

Applications

User interface for HMI applications, Body Control and HVAC applications

Features

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with DMA controller and real-time clock (RTC)
  - 128KB Flash and 16KB SRAM
  - External MHz oscillator (ECO) with PLL and 32KHz watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-ksps single-slope ADC[1]
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I²C, SPI, UART or LIN Slave
- **One Controller Area Network (CAN) Controller**
- **Packages**
  - 40-pin QFN and 64-pin TQFP
- **I/O Subsystem**
  - Up to 54 GPIOs, including 24 Smart I/Os[2]

Collateral

Datasheet: Contact Sales

[1] A simple ADC used to measure slow-moving signals [2] Embedded programmable digital logic in the I/O subsystem

Availability

Sampling: 64-pin TQFP (Now), 40-pin QFN (Q1 2019)

Production: 64-pin TQFP (Q1 2019), 40-pin QFN (Q2 2019)

PSoC® 4100M-Series

Intelligent Analog

Applications

User interface for HMI applications, body Control and HVAC applications

Features

- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM
- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Msps successive approximation register (SAR) ADC
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)
- **Programmable Digital Blocks**
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Packages**
  - 48-pin LQFP and 64-pin TQFP
- **I/O Subsystem**
  - Up to 51 GPIOs

Collateral

Datasheet: Contact Sales

Availability

Sampling: Now **Production**: Q1 2019

PSoC® 4200M-Series
Programmable Digital

Applications

User interface for HMI applications, body Control and HVAC applications

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM
- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I^2C master or slave, SPI master or slave, or UART
- **Two Controller Area Network (CAN) Controllers**
- **Packages**
  - 48-pin LQFP, 56-pin QFN and 64-pin TQFP

Collateral

Datasheet: Contact Sales

Availability

Sampling: Now **Production**: Q1 2019

Automotive PSoC Packages

Family	Package	QFN			SOIC	SSOP		
	Pins	24	40	56	16	20	28	48
	Body Size (mm)	4 x 4	6 x 6	8 x 8	3.8 x 9.9	5.3 x 7.3	5.3 x 10.3	7.5 x 15.8
	Pitch (mm)	0.5	0.5	0.5	1.27	0.65	0.65	0.635
PSoC 1	2XX45						✓	✓
	21X34					✓	✓	
	24X23					✓	✓	
	24894			✓				
	29X66						✓	✓
PSoC 4	4000	✓			✓			
	41/42XX						✓	
	40XXS	✓[1]					✓	
	41XXS		✓[1]				✓	

[1] Wettable flanks package to allow automated optical inspection (AOI)

Cypress Roadmap: Automotive RAM

F-RAM™ Portfolio

Low Power | High Endurance

	LPC[1] F-RAM			Processor Companion	Parallel F-RAM	
512Kb–4Mb	**FM25V20A** **2Mb**; 2.0–3.6 V 40-MHz SPI; Ind[2]	**CY15B104Q** **4Mb;** 2.0–3.6 V 40-MHz SPI; Ind	**Excelon[3] F-RAM** **Up to 16Mb** **1.8V, 108-MHz QSPI[4]**		**FM22L16/LD16** **4Mb**; 2.7–3.6 V 55 ns; x8; Ind	
	CY15B102Q **2Mb;** 2.0–3.6 V 25-MHz SPI; Auto E[5]	**FM25V10/VN10** **1Mb**; 2.0–3.6 V 40-MHz SPI; Ind, Auto A[6]	**FM24V10/VN10** **1Mb**; 2.0–3.6 V 3.4-MHz I²C; Ind, Auto A		**FM28V102A** **1Mb;** 2.0–3.6 V 60 ns; x16; Ind	**FM28V202A** **2Mb;** 2.0–3.6 V 60 ns; x16; Ind
	FM25V05 **512Kb**; 2.0–3.6 V 40-MHz SPI; Ind, Auto A		**FM24V05** **512Kb**; 2.0–3.6 V 3.4-MHz I²C; Ind, Auto A		**CY15B101N** **1Mb;** 2.0–3.6 V 60 ns; x16; Auto A	**CY15B102N** **2Mb;** 2.0–3.6 V 60 ns; x16; Auto A
4Kb–256Kb	**FM25V02A/W256** **256Kb**; V02A: 2.0–3.6 V W256: 2.7–5.5 V 40-MHz SPI; Ind, Auto A		**FM24V02A/W256** **256Kb**; V02A: 2.0–3.6 V W256: 2.7–5.5 V 3.4-MHz I²C; Ind, Auto A	**FM33256** **256Kb**; 3.3V; 16-MHz SPI Ind; RTC[7]; Power Fail Watchdog; Counter	**FM28V020** **256Kb**; 2.0–3.6 V 70 ns; x8; Ind	**FM18W08** **256Kb**; 2.7–5.5 V 70 ns; x8; Ind
	FM25V01A **128Kb**; 2.0–3.6 V 40-MHz SPI; Ind, Auto A		**FM24V01A** **128Kb**; 2.0–3.6 V 3.4-MHz I²C; Ind, Auto A	**FM31256/31(L)278** **256Kb**; 3.3, 5.0V; 1-MHz I²C; Ind; RTC; Power Fail; Watchdog; Counter	**FM1808B** **256Kb**; 5.0 V 70 ns; x8; Ind	**FM16W08** **64Kb**; 2.7–5.5 V 70 ns; x8; Ind
	FM25640/CL64 **64Kb**; 3.3, 5.0 V 20-MHz SPI; Ind, Auto E		**FM24C64/CL64** **64Kb**; 3.3, 5.0 V 1-MHz I²C; Ind, Auto E	**FM3164/31(L)276** **64Kb**; 3.3, 5.0 V; 1-MHz I²C; Ind; RTC; Power Fail; Watchdog; Counter		
	FM25C160/L16 **16Kb**; 3.3, 5.0 V 20-MHz SPI; Ind, Auto E		**FM24C16/CL16** **16Kb**; 3.3, 5.0 V 1-MHz I²C; Ind, Auto A			
	FM25040/L04 **4Kb**; 3.3, 5.0 V 20-MHz SPI; Ind, Auto E		**FM24C04/CL04** **4Kb**; 3.3, 5.0 V 1-MHz I²C; Ind, Auto A			

[1] Low-pin-count
[2] Industrial grade -40°C to +85°C
[3] Ultra-Low-Energy
[4] Quad serial peripheral interface
[5] AEC-Q100 -40°C to +85°C
[6] AEC-Q100 -40°C to +125°C
[7] Real-time clock

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

Nonvolatile RAM Roadmap

Product Family	Density	(ES) [EOL]
Serial Excelon F-RAM QSPI, SPI 1.71–1.89 V 1.8–3.6 V	4/8Mb 2Mb 16Mb	(Q1'18) (Q4'18) (Q2'19)
Serial F-RAM SPI, I^2C 3.3/5 V	4Kb–4Mb	
Processor Companion F-RAM I^2C 3.3/5 V	64Kb, 256Kb	
Parallel F-RAM x8, x16 3.3/5 V	64Kb–4Mb	
Parallel nvSRAM x8, x16 3 V, 5 V	64Kb–16Mb	
Serial nvSRAM I^2C, SPI, QSPI 3 V, 5 V	64Kb–1Mb	

2Mb-to-16Mb Excelon™ F-RAM Family

Applications

Medical devices, wearables, industrial control and automation, automotive

Features

- **Excelon-Ultra**
  - 4Mb
  - 108-MHz Single Data Rate (SDR)/54-MHz Double Data Rate (DDR) Quad SPI
  - Industrial temperature range: -40°C to +85°C
- **Excelon-Auto**
  - 2Mb Auto E, 4Mb Auto A
  - 50-MHz SPI
  - Automotive (AEC-Q100) temperature range grade A: -40°C to +85°C
  - Automotive (AEC-Q100) temperature range grade E: -40°C to +125°C
- **Common Features for Excelon-Ultra/Auto**
  - Operating voltage range: 1.71–1.89 V, 1.80–3.60 V
  - 100-trillion read/write cycle endurance
  - 100-year data retention

Collateral

Preliminary Datasheet: Contact Sales (Available Now)

Excelon F-RAM

Family Table

Density	Standby Current (Typ.)	Active Current (Typ.)	Packages
2Mb	1 µA	3 mA	SOIC (8)
4Mb	1 µA	3 mA	SOIC (8), GQFN (8)
8Mb	1 µA	3 mA	GQFN (8)
16Mb	1 µA	3 mA	SOIC (8), GQNF (8)

Availability

Samples: Now (2Mb Auto, 4Mb, 8Mb), Q2 2019 (2Mb, 16Mb)
Production: Q4 2018 (2Mb Auto, 4Mb, 8Mb), Q4 2019 (2Mb, 16Mb)

Asynchronous SRAM Portfolio

High Density | Wide Voltage Range | Automotive A[1], E[2] | On-Chip ECC

Density	Fast SRAM			Low-Power SRAM (MoBL®[3])			PowerSnooze™[4]
	Non-ECC (≥90nm)		ECC (65nm)	Non-ECC (≥90nm)	ECC (65nm)	ECC (65nm) ULP[5]	ECC (65nm)
32Mb–64Mb	**CY7C107x** **32Mb**; 3.3 V 12 ns; x8, x16 Ind			**CY6218x** **64Mb**; 1.8, 3.0 V 55 ns; x16 Ind **CY6217x** **32Mb**; 1.8-5.0 V 55 ns; x16 Ind	**CY6218x** **64Mb**; 1.8, 3.0 V 45 ns; x16 Ind, Auto E **CY6217x** **32Mb**; 1.8, 3.0 V 45 ns; x16 Ind, Auto E	**CY6218x** **64Mb**; 3.0 V 45 ns; x16 Ind **CY6217x** **32Mb**; 3.0 V 45 ns; x16 Ind	
2Mb–16Mb	**CY7C106xGN** **16Mb**; 1.8, 3.3 V 10 ns; x8, x16, x32 Ind **CY7C105x** **8Mb**; 3.3 V 10 ns; x8, x16 Ind **CY7C1012** **12Mb**; 3.3 V 10 ns; x24 Ind **CY7C104x** **4Mb**; 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A, E **CY7C1034** **6Mb**; 3.3 V 10 ns; x24 Ind **CY7C1010/11** **2Mb**; 3.3 V 10 ns; x8, x16 Ind, Auto A, E **CY7C1024** **3Mb**; 3.3 V 10 ns; x24 Ind		**CY7C106xG/GE** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind, Auto E **CY7C105x** **8Mb**; 3.3, 5.0 V 10 ns; x8, x16 Ind, Auto E **CY7C104x** **4Mb**; 1.8-5.0 V 10 ns; x8, x16 Ind, Auto E	**CY6216x** **16Mb**;1.8, 3.0, 5.0 V 45 ns; x8, x16 Ind, Auto A **CY6215x** **8Mb**; 1.8, 3.0, 2.5-5V 45 ns; x8, x16 Ind, Auto A, E **CY6214x** **4Mb**; 1.8, 3.0, 2.5-5V 45 ns; x8, x16 Ind **CY6213x** **2Mb**; 1.8, 2.5-5.0 V 45 ns; x8, x16 Ind, Auto A, E	**CY6216x** **16Mb;** 1.8-5.0 V 45 ns; x8, x16, x32 Ind, Auto E **CY6216x** **8Mb;** 3.3, 5.0 V 45 ns; x8, x16, x32 Ind, Auto E **CY6214x** **4Mb**; 1.8-5.0 V 45 ns; x8, x16 Ind, Auto A, E	**CY6216x** **16Mb;** 3.0 V 45 ns; x8, x16, x32 Ind	**CY7S106x** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind **CY7S104x** **4Mb**; 1.8-5.0 V 10 ns; x8, x16 Ind
64Kb–1Mb	**CY7C1020** **512Kb**; 2.6, 3.3, 5.0 V 10 ns; x16 Ind, Auto E **CY7C1019/21/100x** **1Mb**; 2.6, 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A, E **CY7C19x/1399** **256Kb**; 3.3, 5.0 V 10 ns; x4, x8 Ind, Auto A			**CY6212x** **1Mb**; 2.5-5.0 V 45 ns; x8, x16 Ind, Auto A, E **CY62256** **256Kb**; 1.8, 3.0, 5V 55 ns, 70 ns; x8 Ind, Auto A, E			

[1] AEC-Q100 -40°C to +85°C
[2] AEC-Q100 -40°C to +125°C
[3] More Battery Life
[4] A Fast SRAM with a deep-sleep mode in addition to the conventional standby
[5] Ultra-Low-Power

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

Asynchronous SRAM Roadmap

Product Family	Density	(ES) [EOL]
MoBL SRAM ULP 65nm, ECC Parallel Asynchronous	16Mb 32Mb/64Mb	(Q3'20) (Q1'20)
MoBL SRAM 65nm, ECC Parallel Asynchronous	4Mb, 8Mb, 16Mb	
MoBL SRAM ≥ 90nm, Parallel Asynchronous	64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb	
PowerSnooze SRAM 65nm, ECC Parallel Asynchronous	4Mb, 16Mb	
Fast SRAM 65nm, ECC Parallel Asynchronous	2Mb, 4Mb, 8Mb, 16Mb	
Fast SRAM ≥ 90nm Parallel Asynchronous	64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 3Mb, 6Mb, 8Mb, 12Mb, 32Mb, 64Mb	

Low-Power SRAM Family with ECC[1]

Applications

Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers and automotive

Features

- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Standby current: 8.7 µA for 4Mb
- **Features**
  - ECC[1] logic to detect and correct single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS[2]-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

Collateral

Datasheet: Asynchronous SRAM with ECC

SRAM with ECC

Family Table

Density	MPN	Standby Current (Maximum at 85°C)	Standby Current (Typical at 25°C)
4Mb	CY6214x	8.7 µA	3.5 µA
8Mb	CY6215x	16.0 µA	5.5 µA
16Mb	CY6216x	16.0 µA	5.5 µA

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Fast SRAM Family with PowerSnooze™[1]

Applications

Programmable logic controllers, handheld devices, multifunction printers, computation servers and automotive

Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Deep-sleep current: 15 µA for 4Mb
- **Features**
  - ECC[2] logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS[3]-Compliant Packages**
  - 48-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 36-pin and 44-pin SOJ

Collateral

Datasheet: Asynchronous SRAM with ECC

[1] A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode
[2] Error-correcting code
[3] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

SRAM with PowerSnooze

Family Table

Density	MPN	Access Time	Deep Sleep Current (Maximum at 85ºC)
4Mb	CY7S104x	10 ns	15 µA
16Mb	CY7S106x	10 ns	22 µA

Availability

Production: Now

Fast SRAM Family with ECC[1]

Applications

Switches and routers, IP phones, test equipment, computation servers, automotive, military and aerospace systems

Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS[2]-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

Collateral

Datasheet: Asynchronous SRAM with ECC

SRAM with ECC

Family Table

Density	MPN	Access Time	Operating Current (Maximum at 85°C)
4Mb	CY7C104x	10 ns	45 mA
8Mb	CY7C105X	10 ns	110 mA
16Mb	CY7C106x	10 ns	110 mA

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Asynchronous SRAM Packages

Family	Density	28-pin TSOP I	32-pin TSOP I	48-pin TSOP I	32-pin TSOP II	44-pin TSOP II	48-pin TSOP II	54-pin TSOP II	36-ball BGA	48-ball BGA	119-ball BGA	28-pin PDIP	28-pin SOJ	32-pin SOJ	36-pin SOJ	44-pin SOJ	32-pin SOIC	28-pin SNC	60-ball CSP	Wafer
Fast	256Kb	✓											✓							✓
	512Kb					✓										✓				
	1Mb		✓		✓	✓				✓			✓	✓		✓				✓
	2Mb					✓				✓					✓					
	3Mb										✓									
	4Mb					✓				✓					✓	✓				✓
	6Mb										✓									
	8Mb					✓				✓										
	12Mb										✓									
	16Mb			✓				✓		✓	✓									
	32Mb									✓										
Low-Power	256Kb	✓										✓						✓		
	1Mb		✓			✓				✓							✓			✓
	2Mb		✓		✓	✓			✓	✓							✓			✓
	4Mb		✓		✓	✓				✓							✓			✓
	8Mb			✓		✓				✓										✓
	16Mb									✓	✓								✓	✓
	32Mb						✓			✓										
	64Mb									✓										

Synchronous SRAM Portfolio

High Random Transaction Rate (RTR)[1] | Low Latency | High Bandwidth

Standard Sync and NoBL®	Standard Sync and NoBL with ECC[2]	QDR®-II/ DDR-II	QDR-II+/ DDR-II+	QDR-II+X/ DDR-II+X	QDR-IV
RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes	RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes	RTR: 666 MT/s (max.) BW: 47.9 Gbps (max.) Latency: 1.5 Cycles CIO[3] and SIO[4]	RTR: 666 MT/s (max.) BW: 79.2 Gbps (max.) Latency: 2 or 2.5 Cycles CIO and SIO, ODT[5]	RTR: 900 MT/s (max.) BW: 91.1 Gbps (max.) Latency: 2.5 Cycles SIO, ODT	RTR: 2.1 GT/s (max.) BW: 153.5 Gbps (max.) Latency: 5 or 8 Cycles Dual-Port Bidirectional ODT
		CY7C161/2xKV18 **144Mb**; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4	**CY7Cx4/5/6/7xKV18** **144Mb**; 300–550 MHz 1.8 V; x18, x36 Burst 2, 4		**CY7C41xKV13** **144Mb**; 667–1,066 MHz 1.3 V; x18, x36 Burst 2
CY7C147/8xB **72Mb**; 133–250 MHz 2.5, 3.3 V; x18, x36		**CY7C151/2xKV18** **72Mb**; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4	**CY7Cx54/5/6/7KV18** **72Mb**; 250–550 MHz 1.8 V; x18, x36 RH[6]; Burst 2, 4	**CY7C156/7xXV18** **72Mb**; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4	**CY7C40xKV13** **72Mb**; 667–1,066 MHz 1.3 V; x18, x36 Burst 2
CY7C144/6xK **36Mb**; 133–250 MHz 2.5, 3.3 V; x36, x72	**CY7C144/6xKVE** **36Mb**; 133–250 MHz 2.5, 3.3 V; x18, x36	**CY7C141/2xKV18** **36Mb**; 250–333 MHz 1.8 V; x8, x9, x18, x36 Burst 2, 4	**CY7Cx24/5/6/7xKV18** **36Mb**; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4	**CY7C126/7x** **36Mb**; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4	
CY7C137/8xD/K **18Mb**; 100–250 MHz 3.3 V; x18, x32, x36	**CY7C137/8xKVE** **18Mb**; 100–250 MHz 2.5, 3.3 V; x18, x36	**CY7C131/2/9xKV18** **18Mb**; 250–333 MHz 1.8 V; x8, x18, x36 Burst 2, 4	**CY7Cx14/5/6/7xKV18** **18Mb**; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4		
CY7C135/6xC **9Mb**; 100–250 MHz 3.3 V; x18, x32, x36 Auto E[7]		**CY7C1911xKV18** **18Mb**; 250–333 MHz 1.8 V; x9 Burst 2, 4			
CY7C134/2xG **2–4Mb**; 100–250 MHz 3.3 V; x18, x32, x36					

Density ↑

Random Transaction Rate →

[1] Rate of truly random accesses to memory, expressed in transactions per second (MT/s, GT/s)
[2] Error-correcting code
[3] Common I/O
[4] Separate I/O
[5] On-die termination
[6] Radiation hardened, military grade
[7] AEC-Q100: -40°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

Synchronous SRAM Roadmap

Product Family	Density (Prod) [EOL]
QDR-IV SRAM 65nm, ECC 2.1 GT/s, 153.5 Gbps	72Mb, 144Mb
QDR-II+X SRAM 65nm, ECC 900 MT/s, 91.1 Gbps	36Mb, 72Mb
QDR-II+ SRAM 65nm, ECC 666 MT/s, 79.2 Gbps	18Mb, 36Mb, 72Mb[1], 144Mb
QDR-II SRAM 65nm 666 MT/s, 47.9 Gbps	18Mb, 36Mb, 72Mb, 144Mb
Standard Sync and NoBL® SRAM 65nm, ECC 250 MT/s, 18 Gbps	18Mb, 36Mb
Standard Sync and NoBL SRAM 65nm/90nm 250 MT/s, 18 Gbps	2Mb, 4Mb, 9Mb[2], 18Mb[3], 36Mb[3], 72Mb
Standard Sync and NoBL SRAM 90nm 250 MT/s, 18 Gbps	36Mb [LTS Q2'18]

[1] Radiation hardened, military grade
[2] AEC-Q100 -40°C to +125°C
[3] 65-nm

Concept Samples Production EOL

Standard Synchronous SRAM With On-Chip ECC[1]

Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features

- **Speed**
  - Available in two modes[2]: Pipeline and Flow-Through
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options[3]
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral

Datasheets: 36M Sync SRAM, 18M Sync SRAM

Synchronous SRAM

Family Table

Option	Density	MPN	RTR	FIT/Mb[4]
Standard Sync with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1370/2K CY7C1440/2K	250 MT/s	<0.01
Standard Sync with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1371/3K CY7C1441/3K	133 MT/s	<0.01

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[3] Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
[4] The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

NoBL® SRAM With On-Chip ECC[1]

Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features

- **Speed**
  - Available in two modes[2]: Pipeline and Flow-Through
  - No Bus Latency™ (NoBL) architecture for balanced read and write
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral

Datasheets: 36M NoBL SRAM, 18M NoBL SRAM

NoBL SRAM

Family Table

Option	Density	MPN	RTR	FIT/Mb[3]
NoBL with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1380/2K CY7C1460/2K	250 MT/s	<0.01
NoBL with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1381/3K CY7C1461/3K	133 MT/s	<0.01

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[3] The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

Synchronous SRAM Packages

Family	Density	100-pin TQFP	119-ball BGA	165-ball BGA	209-ball BGA	361-ball BGA	Wafer
Std Sync	18Mb	✓		✓			
	36Mb			✓			
NoBL	2Mb	✓					
	4Mb	✓	✓				
	9Mb	✓	✓	✓			✓
	18Mb	✓	✓	✓			
	36Mb	✓		✓			✓
	72Mb	✓		✓	✓		✓
QDR	9Mb			✓			
	18Mb			✓			
	36Mb			✓			
	72Mb			✓		✓	
	144Mb			✓		✓	

NOR Flash Memory Automotive Family

NOR Flash Memory Automotive Family Decoder

S 25 H S 512 T

Technology:	J = 110-nm Floating Gate (FG)		N = 110-nm MirrorBit® (MB)	1 = 63-nm DRAM (DR)
	K = 90-nm FG		P = 90-nm MB	
	L = 65-nm FG		S = 65-nm MB	
	M = 50-nm FG		T = 45-nm MB	
Density:	008 = 8Mb	064 = 64Mb	512 = 512Mb	04G = 4Gb
	016 = 16Mb	128 = 128Mb	01G = 1Gb	
	032 = 32Mb	256 = 256Mb	02G = 2Gb	
Voltage:	D = 2.5 V	L = 3.0 V	S = 1.8 V	
Family:	A = Standard Address-Data Parallel (ADP)			
	C = Burst Mode ADP			
	F = Serial			
	G = Page Mode			
	H = High-Performance Serial			
	J = Simultaneous Read/Write ADP			
	K = HyperBus™			
	P = Page Mode Simultaneous Read/Write ADP			
Series:	25 = SPI	26 = HyperBus™	28 = Octal	
	29 = Parallel	70 = Stacked Die	79 = Dual Quad SPI	
Prefix:	S			

NOR Flash Memory Automotive Product Portfolio: New Products

Family	Interface	Sector Size	Series	Voltage	Densities	Lead	Tech	2018	2019	2020	2021	2022	2023	2024
Semper™ Flash	Quad SPI	Hybrid	S25HS-T S25HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45nm MB							
	HyperBus™[1]		S26HS-T S26HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45nm MB							
	Octal[1]		S28HS-T S28HL-T	1.8 V 3.0 V	256Mb–4Gb	512Mb	45nm MB							
QSPI	QSPI	Hybrid	S25FS-S	1.8 V	64Mb–1Gb	-	65nm MB							
			S25FL-S	3.0 V	128Mb–1Gb	-	65nm MB							
			S25FL-L	3.0 V	64–256Mb	-	65nm FG							
Dual Quad SPI	QSPI	Hybrid	S79FS-S S79FL-S	1.8 V 3.0 V	256Mb–1Gb	-	65nm MB							
HyperFlash	HyperBus	Hybrid	S26KS-S S26KL-S	1.8 V 3.0 V	128–512Mb	-	65nm MB							
Parallel	Parallel	Hybrid	S29GL-T	3.0V	512Mb-2Gb	-	45nm MB							

[1] JEDEC xSPI Compliant

Concept | Samples | Production | EOL

x8 Memory Automotive Roadmap

Product Family	Density	(Prod[1]) [EOL]
S28HS-T[2] (1.8 V) S28HL-T[2] (3.0 V) Semper™ Flash with Octal Interface 45-nm MB[3]	4Gb[4] 2Gb[4] 1Gb 512Mb 256Mb	(TBD) (TBD) (Q4'19) (Q1'19) (Q2'20)
S26HS-T[2] (1.8 V) S26HL-T[2] (3.0 V) Semper Flash with HyperBus™ Interface 45-nm MB[3]	4Gb[4] 2Gb[4] 1Gb 512Mb 256Mb	(TBD) (TBD) (Q4'19) (Q1'19) (Q2'20)
S26KS-S (1.8 V) S26KL-S (3.0 V) HyperFlash 65-nm MB[3]	512Mb 256Mb 128Mb	
S79FS-S (1.8 V) S79FL-S (3.0 V) QSPI 65-nm MB[3]	1Gb[5] 512Mb[5] 256Mb[5]	

[1] AEC-Q100
[2] JEDEC xSPI Compliant
[3] Hybrid Sector
[4] Stacked Die
[5] S79 Series (stacked die)

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

x8 Serial Memory Automotive Portfolio

	Dual Quad SPI S79FL-S[1, 2] 65-nm MB, 3.0 V	HyperFlash S26KL-S[1] 65-nm MB, 3.0 V	Semper™ Flash[3] S26HL-T[1, 4] 45-nm MB, 3.0 V	Semper Flash[5] S28HL-T[1, 4] 45-nm MB, 3.0 V	Dual Quad SPI S79FS-S[1, 2] 65-nm MB, 1.8 V	HyperFlash S26KS-S[1] 65-nm MB, 1.8 V	Semper Flash[3] S26HS-T[1, 4] 45-nm MB, 1.8 V	Semper Flash[5] S28HS-T[1, 4] 45-nm MB, 1.8 V
	Density Initial Access/DDR Clock * Temperature Range	**Density (S79)** SDR Clock / DDR Clock * Temperature Range						
	All parts supported by Longevity Program unless noted							
≥256Mb			**4Gb[6, 7]** 80 ns/166 MHz * A, B, M	**4Gb[6, 7]** 80 ns/166 MHz * A, B, M			**4Gb[6, 7]** 80 ns/200 MHz * A, B, M	**4Gb[6, 7]** 80 ns/200 MHz * A, B, M
≥256Mb			**2Gb[6, 7]** 80 ns/166 MHz * A, B, M	**2Gb[6, 7]** 80 ns/166 MHz * A, B, M			**2Gb[6, 7]** 80 ns/200 MHz * A, B, M	**2Gb[6, 7]** 80 ns/200 MHz * A, B, M
≥256Mb	**1Gb** 133 MHz/80 MHz * A, B		Q219 **1Gb** Q419 80 ns/166 MHz * A, B, M	Q219 **1Gb** Q419 80 ns/166 MHz * A, B, M	**1Gb** 133 MHz/102 MHz * A, B		Q219 **1Gb** Q419 80 ns/200 MHz * A, B, M	Q219 **1Gb** Q419 80 ns/200 MHz * A, B, M
≥256Mb	**512Mb** 133 MHz/80 MHz * A, B	**512Mb** 96 ns/166 MHz * A, B, M	**512Mb** Q219 80 ns/166 MHz * A, B, M	**512Mb** Q219 80 ns/166 MHz * A, B, M	**512Mb** 133 MHz/80 MHz * A, B	**512Mb** 96 ns/166 MHz * A, B, M	**512Mb** Q119 80 ns/200 MHz * A, B, M	**512Mb** Q119 80 ns/200 MHz * A, B, M
≥256Mb	**256Mb** 133 MHz/80 MHz * A, B	**256Mb** 96 ns/166 MHz * A, B, M	Q419 **256Mb** Q220 80 ns/166 MHz * A, B, M	Q419 **256Mb** Q220 80 ns/166 MHz * A, B, M	**256Mb** 133 MHz/80 MHz * A, B	**256Mb** 96 ns/166 MHz * A, B, M	Q419 **256Mb** Q220 80 ns/200 MHz * A, B, M	Q419 **256Mb** Q220 80 ns/200 MHz * A, B, M
64–128Mb		**128Mb** 96 ns/166 MHz * A, B, M				**128Mb** 96 ns/166 MHz * A, B, M		

[1] Hybrid Sector
[2] S79 series (stacked die)
[3] With HyperBus™ Interface
[4] JEDEC xSPI Compliant
[5] With Octal Interface
[6] Contact Sales
[7] Stacked die

* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

x4 NOR Flash Memory Automotive Roadmap

Product Family	Density	(Prod[1]) [EOL]
S25HS-T (1.8 V) S25HL-T (3.0 V) Semper™ Flash with QSPI 45-nm MB[2]	4Gb[5] 2Gb[5] 1Gb 512Mb 256Mb	(TBD) (Q2'19) (Q4'19) (Q1'19) (Q4'20)
S25FS-S (1.8 V) S25FL-S[3] (3.0 V) QSPI 65-nm MB[2]	1Gb[6] 512Mb 256Mb 128Mb[7] 64Mb[8]	
S25FL-L (3. 0 V) QSPI 65-nm FG[4]	256Mb 128Mb 64Mb	
S25FL-P (3.0 V) QSPI 90-nm MB[2]	256Mb[6] 128Mb[9] 64Mb 32Mb	
S25FL1-K (3.0 V) QSPI 90-nm FG[4]	64Mb 32Mb 16Mb	[Q1'20] [Q1'20] [Q1'20]

[1] AEC-Q100
[2] Hybrid Sector
[3] VIO 1.8V to 3.0V
[4] Uniform Sector
[5] Stacked Die
[6] S70 Series (stacked die)
[7] S25FL127S and S25FL128S
[8] FS-S only
[9] S25FL128P and S25FL129P

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

x4 NOR Flash Memory Automotive Portfolio

	QSPI S25FL1-K[1] 90 nm, 3.0 V	QSPI S25FL-P[1] 90 nm, 3.0 V	QSPI S25FL-S[1] 65 nm, 3.0 V	QSPI S25FL-L[2] 65 nm, 3.0 V	Semper™ Flash[3] S25HL-T[1] 45 nm, 3.0 V	QSPI S25FS-S[1] 65 nm, 1.8 V	Semper Flash[3] S25HS-T[1] 45 nm, 1.8 V
≥256Mb	**Density (Name)** SDR Clock / DDR Clock * Temp Range All parts supported by Longevity Program unless noted				**4Gb[4]** 166 MHz / 102 MHz * A, B, M Q119 **2Gb[4]** Q219 166 MHz / 102 MHz * A[10], B, M[10] Q418 **1Gb** Q219 166 MHz / 102 MHz * A, B, M **512Mb** Q219 166 MHz / 102 MHz * A, B, M Q419 **256Mb** Q220 166 MHz / 102 MHz * A, B, M		**4Gb[4]** 166 MHz / 102 MHz * A, B, M **2Gb[4]** 166 MHz / 102 MHz * A, B, M Q219 **1Gb** Q419 166 MHz / 102 MHz * A, B, M **512Mb** Q119 166 MHz / 102 MHz * A, B, M Q419 **256Mb** Q220 166 MHz / 102 MHz * A, B, M
			1Gb[5] 133 MHz / 80 MHz * A, B, M **512Mb** 133 MHz / 80 MHz * A, B, M			**1Gb[5]** 133 MHz / 80 MHz * A, B, M **512Mb** 133 MHz / 80 MHz * A, B, M	
		256Mb[5] 104 MHz / -- * A	**256Mb** 133 MHz / 80 MHz * A, B, M	**256Mb** 133 MHz / 66 MHz * A, B, M		**256Mb** 133 MHz / 80 MHz * A, B, M	
64–128Mb		**128Mb[6]** 104 MHz / -- * A, B **128Mb[7]** 104 MHz / -- * A, B	**128Mb[8]** 133 MHz / 80 MHz * A, B, M **128Mb[9]** 108 MHz / -- * A, B	**128Mb** 133 MHz / 66 MHz * A, B, M		**128Mb** 133 MHz / 80 MHz * A, B, M	
	Q120 **64Mb** 108 MHz / -- * A, B	**64Mb** 104 MHz / -- * A, B		**64Mb** 108 MHz / 54 MHz * A, B, M		**64Mb** 133 MHz / 80 MHz * A, B, M	
≤32Mb	Q120 **32Mb** 108 MHz / -- * A, B Q120 **16Mb** 108 MHz / -- * A, B	**32Mb** 104 MHz / -- * A, B					

[1] Hybrid Sector
[2] Uniform Sector
[3] With QSPI
[4] Stacked die
[5] S70 series (stacked die)
[6] S25FL129P Quad SPI
[7] S25FL128P Dual SPI
[8] S25FL128S 133-MHz SDR / 80-MHz DDR
[9] S25FL127S 108-MHz SDR
[10] Contact Sales

* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

	Concept	Development	Engineering Sampling	AEC-Q100/ Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

CYPRESS EMBEDDED IN TOMORROW™

Parallel and Burst Parallel NOR Flash Memory Automotive Roadmap

Product Family	Density	(Prod[1]) [EOL]
S29GL-T[2] (3.0 V) 45-nm MB	2Gb[4] 1Gb 512Mb	
S29GL-S[2] (3.0 V) 65-nm MB	2Gb[4] 1Gb 512Mb 256Mb 128Mb 64Mb	
S29GL-N[2] (3.0 V) 110-nm MB	64Mb 32Mb	
S29PL-J[2, 3] (3.0 V) 110-nm FG	128Mb 64Mb 32Mb	
S29JL-J[3] (3.0 V) 110-nm FG	64Mb 32Mb	
S29AL-J (3.0 V) 110-nm FG	16M	
S29AL-J (3.0 V) 110-nm FG	8Mb	[Q1'19]
S29AS-J (1.8 V) 110-nm FG	16Mb 8Mb	
S29CD-J (2.5 V) Burst Parallel 110-nm FG	32Mb 16Mb	
S29CL-J (3.0 V) Burst Parallel 110-nm FG	32Mb 16Mb	

[1] AEC-Q100
[2] Supports Page Mode
[3] Supports Simultaneous Read/Write Operation
[4] S70 series (stacked die)

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

CYPRESS EMBEDDED IN TOMORROW™

Parallel and Burst Parallel NOR Flash Memory Automotive Portfolio

	Burst Parallel S29CL-J[1] 110 nm, 3.0 V	Burst Parallel S29CD-J[1] 110 nm, 2.5 V	S29AS-J 110 nm, 1.8 V	S29AL-J 110 nm, 3.0 V	S29JL-J[2] 110 nm, 3.0 V	S29PL-J[2, 3] 110 nm, 3.0 V	S29GL-N[3] 110 nm, 3.0 V	S29GL-S[3] 65 nm, 3.0 V	S29GL-T[3] 45 nm, 3.0 V
≥256Mb	**Density** Initial / Page Access * Temp Range All parts supported by Longevity Program unless noted							**2Gb**[4] 110 ns / 20 ns * A, B **1Gb** 100 ns / 15 ns * A, B **512Mb** 100 ns / 15 ns * A, B **256Mb** 90 ns / 15 ns * A, B	**2Gb**[4] 110 ns / 20 ns * A, B **1Gb** 100 ns / 15 ns * A, B **512Mb** 100 ns / 15 ns * A, B
64–128Mb					**64Mb** 55 ns / -- * A	**128Mb** 60 ns / 20 ns * A **64Mb** 55 ns / 20 ns * A	**64Mb** 90 ns / 25 ns * A	**128Mb** 90 ns / 15 ns * A, B **64Mb** 70 ns / 15 ns * A, B	
≤32Mb	**32Mb** 54 ns / 75 MHz * A , M, T **16Mb** 54 ns / 66 MHz * A , M, T	**32Mb** 54 ns / 75 MHz * A , M, T **16Mb** 54 ns / 66 MHz * A , M, T	**16Mb** 70 ns / -- * A **8Mb** Q119 70 ns / -- * A	**16Mb** **55 ns / --** * A, M **8Mb** 55 ns / -- * A, M	**32Mb** 60 ns / -- * A	**32Mb** 55 ns / 20 ns * A	**32Mb** 90 ns / 25 ns * A		

[1] Address Data Parallel (ADP) Burst
[2] Supports Simultaneous Read/Write Operation
[3] Supports Page Mode
[4] S70 series (stacked die)

* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
T = Automotive, AEC-Q100 Grade 0: -40°C to +145°C

	Concept	Development	Engineering Sampling	AEC-Q100/ Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

NAND Flash Memory Automotive Family

NAND Flash Memory Automotive Family Decoder

S 34 M L 08G 2

Technology:	1 = 4x-nm	2 = 32-nm	3 = 16-nm
Density:	01G = 1Gb 02G = 2Gb	04G = 4Gb 08G = 8Gb	16G = 16Gb
Voltage:	L = 3.0 V	S = 1.8 V	
Family:	M = NAND (Address-Data Multiplexed) S = SecureNAND (Address-Data Multiplexed)		
Series:	34 = NAND		
Prefix:	S		

SLC NAND Flash Memory Automotive Roadmap

Product Family	Density	(Prod[1]) [EOL]
S34MS-2 (1.8 V) 32-nm SLC ONFI[2] 1.0	16Gb 8Gb 4Gb 2Gb 1Gb	
S34MS-1 (1.8 V) 4x-nm SLC ONFI[2] 1.0	4Gb 2Gb 1Gb	[Q4'21] [Q4'21] [Q4'21]
S34SL-2 (3.0 V) 32-nm SLC ONFI[2] 1.0	4Gb 2Gb 1Gb	
S34ML-3 (3.0 V) 16-nm SLC ONFI[2] 1.0	16Gb 8Gb 4Gb	(Q1'19) (Q1'19) (Q4'18)
S34ML-2 (3.0 V) 32-nm SLC ONFI[2] 1.0	16Gb 8Gb 4Gb 2Gb 1Gb	
S34ML-1 (3.0 V) 4x-nm SLC ONFI[2] 1.0	8Gb 4Gb 2Gb 1Gb	[Q4'21] [Q4'21] [Q4'21] [Q4'21]

[1] AEC-Q100
[2] Open NAND Flash Interface

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

SLC NAND Flash Memory Automotive Portfolio

	S34ML-1[1] 4x nm, 3.0 V SLC, ONFI 1.0[2]	S34ML-2[3] 32 nm, 3.0 V SLC, ONFI 1.0[2]	S34ML-3[1] 16 nm, 3.0 V SLC, ONFI 1.0[2]	S34SL-2[3, 4] 32 nm, 3.0 V SLC, ONFI 1.0[2]	S34MS-1[1] 4x nm, 1.8 V SLC, ONFI 1.0[2]	S34MS-2[3] 32 nm, 1.8 V SLC, ONFI 1.0[2]
8–16Gb	**Density; Bus Width** Interface Bandwidth * Temp Range All parts supported by Longevity Program unless noted **8Gb; x8** Q421 40 MBps * A, B	**16Gb; x8** 40 MBps * I, V[5] **8Gb; x8** 40 MBps * A, B	**16Gb; x8** Q119 40 MBps * A, B **8Gb; x8** Q119 40 MBps * A, B			**16Gb; x8** 40 MBps * I, V[5] **8Gb; x8** 40 MBps * A, B
1–4Gb	**4Gb; x8/16** Q421 40 MBps * A, B **2Gb; x8/16** Q421 40 MBps * A, B **1Gb; x8** Q421 40 MBps * A, B	**4Gb; x8/16** 40 MBps * A, B **2Gb; x8/16** 40 MBps * A, B **1Gb; x8/16** 40 MBps * A, B	**4Gb; x8** Q418 40 MBps * A, B	**4Gb; x8** 40 MBps * I, V **2Gb; x8** 40 MBps * I, V[5] **1Gb; x8** 40 MBps * I, V	**4Gb; x8** Q421 40 MBps * A, B **2Gb; x8/16** Q421 40 MBps * A, B **1Gb; x8/16** Q421 40 MBps * A, B	**4Gb; x8/16** 40 MBps * A, B **2Gb; x8/16** 40 MBps * I, V[5] **1Gb; x8/16** 40 MBps * A, B

[1] 1-bit error-correcting code (ECC)
[2] Open NAND Flash Interface
[3] 4-bit error-correcting code (ECC)
[4] SecureNAND™: Cypress's SLC NAND Flash Memory with full-capacity volatile and nonvolatile block protection
[5] Contact Sales

* I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

	Concept	Development	Engineering Sampling	AEC-Q100/ Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

Flash and RAM Memory Automotive MCP

Flash and RAM Memory Automotive MCP Decoder

S 71 K S 512 R D

RAM Density:	A = 16Mb	B = 32Mb	C = 64Mb	D = 128Mb	E = 256Mb
Flash Technology:	S = 65-nm MirrorBit (MB)		T = 45-nm MB		
Flash Density:	128 = 128Mb	256 = 256Mb	512 = 512Mb	01G = 1Gb	
Voltage:	L = 3.0 V	S = 1.8 V			
Family:	H = High-Performance Serial K = HyperFlash				
Series:	71 = NOR Flash + pSRAM				
Prefix:	S				

Flash and RAM Memory Automotive MCP Roadmap

Product Family Flash / RAM	Flash / RAM Density	(Prod[1]) [EOL]
S71HS-T (1.8 V) 45-nm Semper™ Flash / HyperRAM™	1Gb / 64Mb 512Mb / 64Mb	(TBD) (TBD)
S71KS-S (1.8 V) 65-nm HyperFlash / HyperRAM	512Mb / 64Mb 256Mb / 64Mb 128Mb / 64Mb	 (TBD) (TBD)
S71HL-T (3.0 V) 45-nm Semper Flash / HyperRAM	1Gb / 64Mb 512Mb / 64Mb	(TBD) (TBD)
S71KL-S (3.0 V) 65-nm HyperFlash / HyperRAM	512Mb / 64Mb 256Mb / 64Mb 128Mb / 64Mb	 (TBD)

[1] AEC-Q100

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Flash and RAM Memory Automotive MCP Portfolio

	S71KL-S 65-nm MB, 3.0 V	S71HL-T 45-nm MB, 3.0 V	S71KS-S 65-nm MB, 1.8 V	S71HS-T 45-nm MB, 1.8 V
≥256Mb	**Flash Density** **RAM Density** * Temp Range			
	All parts supported by Longevity Program unless noted	**1Gb[1]** **64Mb[2]** * A, B		**1Gb[1]** **64Mb[2]** * A, B
	512Mb[1] **64Mb[2]** * A, B	**512Mb[1]** **64Mb[2]** * A, B	**512Mb[1]** **64Mb[2]** * A, B	**512Mb[1]** **64Mb[2]** * A, B
	256Mb[1] **64Mb[2]** * A, B		**256Mb[1]** **64Mb[2]** * A, B	
64–128Mb	**128Mb[1]** **64Mb[2]** * A, B		**128Mb[1]** **64Mb[2]** * A, B	

[1] HyperFlash
[2] HyperRAM™

* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

	Concept	Development	Engineering Sampling	AEC-Q100/ Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY

x8 NOR Flash Memory Packages

Family	Interface	Series	Density	Device	SOIC-16 300 mil	BGA24 8 x 8 mm 5 x 5 Ball	BGA24 8 x 6 mm 5 x 5 Ball	KGD
Semper™ Flash	HyperBus™	HS-T	256Mb	S26HS256T & S28HS256T			CF	CF
			512Mb	S26HS512T & S28HS512T			UD	CF
			1Gb	S26HS01GT & S28HS01GT		UD		CF
			2Gb	S26HS02GT & S28HS02GT		CF		
			4Gb	S26HS04GT & S28HS04GT		CF		
		HL-T	256Mb	S26HL256T & S28HL256T			CF	CF
			512Mb	S26HL512T & S28HL512T			UD	CF
			1Gb	S26HL01GT & S28HL01GT		UD		CF
			2Gb	S26HL02GT & S28HL02GT		CF		
			4Gb	S26HL04GT & S28HL04GT		CF		
HyperFlash		KS-S	128Mb	S26KS128S			✓	CF
			256Mb	S26KS256S			✓	CF
			512Mb	S26KS512S			✓	CF
			1Gb	S70KS01GS			✓	
		KL-S	128Mb	S26KL128S			✓	CF
			256Mb	S26KL256S			✓	CF
			512Mb	S26KL512S			✓	CF
			1Gb	S70KL01GS			✓	
Dual Quad SPI	QSPI	FS-S Dual Quad	256Mb	S79FS256S	✓			
			512Mb	S79FS512S	✓			
			1Gb	S79FS01GS			✓	
		FL-S Dual Quad	256Mb	S79FL256S	✓			
			512Mb	S79FL512S	✓			
			1Gb	S79FL01GS			✓	

CF = Contact Factory
UD = Under Development

CYPRESS EMBEDDED IN TOMORROW™

x4 NOR Flash Memory Packages

Family	Interface	Series	Density	Device	SOIC-8 150 mil	SOIC-8 208 mil	SOIC-16 300 mil	WSON 4 x 4 mm	WSON 6 x 5 mm	WSON 8 x 6 mm	BGA24 8 x 8 mm 5 x 5 Ball	BGA24 8 x 6 mm 5 x 5 Ball	BGA24 8 x 6 mm 4 x 6 Ball	KGD
Semper™ Flash	QSPI	HS-T	256Mb	S25HS256T			CF					UD		CF
			512Mb	S25HS512T			UD			UD		UD		CF
			1Gb	S25HS01GT			UD				UD			CF
			2Gb	S25HS02GT							CF			
			4Gb	S25HS04GT							CF			
		HL-T	256Mb	S25HL256T			CF					UD		CF
			512Mb	S25HL512T			UD			UD		UD		CF
			1Gb	S25HL01GT			UD				UD			CF
			2Gb	S25HL02GT							UD			
			4Gb	S25HL04GT							CF			
QSPI		FS-S	64Mb	S25FS064S		✓			✓			✓		✓
			128Mb	S25FS128S		✓	CF		✓	✓		✓	✓	CF
			256Mb	S25FS256S			✓			✓		✓	✓	✓
			512Mb	S25FS512S			✓			✓		✓	✓	CF
			1Gb	S70FS01GS			✓					✓		
		FL-S	128Mb	S25FL127S		✓	✓		✓			✓	✓	
			128Mb	S25FL128S			✓			✓		✓	✓	
			256Mb	S25FL256S			✓			✓		✓	✓	
			512Mb	S25FL512S			✓					✓	✓	✓
			1Gb	S70FL01GS			✓					✓		
		FL-P	32Mb	S25FL032P		✓	✓		✓	✓		✓	✓	✓
			64Mb	S25FL064P			✓			✓		✓	✓	✓
			128Mb	S25FL128P			✓			✓				
			128Mb	S25FL129P			✓			✓		✓	✓	
			256Mb	S70FL256P			✓			✓		✓		
		FL-L	64Mb	S25FL064L		✓	UD	✓	UD			✓	✓	CF
			128Mb	S25FL128L		✓	UD		✓			✓	✓	CF
			256Mb	S25FL256L			✓			✓		✓	✓	CF
		FL1-K	16Mb	S25FL116K	✓	✓			✓			✓	✓	✓
			32Mb	S25FL132K	✓	✓		✓	✓			✓	✓	✓
			64Mb	S25FL164K		✓	✓		✓			✓	✓	✓

CF = Contact Factory
UD = Under Development

CYPRESS EMBEDDED IN TOMORROW™

Parallel and Burst Parallel NOR Flash Memory Packages

Series	Density	Device	48-Ball FBGA (0.8-mm pitch)	48-Ball FBGA (0.5-mm pitch)	56-Ball BGA (0.8-mm pitch)	64-Ball BGA (0.8-mm pitch)	64-Ball Fortified BGA (1.0-mm pitch)	48-Pin TSOP	56-Pin TSOP	80-Ball FBGA (1.0-mm pitch)	80-Pin PQFP	KGD
GL-T	512Mb	S29GL512T			✓		✓		✓			
	1Gb	S29GL01GT			✓		✓		✓			
	2Gb	S70GL02GT					✓					
GL-S	64Mb	S29GL064S	✓				✓	✓	✓			
	128Mb	S29GL128S			✓		✓		✓			
	256Mb	S29GL256S			✓		✓		✓			
	512Mb	S29GL512S			✓		✓		✓			
	1Gb	S29GL01GS					✓		✓			
	2Gb	S70GL02GS					✓					
GL-N	32Mb	S29GL032N	✓				✓	✓	✓			
	64Mb	S29GL064N	✓				✓	✓	✓			
PL-J	32Mb	S29PL032J	✓		✓							
	64Mb	S29PL064J	✓		✓							
	128Mb	S29PL127J				✓			✓			
JL-J	32Mb	S29JL032J	✓					✓				
	64Mb	S29JL064J	✓					✓				
AL-J	8Mb	S29AL008J	✓					✓				
	16Mb	S29AL016J	✓				✓	✓				
AS-J	8Mb	S29AS008J	✓					✓				
	16Mb	S29AS016J	✓	✓				✓				
CD-J	16Mb	S29CD016J								✓	✓	✓
	32Mb	S29CD032J								✓	✓	
CL-J	16Mb	S29CL016J								✓	✓	
	32Mb	S29CL032J								✓	✓	

CYPRESS EMBEDDED IN TOMORROW™

SLC NAND and SecureNAND Flash Memory Packages

Family	Density	Device	63-Ball BGA (0.8-mm pitch)	67-Ball BGA (0.8-mm pitch)	48-Pin TSOP
MS-2	1Gb	S34MS01G2	✓	✓	✓
	2Gb	S34MS02G2	✓	✓	✓
	4Gb	S34MS04G2	✓		✓
	8Gb	S34MS08G2	✓		
	16Gb	S34MS16G2	✓		
MS-1	1Gb	S34MS01G1	✓		
	2Gb	S34MS02G1	✓		✓
	4Gb	S34MS04G1	✓		✓
ML-3	4Gb	S34ML04G3	✓		✓
	8Gb	S34ML08G3	✓		✓
	16Gb	S34ML16G3	✓		✓
ML-2	1Gb	S34ML01G2	✓	✓	✓
	2Gb	S34ML02G2	✓	✓	✓
	4Gb	S34ML04G2	✓		✓
	8Gb	S34ML08G2	✓		✓
	16Gb	S34ML16G2	✓		✓
ML-1	1Gb	S34ML01G1	✓		✓
	2Gb	S34ML02G1	✓		✓
	4Gb	S34ML04G1	✓		✓
	8Gb	S34ML08G1	✓		✓
SL-2	1Gb	S34SL01G2	✓		
	2Gb	S34SL02G2	✓		
	4Gb	S34SL04G2	✓		

CYPRESS EMBEDDED IN TOMORROW™

Flash and RAM Memory MCP Packages

Family	Flash Density	RAM Density	BGA24 8 x 6 mm, 1.0 mm pitch 5 x 5 Ball
S71HS-T	512Mb	64Mb	CF
	1Gb	64Mb	CF
S71KS-S	128Mb	64Mb	✓
	256Mb	64Mb	✓
	512Mb	64Mb	✓
S71HL-T	512Mb	64Mb	CF
	1Gb	64Mb	CF
S71KL-S	128Mb	64Mb	✓
	256Mb	64Mb	✓
	512Mb	64Mb	✓

CF = Contact Factory

Cypress Roadmap: Automotive Timing Solutions

Clock Synthesizer Roadmap

	Product Family	Features	(Prod) [EOL]	2018 Q1	2018 Q2	2018 Q3	2018 Q4	2019 Q1	2019 Q2	2019 Q3	2019 Q4	2020 Q1	2020 Q2	2020 Q3	2020 Q4	2021 Q1	2021 Q2	2021 Q3	2021 Q4	2022 Q1	2022 Q2	2022 Q3	2022 Q4
High Performance	CY27430	4-PLL; Maximum Frequency: 700 MHz 12 Outputs; Diff[1] & SE[1]; PCIe 3.0; VCXO[2]; EMI[3]; 0.7-ps RMS Jitter[4] 1.8 V/2.5 V/3.3 V; Ind[5]; 48-QFN																					
High Performance	CY27410	4-PLL; Maximum Frequency: 700 MHz 8 Outputs; Diff & SE; PCIe 3.0; VCXO; EMI; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; Auto A[6] S[7]; 48-QFN																					
High Performance	CCY254x/CY251x	1-4 PLL; Maximum Frequency: 200 MHz 3-9 Outputs; I²C; EMI; Low Power[8] 100-ps CCJ[9]; Ind; 1.8 V/2.5 V/3.0 V/3.3 V 8-SOIC; 8/16/20-TSSOP; 24-QFN																					
Standard Performance	CY229x/CY2238x	3-4 PLL; Maximum Frequency: 166 MHz 3-8 Outputs; CMOS; Low Power 200-ps PPJ[10]; VCXO; Ind; 3.3 V/5 V 8/16/20-SOIC; 16-TSSOP																					
Standard Performance	CY2429x	1-PLL; Maximum Frequency: 200 MHz 2-5 Outputs; HCSL, CMOS; EMI 75-ps CCJ; PCIe 1.1; Ind; Auto A 3.3 V; 16-TSSOP; 32-QFN																					
Standard Performance	CY2239x	3-4 PLL; Maximum Frequency: 400 MHz 5-8 Outputs; LVPECL, CMOS; I²C 400-ps PPJ; VCXO; 3.3 V Ind; Auto A E[11]; 16-TSSOP; 32-QFN																					
Standard Performance	CY22800/801/CY2581x	1-PLL; Maximum Frequency: 200 MHz 1-3 Outputs; CMOS; EMI 110-ps CCJ; VCXO; Ind; 3.3 V; 8-SOIC; 8-TSSOP																					
Standard Performance	CY22050/150	1-PLL; Maximum Frequency: 200 MHz 6 Outputs; CMOS; I²C 250-ps PPJ; Ind 2.5 V/3.3 V; 16-TSSOP																					

[1] Differential and single-ended outputs
[2] Voltage-controlled crystal oscillation
[3] Electro Magnetic Interference reduction using Lexmark profile
[4] Integrated phase noise across 12-kHz to 20-MHz offset
[5] Industrial grade: -40°C to +85°C
[6] AEC-Q100: -40°C to +85°C
[7] AEC-Q100: -40°C to +105°C
[8] Power management options
[9] Cycle-to-cycle jitter
[10] Peak-to-peak period jitter
[11] AEC-Q100: -40°C to +125°C

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Clock Buffer Roadmap

	Product Family	Features	(Prod) [EOL]
High Performance	CY2DPx/CPx	Maximum Frequency: 1.5 GHz 2-10 Outputs; LVPECL; 2.5 V/3.3 V 0.11-ps Additive Jitter[1]; Ind[2] 8/20-TSSOP; 8-SOIC; 32-TQFP	
High Performance	CY2DMx/DLx	Maximum Frequency: 1.5 GHz 2-10 Outputs; LVDS, CML; 2.5 V/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 32-TQFP	
High Performance	CY230x/EP0x (Zero Delay)	Maximum Frequency: 220 MHz 2-9 Outputs; LVCMOS; 2.5 V/3.3 V/5 V 22-ps CCJ[3]; Ind; Auto A[4] 8/16-SOIC; 16-TSSOP; WAFER	
Standard Performance	CY230xNZ/ 2994x (Non-Zero Delay)	Maximum Frequency: 200 MHz 4-18 Outputs; LVCMOS 100-ps Op-Op Skew; Ind 2.5 V/3.3 V; 8-TSSOP, 16-SOIC	
Standard Performance	CY23FS04/08/FP12 (Zero Delay)	Maximum Frequency: 200 MHz 4-12 Outputs; LVCMOS; Fail Safe 200-ps CCJ; Ind; 2.5 V/3.3 V 16/28-SSOP	
Standard Performance	CY23S0x (Zero Delay)	Maximum Frequency: 133 MHz 5-9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind; 2.5 V/3.3 V; 8/16-SOIC; 16-TSSOP	
Standard Performance	CY7B99x (RoboClock™)	Maximum Frequency: 200 MHz; 8-13 Outputs Configurable Skew; 2.5 V/3.3 V/5.0 V 50-ps CCJ; Ind; 24-SOIC; 32-PLCC; 32/44/52,100-TQFP; 100-BGA	

[1] Additive RMS phase jitter
[2] Industrial grade: -40°C to +85°C
[3] Cycle-to-cycle jitter
[4] AEC-Q100: -40°C to +85°C

Products supported by Longevity Program unless noted

Concept
Samples
Production
EOL - LTB
EOL - LTS

Timing Solutions Portfolio

Programmable | High-Performance | EMI Reduction | Automotive

	Clock Synthesizers		Oscillators		Clock Buffers	
High Performance	**CY27410** 4-PLL; Max Freq: 700 MHz 12 Outputs; Diff[1] & SE[1]; PCIe 3.0 VCXO[2]; EMI[3]; 0.7-ps RMS Jitter[4] 1.8 V/2.5 V/3.3 V; Ind[5]; 48-QFN	**CY27430** 4-PLL; Max Freq: 700 MHz 8 Outputs; Diff & SE; PCIe 3.0 VCXO; EMI; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; Auto A[6] S[7]; 48-QFN	**CY2941x/2x** 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff & SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 8-LCC (7 x 5, 5 x 3.2)	**CY51x7** 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff & SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 1.8 V/2.5 V/3.3 V; WAFER/DIE	**CY2DPx/CPx** Max Freq: 1.5 GHz 2–10 Outputs; LVPECL; 2.5/3.3 V 0.11-ps Additive Jitter[8]; Ind 8/20-TSSOP; 8-SOIC; 32-TQFP	**CY2DMx/DLx** Max Freq: 1.5 GHz 2–10 Outputs; LVDS, CML; 2.5/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 32-TQFP
	CY29430 1-PLL; Max Freq: 2.1 GHz 1 Output; Diff & SE; 40/100 GbE VCXO; 0.11-ps RMS Jitter; Ind 16-QFN		**CY2Xx (FleXO™)** Q320 1 PLL; Max Freq: 690 MHz 1 Output; LVCMOS, LVDS, LVPECL Freq Margining; 0.6-ps RMS Jitter Ind · 6-LCC (7x5, 5x3.2); 8-TSSOP			
Standard Performance	**CY254x/CY251x** 1–4 PLL; Max Freq: 200 MHz 3–9 Outputs; I²C; EMI; Low Power[9] 100-ps CCJ[10]; Ind; 1.8/2.5/3.0/3.3 V 8-SOIC; 8/16/20-TSSOP; 24-QFN	**CY229x/CY2238x** 3–4 PLL; Max Freq: 166 MHz 3–8 Outputs; CMOS; Low Power 200-ps PPJ[11]; VCXO; Ind; 3.3/5 V 8/16/20-SOIC; 16-TSSOP	**CY25701** 1-PLL; Max Freq: 166 MHz 1 Output; CMOS; EMI 85-ps CCJ; Ind 3.3 V; 4-LCC (5 x 3.2)	**CY2037/ 5037** 1-PLL; Max Freq: 133 MHz 1 Output; CMOS 100-ps CCJ; Ind 3.3/5.0 V; WAFER	**CY230x/EP0x (Zero Delay)** Max Freq: 220 MHz 2–9 Outputs; LVCMOS ; 2.5/3.3/5 V 22-ps CCJ; Ind[5]; Auto A 8/16-SOIC; 16-TSSOP; WAFER	**CY230xNZ/ 2994x (Non-Zero Delay)** Max Freq: 200 MHz 4–18 Outputs; LVCMOS 100-ps Op-Op Skew; Ind 2.5/3.3 V; 8-TSSOP, 16-SOIC
	CY2429x 1-PLL; Max Freq: 200 MHz 2-5 Outputs; HCSL, CMOS; EMI 75-ps CCJ; PCIe 1.1; Ind; Auto A 3.3 V; 16-TSSOP; 32-QFN	**CY2239x** 3–4 PLL; Max Freq: 400 MHz 5–8 Outputs; LVPECL, CMOS; I²C 400-ps PPJ; VCXO; 3.3 V Ind; Auto A E[12]; 16-TSSOP; 32-QFN	**CY5077** 1-PLLMax Freq: 166 MHz 1 Output; CMOS 75-ps CCJ; Ind 1.8/2.5/3.0/3.3 V; WAFER	**CY5057** 1-PLL; Max Freq: 170 MHz 1 Output; CMOS; EMI <200-ps CCJ; Ind 3.3/5.0 V; WAFER	**CY23FS04/08/FP12 (Zero Delay)** Max Freq: 200 MHz 4–12 Outputs; LVCMOS; Fail Safe 200-ps CCJ; Ind; 2.5/3.3 V 16/28-SSOP	**CY7B99x (RoboClock™)** Q319 Max Freq: 200 MHz; 8–13 Outputs Configurable Skew; 2.5/3.3/5.0 V 50-ps CCJ; Ind; 24-SOIC; 32-PLCC 32/44/52/100-TQFP; 100-BGA
	CY22800/801/CY2581x 1-PLL; Max Freq: 200 MHz 1-3 Outputs; CMOS; EMI 110-ps CCJ; VCXO; Ind 3.3 V; 8-SOIC; 8-TSSOP	**CY22050/150** 1-PLL; Max Freq: 200 MHz 6 Outputs; CMOS; I²C 250-ps PPJ; Ind[5] 2.5/3.3 V; 16-TSSOP			**CY23S0x (Zero Delay)** Max Freq: 133 MHz 5–9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind 2.5/3.3 V; 8,16-SOIC; 16-TSSOP	

[1] Differential and single-ended outputs
[2] Voltage-controlled crystal oscillation
[3] Electromagnetic interference reduction using Lexmark profile
[4] Integrated phase noise across 12-kHz to 20-MHz offset
[5] Industrial grade: -40°C to +85°C
[6] AEC-Q100: -40°C to +85°C
[7] AEC-Q100: -40°C to +105°C
[8] Additive RMS phase jitter
[9] Power management options
[10] Cycle-to-cycle jitter
[11] Peak-to-peak period jitter
[12] AEC-Q100: -40°C to +125°C

	Concept	Development	Sampling	Production	EOL
Status					
Availability			QQYY	QQYY	QQYY

CYPRESS EMBEDDED IN TOMORROW™

Cypress Roadmap: Automotive PMIC

Automotive PMIC Family Portfolio

Typical Input Voltage	Single-channel PMIC	Multi-Channel PMIC Instrument Cluster & Body, ADAS (works with Cypress Traveo/Traveo II)
48 V	**Bi-Directional SMPS** Conversion between 48 V and 12 V	
12 V	**S6BP203A** V_{BAT} [1] → 3.3V 2.4A, 2-MHz Buck-Boost [2], PG [3], 16-Pin TSSOP **S6BP202A** V_{BAT} → 5.0V (2.4A), 2-MHz Buck-Boost, PG, 16-Pin TSSOP **S6BP201A** V_{BAT} → 5.0V (1.0A) 2-MHz Buck-Boost, PG 16-Pin TSSOP	**S6BP502A** V_{BAT} → 5.0V / 3.3 / 1.1V (2.0A), 400-kHz Buck [4], 2-MHz Buck, 2-MHz Boost [5], PG, SSCG [6], HOT [7], 32-Pin wettable QFN [8] **S6BP501A** V_{BAT} → 5.0V / 3.3 / 1.1V (1.4A), 400-kHz Buck, 2-MHz Buck, 2-MHz Boost, PG, SSCG, HOT, 32-Pin wettable QFN
5.0 V/3.3 V		**S6BP401A** 5V → six output rails, 2-MHz Buck x4, LDO x2, PG, WDT [9], 40-Pin QFN

[1] Lead-acid battery whose typical voltage is 12V.
[2] Topology to supply stable output regardless of input variation
[3] Power-Good signal output
[4] Step-down voltage regulator
[5] Step-up voltage regulator
[6] Spread-spectrum clock generator which deliberately varies the internal clock signal frequency to lower the electromagnetic radiation
[7] Hard pin output that indicates the die is getting hot
[8] QFN packages whose pin is processed so that the solder fillet would form between the pin and pad
[9] Watchdog timer

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY

S6BP20xA

One-Channel Buck-Boost Automotive PMIC

Applications

Instrument clusters, body electronics and ADAS

Features

- **1-Channel PMIC:** Synchronous buck-boost converter
- **Wide Input Voltage Range:** 2.5–42 V
- **Low Quiescent Current:** 20 µA
- **Programmable Switching Frequency:** 0.2–2.1 MHz
  - Synchronization with external clock from 200 kHz to 400 kHz
  - Autonomous PFM/PWM[1] switching
- **BOM Integration:** Built-in switching transistors
- **System Safety Function[2] Support:**
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with power good[3] pin
- **Operating Temperature Range:** -40°C to +125°C
- **Package:** 16-pin thermally enhanced TSSOP (5-mm x 6.4-mm)
- **Qualification:** AEC-Q100 Grade-1

Collateral

Datasheet: S6BP201A, S6BP202A and S6BP203A
Evaluation Kit: S6BP201A, S6BP202A and S6BP203A

[1] Pulse-frequency modulation / pulse-width modulation
[2] A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
[3] An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
[4] S6BP201A and S6BP202A have factory-selectable options of output voltage, power-on-reset time, UVP/OVP threshold, and SYNC Function

S6BP20x overview

Family Table

Output Voltage[4]	Max. Output Current	MPN	UVP/OVP Threshold
5.0–5.2 V	1.0 A	S6BP201A	±4.5%
5.0–5.2 V	2.4 A	S6BP202A	±4.5%, ±8.0%
3.3 V	2.4 A	S6BP203A	±8.0%

Availability

Sampling: Now **Production:** Now

S6BP50xA

Three-Channel Automotive PMIC

Applications

Low-end to mid-range hybrid automotive cluster systems

Features

- **3-Channels:** Buck controller with load switch, boost converter, buck converter
- **Wide Range Input:** 2.5-42 V
- **Low Quiescent Current:** 15 µA
- **High Switching Frequency:**
  - Boost converter and buck converter: 2.1 MHz
  - Built-in spread-spectrum clock generator (SSCG)
  - Synchronization with external clock from 1.8–2.4 MHz
- **System Safety Function[1] Support:**
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Thermal warning
  - Window-monitoring voltage supervisors with independent power good[2] pins
- **Operating Temperature Range:** -40°C to +105°C
- **Package:** 32-pin thermally enhanced side-wettable[3] QFN (5-mm x 5-mm)
- **Qualification:** AEC-Q100 Grade-2

Collateral

Preliminary Datasheet: S6BP501A/S6BP502A
Evaluation Kit: S6SBP501A00VA1001/S6SBP502A00VA1001

[1] A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
[2] An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
[3] QFN packages whose pin is processed so that the solder fillet would form between the pin and pad
[4] Output voltages are finely adjustable with external resistive dividers

S6BP50x: Three-Channel Automotive PMIC

Family Table

Buck Converter Output Specification[4]	MPN	Buck Controller Output Specification	Boost Converter Output Specification
1.15 V, 1.4 A	S6BP501A	3.3 V, 1.6 A	5.0 V, 1.3 A
1.2 V, 2.0 A	S6BP502A	3.3 V, 1.9 A	5.0 V, 1.3 A

Availability

Sampling: Now **Production:** Now

S6BP401A

Six-Channel Automotive PMIC

Applications

Advanced driver assistance systems (ADAS), security camera systems

Features

- **6-Channel PMIC:** 4-channel buck converters, 2-channel LDOs
- **Input Voltage Range:** 4.5–5.5 V
  - Input voltage for LDO: 1.62–5.5 V
- **High Switching Frequency:** 2.1 MHz
  - Synchronization with external clock from 1.8–2.4 MHz
- **BOM Integration:**
  - Switching transistors, voltage setting resistors, and compensation circuitry
- **System Safety Function[1] Support:**
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with independent power good[2] pins
  - Built-in windowed watchdog timer (WDT)
  - Independent enable pins
- **Operating Temperature Range:** -40°C to +125°C
- **Package and Qualification:** 40-pin QFN (6-mm x 6-mm), AEC-Q100 Grade-1

Collateral

Datasheet: S6BP401A
Evaluation Kit: S6SBP401AJ0SA1001, S6SBP401AM2SA1001

Availability

Sampling: Now **Production:** Now

[1] A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
[2] An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
[3] S6BP401A has factory-selectable options of output voltage for each channel

Compatibility with Traveo™ MCU

		Cypress Automotive PMIC				
		S6BP201A	S6BP202A	S6BP203A	S6BP501A	S6BP502A
Traveo MCU for Instrument Cluster	S6J3120	✓	✓			
	S6J3300	✓	✓			
	S6J3300				✓	✓
	S6J3200)					✓
Traveo MCU for Body Control	S6J3110	✓	✓			
	S6J3400	✓	✓	✓		
	S6J3500	✓	✓	✓		
	S6J3350				✓	✓

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