A Thomas Ware Capstone Project.

Solutions Calculator Club product development

Lesson 1

ELTR-160
Project Management

“Plan For Success.”

Solutions Calculator Club Product Development

Project Charter

Scope:

Tasked with developing an educational tool to show how a Computational System and Subsystems processes inputs and outputs.

Resources:

A research grant for a development ***budget*** of $20,000.
The project **research phase time frame** of 4 months and an **implementation phase *time frame*** was 4 months.

Stakeholders:

Solutions calculator Club are the ***investors***
Thomas Ware is the ***project developer***
Trevor Murray ***consultant***
UFV potential ***client***
Ben Eater *8-bit computer kit* ***Supplier***

Risks and assessments:

Scope of the project for a single person, supply chain issues like chip shortages or obsolete components and shipping time if replacements are required. Limitations of the ALU and memory size of registers.

Gantt Chart

Lesson Plans

CMNS-125
Communication For Professionals

Solutions Calculator Club Product Development

CMNS-125 Research:

History and Innovations of the Calculator

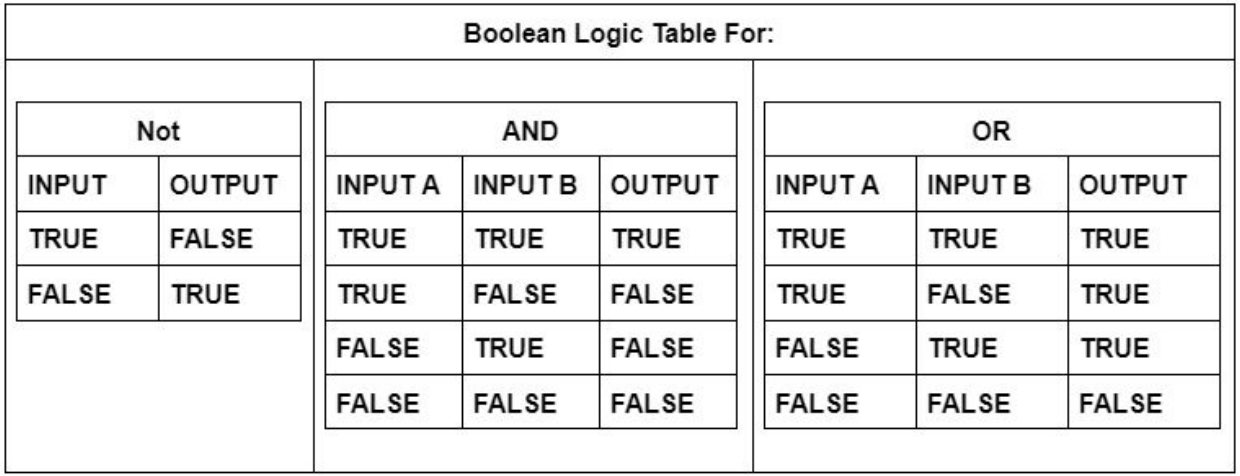
History and Innovations of the Calculator

The Abacus

- Binary
- Weighed Sum
- Register

The first calculating device known was the **Abacus.** Invented in China around the **2nd century B.C**. However, Abacus-like devices are first attested from ancient Mesopotamia around **2700 B.C.**

History and Innovations of the Calculator



Boolean Logic Table For:

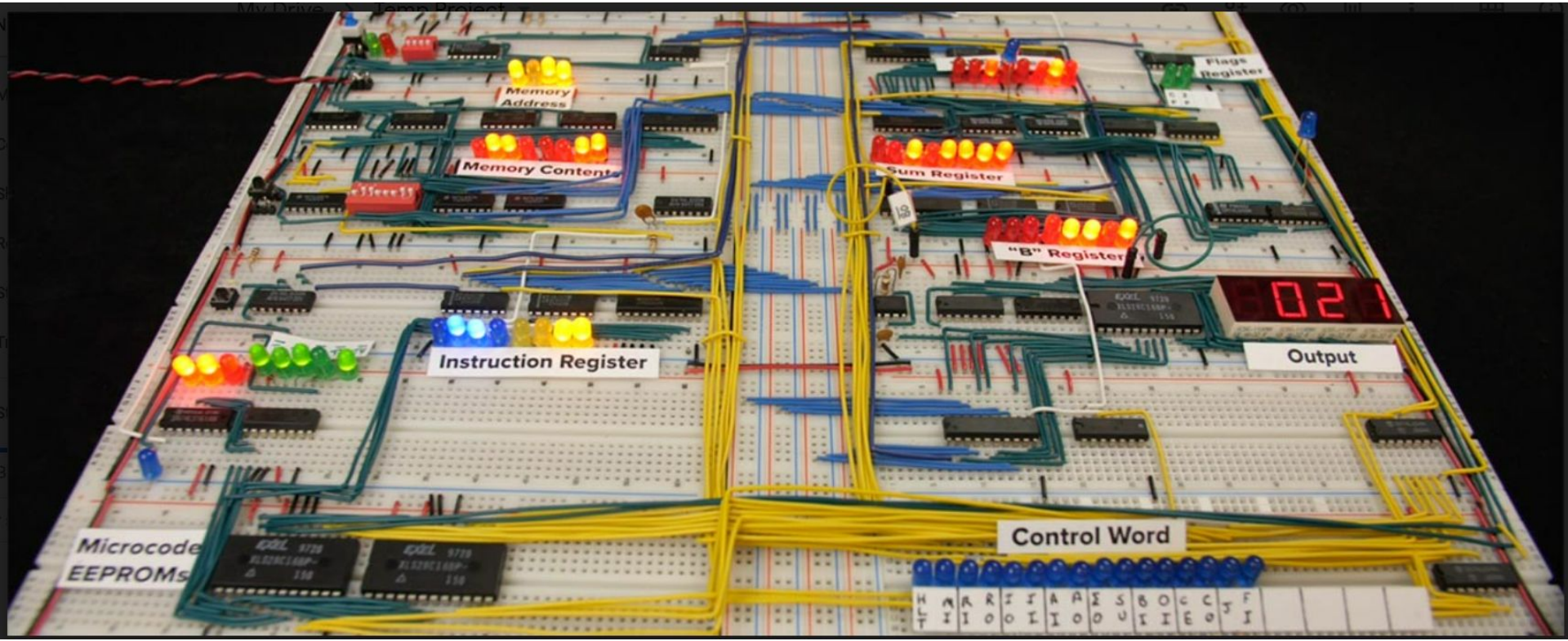
Not	
INPUT	OUTPUT
TRUE	FALSE
FALSE	TRUE

AND		
INPUT A	INPUT B	OUTPUT
TRUE	TRUE	TRUE
TRUE	FALSE	FALSE
FALSE	TRUE	FALSE
FALSE	FALSE	FALSE

OR		
INPUT A	INPUT B	OUTPUT
TRUE	TRUE	TRUE
TRUE	FALSE	TRUE
FALSE	TRUE	TRUE
FALSE	FALSE	FALSE

ELTR-130 Data Logic

Ben Eater's 8 Bit Computer



(2016)

Ben Eater’s 8 Bit Computer

Module 1 The System Clock

Module 2

Registers
- A register
- B register
- Instruction Register

Arithmetic unit (ALU)

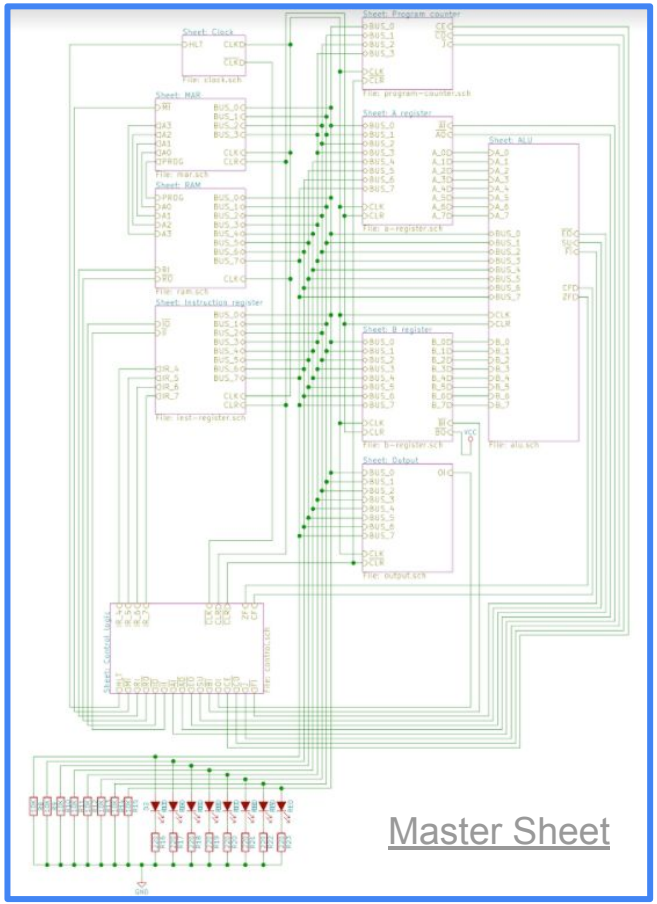
Module 3

Memory Address Register (MAR)
Random access memory (RAM)
Program counter

Module 4

CPU control logic
Output Register (Display 7 Segment)
The Bus communication
Flag Register (Carry bit, Zero)

Module 5 AC adapter for development of project and safety.



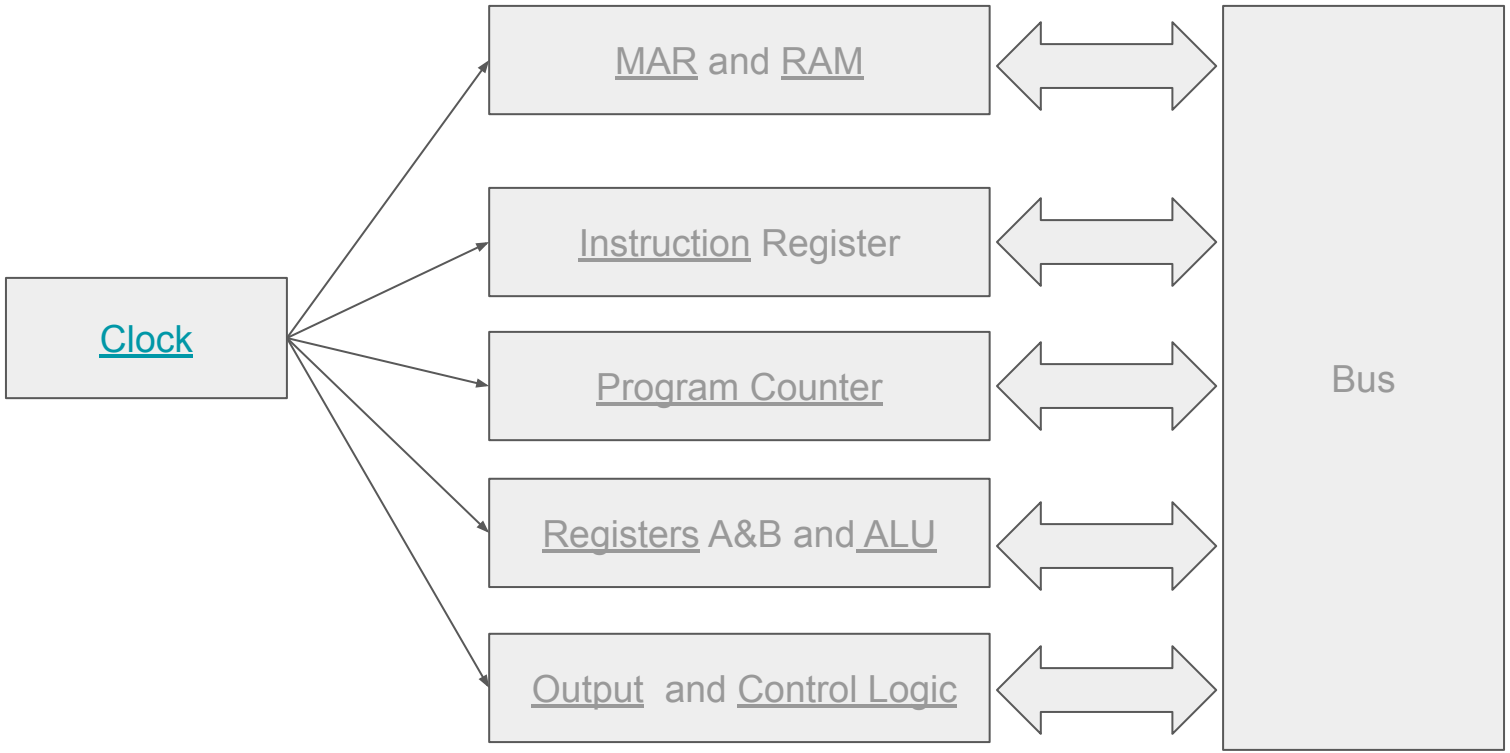
Lesson Plans

ELTR-170
Electronic System Integration

Wiring subsystems
- Wire Preparation

Troubleshooting
- Interconnections of Modules

Ben Eater's 8 Bit Computer

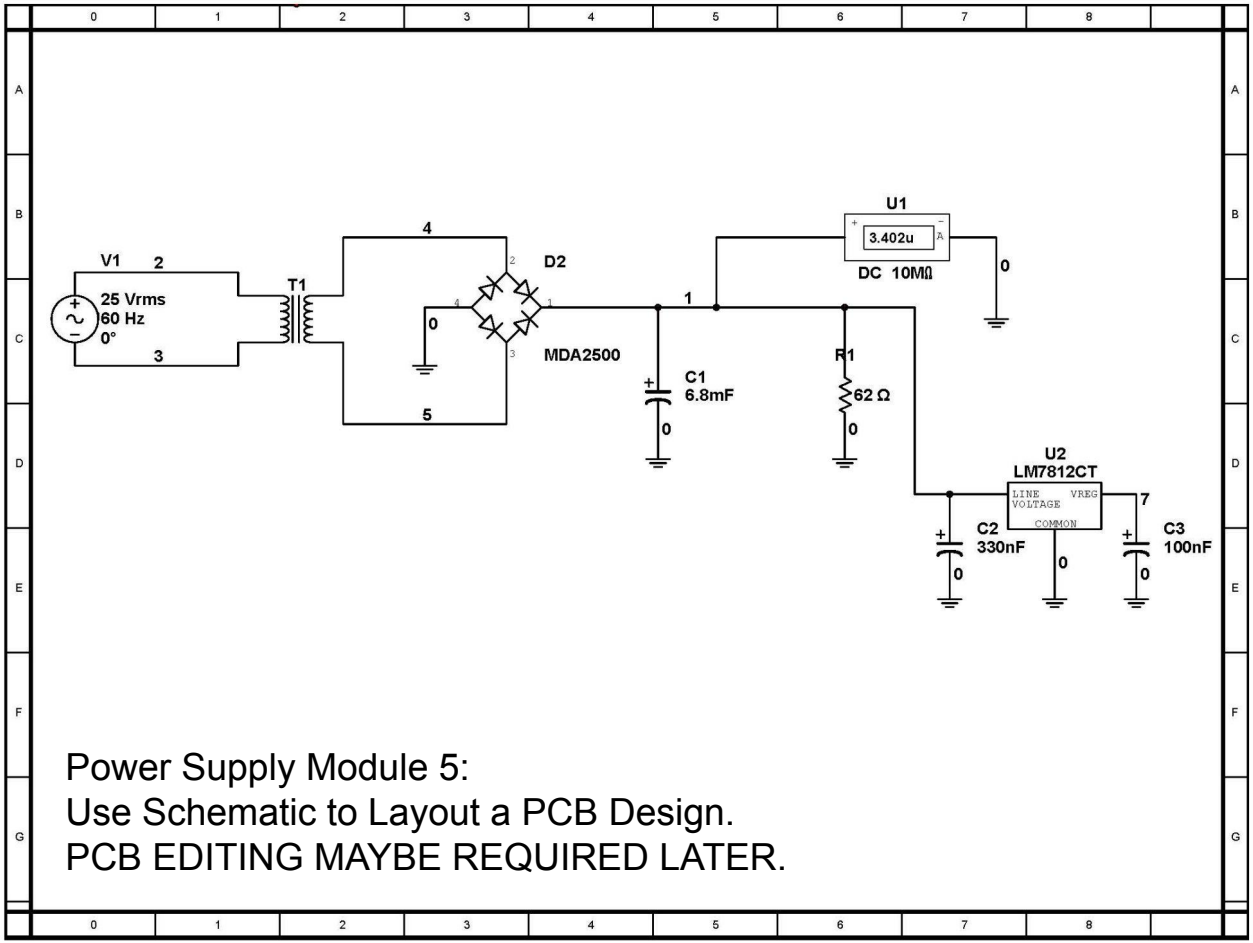


Lesson Plans

ELTR-110
Manufacturing Processes

Project 1

Using MULTISIM Design a 12v Power Supply



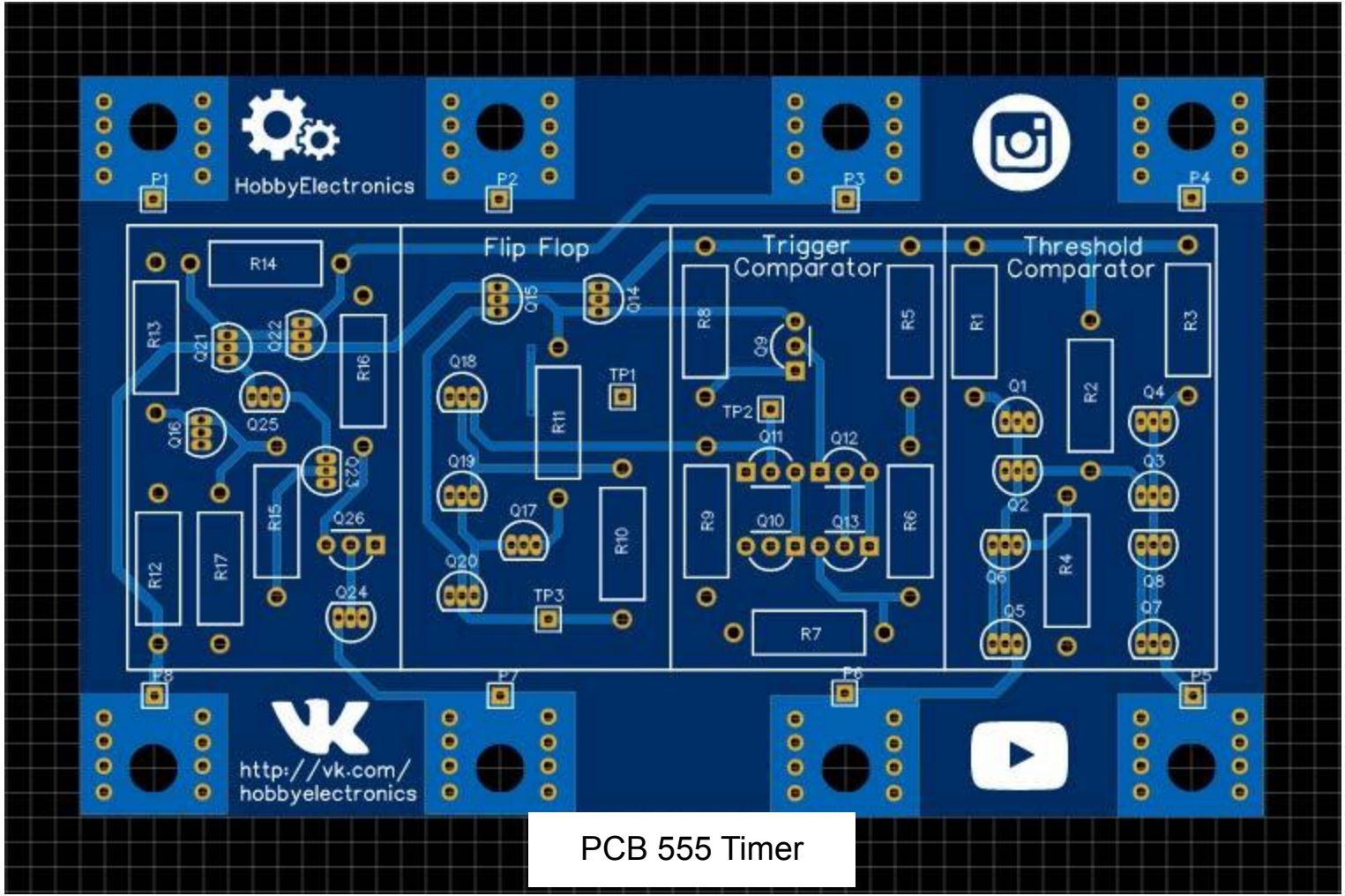
Power Supply Module 5:
Use Schematic to Layout a PCB Design.
PCB EDITING MAYBE REQUIRED LATER.

Lesson Plans

ELTR-110
Manufacturing Processes

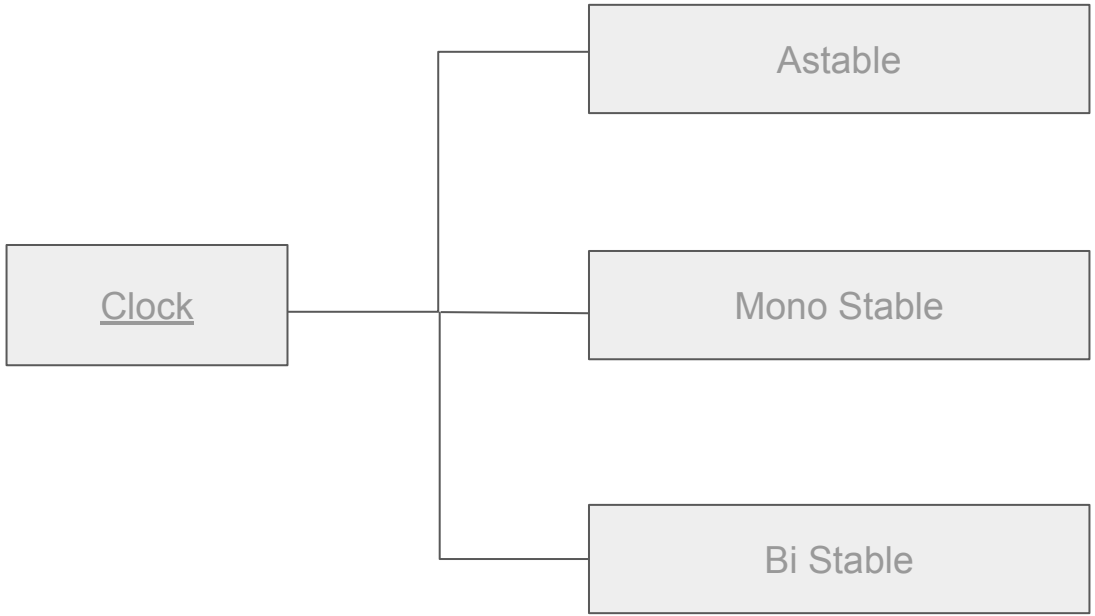
Project 2

Building The Clock Module



PCB 555 Timer

The Clock Module



Lesson Plans

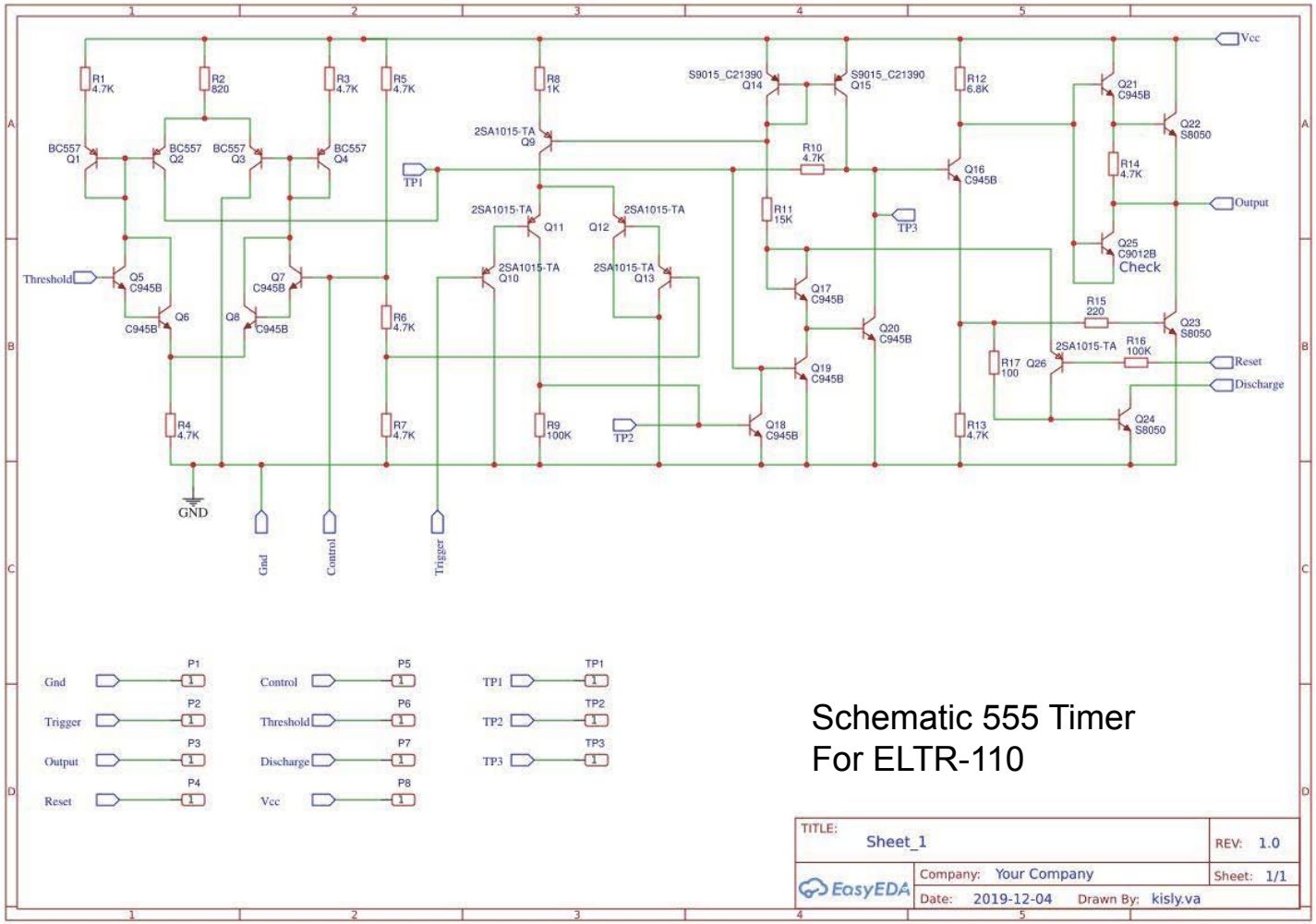
ELTR-100
Electrical Network Analysis

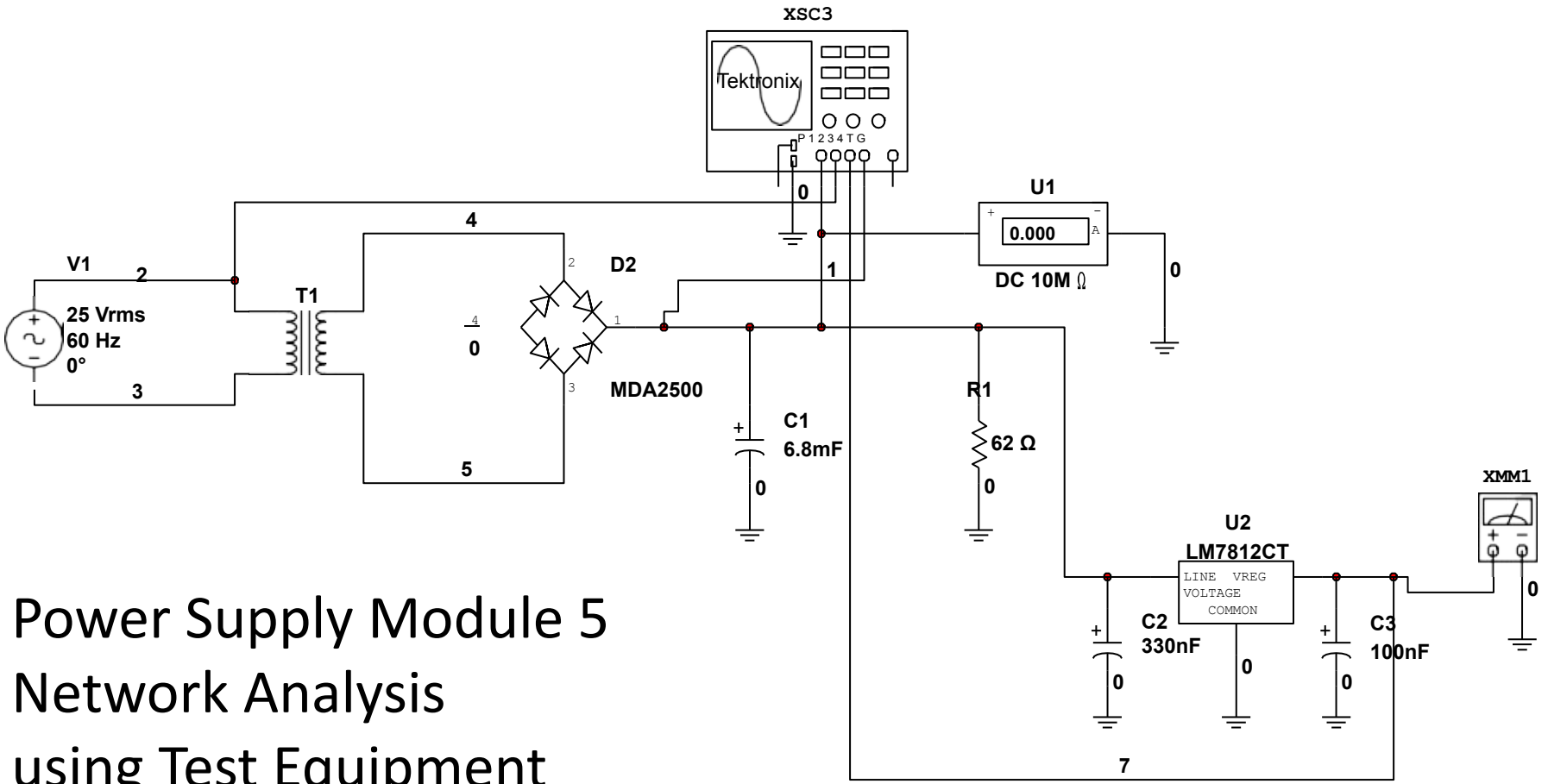
Analysis Project 1 using Project 2 from ELTR-110

- Cicuit Analysis of 555 Timer
  - Circuit Schematic Designed with Discrete components

Analysis Porject 2 using Project 1 from ELTR-110

- Power Supply Circuit
  - How to safely measure AC Power and the Power Supply Circuit


R1 4.7K
R2 820
R3 4.7K
R5 4.7K
R8 1K
S9015_C21390 Q14
S9015_C21390 Q15
R12 6.8K
Vcc
Q21 C945B
Q22 S8050
BC557 Q1
BC557 Q2
BC557 Q3
BC557 Q4
2SA1015-TA Q9
R10 4.7K
TP1
R14 4.7K
Output
Q16 C945B
R11 15K
TP3
2SA1015-TA Q11
2SA1015-TA Q12
Q25 C9012B
Check
Threshold
Q5 C945B
Q7 C945B
2SA1015-TA Q10
2SA1015-TA Q13
Q17 C945B
R15 220
Q23 S8050
Q6 C945B
Q8 C945B
R6 4.7K
Q20 C945B
2SA1015-TA Q26
R16 100K
R17 100
Reset
Discharge
Q19 C945B
R4 4.7K
R7 4.7K
R9 100K
TP2
Q18 C945B
R13 4.7K
Q24 S8050
GND
Gnd
Control
Trigger
P1
Gnd
P2
Trigger
P3
Output
P4
Reset
P5
Control
P6
Threshold
P7
Discharge
P8
Vcc
TP1
TP2
TP3
Schematic 555 Timer
For ELTR-110
TITLE:
Sheet_1
REV: 1.0
EasyEDA
Company: Your Company
Sheet: 1/1
Date: 2019-12-04
Drawn By: kisly.va



Power Supply Module 5
Network Analysis
using Test Equipment

Lesson Plans

ELTR-150
Solid State Semiconductor Devices

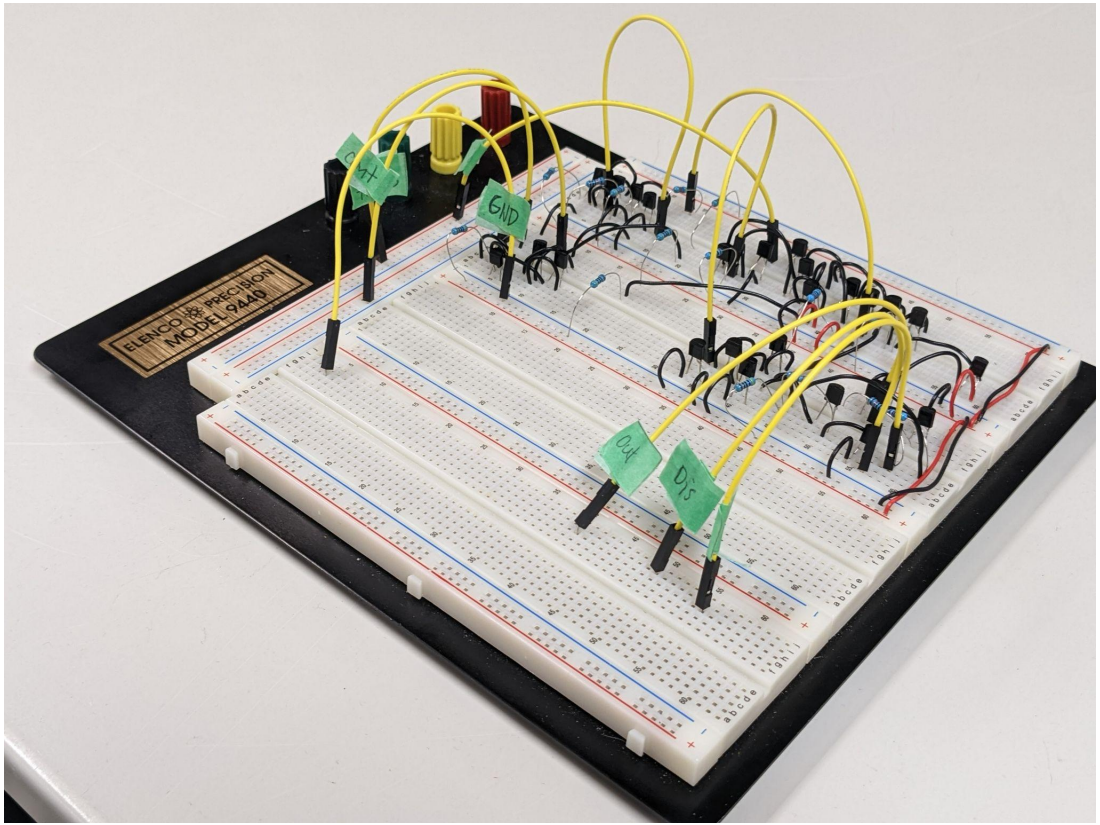
Use Analysis Project from ELTR-100

- Build a 555 Timer from Discrete components

Revision of ELTR-110 Project 1

- Revise Power Supply to work with your Capstone Project for ELTR-190

ELTR-150: 555 Timer from Discrete components



Example: Photo of prototype on Breadboard

Lesson Plans

ELTR-130
Digital Logic Systems

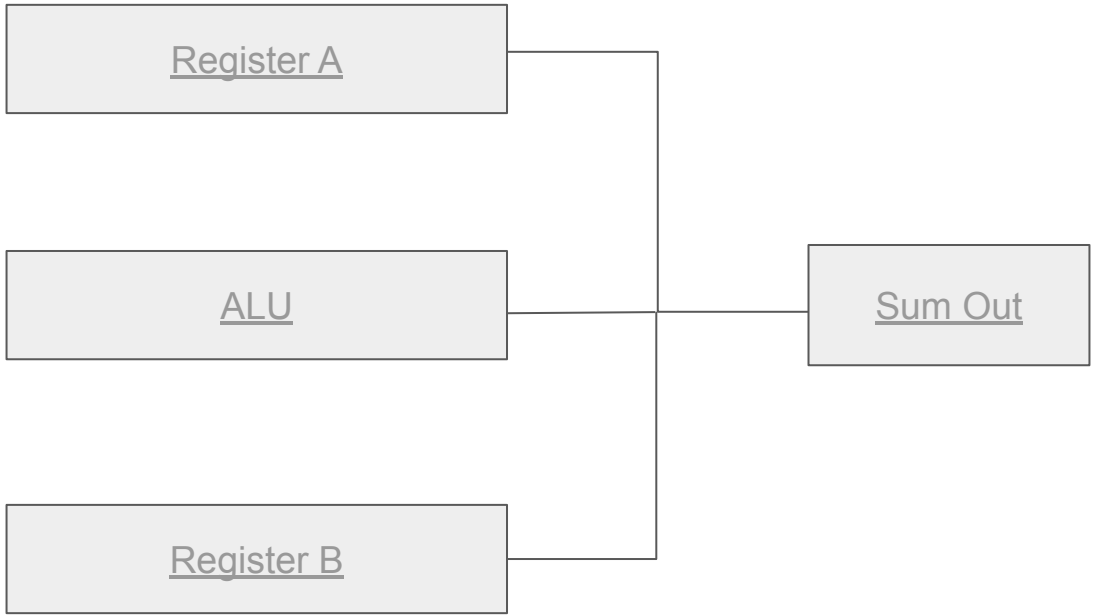
Use Analysis Project 1 from ELTR-100

- Build AND OR NOT Logic from Discrete components

Use LOGISIM to construct Logical Circuits for:

- Comparator, Adders, Latches, Registers, Counters, Encoders, Decoders, Selector/Multiplexers, ALU, 7 Segment Display, Control Logic, and CPU

Ben Eater’s 8 Bit Computer



ADD and Subtraction Operations

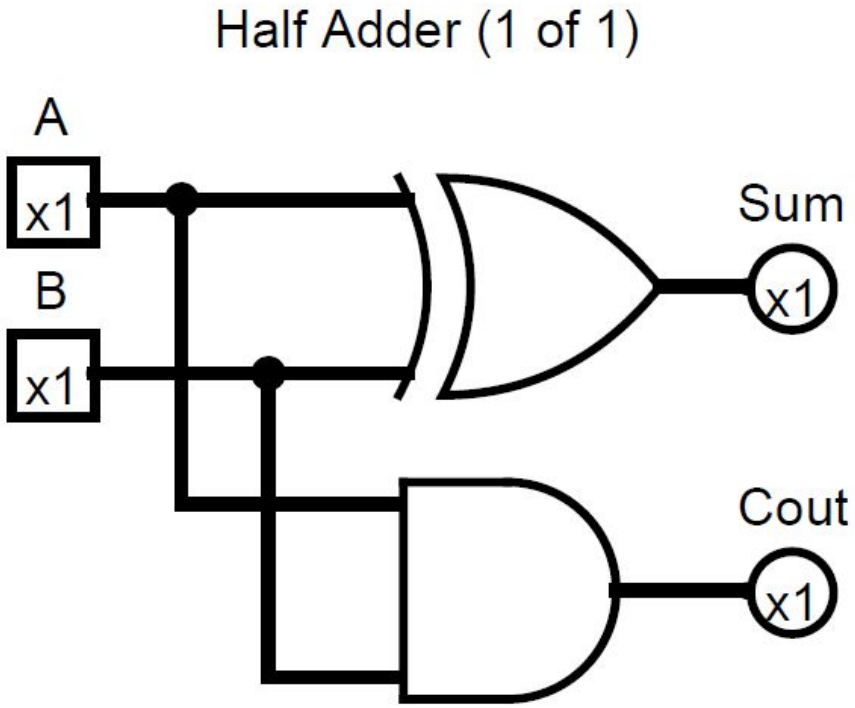
Ben Eater’s 8 Bit Computer

ELTR-130 Data logic

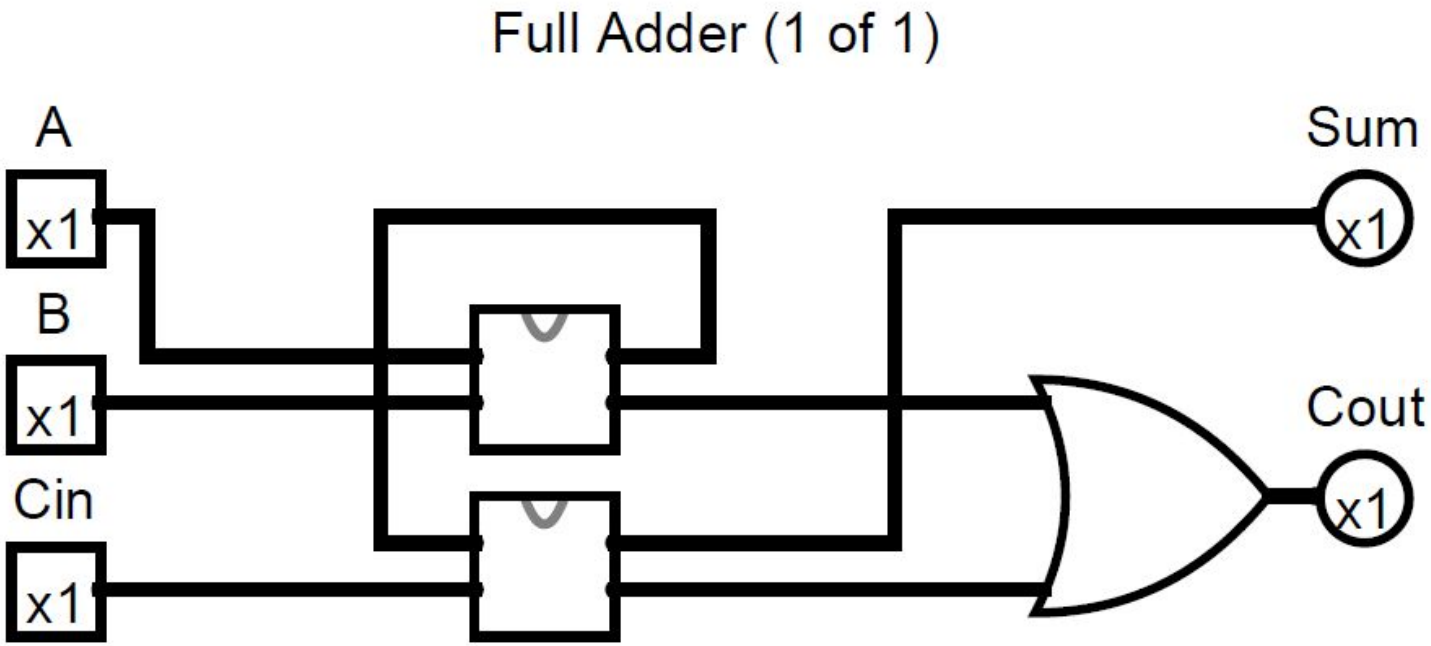
How Do Binary Values ADD?

	00011100			28
+	00001110	+		14
	00101010			42

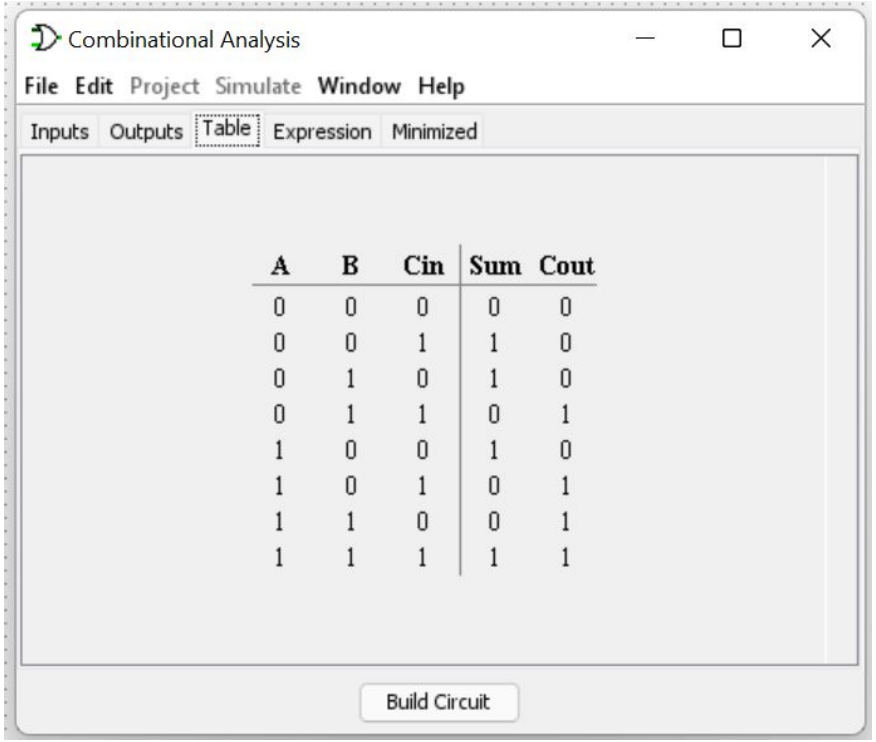
Ben Eater’s 8 Bit Computer



Ben Eater’s 8 Bit Computer

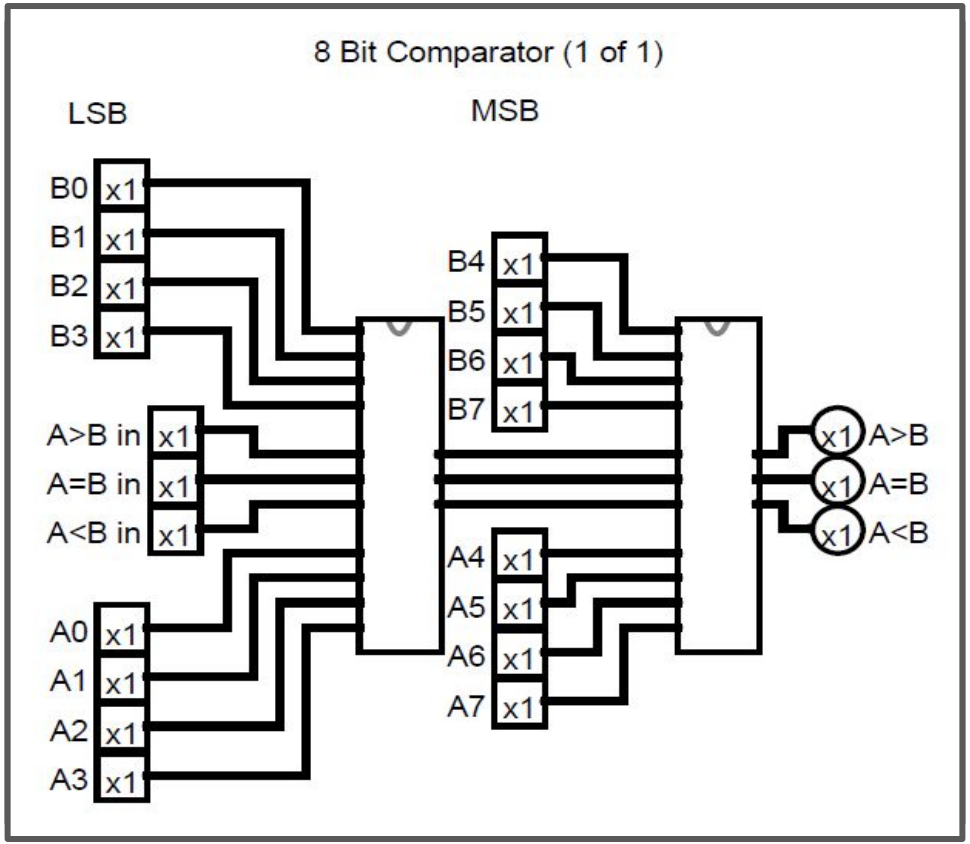


Ben Eater’s 8 Bit Computer

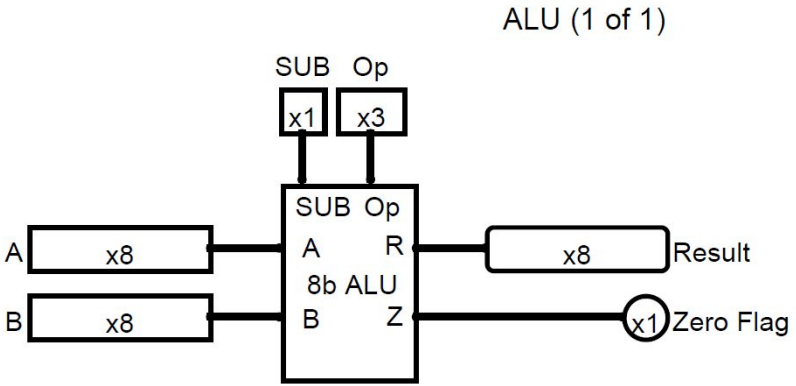


A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Ben Eater’s 8 Bit Computer



Ben Eater’s 8 Bit Computer



ALU Operations

000 AND
001 OR
010 XOR
011 NOR
100 ADD/SUB
101 LESS

Logisim ALU
RUN Here.

Ben Eater’s 8 Bit Computer

ADD	A and B are summed
ADD with CARRY	A and B and a Carry-In bit are all summed
SUBTRACT	B is subtracted from A (or vice versa)
SUBTRACT with BORROW	B is subtracted from A (or vice versa) with borrow (carry-in)
NEGATE	A is subtracted from zero, flipping its sign (from - to +, or + to -)
INCREMENT	Add 1 to A
DECREMENT	Subtract 1 from A
PASS THROUGH	All bits of A are passed through unmodified

8 Operations Circuits:

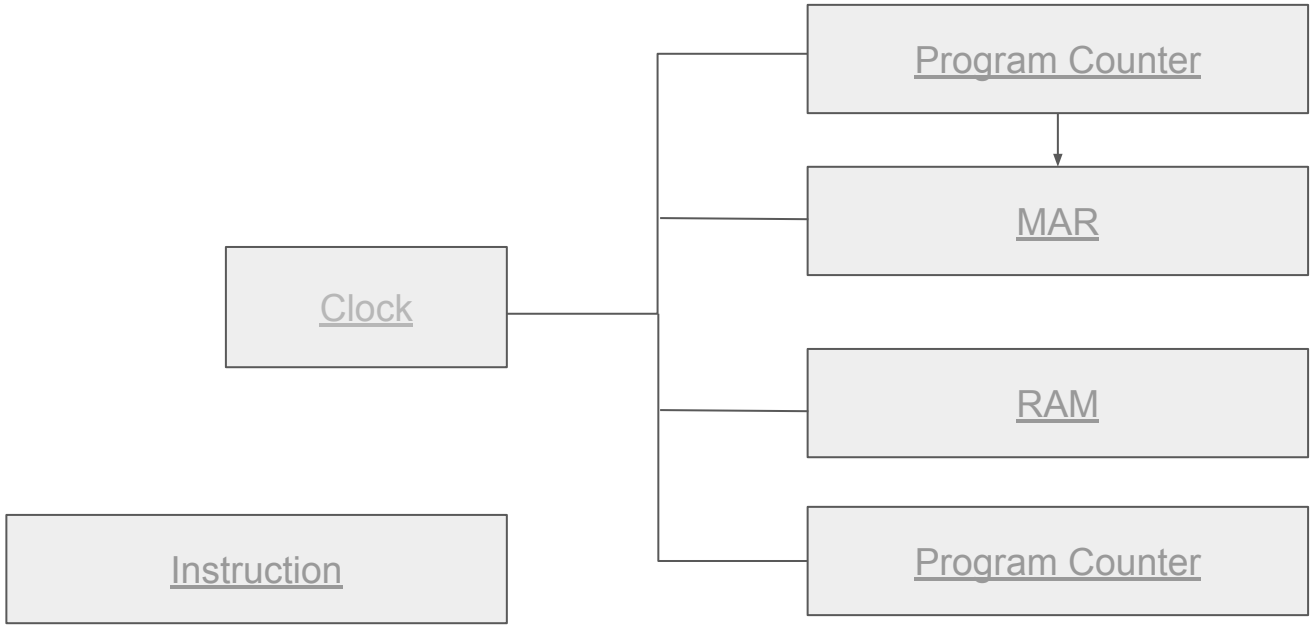
Ben Eater’s 8 Bit Computer

Write to memory
Read from memory

Registers are groups of latches, which holds a single number, and the number of bits in a register is called its width.

RAM or Random Access Memory
Persistent Memory

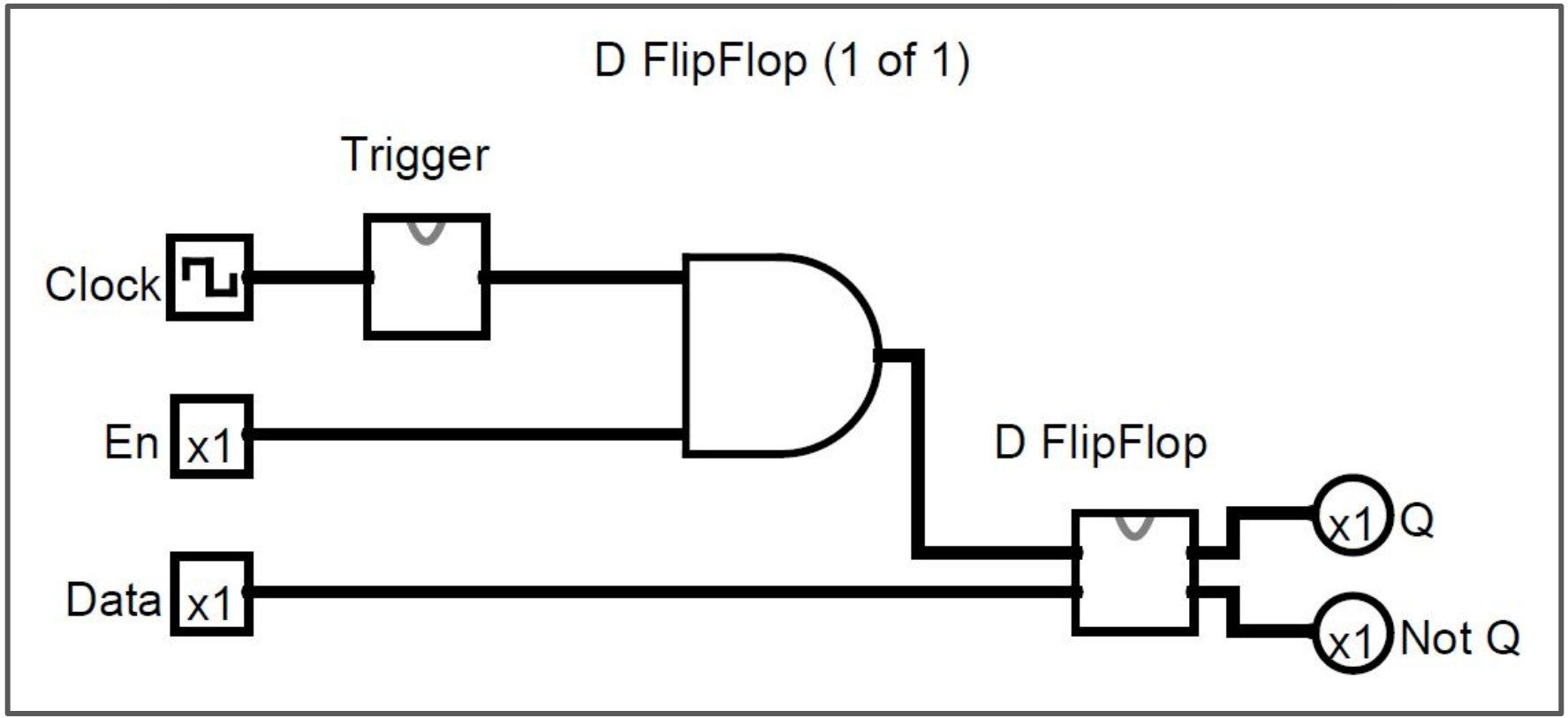
Ben Eater’s 8 Bit Computer



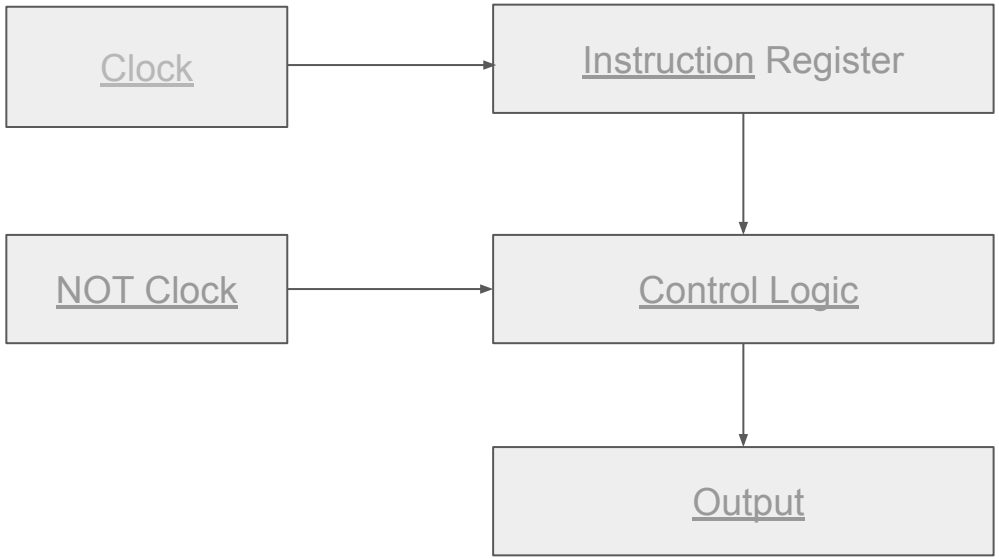
Memory, Address Instructions

Run Mode And Program Mode

Ben Eater's 8 Bit Computer

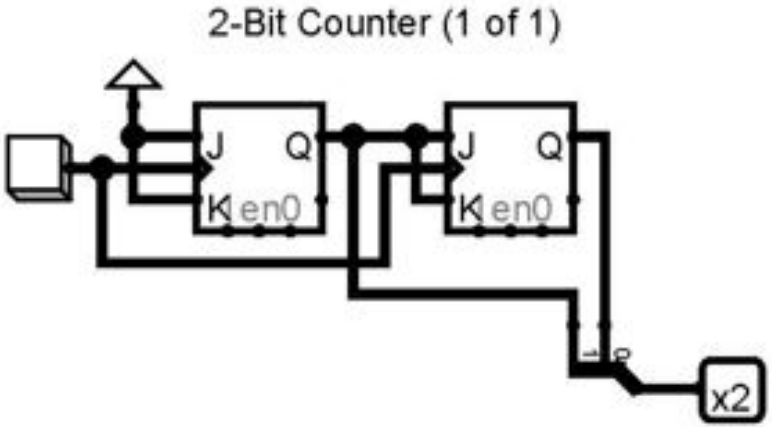


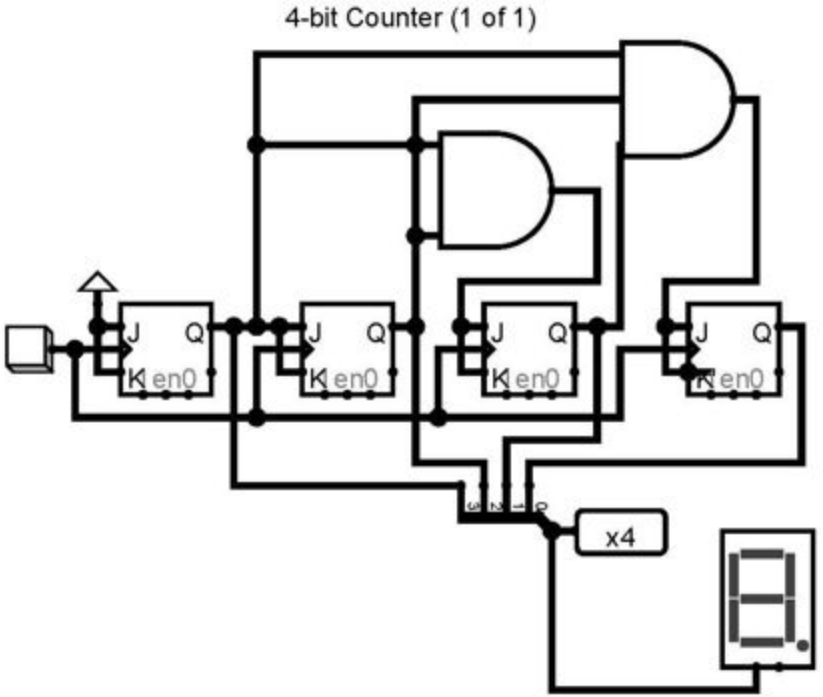
Ben Eater’s 8 Bit Computer



Control Logic

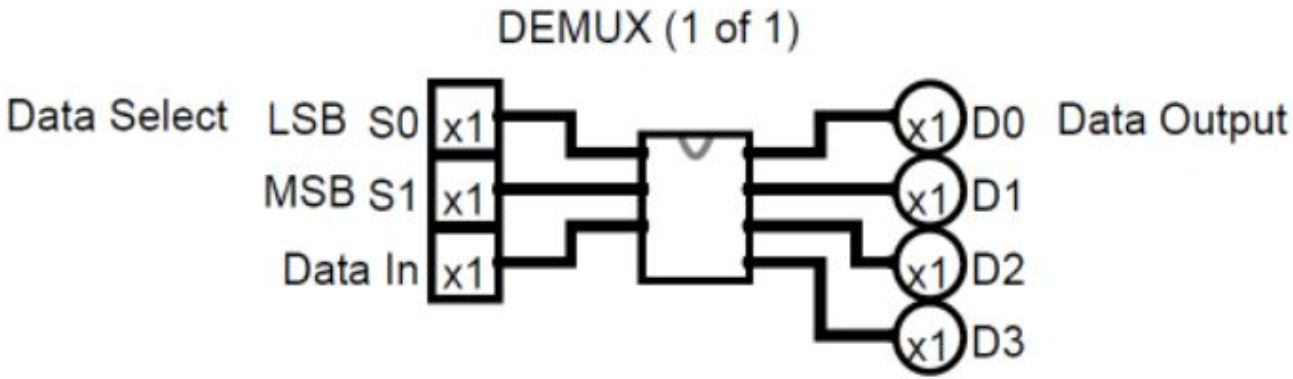
Ben Eater’s 8 Bit Computer





2 Bit Counter used in Instruction Step Counter
4 Bit Counter used in Program Counter
4 Bit Counter used in OUTPUT Display

Ben Eater’s 8 Bit Computer



Ben Eater’s 8 Bit Computer

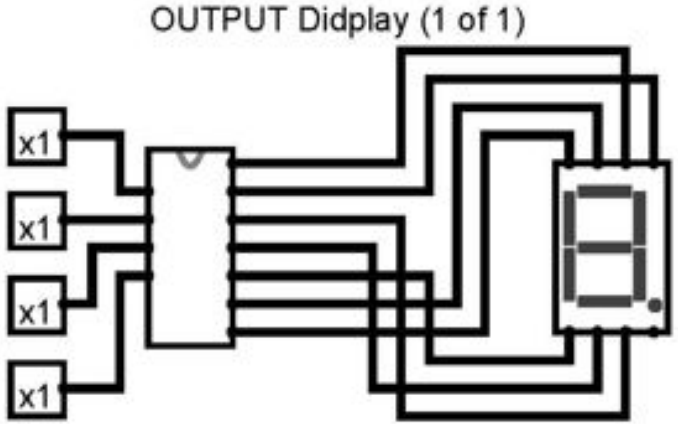


Figure from LOGISIM File.

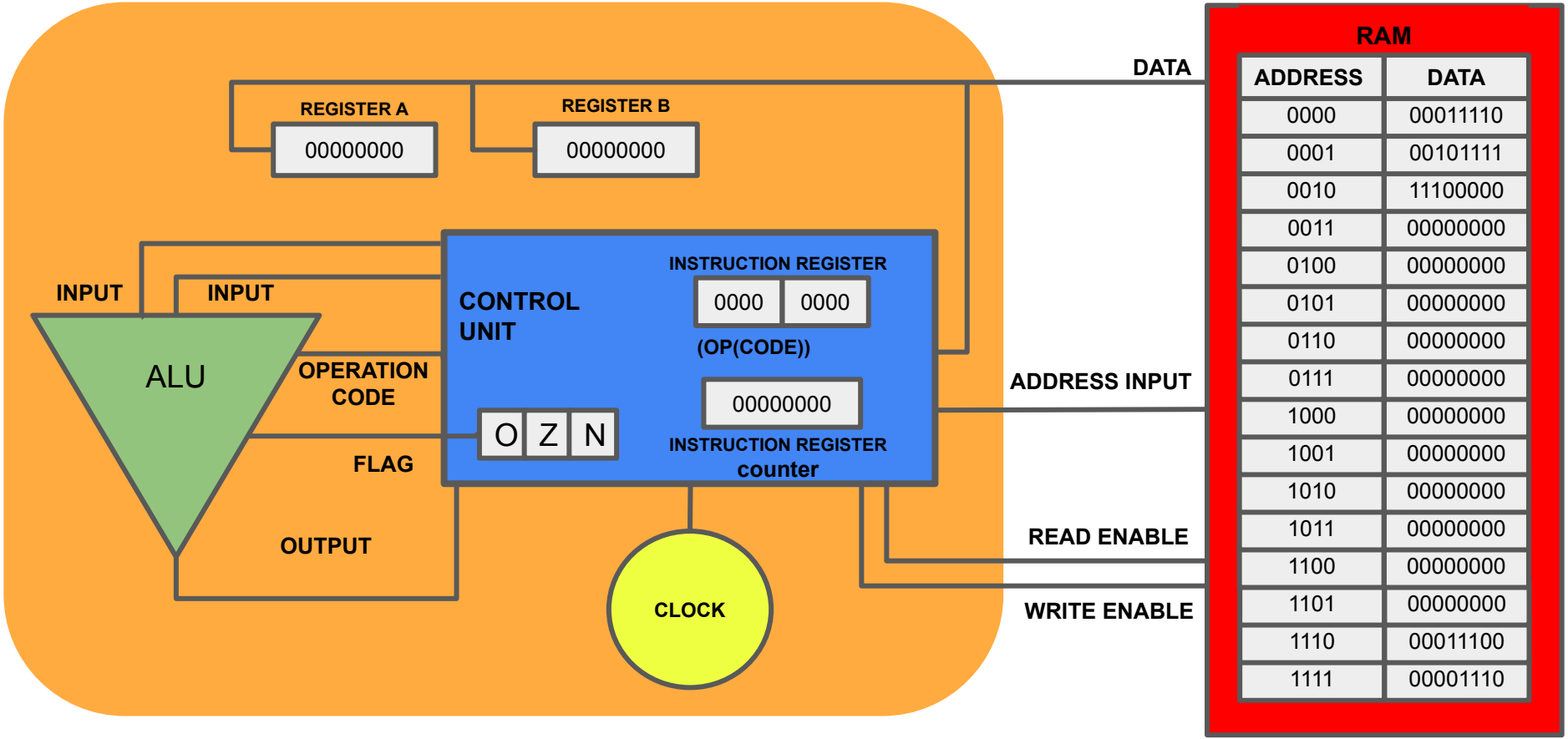
Binary To Decimal to 7 Segment Conversion

Ben Eater's 8 Bit Computer Instructions

NAME	INSTRUCTION				STEP	HLT	MI	RI	RO	IO	II	AI	AO	EO	SU	BI	OI	CE	CO	J	FL
FETCH	X	X	X	X	0 0 0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	
	X	X	X	X	0 0 1	0	0	0	1	0	1	0	0	0	0	0	0	1	0	0	
LDA	0	0	0	1	0 1 0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	
	0	0	0	1	0 1 1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	
	0	0	0	1	1 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ADD	0	0	1	0	0 1 0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	
	0	0	1	0	0 1 1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	
	0	0	1	0	1 0 0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	
OUT	1	1	1	0	0 1 0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	
	1	1	1	0	0 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	1	0	1 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Control Logic and Programing

CENTRAL PROCESSING UNIT(CPU)



ADDRESS	DATA
0000	00011110
0001	00101111
0010	11100000
0011	00000000
0100	00000000
0101	00000000
0110	00000000
0111	00000000
1000	00000000
1001	00000000
1010	00000000
1011	00000000
1100	00000000
1101	00000000
1110	00011100
1111	00001110

VAR NAME: CHNGBASE

```
ClrHome
Input "DIGITS: ",D
Input "NUMBER: ",A
Input "IN BASE: ",B
Input "TO BASE: ",F
Ø→T
Ø→C
For(J,Ø,D-1)
int(A/(1Ø^(D-1-J)))→C
C*B^(D-1-J)+T→T
A-C*1Ø^(D-1-J)→A
End
1→P
Ø→E
For(K,Ø,15)
int(T/(F^(15-K)))→E
Output(5,P,E)
T-(E*F^(15-K))→T
P+1→P
End
Disp "
```

EXAMPLE OF ASM PROGRAM
On a TI-xxxx

Lesson Plans

ELTR-180
Networking and Data Communications

Project 1 build a 6502 to network with a partner:
https://eater.net/6502

Use the 6502 to do practical lessons with error correction:
https://eater.net/crc

Ben Eater's 8 Bit Computer

Testing and TroubleShooting

Testing:

Run a Functional Module Check. You may Need to hookup the required INPUTS and OUTPUTS to see if the Module is operational.

Running the subsystem checks before networking them together or through the BUS will help isolate for troubleshooting.

ADD another module Test operations if good then add one more and Test. Do this until they Master System is completed.

TroubleShooting:

Problem

Clock has an inverter OUTPUT and only lights if the LED is place in circuit with Cathode to pin 8 of the 74LS08 AND Gate and Anode to VCC.

Solution

Maksure the ICs have VCC and Ground connected

Power distribution Problems

Why does an LED light when the INPUT is 0 v?

Solution

Trace signal on bus by remove each modules connection on by one until you find the one. Sometimes damaged ICS will send random signals,

APA Citation

Eater, B. (n.d.). *8 Bit Computer*. Eater.Net. https://eater.net/8bit

8 bit-computer.jpeg image

X,B.(n.d). Using the 555 Timer. *DroneBot Workshop*.https://dronebotworkshop.com/555-timer/

image of 555 timer schematic

Eater,B. [Ben Eater]. (Year, Month Day). *Clock logic - 8-bit computer clock - part 4* [Video]. YouTube. https://www.youtube.com/watch?v=SmQ5K7UQPMM

Anne,C. [*Crash Course*]. (Year, Month Day). *Crash Course-* The Central Processing Unit (CPU) Crash Course Computer Science #7 [Video]. YouTube. https://www.youtube.com/watch?v=FZGugFqdr60&t=548s

10:28 CPU SLIDE

Ben Eater 8 Bit Computer

GUIDE TO GETTING STARTED

Thank You