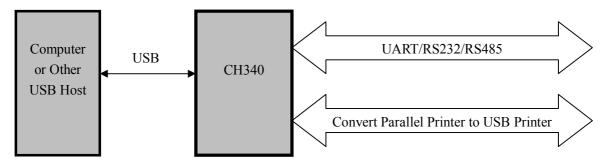
USB to Serial Port Chip CH340

Datasheet Version: 3B http://wch.cn

1. Introduction

CH340 is a USB bus converter chip which converts USB to serial port or printer port.

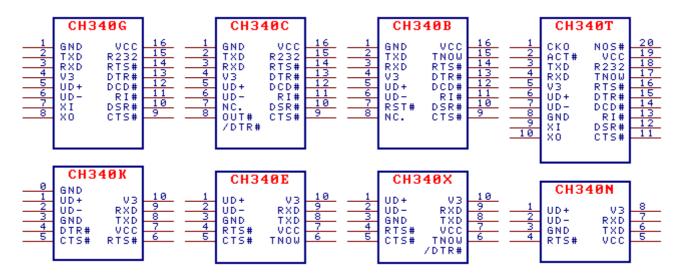
In UART mode, CH340 provides standard MODEM signals, used to extend serial port for computers, or upgrade directly from normal serial device to USB bus. For more information about converting USB to printer interface, please refer to the CH340DS2 datasheet.



2. Features

- Full-speed USB device interface, USB 2.0 compatible.
- Emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original UART applications are totally compatible without any modification in Windows operating systems.
- Hardware full duplex UART interface, integrated transmit-receive buffer, supports communication baud rate varies from 50bps to 2Mbps.
- Supports common MODEM interface signals RTS, DTR, DCD, RI, DSR and CTS.
- Provides further RS232, RS485, RS422 interface, etc. through external voltage conversion chip.
- CH340R supports IrDA criterion SIR infrared communication, supports baud rate varies from 2400bps to 115200bps.
- Built-in firmware, software compatible with CH341, use VCP driver of CH341 directly.
- Supports 5V and 3.3V power supply voltages.
- CH340C/N/K/E/X/B have integrated clock, no external crystal required, CH340B also integrates EEPROM used to configure the serial number, etc.
- RoHS compliant SOP-16, SOP-8, SSOP-20 and ESSOP-10, MSOP-10 lead-free package.

3. Packages



Package	Body	size	Lead pitch		Description	Part No.
SOP-16	3.9mm	150mil	1.27mm	50mil	Small outline 16-pin patch	CH340G
SOP-16	3.9mm	150mil	1.27mm	50mil	Small outline 16-pin patch	CH340C
SOP-16	3.9mm	150mil	1.27mm	50mil	Small outline 16-pin patch	CH340B
SOP-8	3.9mm	150mil	1.27mm	50mil	Small outline 8-pin patch	CH340N
ESSOP-10	3.9mm	150mil	1.00mm	39mil	Shrink Small outline 10-pin patch with EPAD	CH340K
MSOP-10	3.0mm	118mil	0.50mm	19.7mil	Micro Small outline 10-pin patch	CH340E
MSOP-10	3.0mm	118mil	0.50mm	19.7mil	Micro Small outline 10-pin patch	CH340X
SSOP-20	5.3mm	209mil	0.65mm	25mil	Shrink Small outline 20-pin patch	СН340Т
SSOP-20	5.3mm	209mil	0.65mm	25mil	Shrink Small outline 20-pin patch	CH340R

Note:

CH340C, CH340N, CH340K, CH340E, CH340X and CH340B have integrated clock, no external crystal required.

CH340B has integrated EEPROM used to configure serial number, some functions can be customized, etc.

CH340K has 3 built-in diodes to reduce current flow backwards between the I/O pins of the MCU.

The EPAD of CH340K is 0# pin (GND), which is an optional connection; the 3# pin (GND) is the necessary connection.

CH340X is improved based on CH340E, with 5V tolerant characteristic added when the power supply is 3.3V.

6# pin of CH340X can be changed from TNOW to DTR# when an external resistor is connected, see Section 5.3 for the two configurations.

CH340C whose batch number begins with 4 and last 3-digit greater than B40, 8# pin can be changed to DTR# when a $4.7K\Omega$ pull-down resistor is connected.

CH340R provides reverse polarity TXD and MODEM interface signals, discontinued.

The USB transceiver of CH340 is designed according to the built-in design of USB2.0, and it is

recommended that no external resistor is in series with UD+ and UD- pins.

4. Pin definitions

SSOP20 Pin No.	SOP16 Pin No.	ESSOP10 Pin No.	SOP8 Pin No.	Pin Name	Pin Type	Pin Description (description in bracket is only applied for CH340R)	
19	16	7	5	VCC	POWER	Power supply voltage input, requires an external 0.1uF decoupling capacitor	
8	1	3, 0	3	GND	POWER	Ground, connected to ground of USB bus directly	
5	4	10	8	V3	POWER	Connect to VCC when VCC is 3V3, connect to 0.1uF decoupling capacitor when VCC is 5V	
				XI	IN	CH340T/R/G: Input of crystal oscillator, connect to 12MHz crystal and capacitor	
9	7	NONE	NONE	NC.	NONE	CH340C: No Connection, do not connect	
				RST#	IN	CH340B: Input of external reset, active low, integrated pull-up resistor	
				XO	OUT	CH340T/R/G: Output of crystal oscillator, connect to 12MHz crystal and capacitor	
10	8	NONE	NONE	OUT#	OUT	CH340C: MODEM output IO, software controlled, active low. Part of batch number in CH340C switch to 2nd DTR# optionally	
				NC.	NONE	CH340B: No Connection, do not connect	
6	5	1	1	UD+	USB signal	Connect to USB D+ Signal directly, do not series resistors	
7	6	2	2	UD-	USB signal	Connect to USB D- Signal directly, do not series resistors	
20	NONE	NONE	NONE	NOS#	IN	Forbid USB device suspending, active low, integrated pull-up resistor	
3	2	8	6	TXD	OUT	Transmit asynchronous data output (reverse output for CH340R)	
4	3	9	7	RXD	IN	Receive asynchronous data input, integrated configurable pull-up and pull-down resistor	
11	9	5	NONE	CTS#	IN	MODEM input signal, clear to send, active low(high)	
12	10	NONE	NONE	DSR#	IN	MODEM input signal, data set ready, active	

	,			1			
						low(high)	
13	11	NONE	NONE	RI#	IN	MODEM input signal, ring indicator, active low(high)	
14	12	NONE	NONE	DCD#	IN	MODEM input signal, data carrier detect, active low(high)	
15	13	4	NONE	DTR#	OUT	MODEM output signal, data terminal ready, active low(high)	
16	14	6	4	RTS#	OUT	MODEM output signal, request to send, active low(high)	
2	NONE	NONE	NONE	ACT#	OUT	USB configuration completed state outpactive low	
18	15	NONE	NONE	R232	IN	CH340T/R/G/C: Assistant RS232 enable, active high, integrated pull-down resistor	
				TNOW	OUT	CH340T/E/X/B: Ongoing data transmission status indicator, active high. CH340X can switch to DTR# optionally by connecting an external resistor	
17	15	NONE	NONE	NONE CH340R:Serial mode inp integrated pull-up resistor, we infrared UART mode when the		integrated pull-up resistor, works on SIR infrared UART mode when the pin is low and normal UART mode when the pin is	
1	NONE	NONE	NONE	CK0	OUT	CH340T: clock output	
1	110111	110111	TIONE	NC.	NONE	CH340R:No Connection, do not connect	

Note: Unused I/O pins of CH340 should be NC. The application diagram takes CH340T as an example and also applies to CH340G/C/N/K/E/X/B, etc.

5. Function descriptions

5.1. Clock, reset, power, connect

CH340G/CH340T/CH340R need to work with 12MHz clock signal supplied to XI pin. Generally, clock signal is generated by the inverter in CH340 through crystal oscillation. The peripheral circuit needs to place a crystal of 12MHz between XI and XO, and connect to a capacitor to ground separately.

CH340C/N/K/E/X/B have integrated clock generator, no external crystal and oscillating capacitor required.

CH340 has integrated power-on reset circuit. CH340B also provides an external reset pin (active low).

CH340 supports 5V and 3.3V power supply. When using 5V power supply, the VCC pin connects 5V power and the V3 pin should connect with a 0.1uF decoupling capacitor. When using 3.3V power supply, V3 should connect with VCC, both powered with 3.3V power supply, and the other circuit voltage which connected with CH340 cannot exceed 3.3V.

For CH340X and CH340C/N whose last 3-digit batch number is greater than B40, IO supports 5V, avoiding inward current poured backwards.

CH340K not only avoids inward current poured backwards, but also reduces drive capacity to external, avoiding current poured backwards from CH340 to external.

CH340 supports USB device suspending automatically to save power. USB device suspending is forbidden when NOS# is driven low.

DTR# pin of CH340G/C/T/K is used as a configuration input pin before the USB configuration completion. An external $4.7K\Omega$ pull-down resistor can be connected with this pin to generate default low during USB enumeration, to apply larger supply current from USB bus via the configuration descriptor.

CH340 has integrated USB pull-up resistor, UD+ and UD- pins should be connected to USB bus directly.

In serial UART mode, CH340 contains these pins: data transfer pins, MODEM interface signals and assistant pins.

Data transfer pins contain: TXD and RXD. RXD keeps high when UART reception is idle. For CH340G/C/T/R, if the R232 pin is driven high, assistant RS232 function will be enabled, an internal inverter will automatically insert to the RXD, and the pin becomes low by default. When UART transmission is idle, the TXD of CH340G/C/N/E/X/B/T keeps high, CH340K is weak high, while CH340R keeps low.

MODEM interface signals contain: CTS#, DSR#, RI#, DCD#, DTR# and RTS#, CH340C also provides OUT# pin. All these MODEM interface signals are controlled and function defined by computer applications.

Assistant pins contain: IR#, R232, CK0, ACT# and TNOW. When IR# is low, infrared serial interface mode is enabled. R232 is used to control assistant RS232 function. If R232 is driven high, the RXD input will be reversed automatically. ACT# is USB device configuration complete status output (such as USB infrared adapter ready). TNOW indicates CH340 is transmitting data from UART when it is high and becomes low when transmits over. In RS485 and other half-duplex mode, TNOW could be used to indicate UART transmit-receive status. IR# and R232 are detected only once after power on reset.

5.2. Configuration information of CH340B

CH340B also provides EEPROM for configuring data area, product serial number and other information could be customized for each chip by specific software tools, configurable data area is shown in the table below.

Byte Address	Abbreviation	Description Of Chip Configuration Data Area	Default
00Н	SIG	For CH340B: internal configuration information valid indicator, must be 58H. For CH340H/S: external configuration information valid indicator, must be 53H. Invalid for other value	00Н
01H	MODE	Serial mode, must be 23H	23Н
02H	CFG	Specific configuration of chip, bit5 is used to configure product Serial Number: 0= valid; 1= invalid.	FEH

03Н	WP	Internal configuration information write protect flag 57H imply read only, otherwise can be rewrite	00Н
05H~04H	VID	Vendor ID, high byte is behind, any value. Set to 0000H or 0FFFFH implies VID and PID using vendor default value	1А86Н
07H~06H	PID	Product ID, high byte is behind, any value	7523Н
0AH	PWR	Max Power, The maximum supply current in 2mA units	31H
17H~10H	SN	Serial Number, the length of ASCII string is 8, disable the Serial number when the first byte is not ASCII character (21H~7FH)	12345678
3FH~1AH	PROD	For CH340B: Product String, Unicode string for product description. The first byte is by total bytes (less than 26H), the next byte is 03H, Unicode string after that, using vendor default description when do not meet characteristics above.	Using product default description when the first byte is 00H
Others		(Reserved)	00H or FFH

5.3. DTR and multi-mode MCU download

For CH340X, 6# Pin defaults to TNOW, weak pull-up during power-on or reset, output TNOW during normal operation used for half-duplex transceiver switchover. By connecting an external resistor with 6# pin, TNOW can be switch to DTR#, the two options are as follows:

- ① If the $4.7K\Omega$ pull-down resistor is connected to GND with the 6# pin, it will enter the open source DTR enhanced mode, and the 6# pin will automatically switch to the open source driven DTR# pin , which is used to connect the boot mode pin of MCU. The default DTR # is not output and is kept low by the external resistor, but the DTR# pin can be set to output high level or not output by the application program, which is used for multi-mode MCU download with DTR# default low level.
- ② If a 4.7KΩ resistor is connected between the 6# pin and the 5# pin, it will enter the push-pull DTR enhanced mode, and the 6# pin will automatically switch to the push-pull driven DTR# for connecting to the control pin of the MCU. The application program sets the DTR# pin to output high or low level for multi-mode MCU download with DTR# default high level.

For CH340C with batch number begin with 4 and last 3-digit greater than B40, 8# pin defaults to OUT#, weak pull-up during power-on or reset, output MODEM OUT# during normal operation. If 8# pin is connected to a $4.7 \mathrm{K}\,\Omega$ pull-down resistor, into open source DTR enhanced mode, 8# pin switches to the open source driver's second DTR# automatically, connects BOOT mode of MCU, By default the second DTR# is not output, kept low by external resistor, but DTR# pin can be set by the application to output high or no, for DTR# default low level Multi-mode MCU download. In addition, 13# pin original DTR# is used for DTR# default high level Multi-mode MCU download.

5.4. UART features

CH340 has integrated separate transmit-receive buffer and supports simplex, half-duplex and full duplex UART communication. Serial data contains one low-level start bit, 5, 6, 7 or 8 data bits and 1 or 2 high-level stop bits, supports odd/even/mark/space/none parity CH340 supports common baud rate: 50, 75, 100, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000,

57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1500000, 2000000, etc.

For one-directional 1Mbps and above, or bi-directional 500Kbps and above, recommended to use CH343, enable automatic hardware flow control.

The baud rate error of CH340 UART reception is about 2%, the baud rate error of CH340G/CH340T/CH340R UART transmission is less than 0.3%, and the baud rate of CH340C/CH340N/CH340K/CH340E/CH340X/CH340B is less than 1.2%.

In Windows OS of computer, CH340 driver can emulate standard UART. So the mostly original serial applications are totally compatible, without any modification.

CH340 can be used to upgrade the serial interface peripherals, or expand extra UART for computers via USB bus, through external level conversion chip provide further RS232, RS485, RS422 interface, etc.

Through extra infrared transceiver, CH340R can expand SIR infrared adapter for computer via USB bus, realize infrared communication between computers and peripheral equipment that comply with IrDA specifications.

6. Parameters

6.1. Absolute maximum ratings

(Operating in critical ratings or exceeding the absolute maximum ratings may cause chip to not work or even be damaged.)

Symbol	Paran	neter Description	Min.	Max.	Unit
TA	Operating ambient temperature	CH340G/CH340T/CH340R	-40	85	$^{\circ}$
		CH340C/CH340N/CH340K/ CH340E/CH340B	-20	70	$^{\circ}$
		CH340X/ CH340C/N whose batch number begins with 4	-40	85	${\mathbb C}$
TS	Stor	age temperature	-55	125	${\mathbb C}$
VCC	Supply voltage(VCC co	-0.5	6.0	V	
VIO	Voltage of	n input or output pins	-0.5	VCC+0.5	V

6.2. Electrical characteristics (5V)

(Test conditions: TA=25°C, VCC=5V, exclude pins connected to USB bus.)

Symbol		Parameter Descr	Min.	Тур.	Max.	Unit	
VCC	Supply voltage	1	an external capacitor, nnect to VCC	4.0	5	5.3	V
ICC			CH340G/C/N/K/E/ X/T/R		7	20	mA
			CH340B		6	15	mA

ISLP	Total supply current when	CH340G/K/T/R/B		0.09	0.2	mA
IOLI	USB is suspended	CH340C/N/E/X	0.05 0.15	0.15	mA	
VIL	Input low volt	age	0		0.9	V
VIH	Input high volt	2.3		VCC	V	
VOL	Output low voltage(6mA			0.5	V	
VOH	Output high voltage(2mA s	VCC-0.6			V	
IUP	Sunk current of input with integ	rated pull-up resistor	3	150	300	uA
IDN	Sunk current of input with int resistor	egrated pull-down	-40	-100	-300	uA
VR	Voltage threshold when p	oower-on reset	2.4	2.6	2.8	V

6.3. Electrical characteristics (3.3V)

(Test conditions: TA=25°C, VCC=V3=3.3V, exclude pins connected to USB bus.)

Symbol	Parameter Description			Min.	Тур.	Max.	Unit
VCC	Supply	V3 connects	CH340G/T/R	2.9	3.3	3.6	V
V C C	voltage	to VCC	CH340C/N/K/E/X/B	3.1	3.3	3.6	, v
ICC	Operating	g total supply	CH340G/C/N/K/E/X/T/R		4	12	mA
icc	cı	ırrent	CH340B		3	9	mA
ISLP	Total su	pply current	CH340G/K/T/R/B		0.08	0.2	mA
ISLI	when USB is suspended		CH340C/N/E/X		0.04	0.15	mA
VIL	Input low voltage			0		0.8	V
VIH		Input hig	h voltage	1.9		VCC	V
VOL	Out	put low voltage	(4mA sunk current)			0.5	V
VOH	-	Output high voltage(2mA sourced current) (40uA sourced current during chip reset)					V
IUP	Sunk current of input with integrated pull-up resistor			3	70	200	uA
IDN	Sunk current of input with integrated pull-down resistor			-30	-70	-200	uA
VR	Volt	age threshold w	hen power-on reset	2.4	2.6	2.8	V

6.4. Timing parameters

(Test conditions: TA=25°C, VCC=5V or 3.3V.)

Symbol	Parameter Description	Min.	Тур.	Max.	Unit
FCLK	Frequency of input clock in XI	11.98	12.00	12.02	MHz

Ī	TPR	Reset time of power-up	20	35	50	mS
ı	111	Reset time of power-up	20	33	30	1113

7. Applications

7.1. USB to 9-line RS232 UART (figure below)

The figure below shows that CH340T (or CH340C/B) converts USB to RS232 UART. CH340 provides common UART and MODEM signals, and converts TTL to RS232 through level converter chip U8. The P11 port is DB9 connector, the pins and their functions are the same as common PC DB9 connector, the chips similar with U8 is MAX213/ADM213/SP213/MAX211 etc.

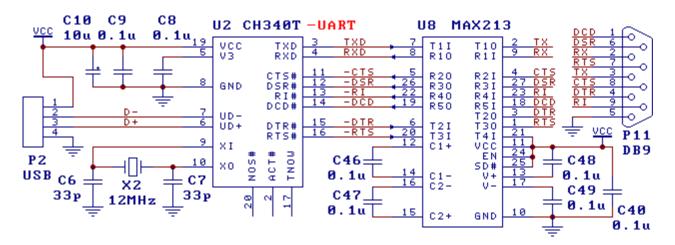
U8 and C46/C47/C48/C49/C40 could be removed when realize USB to TTL converter only. For the signal lines shown in the figure, only RXD, TXD and public ground need to be connected, the other signal lines should not connect when not used.

P2 is a USB port. USB bus contains a pair of 5V power lines and a pair of data signal lines. Usually, the color of +5V power lines is red, the black one is ground. D+ signal line is green and the D- signal line is white. The max supply current of USB bus is up to 500mA. Generally, CH340 and low-power USB products can use the 5V power supplied by USB bus directly. If the USB products supply standing power by other manner, CH340 should use this power too, this can help avoid I/O current poured backwards between USB power supplies. If the USB bus power and standing power are necessary at the same time, connect a 1Ω resistor between USB bus 5V power line and USB products 5V standing power line, and connect the ground lines of these two power directly.

The C8 capacitor on V3 is 0.1uF, used to CH340 internal power node decoupling. The C9 capacitor is 0.1uF, used to external power decoupling.

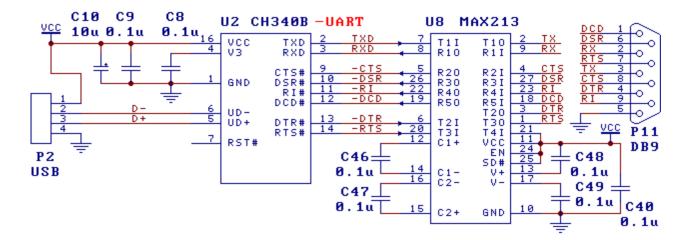
For CH340G/T/R, the X2 crystal, C6 and C7 capacitors are used for clock oscillation circuit. The X2 is a 12MHz quartz crystal, C6 and C7 are monolithic or high frequency ceramic capacitors with 33pF. If X2 is a low-cost ceramic, C6 and C7 must use the recommended value of crystal manufacturer and generally is 47pF. For the crystal which is difficult to oscillate, halved value is suggested for C6.

For CH340C/N/K/E/X/B, the X2 crystal, C6 and C7 capacitors are not required.



When designing the PCB, pay attention to: C8 and C9 decoupling capacitors must keep close to connection pin of CH340; make sure D+ and D- signal lines are parallel and provide ground or pour copper on both

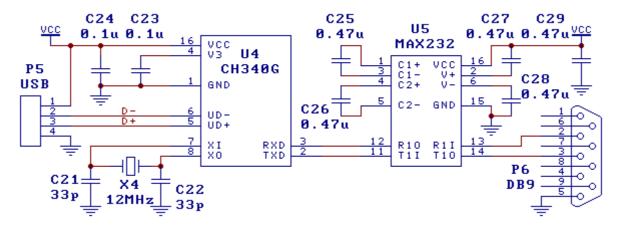
sides to reduce outside interference; the signal lines relevant to XI and XO should be kept as short as possible. In order to reduce the high frequency interference, around the ground or pour copper around the relevant components.



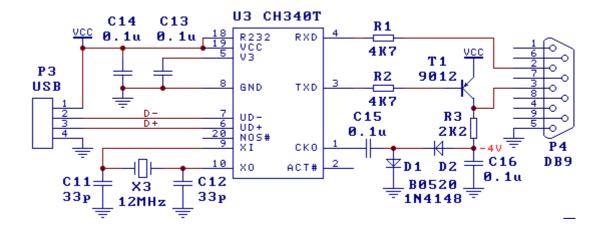
7.2. USB to 3-line RS232 UART (figure below)

The figure below shows that USB is converted to 3-line RS232 which is the most basic and most commonly used. For U5, select MAX232/ICL232/SP232 etc.

Unused CH340 pins can be not connected. For CH340C/N/K/E/X/B, X4, C21 and C22 are not required.



7.3. USB to RS232 UART, simplified version (figure below)



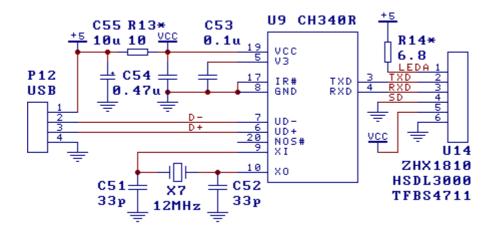
The figure above also shows that USB is converted to RS232. This circuit has the same function as the circuit shown in Section 7.2 except the range of output RS232 is narrower. When R232 pin is driven high, the assistant RS232 function will be enabled, just need to add some diodes, transistors, resistors and capacitors, the special level converter chip U5 in Section 7.2 could be replaced and the hardware cost is lower.

7.4. USB to RS485 UART

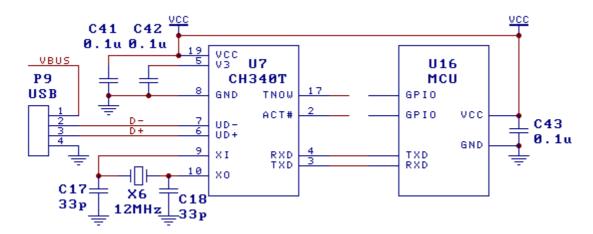
TNOW pin can be used to control DE (active high and transmit enabled) and RE# (active low and receive enabled) pins of RS485 transceiver.

7.5. USB to Infrared adapter (figure below)

The figure below shows a USB to infrared adapter design which is composed of a USB to IrDA infrared chip (CH340R) and an infrared transceiver U14 (ZHX1810/HSDL3000 etc). The R13 resistor is used to weaken influence of large current in infrared transmitting. The R14 current limiting resistor should be adjusted according to the manufacturer's recommended value of the U14 infrared transceiver.



7.6. Connect to MCU and supply power together (figure below)

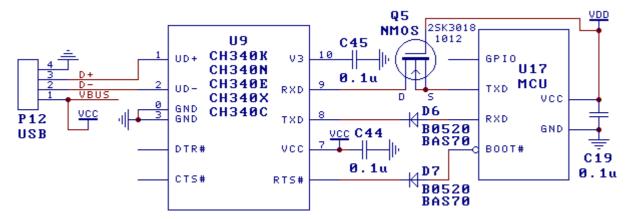


The figure above is a reference design to achieve USB connection on an MCU by connecting it to a CH340 via TTL UART. Here self-power mode is selected, VCC supports 5V or 3.3V (V3 shorted to VCC if VCC is 3.3V), and USB bus power (VBUS) is not used at all (Can be tested by connecting series resistor to I/O of MCU if needed). CH340 shares the same power source with MCU, hence there would be no current inrush

through I/O between CH340 and MCU.

Unused CH340 pins can be not connected. For CH340C/N/K/E/X/B, X6, C17 and C18 are not required.

7.7. Connect to MCU and supply power separately, avoiding bi-directional current poured backwards (figure below)



The figure above is a reference design to achieve USB connection on an MCU by connecting it to a CH340 via TTL UART. CH340 is powered by USB bus VBUS. MCU is powered by another power source VDD, VDD supports 5V, 3.3V and even 2.5V, 1.8V.

The RXD pin of MCU in the figure should enable the internal pull-up resistor. If not, it is recommended to add $2K\Omega \sim 22K\Omega$ pull-up resistor to the RXD pin and connect it to the power supply VDD of MCU.

Prevent current backward when CH340 is powered on but MCU is not powered on. The D6 and D7 diodes and the Q5 NMOS tube in the figure are used to prevent CH340 from flowing back current to the power-off MCU through the RXD or TXD internal diode of MCU under dual power supply mode. The connection between D7 and RTS/BOOT0# is optional. The D6 diode reverses current to MCU through RXD internal diode of MCU for TXD high level of CH340; The D7 diode reverses current to MCU through the boot internal diode of MCU for RTS high level of CH340; The Q5 NMOS tube reverses the current to the MCU through the TXD internal diode of the MCU for the RXD internal pull-up current of the CH340.

Prevent internal current backward when CH340 is not powered but MCU is powered on. The IO of CH340K, CH340X and CH340C, CH340N with the last three digits of batch number greater than B40 will automatically prevent internal backflow, that is, when CH340 is not powered on, but MCU is powered on, there will be no backflow current. In addition, D6, D7 and Q5 can prevent CH340 from injecting current to the power-off MCU, so the above figure can realize complete bidirectional anti backflow.

For CH340 with other batch numbers or models, additional anti filling circuit shall be added. Usually an NMOS tube is connected in series with a Shottky diode to prevent bidirectional backflow. For example, a Schottky diode is connected in series at the drain D end of Q5, and its anode terminal is connected to the RXD of CH340. An NMOS tube is connected in series between D6 and CH340, and its drain is connected to D6 and its gate is connected to the power supply VCC of CH340.

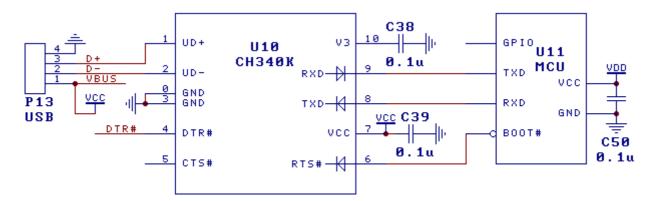
If it is determined that a certain situation will not occur, the corresponding NMOS tube or diode can be removed. For example, the IO of some MCUs supports anti backflow or 5VT, or the MCU has a permanent self-contained power supply. There is no need to worry about CH340 injecting current to the MCU, then D6, D7 and O5 can be removed and shorted.

Prioritized choice for diode is a low-power Schottky diode, such as BAS70, BAT54, B0520, etc.

NMOS tubes with low power and capacitance are preferred, such as 2SK3018, 1012, etc.

Generally, it is not recommended that CH340 and MCU are powered separately. If it is really necessary, it is recommended to use CH340K or CH343 (a USB to UART chip which has VIO power pins and supports I/O independent power supply).

7.8. Connect to MCU and supply power separately, avoiding inward current poured backwards (figure below)



The figure above shows the reference circuit of MCU connecting to CH340K through TTL UART to realize USB communication under dual power supply mode. The CH340K is powered by the USB bus, VBUS (VCC), and the MCU uses another power supply VDD, which supports 5V, 3.3V or even 2.5V and 1.8V. The EPAD of CH340K is an optional GND pin, which can be easily connected to GND or not connected according to PCB routing.

The TXD, RTS# and RXD pins of CH340K have built-in diodes (as shown in the figure) to prevent current backward, and a weak pull-up resistor of about $75 \mathrm{K}\Omega$ is built to maintain the high level in default or idle state (not shown in the figure), which can not only realize low-level drive and weak high-level drive, but also reduce the current backflow when CH340K and MCU supply power independently. CH340K can completely prevent the internal current of MCU power supply to power-off CH340K, but also reduce the external current of CH340K power supply to power-off MCU (no more than $150\mu\mathrm{A}$) $_{\circ}$

In addition, CH340X and CH340C, CH340N with the last three digits of the batch number greater than B40 can also completely prevent the MCU power supply from injecting the current of the power-off CH340, so as to avoid the CH340 wasting the current of the MCU power supply after the USB power is off.

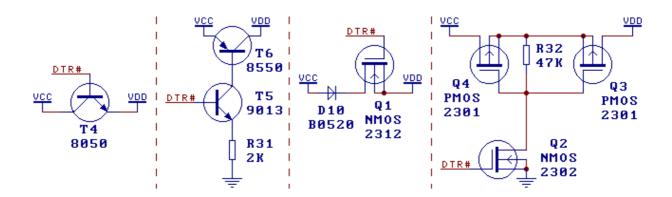
If it is necessary to completely prevent the CH340K power supply from injecting the current to the power-off MCU, refer to the figure in Section 7.7 and add NMOS and diode.

When it is used for communication baud rate above 120Kbps, it is recommended to enable the built-in or external 2K $\Omega \sim$ 22K Ω pull-up resistor for the RX pin of MCU, or select other models of USB to UART chip with VIO power supply pin to support I/O independent power supply.

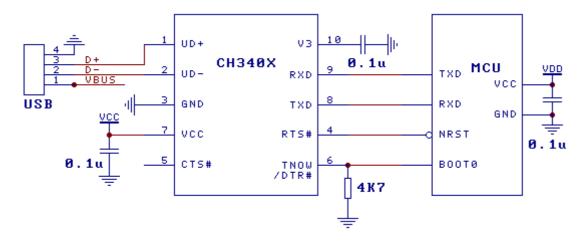
The DTR# pin of CH340K is an ordinary push-pull output, and the CTS# pin is an ordinary input with built-in pull-up resistor. Neither of these two pins has built-in diodes and does not have the function of preventing current backflow. Generally, they are not used to connect MCU.

DTR # can be used to control the power switch of VCC supplying power to VDD. As shown in the figure

below, four power control schemes can be selected. T4 scheme and Q1 scheme (Q1 should choose N-MOSFET with lower Vth) are simplified schemes. The VDD output voltage is about VCC-0.8V and the current does not exceed 200mA; T6 scheme and Q3 scheme are complete schemes. D10 in the figure is used to prevent VDD from supplying power to VCC, which is optional.



7.9. One-click USB download of MCU (figure below)



The figure above shows the reference circuit for one-click download based on a multi-mode USB to UART MCU, without manual setting or manual reset.

The type of MCU targeted in the figure above: the MCU itself needs to support one-click download through the UART. NRST is a reset input (active low). By default, application is selected when BOOT0 is low, and Boot-Loader is selected when it is high. For example 32F103, etc.

The MCU in the figure above is CH340X. The resistance of the $4.7K\Omega$ pull-down resistor can be selected from 3 to $5.6K\Omega$. This resistor also serves as the BOOT0 pull-down resistor of the MCU. For CH340C with the last 3 digits of the batch number greater than or equal to B40, OUT# can be used as the second DTR# to connect to BOOT0.

Note: For other MCUs with opposite BOOT mode levels, you can directly use CH340C/G DTR# to control (default high level), or use DTR# of CH340X with a resistor connected between the 6# pin and the 5# pin to control (push-pull DTR enhanced mode, default high level).

MCU normal working status: The pull-down resistor makes CH340E enter open source DTR enhanced mode. The 6# pin is switched to DTR#, DTR# is not output by default, BOOT0 remains low, RTS# defaults to high, and MCU runs applications normally.

One-click download: The computer download tool program opens the UART, sets DTR# to high level, sets RTS# to low level and then high level, and the MCU enters the BOOT download program. After the download is completed, set DTR# to low level, set RTS# to low level then high level, the MCU runs the application normally, and keep DTR# unchanged before closing the UART. Note that the MODEM data and the pin level are inverted.

Unified power supply mode: CH340X uses the same 5V or 3.3V power supply of MCU. The disadvantage is that CH340X will consume tens of microamps sleep current.

Independent power supply mode: the CH340X uses the USB VBUS power supply, which does not consume the MCU power supply current at all. After the power failure of the CH340X itself, it basically does not affect the IO of the MCU, but it is necessary to avoid the situation that power is poured back to some MCUs because the USB is powered but the MCU is not powered. If it is necessary to completely prevent the CH340 power supply from injecting the current to the power-off MCU, refer to the figure in Section 7.7 and add NMOS and diode.

If NRST pin needs to support additional manual reset, a $1\sim2K\Omega$ resistor or a diode with anode connected to NRST can be connected in series between RTS# and NRST.