1. Demultiplexer and decoder are same. (true/False)
2. Mention the application of Magnitude comparator
3. Draw the Logic diagram of 2:1 MUX
4. Is it possible to implement a combinational logic using MUX?
5. How many select lines are needed to design a 1:8 DEMUX?
6. How priority encoder is different from a normal encoder?
7. Draw the function table for 2:4 Decoder
8. Differentiate combinational and sequential circuit
9. Is it possible to construct a DFF from JKFF. If 'yes' say how. If 'No' say why?
10. Write the characteristic expression of SRFF and D FF
11. The two names of D Flipflop is _____ and _____
12. How JKMS FF overcomes Race around condition
13. A decoder with an Enable input is equal to demultiplexer (True/False)
14. What does a magnitude comparator do?
15. Draw the function table of 8:1MUX
16. Is it possible to implement a combinational logic using an Encoder?
17. How many select lines are needed to design a 16:1 MUX ?
18. Differentiate Priority encoder from a normal encoder
19. Draw the function table for 4:2 Encoder
20. Differentiate Latches and Flipflops
21. Is it possible to construct a TFF from SR FF. If 'yes' say how. If 'No' say why?
22. Write the characteristic expression of JKFF and TFF
23. What is Race around condition
24. Draw an SR Latch using NOR Gates

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25. What is a Multiplexer?
26. what is an Encoder?
27. List two differences between mealy and moore sequential circuit
28. What is a Demultiplexer?
29. What is a decoder?
30. Differentiate Mealy and moore model

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31. Design a multiplier circuit to multiply the following number $A=A_0A_1A_2$ and $B=B_0B_1B_2$ using 4 bit binary adders
32. Implement the following using Multiplexers using 8:1 MUX
    (i) F(A,B,C,D)=A'BD'+ACD+B'CD+A'C'D [4]
    (ii) Full adder [4]
    (iii)F=∑m(0,2,6,10,11,12,13)+d(3,8,14) [4]
    (iv) F=π(0,3,5,8,9,10,12,14) [2]
33. Discuss about (i) Octal to Binary encoder [6]
    (ii) 4 bit Priority encoder [8]
34. Design a multiplier circuit using 4 bit binary adders to multiply two 4 bit binary numbers
35. Design the following using Demultiplexers
    (i) Full subtractor [4]
    (ii) F(A,B,C,D)=A'BD'+ACD+B'CD+A'C'D [4]
    (iii) F1=π(0,2,4,6) F2=∑(0,2,4,6) [4]
    (iv) F1=∑(0,3,5,7) F2=∑(1,4,6) [2]

36. Design the following

(i) Full adder and Full subtractor using a single 3:8 decoder [6]

(ii)Excess 3 to BCD code converter using 4:16 decoder [4]

(iii) Using 4:16 line decoder implement [4]

Y1=A'B'C'D'+A'B'CD+A'B'CD'+A'BCD'+AB'C'D+AB'CD;

Y2=A'B'C'D+A'BC'D'+A'BC'D+ACC'D

Y3=A'BCD+ABCD'+ABCD

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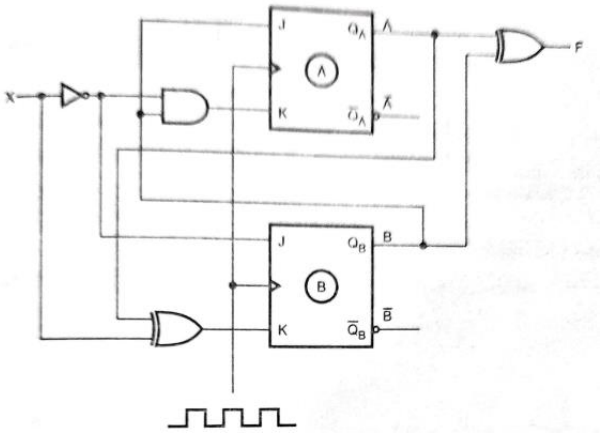
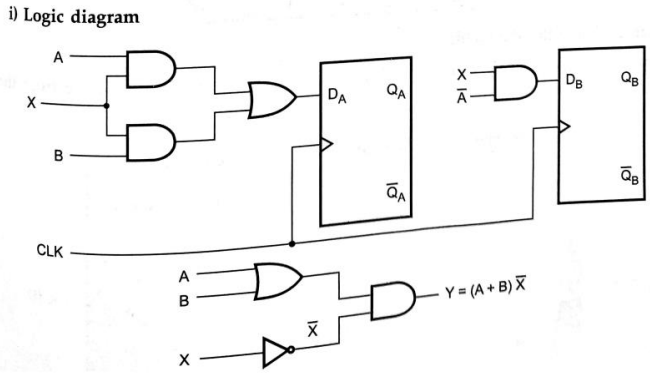
37. Construct Transition table, State table and state **diagram** for the moore sequential circuit



38. A sequential circuit with 2 DFF A and B, input X and output Y, specified by following equation A(t+1) =AX+BX; B(t+1)=A'; Y=(A+B)X. Derive Logic Diagram, State table and State diagram

39. Construct Transition table, State table and state diagram for the following sequential circuit



40. A sequential circuit with 2 JKFF A and B, input X and output Y, specified by following equation JA=B; KA=X'B; JB=X'; KB=X©A; Y=A©B. Derive Logic diagram, transition Table, State Table and state diagram