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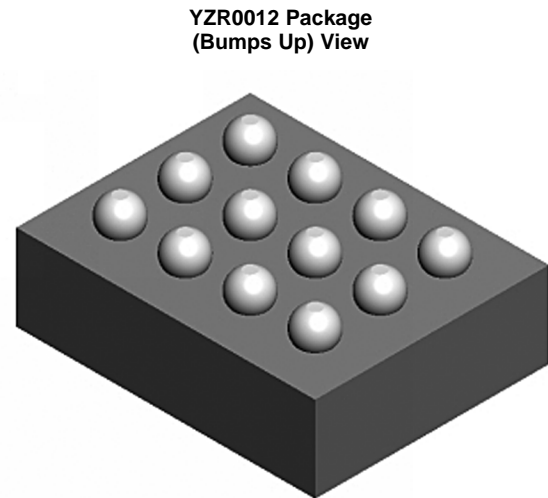
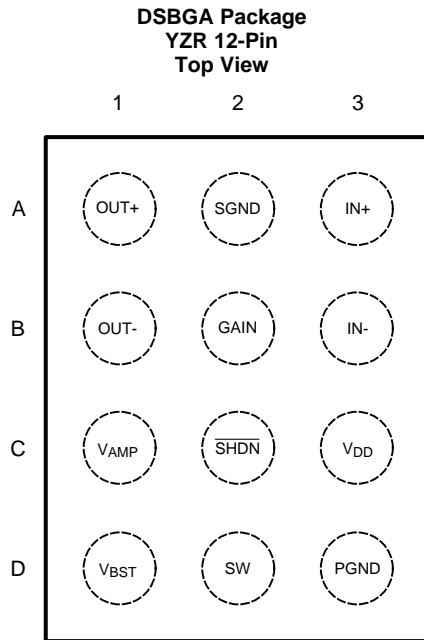
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2013) to Revision B	Page
• Added <i>Device Information</i> table, <i>ESD</i> table, <i>Thermal Information</i> table, <i>Parameter Measurement Information</i> , <i>Feature Description</i> , <i>Device Functional Modes</i> , <i>Power Supply Recommendations</i> , <i>Layout</i> section, <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i>	1
• Deleted the <i>Demoboard Bill of Materials</i> section	12
• Deleted the <i>Demo Board Schematic</i> section.....	12

Changes from Original (February 2010) to Revision A	Page
• Changed layout of National Data Sheet to TI format.	1

5 Pin Configuration and Functions



Pin Functions

Bump	Name	Description
A1	OUT+	Amplifier Non-Inverting Output
A2	SGND	Amplifier Ground
A3	IN+	Amplifier Non-Inverting Input
B1	OUT-	Amplifier Inverting Output
B2	GAIN	Gain Select: GAIN = float: $A_V = 18\text{dB}$ GAIN = GND: $A_V = 24\text{dB}$ GAIN = V_{DD} : $A_V = 30\text{dB}$
B3	IN-	Amplifier Inverting Input
C1	V_{AMP}	Amplifier Supply Voltage. Connect to V_{BST}
C2	$\overline{\text{SHDN}}$	Active Low Shutdown. Drive $\overline{\text{SHDN}}$ low to disable device. Connect $\overline{\text{SHDN}}$ to V_{DD} for normal operation.
C3	V_{DD}	Power Supply
D1	V_{BST}	Boost Converter Output
D2	SW	Boost Converter Switching Node
D3	PGND	Boost Converter Ground

6 Specifications

7 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Supply Voltage		6	V
SW Voltage		25	V
VBST Voltage		21	V
V _{AMP}		17	V
Input Voltage	−0.3	V _{DD} + 0.3	V
Storage temperature, T _{stg}	−65	150	°C
Junction Temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

8 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

9 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature Range	−40	T _A	85	°C
Supply Voltage	2.5	V _{DD}	5.5	V

10 Thermal Information

THERMAL METRIC ⁽¹⁾		LM48580	UNIT
		YZR (DSBGA)	
		12 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	82.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	20.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	20.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

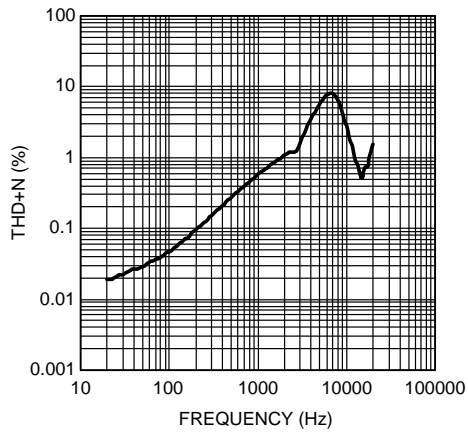
11 Electrical Characteristics: $V_{DD} = 3.6\text{ V}^{(1)}$

The following specifications apply for $R_L = 6\text{ }\mu\text{F} + 10\Omega$, $C_{BST} = 1\text{ }\mu\text{F}$, $C_{IN} = 0.47\text{ }\mu\text{F}$, $A_V = 24\text{ dB}$ unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

PARAMETER	TEST CONDITIONS	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Unit
V_{DD}	Supply Voltage Range	2.5		5.5	V
I_{DD}	Quiescent Power Supply Current, $V_{IN} = 0\text{ V}$, $R_L = \infty$	$V_{DD} = 3.6\text{ V}$	2.7	4	mA
		$V_{DD} = 3\text{ V}$	3		mA
P_D	Power Consumption $V_{OUT} = 25V_{P-P}$, $f = 200\text{ Hz}$	$V_{DD} = 3.6\text{ V}$	800		mW
		$V_{DD} = 3\text{ V}$	830		mW
I_{SD}	Shutdown Current	Shutdown Enabled	0.5	2	μA
T_{WU}	Wake-up Time	From Shutdown	1	1.4	ms
V_{OS}	Differential Output Offset Voltage	$V_{DD} = 3.6\text{ V}$	63	360	mV
A_V	Gain	GAIN = FLOAT	17.5	18	dB
		GAIN = GND	23.5	24	dB
		GAIN = V_{DD}	29.5	30	dB
R_{IN}	Input Resistance		46	52	k Ω
R_{IN}	Gain Input Resistance	to GND		575	k Ω
		to V_{DD}		131	k Ω
V_{IN}	Maximum Input Voltage Range	$A_V = 18\text{ dB}$		3	V_{P-P}
V_{OUT}	Output Voltage $f = 200\text{ Hz}$, THD+N = 1%	$V_{DD} = 3.6\text{ V}$	25	30.5	V_{P-P}
		$V_{DD} = 3\text{ V}$		30.5	V_{P-P}
	Output Voltage $f = 2\text{ kHz}$, THD+N = 5%	$V_{DD} = 3.6\text{ V}$		11	V_{P-P}
		$V_{DD} = 3\text{ V}$		8.5	V_{P-P}
THD+N	Total Harmonic Distortion + Noise	$V_{OUT} = 25V_{P-P}$, $f = 200\text{ Hz}$		0.16%	
PSRR	Power Supply Rejection Ratio $V_{DD} = 3.6\text{ V} + 200\text{ mV}_{P-P}$ sine, Inputs AC GND	$f_{RIPPLE} = 217\text{ Hz}$,		75	dB
		$f_{RIPPLE} = 1\text{ kHz}$		71	dB
CMRR	Common Mode Rejection Ratio $V_{CM} = 200\text{ mV}_{P-P}$ sine	$f_{RIPPLE} = 217\text{ Hz}$		56	dB
		$f_{RIPPLE} = 1\text{ kHz}$		55	dB
f_{SW}	Boost Converter Switching Frequency		2.1		MHz
I_{LIMIT}	Boost Converter Current Limit			1100	mA
V_{IH}	Logic High Input Threshold	$\overline{\text{SHDN}}$	1.2		V
V_{IL}	Logic Low Input Threshold	$\overline{\text{SHDN}}$		0.45	V
I_{IN}	Input Leakage Current	$\overline{\text{SHDN}}$	0.1	1	μA

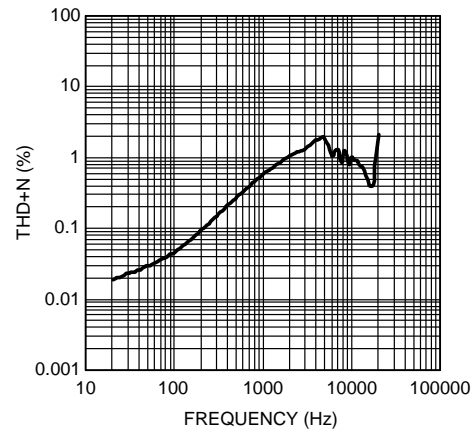
- (1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
- (3) Typical values represent most likely parametric norms at $T_A = +25^\circ\text{C}$, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.

11.1 Typical Performance Characteristics



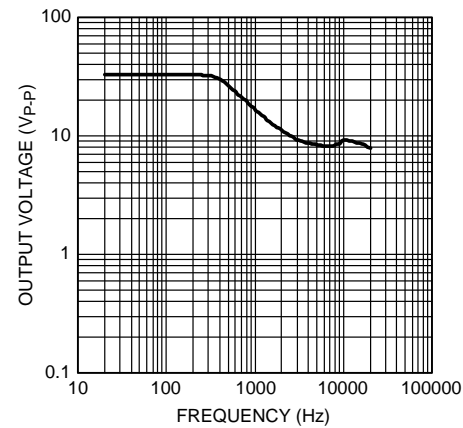
$V_{DD} = 3.6\text{ V}$ $V_{OUT} = 9\text{ V}_{P-P}$ $R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

Figure 1. THD+N vs Frequency



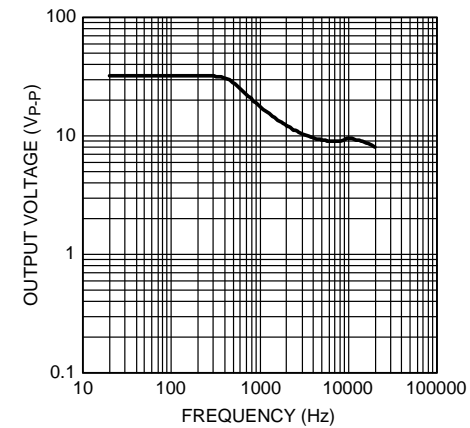
$V_{DD} = 4.2\text{ V}$ $V_{OUT} = 10\text{ V}_{P-P}$ $R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

Figure 2. THD+N vs Frequency



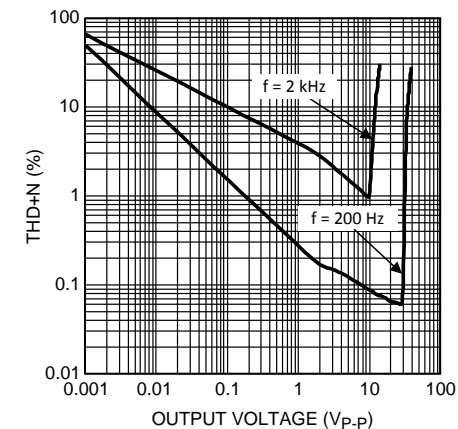
$V_{DD} = 3.6\text{ V}$ $\text{THD+N} = 5\%$ $R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

Figure 3. Output Voltage vs Frequency



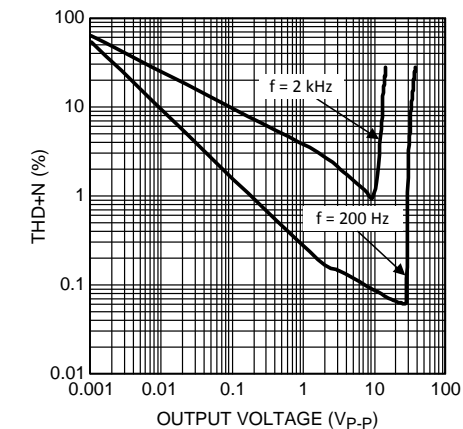
$V_{DD} = 4.2\text{ V}$ $\text{THD+N} = 5\%$ $R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

Figure 4. Output Voltage vs Frequency



$V_{DD} = 3.6\text{ V}$ $R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

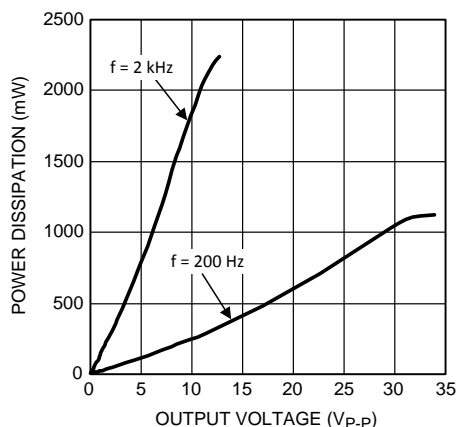
Figure 5. THD+N vs Output Voltage



$V_{DD} = 4.2\text{ V}$ $R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

Figure 6. THD+N vs Output Voltage

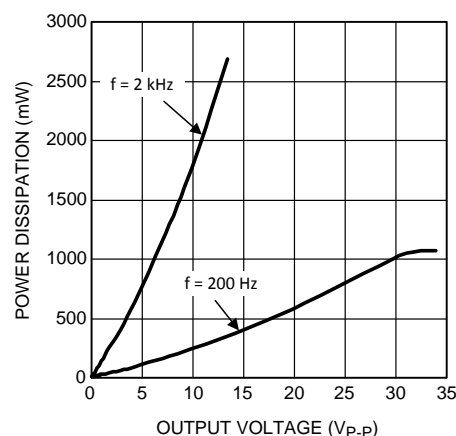
Typical Performance Characteristics (continued)



$V_{DD} = 3.6\text{ V}$

$R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

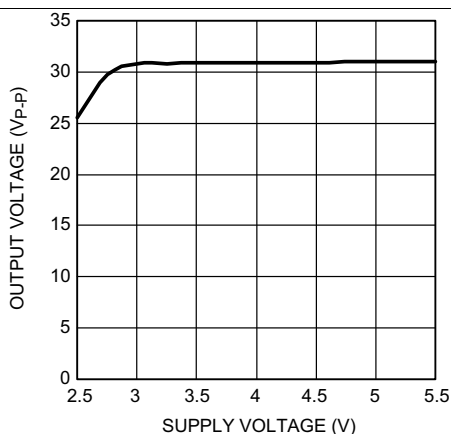
Figure 7. Power Consumption vs Output Voltage



$V_{DD} = 4.2\text{ V}$

$R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

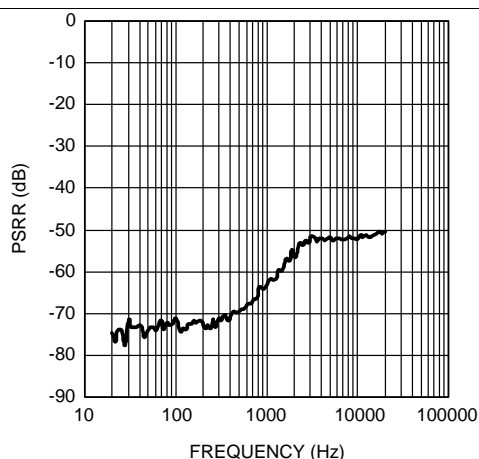
Figure 8. Power Consumption vs Output Voltage



$R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$,

$f = 200\text{ Hz}$

Figure 9. Output Voltage vs Supply Voltage



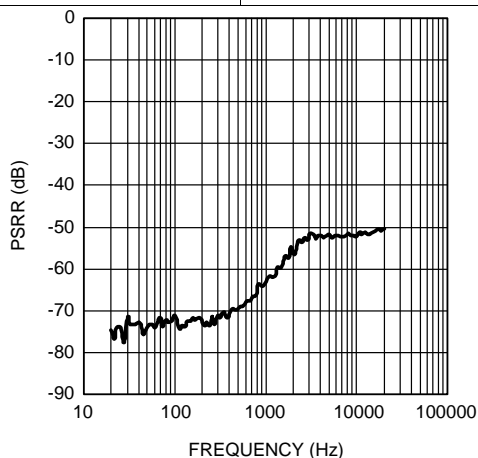
$V_{DD} = 3.6\text{ V}$

$f = 200\text{ Hz}$

$R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$,

$V_{RIPPLE} = 200\text{ mV}_{P-P}$

Figure 10. PSRR vs Frequency



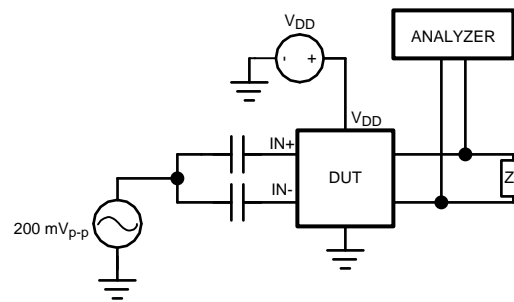
$V_{DD} = 3.6\text{ V}$

$V_{CM} = 1\text{ V}_{P-P}$

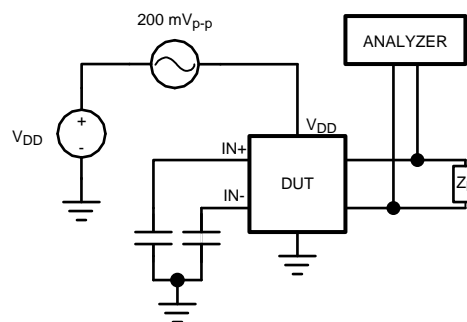
$R_L = 6\text{ }\mu\text{F} + 10\text{ }\Omega$

Figure 11. CMRR vs Frequency

12 Parameter Measurement Information



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Figure 12. PSRR Test Circuit


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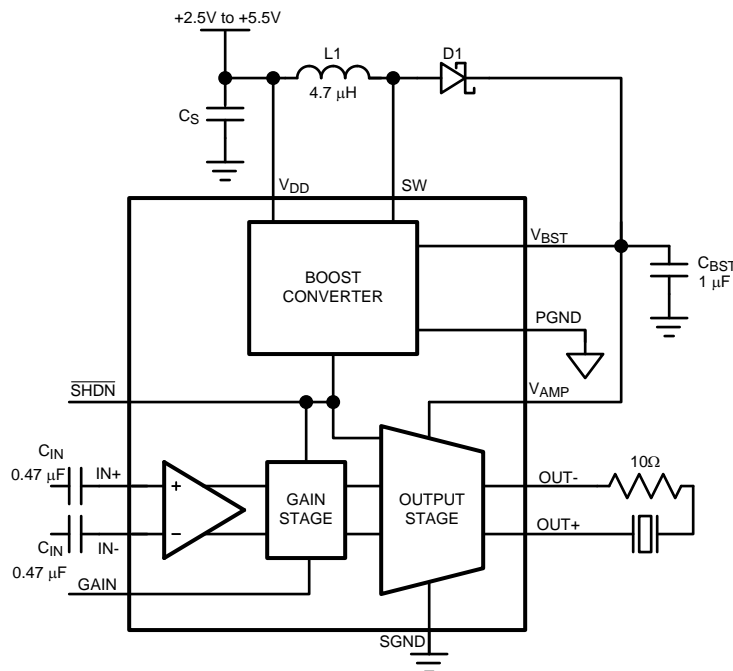
Figure 13. CMRR Test Circuit

13 Detailed Description

13.1 Overview

The LM48580 is a fully differential, Class H ceramic element driver for ceramic speakers and haptic actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier's supply voltage based on the output signal, increasing headroom and improving efficiency compared to a conventional Class AB driver. The fully differential amplifier takes advantage of the increased headroom and bridge-tied load (BTL) architecture, delivering significantly more voltage than a single-ended amplifier.

13.2 Functional Block Diagram



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13.3 Feature Description

13.3.1 Class H Operation

Class H is a modification of another amplifier class (typically Class B or Class AB) to increase efficiency and reduce power dissipation. To decrease power dissipation, Class H uses a tracking power supply that monitors the output signal and adjusts the supply accordingly. When the amplifier output is below $3 V_{P-P}$, the nominal boost voltage is 6 V. As the amplifier output increases above $3 V_{P-P}$, the boost voltage tracks the amplifier output as shown in Figure 14. When the amplifier output falls below $3 V_{P-P}$, the boost converter returns to its nominal output voltage. Power dissipation is greatly reduced compared to conventional Class AB drivers.

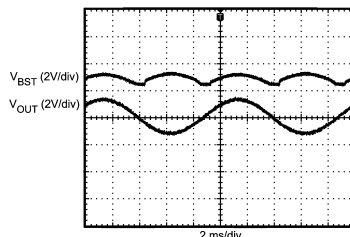


Figure 14. Class H Operation

Feature Description (continued)

13.3.2 Properties of Piezoelectric Elements

Piezoelectric elements such as ceramic speakers or piezoelectric haptic actuators are capacitive in nature. Due to their capacitive nature, piezoelectric elements appear as low impedance loads at high frequencies (typically above 5 kHz). A resistor in series with the piezoelectric element is required to ensure the amplifier does not see a short at high frequencies.

The value of the series resistor depends on the capacitance of the element, the frequency content of the output signal, and the desired frequency response. Higher valued resistors minimize power dissipation at high frequencies, but also impacts the frequency response. This configuration is suited for use with haptic actuators, where the majority of the signal content is typically below 2 kHz. Conversely, lower valued resistors maximize frequency response, while increasing power dissipation at high frequency. This configuration is ideal for ceramic speaker applications, where high frequency audio content needs to be reproduced. Resistor values are typically between 10 Ω and 20 Ω .

13.3.3 Differential Amplifier Explanation

The LM48580 features a fully differential amplifier. A differential amplifier amplifies the difference between the two input signals. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

13.3.4 Thermal Shutdown

The LM48580 features thermal shutdown that protects the device during thermal overload conditions. When the junction temperature exceeds +160°C, the device is disabled. The LM48580 remains disabled until the die temperature falls below the +160°C and SHDN is toggled.

13.3.5 Gain Setting

The LM48580 features three internally configured gain settings 18, 24, and 30 dB. The device gain is selected through a single pin (GAIN). The gain settings are shown in [Table 1](#).

Table 1. Gain Setting

Gain	Gain Setting
FLOAT	18 dB
GND	24 dB
VDD	30 dB

13.4 Device Functional Modes

13.4.1 Shutdown Function

The LM48580 features a low current shutdown mode. Set $\overline{\text{SD}}$ = GND to disable the amplifier and boost converter and reduce supply current to 0.01 μ A.

14 Application and Implementation

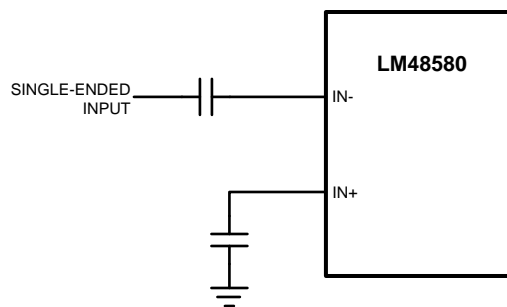
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

14.1 Application Information

14.2 Typical Application

The LM48580 is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. Figure 15 shows the typical single-ended applications circuit.



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Figure 15. Single-Ended Configuration

14.2.1 Design Requirements

14.2.1.1 Proper Selection of External Components

14.2.1.1.1 Boost Converter Capacitor Selection

The LM48580 boost converter requires three external capacitors for proper operation: a 1 μ F supply bypass capacitor, and 1 μ F + 100 pF output reservoir capacitors. Place the supply bypass capacitor as close to V_{DD} as possible. Place the reservoir capacitors as close to VBST and VAMP as possible. Low ESR surface-mount multi-layer ceramic capacitors with X7R or X5R temperature characteristics are recommended. Select output capacitors with voltage rating of 25 V or higher. Tantalum, OS-CON and aluminum electrolytic capacitors are not recommended. See Table 2 for suggested capacitor manufacturers.

Typical Application (continued)

14.2.2 Detailed Design Procedure

14.2.2.1 Boost Converter Output Capacitor Selection

14.2.2.1.1 Inductor Selection

The LM48580 boost converter is designed for use with a 4.7 μH inductor. Table 2 lists various inductors and their manufacturers. Choose an inductor with a saturation current rating greater than the maximum operating peak current of the LM48580 ($> 1\text{ A}$). This ensures that the inductor does not saturate, preventing excess efficiency loss, over heating and possible damage to the inductor. Additionally, choose an inductor with the lowest possible DCR (series resistance) to further minimize efficiency losses.

Table 2. Recommended Inductors⁽¹⁾

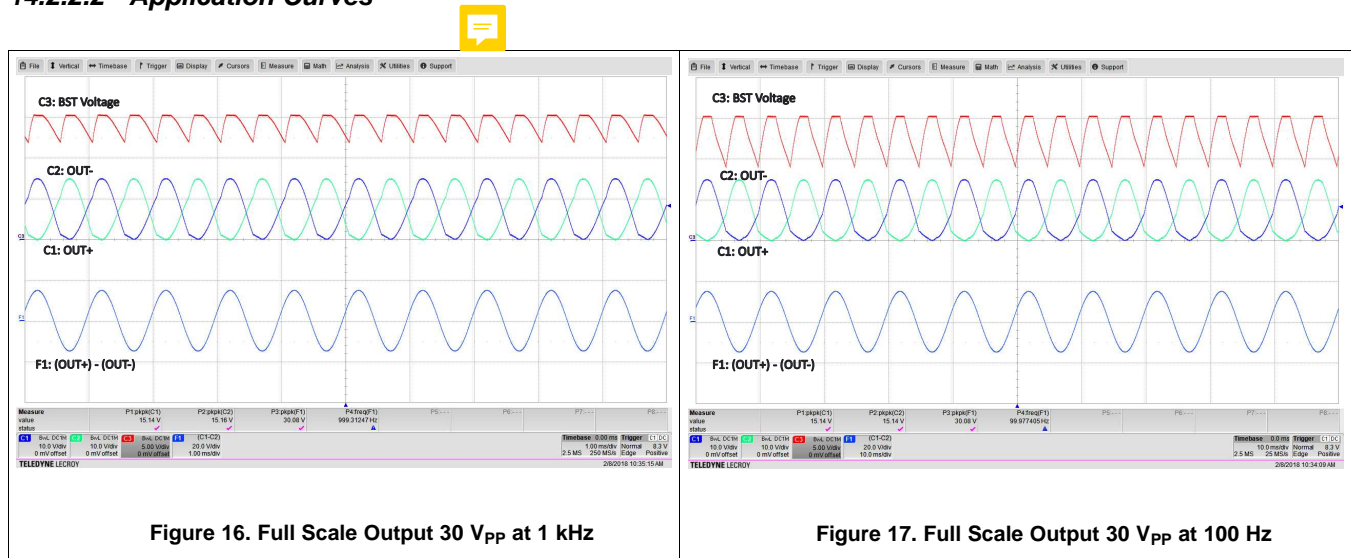
MANUFACTURER	PART#	INDUCTANCE/ISAT
Taiyo Yuden	BRL3225T4R7M	4.7 μH /1.1 A
Coilcraft	LP3015	4.7 μH /1.1 A

(1) See [Development Support](#)

14.2.2.1.2 Diode Selection

Use a Schottkey diode as shown in the *Functional Block Diagram*. A 20 V diode such as the NSR0520V2T1G from On Semiconductor is recommended. The NSR0520V2T1G is designed to handle a maximum average current of 500 mA.

14.2.2.2 Application Curves



15 Power Supply Recommendations

The LM48580 device is designed to operate with a power supply between 2.5 V and 5.5 V. Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1- μF ceramic capacitor from VDD to GND. Additional bulk capacitance may be added as required.

16 Layout

16.1 Layout Guidelines

- Minimize trace impedance of the power, ground and all output traces for optimum performance.
- Voltage loss due to trace resistance between the LM48580 and the load results in decreased output power and efficiency.
- Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power.
- Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device.
- Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal.
- Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

16.2 Layout Example

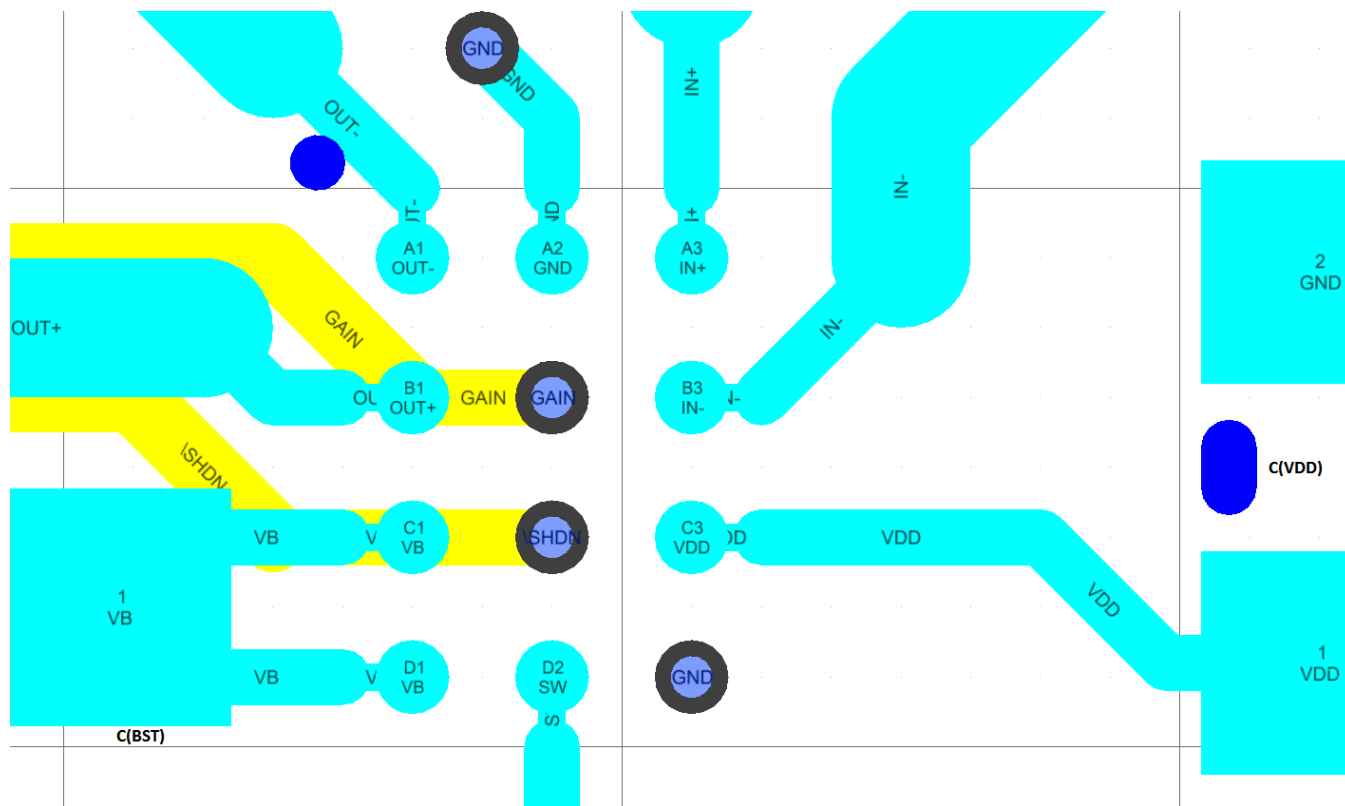


Figure 18. Example Layout

17 Device and Documentation Support

17.1 Device Support

17.1.1 Development Support

17.1.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

17.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

17.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

17.4 Trademarks

Boomer, Powerwise, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

17.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

17.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

18 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM48580TL/NOPB	ACTIVE	DSBGA	YZR	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GM3	Samples
LM48580TLX/NOPB	ACTIVE	DSBGA	YZR	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GM3	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

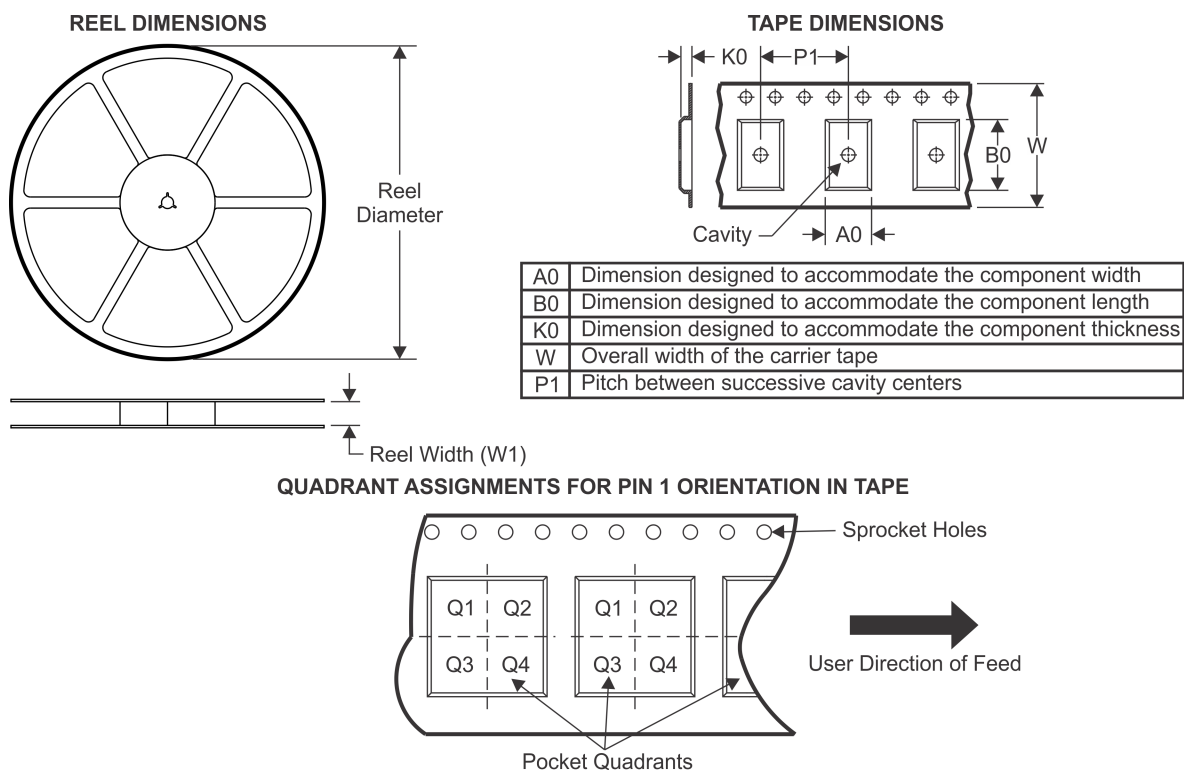
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48580TL/NOPB	DSBGA	YZR	12	250	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
LM48580TLX/NOPB	DSBGA	YZR	12	3000	178.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

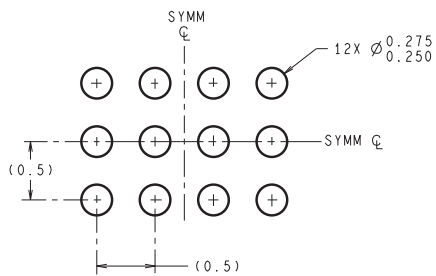
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

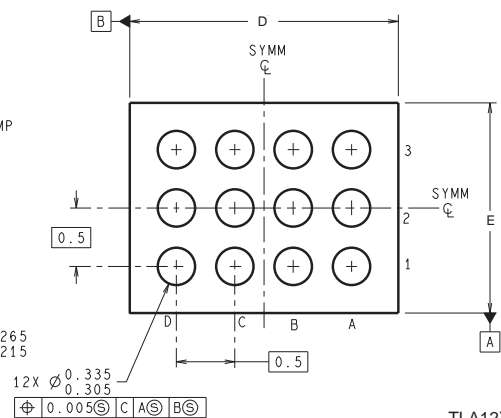
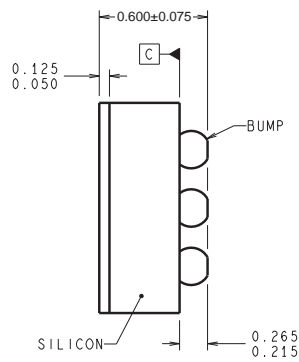
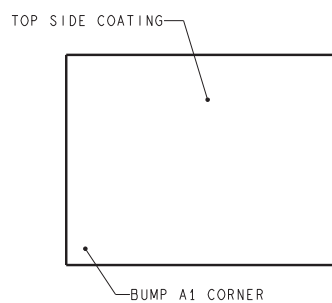
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48580TL/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LM48580TLX/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0

YZR0012



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TLA12XXX (Rev C)

D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.49 mm, Min = 1.43 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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