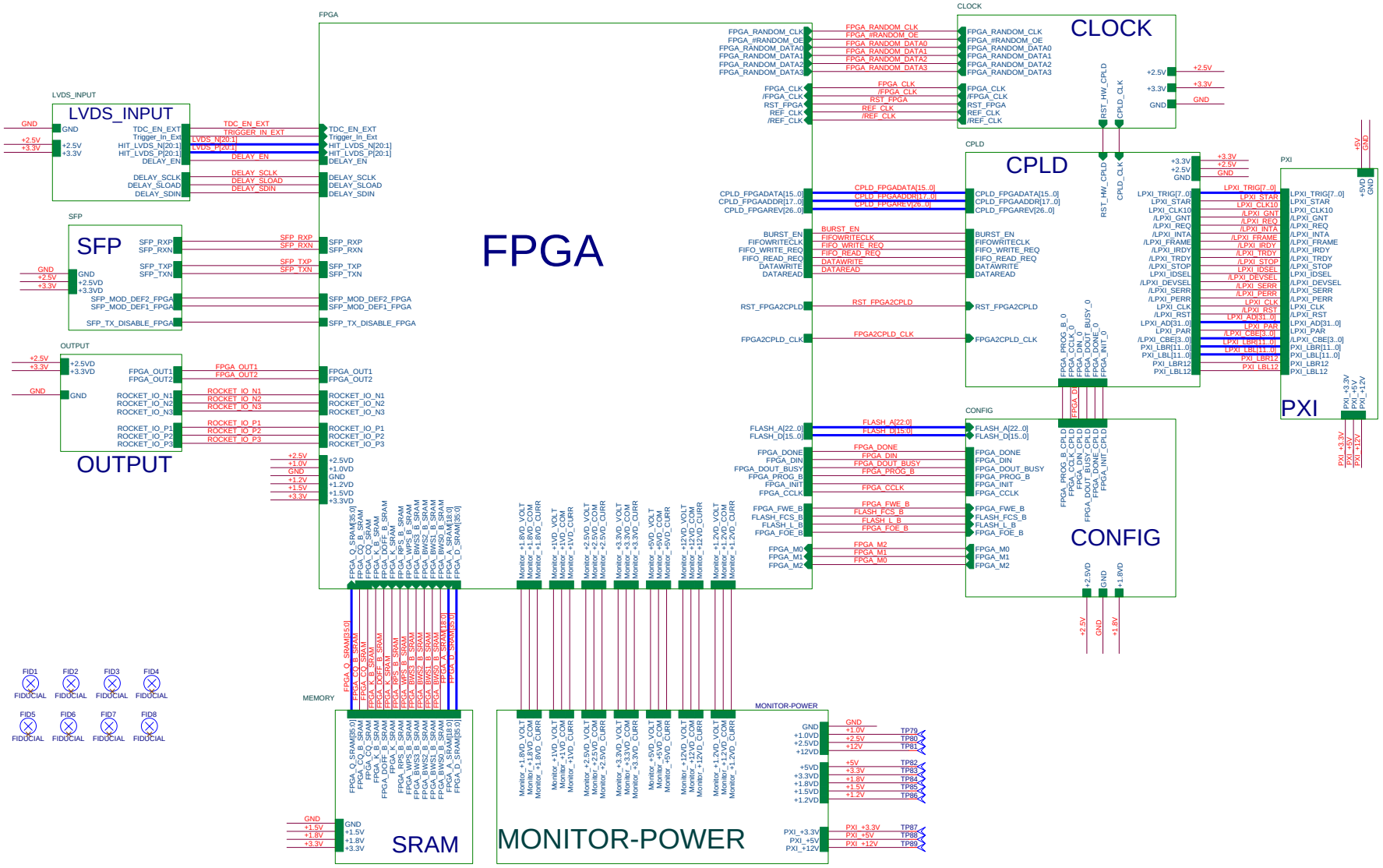

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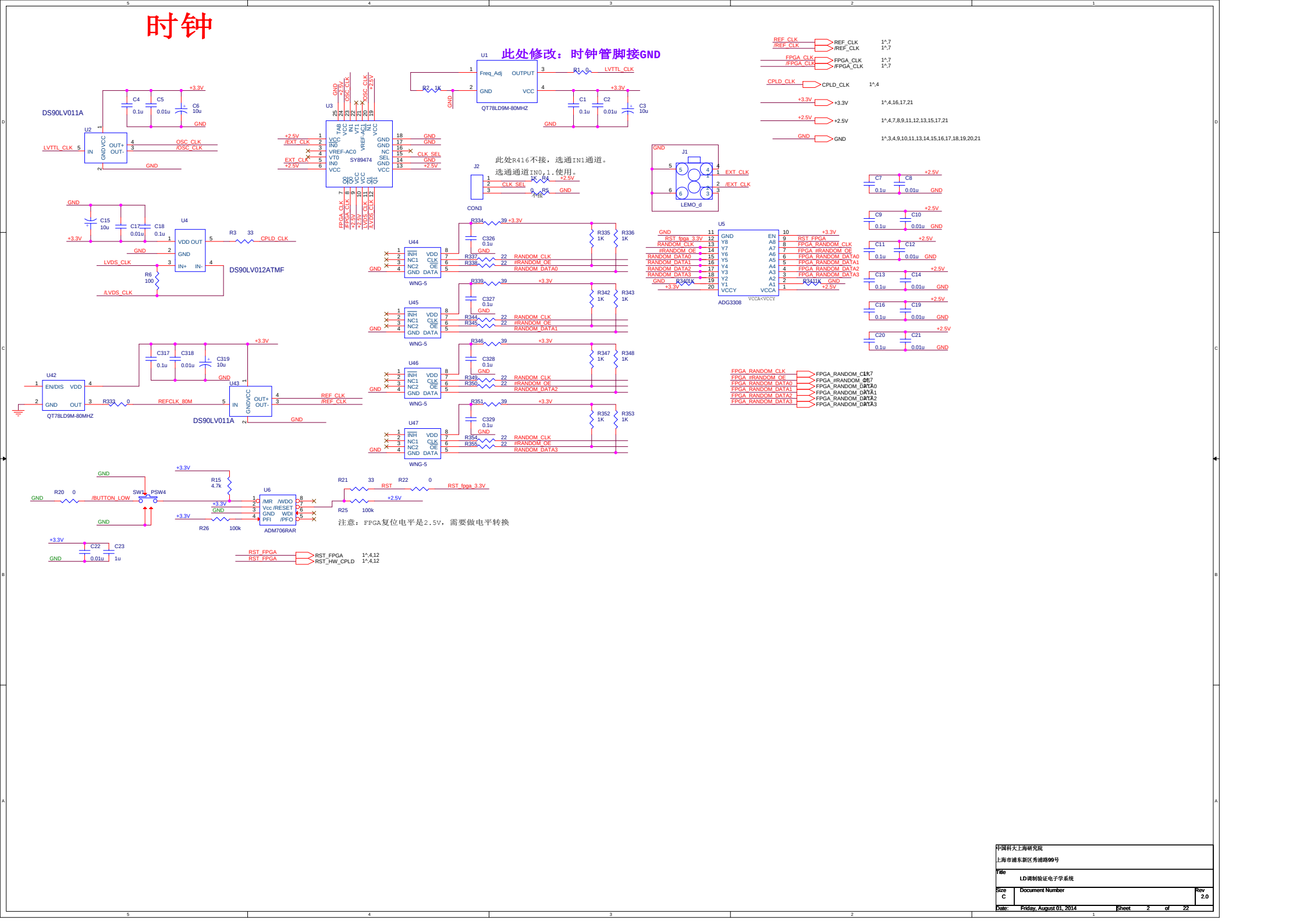
时钟


此处修改：时钟管脚接GND
DS90LV011A
U1
Freq_Adj
OUTPUT
GND
VCC
QT78LD9M-80MHZ
U2
U3
SY89474
U4
DS90LV012ATMF
U42
U43
DS90LV011A
U44
U45
U46
U47
WNG-5
U5
ADG3308
J1
LEMO_d
J2
CON3
此处R416不接，选通IN1通道。
选通通道IN0,1.使用。
U6
ADM706RAR
注意：FPGA复位电平是2.5V，需要做电平转换
REF_CLK
/REF_CLK
FPGA_CLK
/FPGA_CLK
CPLD_CLK
+3.3V
+2.5V
GND
RST_FPGA
RST_HW_CPLD
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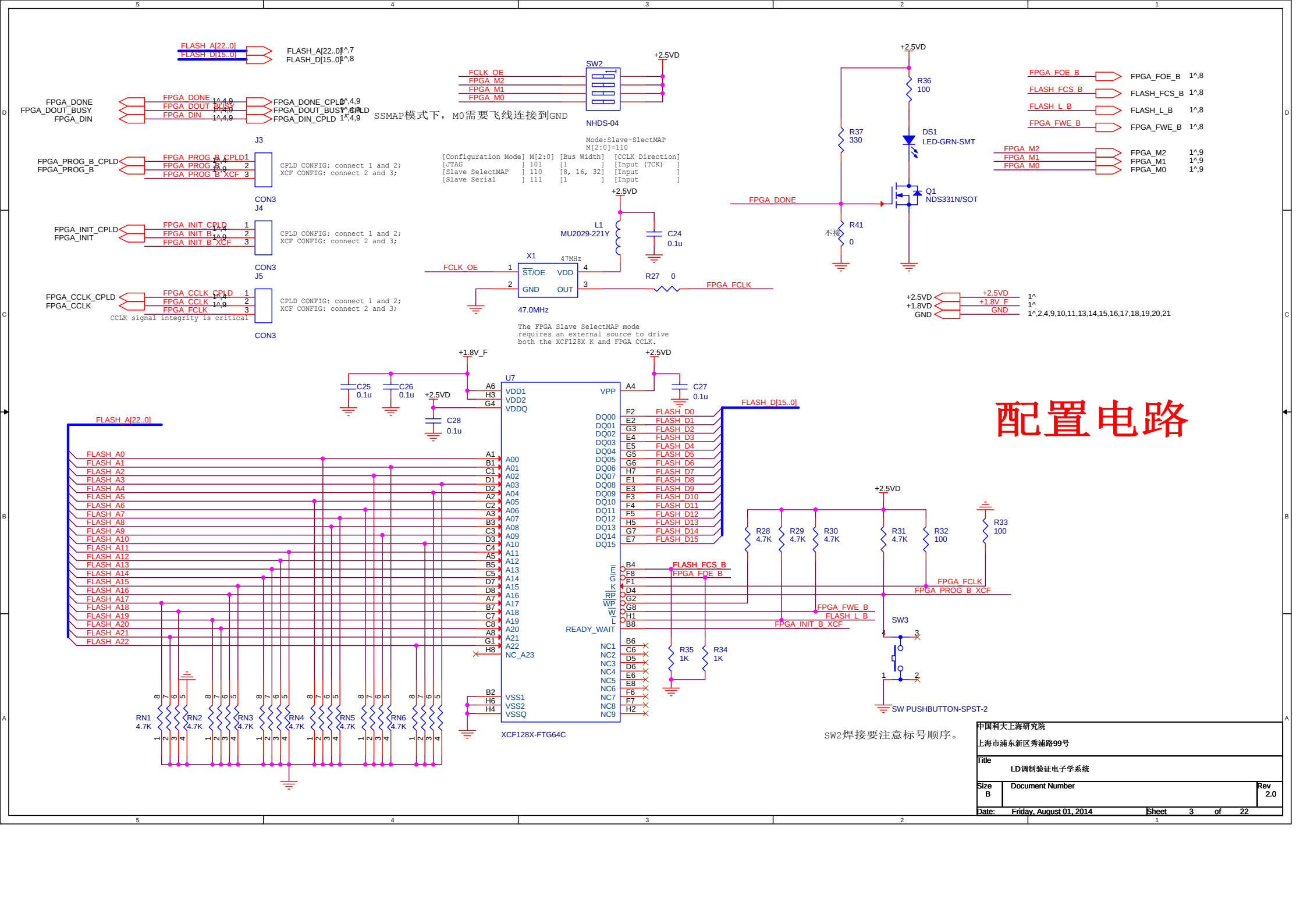
FLASH_A[22..0]
FLASH_D[15..0]
FLASH_A[22..0] 1^,7
FLASH_D[15..0] 1^,8
FPGA_DONE
FPGA_DOUT_BUSY
FPGA_DIN
FPGA_DONE_CPLD
FPGA_DOUT_BUSY_CPLD
FPGA_DIN_CPLD
SSMAP模式下，M0需要飞线连接到GND
SW2
NHDS-04
FCLK_OE
FPGA_M2
FPGA_M1
FPGA_M0
+2.5VD
Mode:Slave-SlectMAP
M[2:0]=110
[Configuration Mode] M[2:0] [Bus Width] [CCLK Direction]
[JTAG] 101 [1] [Input (TCK)]
[Slave SelectMAP] 110 [8, 16, 32] [Input]
[Slave Serial] 111 [1] [Input]
J3
FPGA_PROG_B_CPLD
FPGA_PROG_B
CPLD CONFIG: connect 1 and 2;
XCF CONFIG: connect 2 and 3;
CON3
J4
FPGA_INIT_CPLD
FPGA_INIT
CON3
J5
FPGA_CCLK_CPLD
FPGA_CCLK
CCLK signal integrity is critical
L1
MU2029-221Y
C24
0.1u
X1
47MHz
ST/OE
VDD
GND
OUT
47.0MHz
R27 0
FPGA_FCLK
The FPGA Slave SelectMAP mode
requires an external source to drive
both the XCF128X K and FPGA CCLK.
R36
100
R37
330
DS1
LED-GRN-SMT
Q1
NDS331N/SOT
FPGA_DONE
R41
不接
0
FPGA_FOE_B
FLASH_FCS_B
FLASH_L_B
FPGA_FWE_B
+2.5VD
+1.8V_F
GND
U7
VDD1
VDD2
VDDQ
VPP
C25
0.1u
C26
0.1u
C27
0.1u
C28
0.1u
FLASH_A0
FLASH_A1
FLASH_A2
FLASH_A3
FLASH_A4
FLASH_A5
FLASH_A6
FLASH_A7
FLASH_A8
FLASH_A9
FLASH_A10
FLASH_A11
FLASH_A12
FLASH_A13
FLASH_A14
FLASH_A15
FLASH_A16
FLASH_A17
FLASH_A18
FLASH_A19
FLASH_A20
FLASH_A21
FLASH_A22
NC_A23
FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4
FLASH_D5
FLASH_D6
FLASH_D7
FLASH_D8
FLASH_D9
FLASH_D10
FLASH_D11
FLASH_D12
FLASH_D13
FLASH_D14
FLASH_D15
READY_WAIT
VSS1
VSS2
VSSQ
XCF128X-FTG64C
RN1 4.7K
RN2 4.7K
RN3 4.7K
RN4 4.7K
RN5 4.7K
RN6 4.7K
R28 4.7K
R29 4.7K
R30 4.7K
R31 4.7K
R32 100
R33 100
R34 1K
R35 1K
FPGA_FCLK
FPGA_PROG_B_XCF
FPGA_INIT_B_XCF
SW3
SW PUSHBUTTON-SPST-2
SW2焊接要注意标号顺序。
配置电路
中国科大上海研究院
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CPLD

CPLD-FPGA CONFIG

FPGA2CPLD_CLK
CPLD_CLK
FPGA2CPLD_CLK 1^,7
CPLD_CLK 1^,2
FROM OSILATTOR
RST_FPGA2CPLD
RST_FPGA2CPLD 1^,7
RESET:FPGA TO CPLD
RST_HW_CPLD
RST_HW_CPLD 1^,2,12

FPGA_INIT_0 — FPGA_INIT_0 1^,3
FPGA_DONE_0 — FPGA_DONE_0 1^,3,9
FPGA_DOUT_BUSY_0 — FPGA_DOUT_BUSY_0 1^,9
FPGA_DIN_0 — FPGA_DIN_0 1^,9
FPGA_CCLK_0 — FPGA_CCLK_0 1^,3
FPGA_PROG_B_0 — FPGA_PROG_B_0 1^,3

FPGA SLAVE SERIAL Mode

CPLD-FPGA

CPLD_FPGADATA[15..0] — CPLD_FPGADATA[15..0]
CPLD_FPGAADDR[17..0] — CPLD_FPGAADDR[17..0]
CPLD_FPGAREV[26..0] — CPLD_FPGAREV[26..0]

BURST_EN — BURST_EN 1^,7
FIFOWRITECLK — FIFOWRITECLK 1^,7
FIFO_WRITE_REQ — FIFO_WRITE_REQ 1^,7
FIFO_READ_REQ — FIFO_READ_REQ 1^,7
DATAWRITE — DATAWRITE 1^,7
DATAREAD — DATAREAD 1^,7

PXI

address and data pins

LPXI_AD[31..0] — LPXI_AD[31..0] 1^,20
LPXI_PAR — LPXI_PAR 1^,20
/LPXI_CBE[3..0] — /LPXI_CBE[3..0] 1^,20

system pins

LPXI_CLK — LPXI_CLK 1^,20
/LPXI_RST — /LPXI_RST 1^,20

Error Reporting pins

/LPXI_SERR — /LPXI_SERR 1^,20
/LPXI_PERR — /LPXI_PERR 1^,20

Interface Control Pins

/LPXI_FRAME — /LPXI_FRAME 1^,20
/LPXI_IRDY — /LPXI_IRDY 1^,20
/LPXI_TRDY — /LPXI_TRDY 1^,20
/LPXI_STOP — /LPXI_STOP 1^,20
LPXI_IDSEL — LPXI_IDSEL 1^,20
/LPXI_DEVSEL — /LPXI_DEVSEL 1^,20

Arbitration Pins (Bus Masters Only)

/LPXI_GNT — /LPXI_GNT 1^,20
/LPXI_REQ — /LPXI_REQ 1^,20

Interrupt Pins

/LPXI_INTA — /LPXI_INTA 1^,20

Trigger Bus and Star Trigger

LPXI_TRIG[7..0] — LPXI_TRIG[7..0] 1^,20
LPXI_STAR — LPXI_STAR 1^,20

system reference clock

LPXI_CLK10 — LPXI_CLK10 1^,20

PXI Local Bus

PXI_LBR[11..0] — PXI_LBR[11..0] 1^,18
PXI_LBL[11..0] — PXI_LBL[11..0] 1^,18
PXI_LBR12 — PXI_LBR12 1^,18
PXI_LBL12 — PXI_LBL12 1^,18

U9-1 — EPM2210

IO1-1	C2	CPLD_FPGAREV19	
IO1-2	C3		
IO1-3	D1	CPLD_FPGAADDR9	
IO1-4	D2	CPLD_FPGAREV20	
IO1-5	D3	CPLD_FPGAADDR7	
IO1-6	D4	CPLD_FPGAADDR5	
IO1-7	E1	CPLD_FPGAADDR11	
IO1-8	E2	CPLD_FPGAADDR10	
IO1-9	E3	CPLD_FPGAREV22	
IO1-10	E4		
IO1-11	E5	BURST_EN	
IO1-12	F1	CPLD_FPGAREV21	
IO1-13	F2	CPLD_FPGAADDR13	
IO1-14	F3	CPLD_FPGAADDR12	
IO1-15	F4		
IO1-16	F5		
IO1-17	F6		
IO1-18	G1	CPLD_FPGAREV24	
IO1-19	G2	CPLD_FPGAREV23	
IO1-20	G3	CPLD_FPGAADDR15	
IO1-21	G4		
IO1-22	G5		
IO1-23	G6		
IO1-24	G7		
IO1-25	H1	CPLD_FPGAADDR14	
IO1-26	H2	CPLD_FPGAREV26	
IO1-27	H3	CPLD_FPGAREV25	
IO1-28	H4		
IO1-29	H5		
IO1-30	H6		
IO1-31	J1	CPLD_FPGAADDR17	
IO1-32	J2	CPLD_FPGAADDR16	
IO1-33	J3		
IO1-34	J4		
IO1-68	J5		
IO1-35	J6		
IO1-36	K1	FPGA_PROG_B_0	
IO1-37	K2	FPGA_INIT_0	
IO1-38	K4		
IO1-39	K5		
IO1-40	K6		
IO1-41	L1	CPLD_CLK	
IO1-42	L2	FPGA_CCLK_0	
IO1-43	L3		
IO1-44	L4		
IO1-45	L5		
IO1-46	L6		
IO1-47	M1	FPGA_DONE_0	
IO1-48	M2	FPGA_DOUT_BUSY_0	
IO1-49	M3	FPGA_DIN_0	
IO1-50	M4		
IO1-51	M5		
IO1-52	M6		
IO1-53	M7	TDI	
TDI	N1	LED_P1	
IO1-54	N2	RST_HW_CPLD	
IO1-55	N3		
IO1-56	N4		
IO1-57	N5		
IO1-58	N6	TDO	
TDO	P1	LED_P2	
IO1-59	P2		
IO1-60	P3		
IO1-61	P4		
IO1-62	P5	TMS	
TMS	R1	LED_P4	
IO1-63	R2	LED_P5	
IO1-64	R3		
IO1-65	R4	TCK	
TCK	T2		
IO1-66	T3		
IO1-67			

U9-2 — EPM2210

IO2-1	A10	CPLD_FPGADATA9	
IO2-2	A11	CPLD_FPGADATA7	
IO2-3	A12	CPLD_FPGADATA5	
IO2-4	A13	CPLD_FPGADATA3	
IO2-5	A14	CPLD_FPGADATA1	
IO2-6	A15	CPLD_FPGAREV9	
IO2-7	A17		
IO2-8	A2		
IO2-9	A4		
IO2-10	A5	CPLD_FPGAREV12	
IO2-11	A6	FIFOWRITECLK	
IO2-12	A7	CPLD_FPGADATA14	
IO2-13	A8	CPLD_FPGADATA12	
IO2-14	A9	CPLD_FPGADATA10	
IO2-15	B1	CPLD_FPGAREV18	
IO2-16	B10	CPLD_FPGADATA8	
IO2-17	B11	CPLD_FPGADATA6	
IO2-18	B12	CPLD_FPGADATA4	
IO2-19	B13	CPLD_FPGADATA2	
IO2-20	B14	CPLD_FPGADATA0	
IO2-21	B15	CPLD_FPGAREV10	
IO2-22	B16		
IO2-23	B18	RST_FPGA2CPLD	
IO2-24	B3	CPLD_FPGAREV16	
IO2-25	B4	CPLD_FPGAREV15	
IO2-26	B5	CPLD_FPGAREV13	
IO2-27	B6	CPLD_FPGAREV11	
IO2-28	B7	CPLD_FPGADATA15	
IO2-29	B8	CPLD_FPGADATA13	
IO2-30	B9	CPLD_FPGADATA11	
IO2-31	C10	CPLD_FPGAREV0	
IO2-32	C11	CPLD_FPGAREV2	
IO2-33	C12	CPLD_FPGAREV4	
IO2-66	C13	CPLD_FPGAREV6	
IO2-34	C14	CPLD_FPGAREV8	
IO2-35	C15		
IO2-36	C4	CPLD_FPGAADDR8	
IO2-37	C5	CPLD_FPGAADDR6	
IO2-38	C6	CPLD_FPGAADDR4	
IO2-39	C7	CPLD_FPGAADDR2	
IO2-40	C8	CPLD_FPGAADDR0	
IO2-41	C9	DATAREAD	
IO2-42	D10	FIFO_READ_REQ	
IO2-43	D11	FPGA2CPLD_CLK	
IO2-44	D12	CPLD_FPGAREV5	
IO2-45	D13	CPLD_FPGAREV7	
IO2-46	D14		
IO2-47	D5	CPLD_FPGAADDR3	
IO2-48	D6		
IO2-49	D7	CPLD_FPGAADDR1	
IO2-50	D8	DATAWRITE	
IO2-51	D9	CPLD_FPGAREV3	
IO2-52	E10	CPLD_FPGAREV17	
IO2-53	E11		
IO2-54	E12		
IO2-55	E13		
IO2-56	E6	FIFO_WRITE_REQ	
IO2-57	E7	CPLD_FPGAREV1	
IO2-58	E8		
IO2-59	E9	CPLD_FPGAREV14	
IO2-60	F10		
IO2-61	F11		
IO2-62	F12		
IO2-63	F7		
IO2-64	F8		
IO2-65	F9		

U9-3 — EPM2210

IO3-1	C16	LPXI_TRIG1	
IO3-2	C17	LPXI_AD2	
IO3-3	D15	LPXI_TRIG5	
IO3-4	D16	LPXI_TRIG2	
IO3-5	D17	LPXI_AD7	
IO3-6	D18	LPXI_AD8	
IO3-7	E14	LPXI_AD6	
IO3-8	E15	LPXI_TRIG6	
IO3-9	E16	LPXI_TRIG0	
IO3-10	E17	/LPXI_CBE0	
IO3-11	E18	LPXI_AD9	
IO3-12	F13	LPXI_AD10	
IO3-13	F14	/LPXI_INTA	
IO3-14	F15	LPXI_TRIG4	
IO3-15	F16	LPXI_TRIG7	
IO3-16	F17	LPXI_AD15	
IO3-17	F18	LPXI_AD14	
IO3-18	G12	LPXI_AD12	
IO3-19	G13	/LPXI_RST	
IO3-20	G14	LPXI_CLK	
IO3-21	G15	LPXI_TRIG3	
IO3-22	G16	LPXI_STAR	
IO3-23	G17	LPXI_PAR	
IO3-24	G18	/LPXI_CBE1	
IO3-25	H13		
IO3-26	H14		
IO3-27	H15	LPXI_AD11	
IO3-28	H16	LPXI_CLK10	
IO3-29	H17	/LPXI_SERR	
IO3-30	H18	/LPXI_PERR	
IO3-31	J13		
IO3-32	J14		
IO3-33	J15	LPXI_AD13	
IO3-72	J16		
IO3-34	J17	/LPXI_DEVSEL	
IO3-35	J18	/LPXI_STOP	
IO3-36	K13	LPXI_AD1	
IO3-37	K14	LPXI_AD31	
IO3-38	K15	LPXI_AD27	
IO3-39	K16	LPXI_AD29	
IO3-40	K17	/LPXI_IRDY	
IO3-41	K18	/LPXI_TRDY	
IO3-42	L13	LPXI_AD3	
IO3-43	L14	LPXI_AD30	
IO3-44	L15	LPXI_AD20	
IO3-45	L16	LPXI_AD25	
IO3-46	L17	LPXI_AD17	
IO3-47	L18	/LPXI_FRAME	
IO3-48	M12	LPXI_AD0	
IO3-49	M13	LPXI_AD4	
IO3-50	M14		
IO3-51	M15		
IO3-52	M16		
IO3-53	M17	LPXI_AD16	
IO3-54	M18	/LPXI_CBE2	
IO3-55	N13	LPXI_AD5	
IO3-56	N14	/LPXI_CBE3	
IO3-57	N15	LPXI_AD19	
IO3-58	N16	LPXI_AD21	
IO3-59	N17	LPXI_IDSEL	
IO3-60	N18	LPXI_AD18	
IO3-61	P14		
IO3-62	P15	/LPXI_GNT	
IO3-63	P16	LPXI_AD28	
IO3-64	P17	LPXI_AD22	
IO3-65	P18	LPXI_AD23	
IO3-66	R15		
IO3-67	R16		
IO3-68	R17	LPXI_AD24	
IO3-69	R18	LPXI_AD26	
IO3-70	T16	/LPXI_REQ	
IO3-71	T17		

U9-4 — EPM2210

IO4-1	N10	PXI_LBL0	
IO4-2	N11	PXI_LBL1	
IO4-3	N12		
IO4-4	N7	PXI_LBR0	
IO4-5	N8	PXI_LBR1	
IO4-6	N9	PXI_LBR2	
IO4-7	P10	PXI_LBR4	
IO4-8	P11		
IO4-9	P12		
IO4-10	P13		
IO4-11	P6	PXI_LBR3	
IO4-12	P7		
IO4-13	P8		
IO4-14	P9		
IO4-15	R10		
IO4-16	R11		
IO4-17	R12		
IO4-18	R13		
IO4-19	R14		
IO4-20	R5		
IO4-21	R6		
IO4-22	R7	PXI_LBR5	
IO4-23	R8	PXI_LBL4	
IO4-24	R9	PXI_LBL5	
IO4-25	T10		
IO4-26	T11		
IO4-27	T12		
IO4-28	T13		
IO4-29	T14		
IO4-30	T15		
IO4-31	T4	PXI_LBR10	
IO4-32	T5	PXI_LBL2	
IO4-33	T6	PXI_LBL3	
IO4-34	T7		
IO4-35	T8	PXI_LBR8	
IO4-36	T9	PXI_LBL8	
IO4-37	U1	LED_P6	
IO4-38	U10	PXI_LBL7	
IO4-39	U11	PXI_LBL12	
IO4-40	U12	PXI_LBL10	
IO4-41	U13		
IO4-42	U14	PXI_LBL9	
IO4-43	U15	PXI_LBR11	
IO4-44	U16	PXI_LBR12	
IO4-45	U18		
IO4-46	U3	PXI_LBR9	
IO4-47	U4		
IO4-48	U5	PXI_LBR7	
IO4-49	U6	PXI_LBL6	
IO4-50	U7	PXI_LBR6	
IO4-51	U8		
IO4-52	U9		
IO4-53	V10	SFLASH_Din	
IO4-54	V11	SFLASH_CLK	
IO4-55	V12	PXI_LBL11	
IO4-56	V13		
IO4-57	V14		
IO4-58	V15		
IO4-59	V17		
IO4-60	V2		
IO4-61	V4		
IO4-62	V5		
IO4-63	V6	SFLASH_HOLD	
IO4-64	V7	SFLASH_S	
IO4-65	V8	SFLASH_Qout	
	V9	SFLASH_W	

U9-5 — EPM2210

GNDIO1	A1	GND	
VCCIO2-1	A16	+2.5V	
GNDIO2	A18	GND	
VCCIO2-2	A3	+2.5V	
GNDIO3	B17	GND	
GNDIO4	B2	GND	
VCCIO1-1	C1	+2.5V	
VCCIO3-1	C18	+3.3V	
VCCIO2-3	G10	+2.5V	
VCCINT1	G11	+2.5V	
GNDINT1	G8	GND	
VCCIO2-4	G9	+2.5V	
GNDIO5	H10	GND	
GNDIO6	H11	GND	
VCCINT2	H12	+2.5V	
GNDINT2	H7	GND	
GNDIO7	H8	GND	
GNDIO8	H9	GND	
GNDINT3	J10	GND	
VCCINT3	J11	+2.5V	
VCCIO3-2	J12	+3.3V	
VCCIO1-2	J7	+2.5V	
GNDINT4	J8	GND	
VCCINT4	J9	+2.5V	
VCCINT5	K10	+2.5V	
GNDINT5	K11	GND	
VCCIO3-3	K12	+3.3V	
VCCIO1-3	K7	+2.5V	
VCCINT6	K8	+2.5V	
GNDINT6	K9	GND	
GNDIO9	L10	GND	
GNDIO10	L11	GND	
GNDINT7	L12	GND	
VCCINT7	L7	+2.5V	
GNDIO11	L8	GND	
GNDIO12	L9	GND	
GNDINT8	M11	GND	
VCCIO4-2	M10	+3.3V	
VCCINT8	M8	+2.5V	
VCCIO4-3	M9	+3.3V	
VCCIO1-4	T1	+2.5V	
VCCIO3-4	T18	+3.3V	
GNDIO13	U17	GND	
GNDIO14	U2	GND	
GNDIO15	V1	GND	
VCCIO4-4	V16	+3.3V	
GNDIO16	V18	GND	
VCCIO4-5	V3	+3.3V	

PXI: Band3 VCCIO:3.3V
VCCINT:2.5V
FPGA:BANK1&2 VCCIO 2.5V
其余VCCIO: 3.3V

U10 — M25P128

R43 10K, R44 10K, R45 10K, R47 100K
SFLASH_HOLD, SFLASH_S, SFLASH_Qout, SFLASH_Din, SFLASH_CLK, SFLASH_W
C29 0.1u, C30 0.01u

SFLASH MEMORY CONFIGDATA

R42–R49, R55 4.7k
D1 LED_P1, D2 LED_P2, D3 LED_P4, D4 LED_P5, D5 LED_P6

C31–C34 0.1u, C35–C38 0.1u, C39–C42 0.1u, C43–C46 0.1u, C47–C50 0.1u
C51 10u, C52 0.01u, C53 10u, C54 0.01u, C55 10u, C56 0.01u, C57 10u, C58 0.01u, C59 10u, C60 0.01u

CPLD的JTAG配置电路

male header JTAG connections:

pin#	jtag		
1	TCK	2	GND
3	TDO	4	Vcc
5	TMS	6	Vccio
7	(NC)	8	(NC)
9	TDI	10	GND

R50 10K, R51 10K, R52 10K, R53 10K, R54 10K
J6 — CON10AP
TCK, TDO, TMS, TDI, GND, +3.3V, TRST

CPLD CONFIG JATG

+3.3V, +2.5V, GND
1^,2,16,17,21
1^,2,7,8,9,11,12,13,15,17,21
1^,2,3,9,10,11,13,14,15,16,17,18,19,20,21

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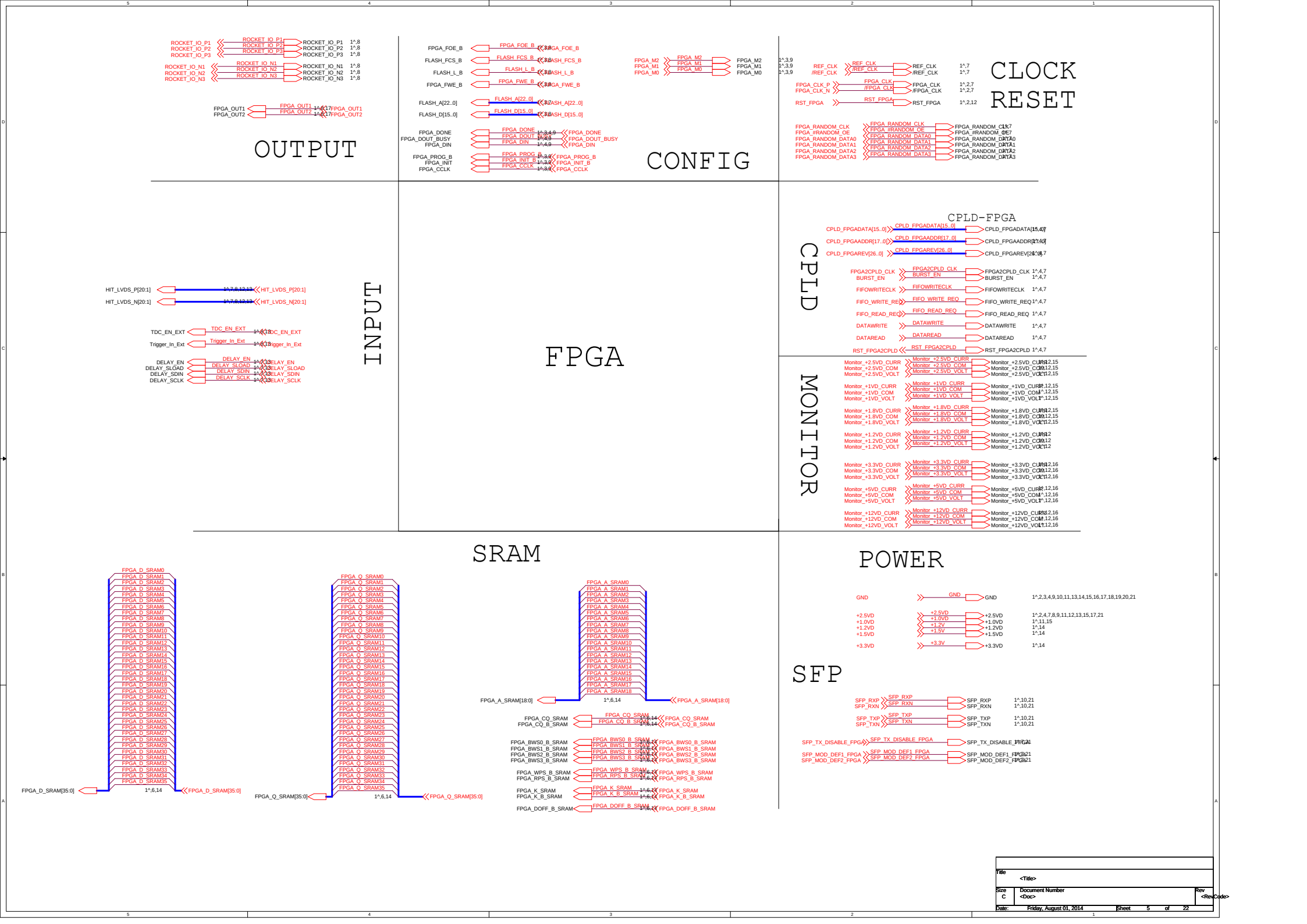
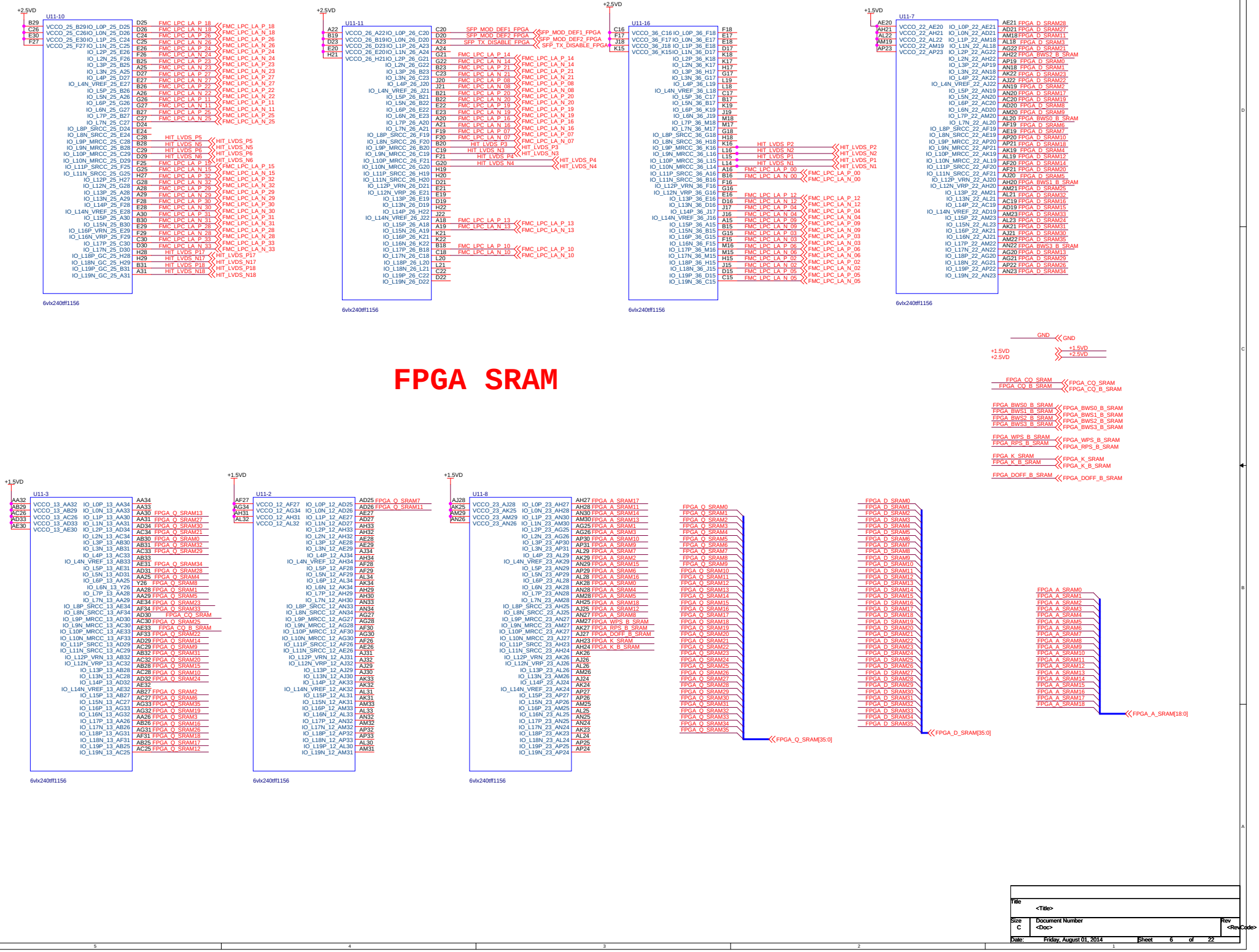

OUTPUT
CONFIG
CLOCK
RESET
INPUT
FPGA
CPLD
CPLD-FPGA
MONITOR
SRAM
POWER
SFP


FPGA SRAM
U11-10
U11-11
U11-16
U11-7
U11-3
U11-2
U11-8
6vlx240tff1156
FPGA_Q_SRAM[35:0]
FPGA_D_SRAM[35:0]
FPGA_A_SRAM[18:0]
GND
+1.5VD
+2.5VD
FPGA_CQ_SRAM
FPGA_CQ_B_SRAM
FPGA_BWS0_B_SRAM
FPGA_BWS1_B_SRAM
FPGA_BWS2_B_SRAM
FPGA_BWS3_B_SRAM
FPGA_WPS_B_SRAM
FPGA_RPS_B_SRAM
FPGA_K_SRAM
FPGA_K_B_SRAM
FPGA_DOFF_B_SRAM
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<Title>
Size C
Document Number <Doc>
Rev <RevCode>
Date: Friday, August 01, 2014
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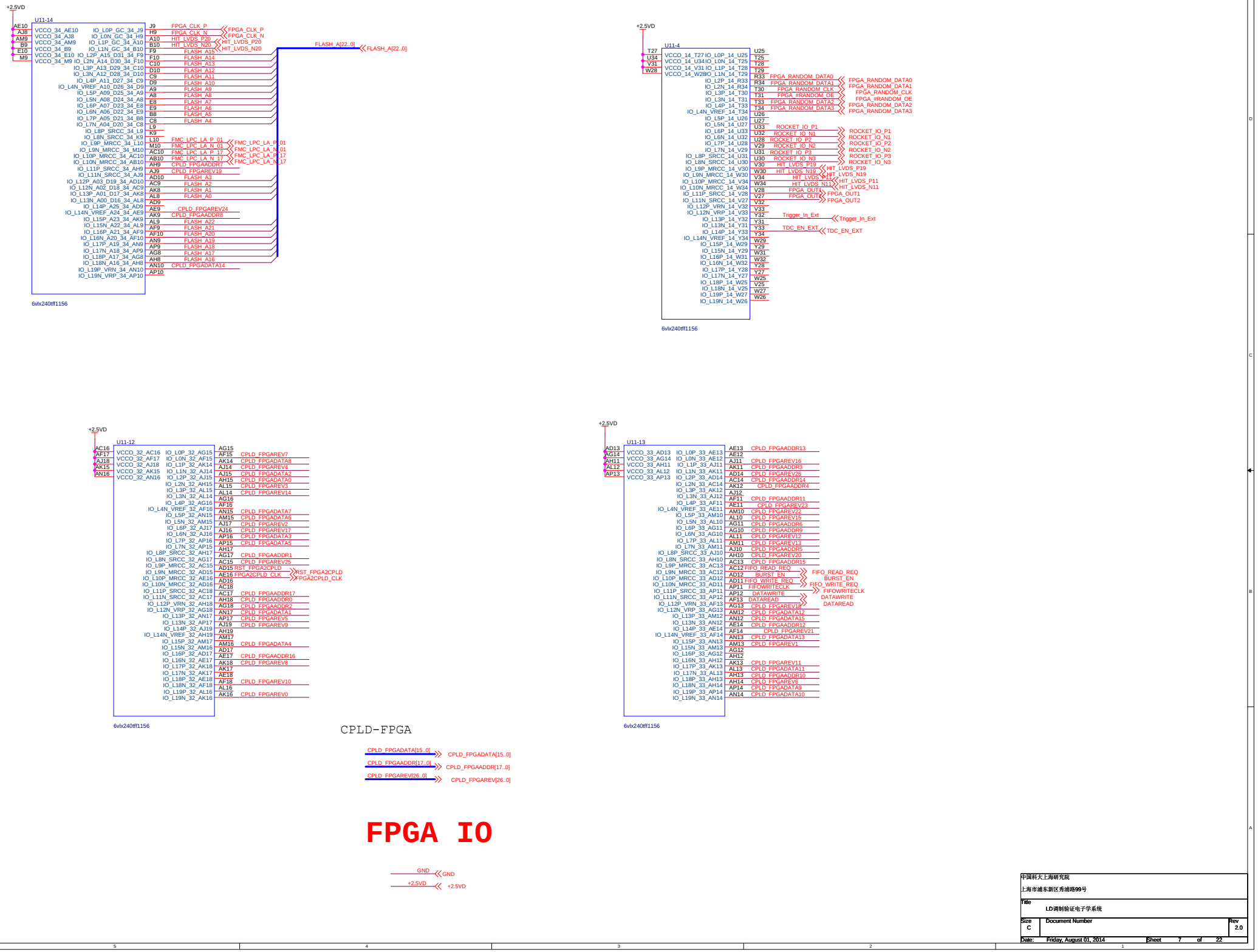
+2.5VD
U11-14
AE10 VCCO_34_AE10
AJ8 VCCO_34_AJ8
AM9 VCCO_34_AM9
B9 VCCO_34_B9
E10 VCCO_34_E10
M9 VCCO_34_M9
IO_L0P_GC_34_J9
IO_L0N_GC_34_H9
IO_L1P_GC_34_A10
IO_L1N_GC_34_B10
IO_L2P_A15_D31_34_F9
IO_L2N_A14_D30_34_F10
IO_L3P_A13_D29_34_C10
IO_L3N_A12_D28_34_D10
IO_L4P_A11_D27_34_C9
IO_L4N_VREF_A10_D26_34_D9
IO_L5P_A09_D25_34_A9
IO_L5N_A08_D24_34_A8
IO_L6P_A07_D23_34_E8
IO_L6N_A06_D22_34_E9
IO_L7P_A05_D21_34_B8
IO_L7N_A04_D20_34_C8
IO_L8P_SRCC_34_L9
IO_L8N_SRCC_34_K9
IO_L9P_MRCC_34_L10
IO_L9N_MRCC_34_M10
IO_L10P_MRCC_34_AC10
IO_L10N_MRCC_34_AB10
IO_L11P_SRCC_34_AH9
IO_L11N_SRCC_34_AJ9
IO_L12P_A03_D19_34_AD10
IO_L12N_A02_D18_34_AC9
IO_L13P_A01_D17_34_AK8
IO_L13N_A00_D16_34_AL8
IO_L14P_A25_34_AD9
IO_L14N_VREF_A24_34_AE9
IO_L15P_A23_34_AK9
IO_L15N_A22_34_AL9
IO_L16P_A21_34_AF9
IO_L16N_A20_34_AF10
IO_L17P_A19_34_AN9
IO_L17N_A18_34_AP9
IO_L18P_A17_34_AG8
IO_L18N_A16_34_AH8
IO_L19P_VRN_34_AN10
IO_L19N_VRP_34_AP10
J9 FPGA_CLK_P
H9 FPGA_CLK_N
A10 HIT_LVDS_P20
B10 HIT_LVDS_N20
F9 FLASH_A15
F10 FLASH_A14
C10 FLASH_A13
D10 FLASH_A12
C9 FLASH_A11
D9 FLASH_A10
A9 FLASH_A9
A8 FLASH_A8
E8 FLASH_A7
E9 FLASH_A6
B8 FLASH_A5
C8 FLASH_A4
L9
K9
L10 FMC_LPC_LA_P_01
M10 FMC_LPC_LA_N_01
AC10 FMC_LPC_LA_P_17
AB10 FMC_LPC_LA_N_17
AH9 CPLD_FPGAADDR7
AJ9 CPLD_FPGAREV19
AD10 FLASH_A3
AC9 FLASH_A2
AK8 FLASH_A1
AL8 FLASH_A0
AD9
AE9 CPLD_FPGAREV24
AK9 CPLD_FPGAADDR8
AL9 FLASH_A22
AF9 FLASH_A21
AF10 FLASH_A20
AN9 FLASH_A19
AP9 FLASH_A18
AG8 FLASH_A17
AH8 FLASH_A16
AN10 CPLD_FPGADATA14
AP10
FPGA_CLK_P
FPGA_CLK_N
HIT_LVDS_P20
HIT_LVDS_N20
FMC_LPC_LA_P_01
FMC_LPC_LA_N_01
FMC_LPC_LA_P_17
FMC_LPC_LA_N_17
FLASH_A[22..0]
FLASH_A[22..0]
6vlx240tff1156
+2.5VD
U11-4
T27 VCCO_14_T27
U34 VCCO_14_U34
V31 VCCO_14_V31
W28 VCCO_14_W28
IO_L0P_14_U25
IO_L0N_14_T25
IO_L1P_14_T26
IO_L1N_14_T29
IO_L2P_14_R33
IO_L2N_14_R34
IO_L3P_14_T30
IO_L3N_14_T31
IO_L4P_14_T33
IO_L4N_VREF_14_T34
IO_L5P_14_U26
IO_L5N_14_U27
IO_L6P_14_U33
IO_L6N_14_U32
IO_L7P_14_U28
IO_L7N_14_V29
IO_L8P_SRCC_14_U31
IO_L8N_SRCC_14_U30
IO_L9P_MRCC_14_V30
IO_L9N_MRCC_14_W30
IO_L10P_MRCC_14_V34
IO_L10N_MRCC_14_W34
IO_L11P_SRCC_14_V28
IO_L11N_SRCC_14_V27
IO_L12P_VRN_14_V32
IO_L12N_VRP_14_V33
IO_L13P_14_Y32
IO_L13N_14_Y31
IO_L14P_14_Y33
IO_L14N_VREF_14_Y34
IO_L15P_14_W29
IO_L15N_14_Y29
IO_L16P_14_W31
IO_L16N_14_W32
IO_L17P_14_Y28
IO_L17N_14_Y27
IO_L18P_14_W25
IO_L18N_14_V25
IO_L19P_14_W27
IO_L19N_14_W26
U25
T25
T28
T29
R33 FPGA_RANDOM_DATA0
R34 FPGA_RANDOM_DATA1
T30 FPGA_RANDOM_CLK
T31 FPGA_#RANDOM_OE
T33 FPGA_RANDOM_DATA2
T34 FPGA_RANDOM_DATA3
U26
U27
U33 ROCKET_IO_P1
U32 ROCKET_IO_N1
U28 ROCKET_IO_P2
V29 ROCKET_IO_N2
U31 ROCKET_IO_P3
U30 ROCKET_IO_N3
V30 HIT_LVDS_P19
W30 HIT_LVDS_N19
V34 HIT_LVDS_P11
W34 HIT_LVDS_N11
V28 FPGA_OUT1
V27 FPGA_OUT2
V32
V33
Y32 Trigger_In_Ext
Y31
Y33 TDC_EN_EXT
Y34
W29
Y29
W31
W32
Y28
Y27
W25
V25
W27
W26
FPGA_RANDOM_DATA0
FPGA_RANDOM_DATA1
FPGA_RANDOM_CLK
FPGA_#RANDOM_OE
FPGA_RANDOM_DATA2
FPGA_RANDOM_DATA3
ROCKET_IO_P1
ROCKET_IO_N1
ROCKET_IO_P2
ROCKET_IO_N2
ROCKET_IO_P3
ROCKET_IO_N3
HIT_LVDS_P19
HIT_LVDS_N19
HIT_LVDS_P11
HIT_LVDS_N11
FPGA_OUT1
FPGA_OUT2
Trigger_In_Ext
TDC_EN_EXT
6vlx240tff1156
+2.5VD
U11-12
AC16 VCCO_32_AC16
AF17 VCCO_32_AF17
AJ18 VCCO_32_AJ18
AK15 VCCO_32_AK15
AN16 VCCO_32_AN16
IO_L0P_32_AG15
IO_L0N_32_AF15
IO_L1P_32_AK14
IO_L1N_32_AJ14
IO_L2P_32_AJ15
IO_L2N_32_AH15
IO_L3P_32_AL15
IO_L3N_32_AL14
IO_L4P_32_AG16
IO_L4N_VREF_32_AF16
IO_L5P_32_AN15
IO_L5N_32_AM15
IO_L6P_32_AJ17
IO_L6N_32_AJ16
IO_L7P_32_AP16
IO_L7N_32_AP15
IO_L8P_SRCC_32_AH17
IO_L8N_SRCC_32_AG17
IO_L9P_MRCC_32_AC15
IO_L9N_MRCC_32_AD15
IO_L10P_MRCC_32_AE16
IO_L10N_MRCC_32_AD16
IO_L11P_SRCC_32_AC18
IO_L11N_SRCC_32_AC17
IO_L12P_VRN_32_AH18
IO_L12N_VRP_32_AG18
IO_L13P_32_AN17
IO_L13N_32_AP17
IO_L14P_32_AJ19
IO_L14N_VREF_32_AH19
IO_L15P_32_AM17
IO_L15N_32_AM16
IO_L16P_32_AD17
IO_L16N_32_AE17
IO_L17P_32_AK18
IO_L17N_32_AK17
IO_L18P_32_AE18
IO_L18N_32_AF18
IO_L19P_32_AL16
IO_L19N_32_AK16
AG15
AF15 CPLD_FPGAREV7
AK14 CPLD_FPGADATA8
AJ14 CPLD_FPGAREV4
AJ15 CPLD_FPGADATA2
AH15 CPLD_FPGADATA0
AL15 CPLD_FPGAREV3
AL14 CPLD_FPGAREV14
AG16
AF16
AN15 CPLD_FPGADATA7
AM15 CPLD_FPGADATA6
AJ17 CPLD_FPGAREV2
AJ16 CPLD_FPGAREV17
AP16 CPLD_FPGADATA3
AP15 CPLD_FPGADATA5
AH17
AG17 CPLD_FPGAADDR1
AC15 CPLD_FPGAREV25
AD15 RST_FPGA2CPLD
AE16 FPGA2CPLD_CLK
AD16
AC18
AC17 CPLD_FPGAADDR17
AH18 CPLD_FPGAADDR0
AG18 CPLD_FPGAADDR2
AN17 CPLD_FPGADATA1
AP17 CPLD_FPGAREV5
AJ19 CPLD_FPGAREV9
AH19
AM17
AM16 CPLD_FPGADATA4
AD17
AE17 CPLD_FPGAADDR16
AK18 CPLD_FPGAREV8
AK17
AE18
AF18 CPLD_FPGAREV10
AL16
AK16 CPLD_FPGAREV0
RST_FPGA2CPLD
FPGA2CPLD_CLK
6vlx240tff1156
+2.5VD
U11-13
AD13 VCCO_33_AD13
AG14 VCCO_33_AG14
AH11 VCCO_33_AH11
AL12 VCCO_33_AL12
AP13 VCCO_33_AP13
IO_L0P_33_AE13
IO_L0N_33_AE12
IO_L1P_33_AJ11
IO_L1N_33_AK11
IO_L2P_33_AD14
IO_L2N_33_AC14
IO_L3P_33_AK12
IO_L3N_33_AJ12
IO_L4P_33_AF11
IO_L4N_VREF_33_AE11
IO_L5P_33_AM10
IO_L5N_33_AL10
IO_L6P_33_AG11
IO_L6N_33_AG10
IO_L7P_33_AL11
IO_L7N_33_AM11
IO_L8P_SRCC_33_AJ10
IO_L8N_SRCC_33_AH10
IO_L9P_MRCC_33_AC13
IO_L9N_MRCC_33_AC12
IO_L10P_MRCC_33_AD12
IO_L10N_MRCC_33_AD11
IO_L11P_SRCC_33_AP11
IO_L11N_SRCC_33_AP12
IO_L12P_VRN_33_AF13
IO_L12N_VRP_33_AG13
IO_L13P_33_AM12
IO_L13N_33_AN12
IO_L14P_33_AE14
IO_L14N_VREF_33_AF14
IO_L15P_33_AN13
IO_L15N_33_AM13
IO_L16P_33_AG12
IO_L16N_33_AH12
IO_L17P_33_AK13
IO_L17N_33_AL13
IO_L18P_33_AH13
IO_L18N_33_AH14
IO_L19P_33_AP14
IO_L19N_33_AN14
AE13 CPLD_FPGAADDR13
AE12
AJ11 CPLD_FPGAREV16
AK11 CPLD_FPGAADDR3
AD14 CPLD_FPGAREV26
AC14 CPLD_FPGAADDR14
AK12 CPLD_FPGAADDR4
AJ12
AF11 CPLD_FPGAADDR11
AE11 CPLD_FPGAREV23
AM10 CPLD_FPGAREV22
AL10 CPLD_FPGAREV15
AG11 CPLD_FPGAADDR6
AG10 CPLD_FPGAADDR9
AL11 CPLD_FPGAREV12
AM11 CPLD_FPGAREV13
AJ10 CPLD_FPGAADDR5
AH10 CPLD_FPGAREV20
AC13 CPLD_FPGAADDR15
AC12 FIFO_READ_REQ
AD12 BURST_EN
AD11 FIFO_WRITE_REQ
AP11 FIFOWRITECLK
AP12 DATAWRITE
AF13 DATAREAD
AG13 CPLD_FPGAREV18
AM12 CPLD_FPGADATA12
AN12 CPLD_FPGADATA15
AE14 CPLD_FPGAADDR12
AF14 CPLD_FPGAREV21
AN13 CPLD_FPGADATA13
AM13 CPLD_FPGAREV1
AG12
AH12
AK13 CPLD_FPGAREV11
AL13 CPLD_FPGADATA11
AH13 CPLD_FPGAADDR10
AH14 CPLD_FPGAREV6
AP14 CPLD_FPGADATA9
AN14 CPLD_FPGADATA10
FIFO_READ_REQ
BURST_EN
FIFO_WRITE_REQ
FIFOWRITECLK
DATAWRITE
DATAREAD
6vlx240tff1156
CPLD-FPGA
CPLD_FPGADATA[15..0]
CPLD_FPGADATA[15..0]
CPLD_FPGAADDR[17..0]
CPLD_FPGAADDR[17..0]
CPLD_FPGAREV[26..0]
CPLD_FPGAREV[26..0]
FPGA IO
GND
GND
+2.5VD
+2.5VD
中国科大上海研究院
上海市浦东新区秀浦路99号
Title
LD调制验证电子学系统
Size C
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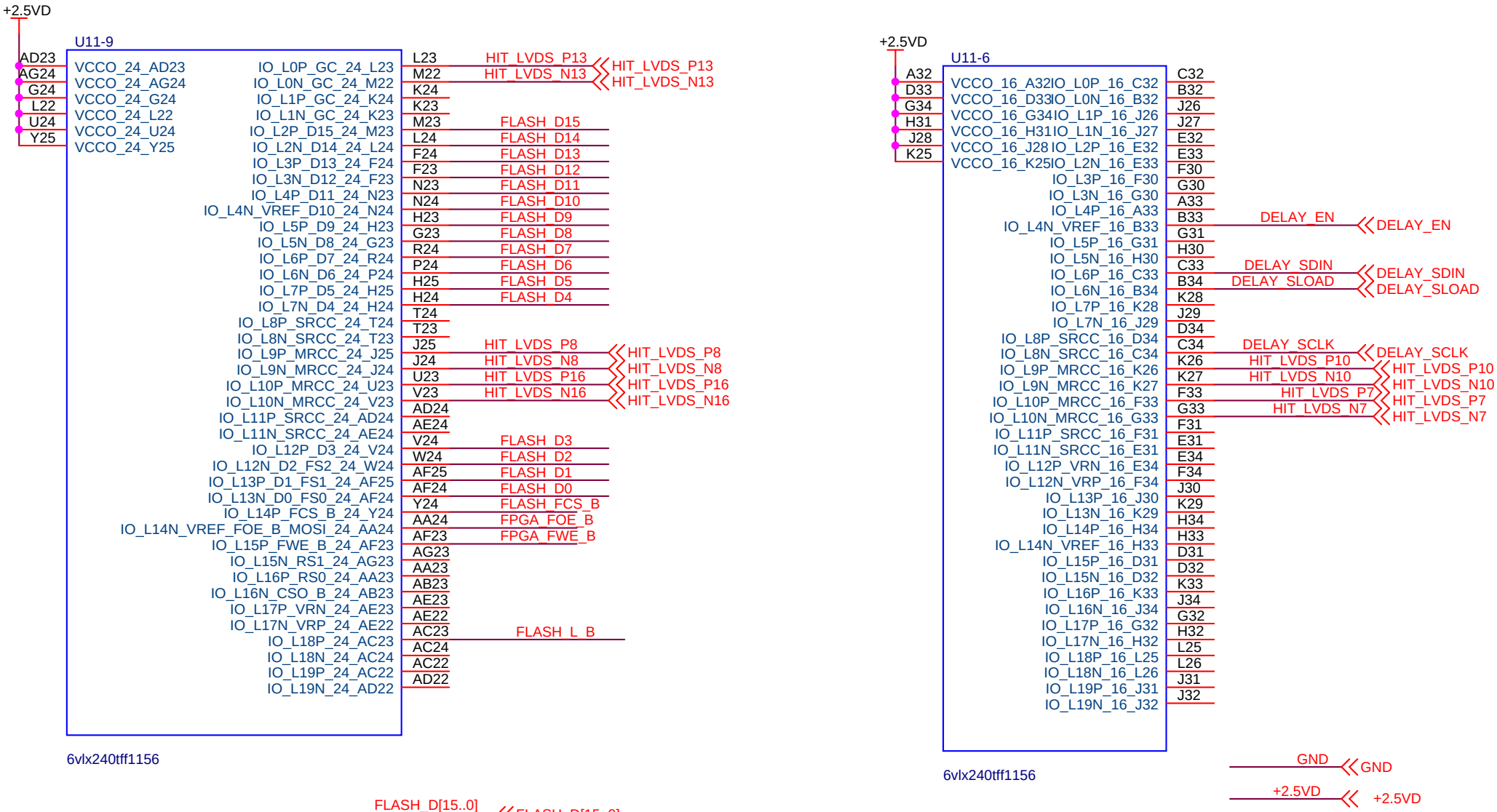
+2.5VD
U11-9
AD23
AG24
G24
L22
U24
Y25
VCCO_24_AD23
VCCO_24_AG24
VCCO_24_G24
VCCO_24_L22
VCCO_24_U24
VCCO_24_Y25
IO_L0P_GC_24_L23
IO_L0N_GC_24_M22
IO_L1P_GC_24_K24
IO_L1N_GC_24_K23
IO_L2P_D15_24_M23
IO_L2N_D14_24_L24
IO_L3P_D13_24_F24
IO_L3N_D12_24_F23
IO_L4P_D11_24_N23
IO_L4N_VREF_D10_24_N24
IO_L5P_D9_24_H23
IO_L5N_D8_24_G23
IO_L6P_D7_24_R24
IO_L6N_D6_24_P24
IO_L7P_D5_24_H25
IO_L7N_D4_24_H24
IO_L8P_SRCC_24_T24
IO_L8N_SRCC_24_T23
IO_L9P_MRCC_24_J25
IO_L9N_MRCC_24_J24
IO_L10P_MRCC_24_U23
IO_L10N_MRCC_24_V23
IO_L11P_SRCC_24_AD24
IO_L11N_SRCC_24_AE24
IO_L12P_D3_24_V24
IO_L12N_D2_FS2_24_W24
IO_L13P_D1_FS1_24_AF25
IO_L13N_D0_FS0_24_AF24
IO_L14P_FCS_B_24_Y24
IO_L14N_VREF_FOE_B_MOSI_24_AA24
IO_L15P_FWE_B_24_AF23
IO_L15N_RS1_24_AG23
IO_L16P_RS0_24_AA23
IO_L16N_CSO_B_24_AB23
IO_L17P_VRN_24_AE23
IO_L17N_VRP_24_AE22
IO_L18P_24_AC23
IO_L18N_24_AC24
IO_L19P_24_AC22
IO_L19N_24_AD22
L23 HIT_LVDS_P13
M22 HIT_LVDS_N13
K24
K23
M23 FLASH_D15
L24 FLASH_D14
F24 FLASH_D13
F23 FLASH_D12
N23 FLASH_D11
N24 FLASH_D10
H23 FLASH_D9
G23 FLASH_D8
R24 FLASH_D7
P24 FLASH_D6
H25 FLASH_D5
H24 FLASH_D4
T24
T23
J25 HIT_LVDS_P8
J24 HIT_LVDS_N8
U23 HIT_LVDS_P16
V23 HIT_LVDS_N16
AD24
AE24
V24 FLASH_D3
W24 FLASH_D2
AF25 FLASH_D1
AF24 FLASH_D0
Y24 FLASH_FCS_B
AA24 FPGA_FOE_B
AF23 FPGA_FWE_B
AG23
AA23
AB23
AE23
AE22
AC23 FLASH_L_B
AC24
AC22
AD22
HIT_LVDS_P13
HIT_LVDS_N13
HIT_LVDS_P8
HIT_LVDS_N8
HIT_LVDS_P16
HIT_LVDS_N16
6vlx240tff1156
+2.5VD
U11-6
A32
D33
G34
H31
J28
K25
VCCO_16_A32
VCCO_16_D33
VCCO_16_G34
VCCO_16_H31
VCCO_16_J28
VCCO_16_K25
IO_L0P_16_C32
IO_L0N_16_B32
IO_L1P_16_J26
IO_L1N_16_J27
IO_L2P_16_E32
IO_L2N_16_E33
IO_L3P_16_F30
IO_L3N_16_G30
IO_L4P_16_A33
IO_L4N_VREF_16_B33
IO_L5P_16_G31
IO_L5N_16_H30
IO_L6P_16_C33
IO_L6N_16_B34
IO_L7P_16_K28
IO_L7N_16_J29
IO_L8P_SRCC_16_D34
IO_L8N_SRCC_16_C34
IO_L9P_MRCC_16_K26
IO_L9N_MRCC_16_K27
IO_L10P_MRCC_16_F33
IO_L10N_MRCC_16_G33
IO_L11P_SRCC_16_F31
IO_L11N_SRCC_16_E31
IO_L12P_VRN_16_E34
IO_L12N_VRP_16_F34
IO_L13P_16_J30
IO_L13N_16_K29
IO_L14P_16_H34
IO_L14N_VREF_16_H33
IO_L15P_16_D31
IO_L15N_16_D32
IO_L16P_16_K33
IO_L16N_16_J34
IO_L17P_16_G32
IO_L17N_16_H32
IO_L18P_16_L25
IO_L18N_16_L26
IO_L19P_16_J31
IO_L19N_16_J32
C32
B32
J26
J27
E32
E33
F30
G30
A33
B33 DELAY_EN
G31
H30
C33 DELAY_SDIN
B34 DELAY_SLOAD
K28
J29
D34
C34 DELAY_SCLK
K26 HIT_LVDS_P10
K27 HIT_LVDS_N10
F33 HIT_LVDS_P7
G33 HIT_LVDS_N7
F31
E31
E34
F34
J30
K29
H34
H33
D31
D32
K33
J34
G32
H32
L25
L26
J31
J32
DELAY_EN
DELAY_SDIN
DELAY_SLOAD
DELAY_SCLK
HIT_LVDS_P10
HIT_LVDS_N10
HIT_LVDS_P7
HIT_LVDS_N7
6vlx240tff1156
GND
GND
+2.5VD
+2.5VD
FLASH_D[15..0]
FLASH_D[15..0]
FLASH_D15
FLASH_D14
FLASH_D13
FLASH_D12
FLASH_D11
FLASH_D10
FLASH_D9
FLASH_D8
FLASH_D7
FLASH_D6
FLASH_D5
FLASH_D4
FLASH_D3
FLASH_D2
FLASH_D1
FLASH_D0
FLASH_FCS_B
FPGA_FOE_B
FPGA_FWE_B
FLASH_L_B
FLASH_FCS_B
FPGA_FOE_B
FPGA_FWE_B
FLASH_L_B
flash_L需要接到FPGA IO_L18P_24pin
中国科大上海研究院
上海市浦东新区秀浦路99号
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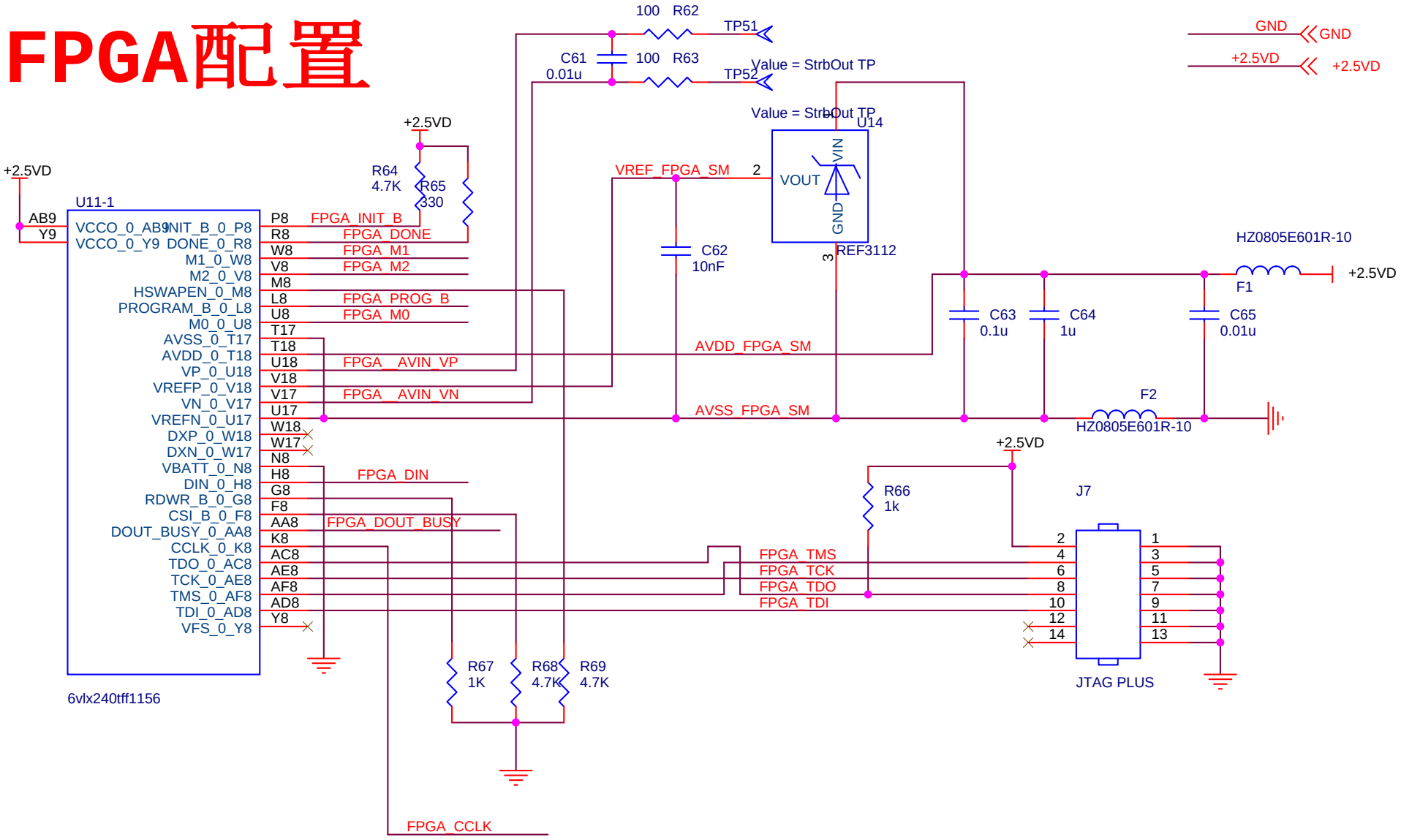
FPGA配置



FPGA_DONE — FPGA_DONE
FPGA_DOUT_BUSY — FPGA_DOUT_BUSY
FPGA_DIN — FPGA_DIN

FPGA_PROG_B — FPGA_PROG_B
FPGA_INIT_B — FPGA_INIT_B
FPGA_CCLK — FPGA_CCLK

FPGA_M2 — FPGA_M2
FPGA_M1 — FPGA_M1
FPGA_M0 — FPGA_M0

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FPGA MGT

U11-17

MGTTXP0_112_AP1	AP1
MGTTXN0_112_AP2	AP2
MGTRXP0_112_AP5	AP5
MGTRXN0_112_AP6	AP6
MGTTXP1_112_AN3	AN3
MGTTXN1_112_AN4	AN4
MGTRXP1_112_AM5	AM5
MGTRXN1_112_AM6	AM6
MGTTXP2_112_AM1	AM1
MGTTXN2_112_AM2	AM2
MGTRXP2_112_AL3	AL3
MGTRXN2_112_AL4	AL4
MGTTXP3_112_AK1	AK1
MGTTXN3_112_AK2	AK2
MGTRXP3_112_AJ3	AJ3
MGTRXN3_112_AJ4	AJ4
MGTREFCLK0P_112_AK6	AK6
MGTREFCLK0N_112_AK5	AK5
MGTREFCLK1P_112_AH6	AH6
MGTREFCLK1N_112_AH5	AH5

6vlx240tff1156

U11-18

MGTTXP0_113_AH1	AH1
MGTTXN0_113_AH2	AH2
MGTRXP0_113_AG3	AG3
MGTRXN0_113_AG4	AG4
MGTTXP1_113_AF1	AF1
MGTTXN1_113_AF2	AF2
MGTRXP1_113_AF5	AF5
MGTRXN1_113_AF6	AF6
MGTTXP2_113_AD1	AD1
MGTTXN2_113_AD2	AD2
MGTRXP2_113_AE3	AE3
MGTRXN2_113_AE4	AE4
MGTTXP3_113_AB1	AB1
MGTTXN3_113_AB2	AB2
MGTRXP3_113_AC3	AC3
MGTRXN3_113_AC4	AC4
MGTREFCLK0P_113_AD6	AD6
MGTREFCLK0N_113_AD5	AD5
MGTREFCLK1P_113_AB6	AB6
MGTREFCLK1N_113_AB5	AB5

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U11-19

MGTTXP0_114_Y1	Y1
MGTTXN0_114_Y2	Y2
MGTRXP0_114_AA3	AA3
MGTRXN0_114_AA4	AA4
MGTTXP1_114_V1	V1
MGTTXN1_114_V2	V2
MGTRXP1_114_W3	W3
MGTRXN1_114_W4	W4
MGTTXP2_114_T1	T1
MGTTXN2_114_T2	T2
MGTRXP2_114_U3	U3
MGTRXN2_114_U4	U4
MGTTXP3_114_P1	P1
MGTTXN3_114_P2	P2
MGTRXP3_114_R3	R3
MGTRXN3_114_R4	R4
MGTREFCLK0P_114_V6	V6
MGTREFCLK0N_114_V5	V5
MGTREFCLK1P_114_T6	T6
MGTREFCLK1N_114_T5	T5

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U11-20

MGTTXP0_115_M1	M1	SFP_TXP
MGTTXN0_115_M2	M2	SFP_TXN
MGTRXP0_115_N3	N3	SFP_RXP
MGTRXN0_115_N4	N4	SFP_RXN
MGTTXP1_115_K1	K1	
MGTTXN1_115_K2	K2	
MGTRXP1_115_L3	L3	
MGTRXN1_115_L4	L4	
MGTTXP2_115_H1	H1	
MGTTXN2_115_H2	H2	
MGTRXP2_115_K5	K5	
MGTRXN2_115_K6	K6	
MGTTXP3_115_F1	F1	FMC_LPC_DP_C2M_P_0
MGTTXN3_115_F2	F2	FMC_LPC_DP_C2M_N_0
MGTRXP3_115_J3	J3	FMC_LPC_DP_M2C_P_0
MGTRXN3_115_J4	J4	FMC_LPC_DP_M2C_N_0
MGTREFCLK0P_115_P6	P6	REF_CLK_FPGA
MGTREFCLK0N_115_P5	P5	/REF_CLK_FPGA
MGTREFCLK1P_115_M6	M6	GBTCLK0_M2C_P
MGTREFCLK1N_115_M5	M5	GBTCLK0_M2C_N
MGTAVTTRCAL_115_AP7	AP7	MGT_AVTT
MGTRREF_115_AN7	AN7	

SFP_TXP SFP_TXN SFP_RXP SFP_RXN

FMC_LPC_DP_C2M_P_0 FMC_LPC_DP_C2M_N_0 FMC_LPC_DP_M2C_P_0 FMC_LPC_DP_M2C_N_0

R332 100 1%

+1.2VD

增加SFP收发管脚

此电阻两端到两个脚AP7、AN7的布线按差分走，尽量短

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U11-21

MGTTXP0_116_D1	D1
MGTTXN0_116_D2	D2
MGTRXP0_116_G3	G3
MGTRXN0_116_G4	G4
MGTTXP1_116_C3	C3
MGTTXN1_116_C4	C4
MGTRXP1_116_E3	E3
MGTRXN1_116_E4	E4
MGTTXP2_116_B1	B1
MGTTXN2_116_B2	B2
MGTRXP2_116_D5	D5
MGTRXN2_116_D6	D6
MGTTXP3_116_A3	A3
MGTTXN3_116_A4	A4
MGTRXP3_116_B5	B5
MGTRXN3_116_B6	B6
MGTREFCLK0P_116_H6	H6
MGTREFCLK0N_116_H5	H5
MGTREFCLK1P_116_F6	F6
MGTREFCLK1N_116_F5	F5

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6vlx240tff1156

REF_CLK_FPGA C320 0.01u REF_CLK → REF_CLK

/REF_CLK_FPGA C321 0.01u /REF_CLK → /REF_CLK

GND → GND

GBTCLK0_M2C_P C322 0.01u FMC_LPC_GBTCLK0_M2C_P → FMC_LPC_GBTCLK0_M2C_P

GBTCLK0_M2C_N C323 0.01u FMC_LPC_GBTCLK0_M2C_N → FMC_LPC_GBTCLK0_M2C_N

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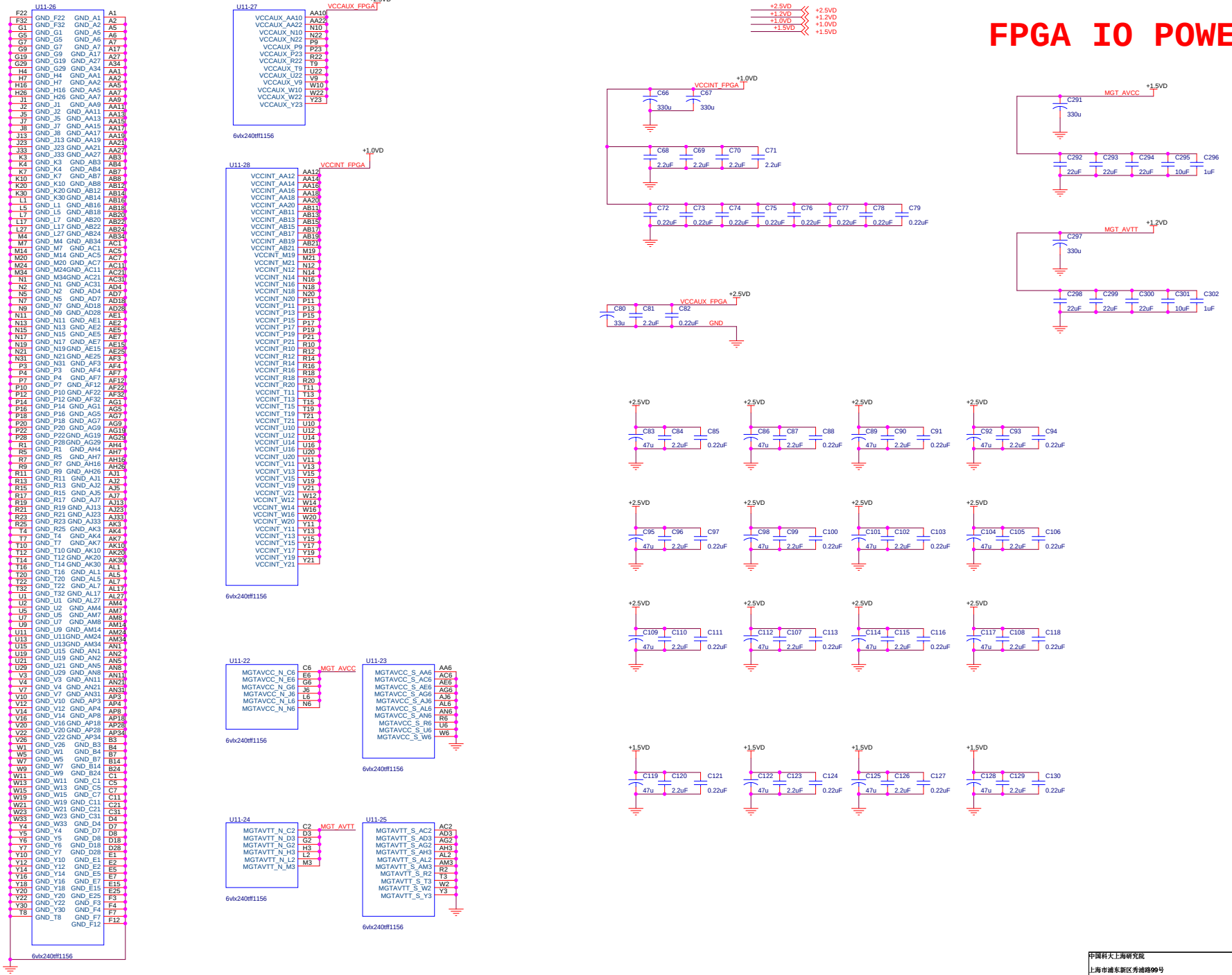
FPGA IO POWER



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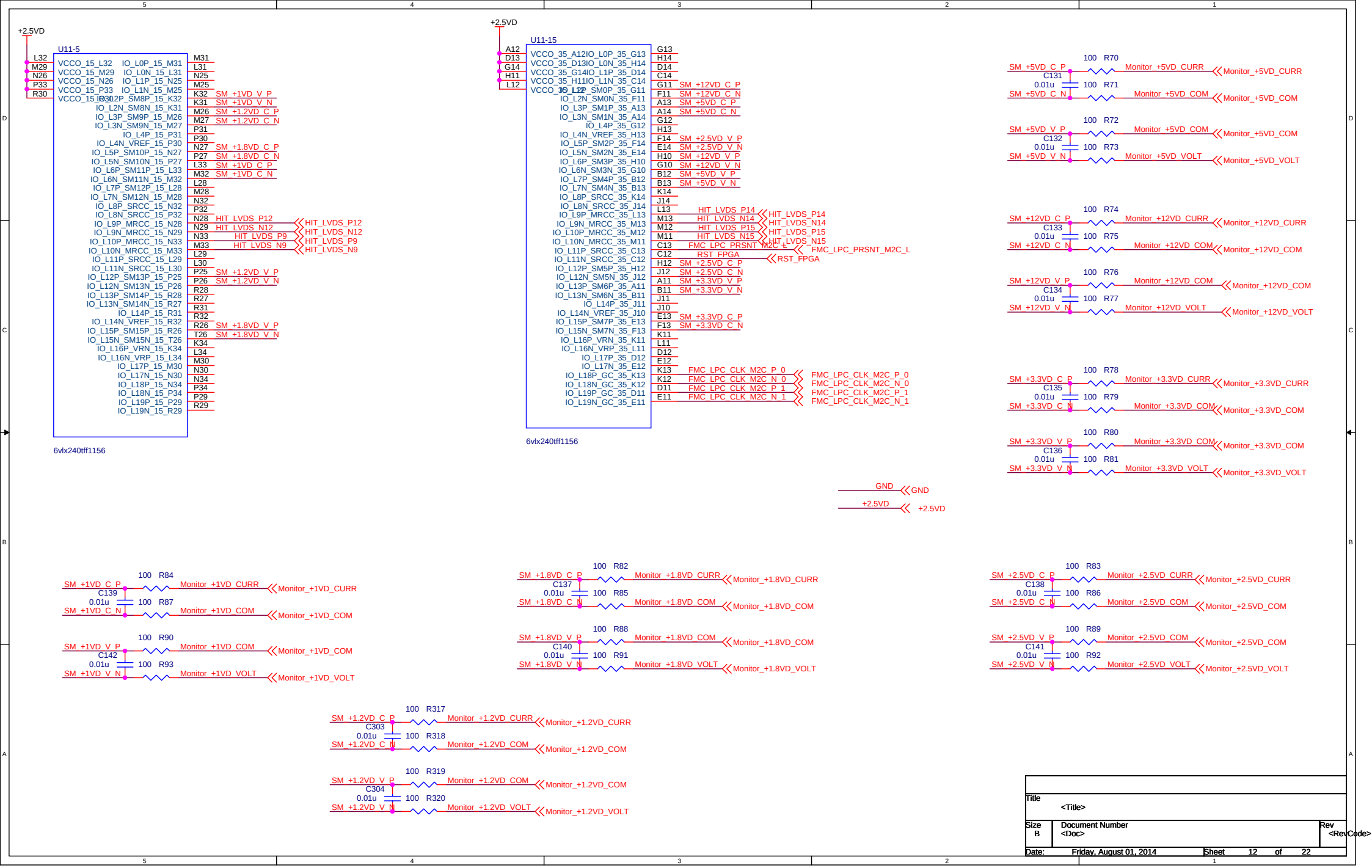
+2.5VD
U11-5
VCCO_15_L32 IO_L0P_15_M31
VCCO_15_M29 IO_L0N_15_L31
VCCO_15_N26 IO_L1P_15_N25
VCCO_15_P33 IO_L1N_15_M25
VCCO_15_R30 IO_L2P_SM8P_15_K32
IO_L2N_SM8N_15_K31
IO_L3P_SM9P_15_M26
IO_L3N_SM9N_15_M27
IO_L4P_15_P31
IO_L4N_VREF_15_P30
IO_L5P_SM10P_15_N27
IO_L5N_SM10N_15_P27
IO_L6P_SM11P_15_L33
IO_L6N_SM11N_15_M32
IO_L7P_SM12P_15_L28
IO_L7N_SM12N_15_M28
IO_L8P_SRCC_15_N32
IO_L8N_SRCC_15_P32
IO_L9P_MRCC_15_N28
IO_L9N_MRCC_15_N29
IO_L10P_MRCC_15_N33
IO_L10N_MRCC_15_M33
IO_L11P_SRCC_15_L29
IO_L11N_SRCC_15_L30
IO_L12P_SM13P_15_P25
IO_L12N_SM13N_15_P26
IO_L13P_SM14P_15_R28
IO_L13N_SM14N_15_R27
IO_L14P_15_R31
IO_L14N_VREF_15_R32
IO_L15P_SM15P_15_R26
IO_L15N_SM15N_15_T26
IO_L16P_VRN_15_K34
IO_L16N_VRP_15_L34
IO_L17P_15_M30
IO_L17N_15_N30
IO_L18P_15_N34
IO_L18N_15_P34
IO_L19P_15_P29
IO_L19N_15_R29
SM_+1VD_V_P
SM_+1VD_V_N
SM_+1.2VD_C_P
SM_+1.2VD_C_N
SM_+1.8VD_C_P
SM_+1.8VD_C_N
SM_+1VD_C_P
SM_+1VD_C_N
SM_+1.2VD_V_P
SM_+1.2VD_V_N
SM_+1.8VD_V_P
SM_+1.8VD_V_N
HIT_LVDS_P12
HIT_LVDS_N12
HIT_LVDS_P9
HIT_LVDS_N9
6vlx240tff1156
+2.5VD
U11-15
VCCO_35_A12IO_L0P_35_G13
VCCO_35_D13IO_L0N_35_H14
VCCO_35_G14IO_L1P_35_D14
VCCO_35_H11IO_L1N_35_C14
VCCO_35_L12IO_L2P_SM0P_35_G11
IO_L2N_SM0N_35_F11
IO_L3P_SM1P_35_A13
IO_L3N_SM1N_35_A14
IO_L4P_35_G12
IO_L4N_VREF_35_H13
IO_L5P_SM2P_35_F14
IO_L5N_SM2N_35_E14
IO_L6P_SM3P_35_H10
IO_L6N_SM3N_35_G10
IO_L7P_SM4P_35_B12
IO_L7N_SM4N_35_B13
IO_L8P_SRCC_35_K14
IO_L8N_SRCC_35_J14
IO_L9P_MRCC_35_L13
IO_L9N_MRCC_35_M13
IO_L10P_MRCC_35_M12
IO_L10N_MRCC_35_M11
IO_L11P_SRCC_35_C13
IO_L11N_SRCC_35_C12
IO_L12P_SM5P_35_H12
IO_L12N_SM5N_35_J12
IO_L13P_SM6P_35_A11
IO_L13N_SM6N_35_B11
IO_L14P_35_J11
IO_L14N_VREF_35_J10
IO_L15P_SM7P_35_E13
IO_L15N_SM7N_35_F13
IO_L16P_VRN_35_K11
IO_L16N_VRP_35_L11
IO_L17P_35_D12
IO_L17N_35_E12
IO_L18P_GC_35_K13
IO_L18N_GC_35_K12
IO_L19P_GC_35_D11
IO_L19N_GC_35_E11
SM_+12VD_C_P
SM_+12VD_C_N
SM_+5VD_C_P
SM_+5VD_C_N
SM_+2.5VD_V_P
SM_+2.5VD_V_N
SM_+12VD_V_N
SM_+12VD_V_P
SM_+5VD_V_P
SM_+5VD_V_N
SM_+3.3VD_C_P
SM_+3.3VD_C_N
SM_+3.3VD_V_P
SM_+3.3VD_V_N
FMC_LPC_PRSNT_M2C_L
RST_FPGA
FMC_LPC_CLK_M2C_P_0
FMC_LPC_CLK_M2C_N_0
FMC_LPC_CLK_M2C_P_1
FMC_LPC_CLK_M2C_N_1
6vlx240tff1156
R70 100
C131 0.01u
R71 100
R72 100
C132 0.01u
R73 100
R74 100
C133 0.01u
R75 100
R76 100
C134 0.01u
R77 100
R78 100
C135 0.01u
R79 100
R80 100
C136 0.01u
R81 100
Monitor_+5VD_CURR
Monitor_+5VD_COM
Monitor_+5VD_VOLT
Monitor_+12VD_CURR
Monitor_+12VD_COM
Monitor_+12VD_VOLT
Monitor_+3.3VD_CURR
Monitor_+3.3VD_COM
Monitor_+3.3VD_VOLT
GND
+2.5VD
R84 100
C139 0.01u
R87 100
R90 100
C142 0.01u
R93 100
R82 100
C137 0.01u
R85 100
R88 100
C140 0.01u
R91 100
R83 100
C138 0.01u
R86 100
R89 100
C141 0.01u
R92 100
Monitor_+1VD_CURR
Monitor_+1VD_COM
Monitor_+1VD_VOLT
Monitor_+1.8VD_CURR
Monitor_+1.8VD_COM
Monitor_+1.8VD_VOLT
Monitor_+2.5VD_CURR
Monitor_+2.5VD_COM
Monitor_+2.5VD_VOLT
R317 100
C303 0.01u
R318 100
R319 100
C304 0.01u
R320 100
Monitor_+1.2VD_CURR
Monitor_+1.2VD_COM
Monitor_+1.2VD_VOLT
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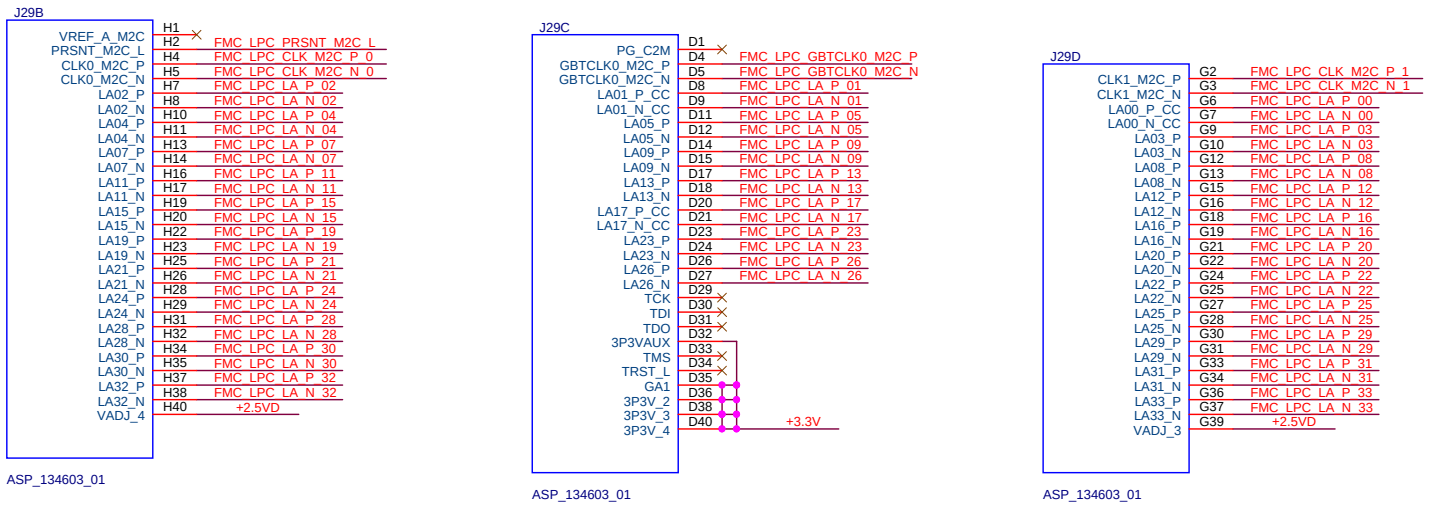
J29B
VREF_A_M2C H1
PRSNT_M2C_L H2 FMC_LPC_PRSNT_M2C_L
CLK0_M2C_P H4 FMC_LPC_CLK_M2C_P_0
CLK0_M2C_N H5 FMC_LPC_CLK_M2C_N_0
LA02_P H7 FMC_LPC_LA_P_02
LA02_N H8 FMC_LPC_LA_N_02
LA04_P H10 FMC_LPC_LA_P_04
LA04_N H11 FMC_LPC_LA_N_04
LA07_P H13 FMC_LPC_LA_P_07
LA07_N H14 FMC_LPC_LA_N_07
LA11_P H16 FMC_LPC_LA_P_11
LA11_N H17 FMC_LPC_LA_N_11
LA15_P H19 FMC_LPC_LA_P_15
LA15_N H20 FMC_LPC_LA_N_15
LA19_P H22 FMC_LPC_LA_P_19
LA19_N H23 FMC_LPC_LA_N_19
LA21_P H25 FMC_LPC_LA_P_21
LA21_N H26 FMC_LPC_LA_N_21
LA24_P H28 FMC_LPC_LA_P_24
LA24_N H29 FMC_LPC_LA_N_24
LA28_P H31 FMC_LPC_LA_P_28
LA28_N H32 FMC_LPC_LA_N_28
LA30_P H34 FMC_LPC_LA_P_30
LA30_N H35 FMC_LPC_LA_N_30
LA32_P H37 FMC_LPC_LA_P_32
LA32_N H38 FMC_LPC_LA_N_32
VADJ_4 H40 +2.5VD
ASP_134603_01
J29C
PG_C2M D1
GBTCLK0_M2C_P D4 FMC_LPC_GBTCLK0_M2C_P
GBTCLK0_M2C_N D5 FMC_LPC_GBTCLK0_M2C_N
LA01_P_CC D8 FMC_LPC_LA_P_01
LA01_N_CC D9 FMC_LPC_LA_N_01
LA05_P D11 FMC_LPC_LA_P_05
LA05_N D12 FMC_LPC_LA_N_05
LA09_P D14 FMC_LPC_LA_P_09
LA09_N D15 FMC_LPC_LA_N_09
LA13_P D17 FMC_LPC_LA_P_13
LA13_N D18 FMC_LPC_LA_N_13
LA17_P_CC D20 FMC_LPC_LA_P_17
LA17_N_CC D21 FMC_LPC_LA_N_17
LA23_P D23 FMC_LPC_LA_P_23
LA23_N D24 FMC_LPC_LA_N_23
LA26_P D26 FMC_LPC_LA_P_26
LA26_N D27 FMC_LPC_LA_N_26
TCK D29
TDI D30
TDO D31
3P3VAUX D32
TMS D33
TRST_L D34
GA1 D35
3P3V_2 D36
3P3V_3 D38
3P3V_4 D40 +3.3V
ASP_134603_01
J29D
CLK1_M2C_P G2 FMC_LPC_CLK_M2C_P_1
CLK1_M2C_N G3 FMC_LPC_CLK_M2C_N_1
LA00_P_CC G6 FMC_LPC_LA_P_00
LA00_N_CC G7 FMC_LPC_LA_N_00
LA03_P G9 FMC_LPC_LA_P_03
LA03_N G10 FMC_LPC_LA_N_03
LA08_P G12 FMC_LPC_LA_P_08
LA08_N G13 FMC_LPC_LA_N_08
LA12_P G15 FMC_LPC_LA_P_12
LA12_N G16 FMC_LPC_LA_N_12
LA16_P G18 FMC_LPC_LA_P_16
LA16_N G19 FMC_LPC_LA_N_16
LA20_P G21 FMC_LPC_LA_P_20
LA20_N G22 FMC_LPC_LA_N_20
LA22_P G24 FMC_LPC_LA_P_22
LA22_N G25 FMC_LPC_LA_N_22
LA25_P G27 FMC_LPC_LA_P_25
LA25_N G28 FMC_LPC_LA_N_25
LA29_P G30 FMC_LPC_LA_P_29
LA29_N G31 FMC_LPC_LA_N_29
LA31_P G33 FMC_LPC_LA_P_31
LA31_N G34 FMC_LPC_LA_N_31
LA33_P G36 FMC_LPC_LA_P_33
LA33_N G37 FMC_LPC_LA_N_33
VADJ_3 G39 +2.5VD
ASP_134603_01
FMC_LPC_LA_P_00 FMC_LPC_LA_P_00
FMC_LPC_LA_P_01 FMC_LPC_LA_P_01
FMC_LPC_LA_P_02 FMC_LPC_LA_P_02
FMC_LPC_LA_P_03 FMC_LPC_LA_P_03
FMC_LPC_LA_P_04 FMC_LPC_LA_P_04
FMC_LPC_LA_P_05 FMC_LPC_LA_P_05
FMC_LPC_LA_P_06 FMC_LPC_LA_P_06
FMC_LPC_LA_P_07 FMC_LPC_LA_P_07
FMC_LPC_LA_P_08 FMC_LPC_LA_P_08
FMC_LPC_LA_P_09 FMC_LPC_LA_P_09
FMC_LPC_LA_P_10 FMC_LPC_LA_P_10
FMC_LPC_LA_P_11 FMC_LPC_LA_P_11
FMC_LPC_LA_P_12 FMC_LPC_LA_P_12
FMC_LPC_LA_P_13 FMC_LPC_LA_P_13
FMC_LPC_LA_P_14 FMC_LPC_LA_P_14
FMC_LPC_LA_P_15 FMC_LPC_LA_P_15
FMC_LPC_LA_P_16 FMC_LPC_LA_P_16
FMC_LPC_LA_P_17 FMC_LPC_LA_P_17
FMC_LPC_LA_P_18 FMC_LPC_LA_P_18
FMC_LPC_LA_P_19 FMC_LPC_LA_P_19
FMC_LPC_LA_P_20 FMC_LPC_LA_P_20
FMC_LPC_LA_P_21 FMC_LPC_LA_P_21
FMC_LPC_LA_P_22 FMC_LPC_LA_P_22
FMC_LPC_LA_P_23 FMC_LPC_LA_P_23
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FMC_LPC_LA_P_31 FMC_LPC_LA_P_31
FMC_LPC_LA_P_32 FMC_LPC_LA_P_32
FMC_LPC_LA_P_33 FMC_LPC_LA_P_33
+3.3V
C324
0.1uF
GND
+2.5VD
C325
0.1uF
GND
J29A
DP0_C2M_P C2 FMC_LPC_DP_C2M_P_0
DP0_C2M_N C3 FMC_LPC_DP_C2M_N_0
DP0_M2C_P C6 FMC_LPC_DP_M2C_P_0
DP0_M2C_N C7 FMC_LPC_DP_M2C_N_0
LA06_P C10 FMC_LPC_LA_P_06
LA06_N C11 FMC_LPC_LA_N_06
LA10_P C14 FMC_LPC_LA_P_10
LA10_N C15 FMC_LPC_LA_N_10
LA14_P C18 FMC_LPC_LA_P_14
LA14_N C19 FMC_LPC_LA_N_14
LA18_P_CC C22 FMC_LPC_LA_P_18
LA18_N_CC C23 FMC_LPC_LA_N_18
LA27_P C26 FMC_LPC_LA_P_27
LA27_N C27 FMC_LPC_LA_N_27
SCL C30
SDA C31
GA0 C34 FMC_LPC_GA0
12P0V_1 C35
12P0V_2 C37
3P3V_1 C39 +3.3V
ASP_134603_01
GND
J29E
C1 C4 C5 C8 C9 C12 C13 C16 C17 C20 C21 C24 C25 C28 C29 C32 C33 C36 C38 C40 D2 D3 D6 D7 D10 D13 D16 D19 D22 D25 D28
GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71
GND_72 GND_73 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114 GND_115 GND_116 GND_117 GND_118 GND_119 GND_120 GND_121 GND_122 GND_123 GND_124 GND_125 GND_126 GND_127 GND_128 GND_129 GND_130
D37 D39 G1 G4 G5 G8 G11 G14 G17 G20 G23 G26 G29 G32 G35 G38 G40 H3 H6 H9 H12 H15 H18 H21 H24 H27 H30 H33 H36 H39
GND
ASP_134603_01
GND GND
+2.5VD +2.5VD
+3.3V +3.3VD
FMC_LPC_PRSNT_M2C_L FMC_LPC_PRSNT_M2C_L
FMC_LPC_CLK_M2C_P_0 FMC_LPC_CLK_M2C_P_0
FMC_LPC_CLK_M2C_N_0 FMC_LPC_CLK_M2C_N_0
FMC_LPC_CLK_M2C_P_1 FMC_LPC_CLK_M2C_P_1
FMC_LPC_CLK_M2C_N_1 FMC_LPC_CLK_M2C_N_1
FMC_LPC_GBTCLK0_M2C_P FMC_LPC_GBTCLK0_M2C_P
FMC_LPC_GBTCLK0_M2C_N FMC_LPC_GBTCLK0_M2C_N
FMC_LPC_DP_C2M_P_0 FMC_LPC_DP_C2M_P_0
FMC_LPC_DP_C2M_N_0 FMC_LPC_DP_C2M_N_0
FMC_LPC_DP_M2C_P_0 FMC_LPC_DP_M2C_P_0
FMC_LPC_DP_M2C_N_0 FMC_LPC_DP_M2C_N_0
FMC_LPC_LA_N_00 FMC_LPC_LA_N_00
FMC_LPC_LA_N_01 FMC_LPC_LA_N_01
FMC_LPC_LA_N_02 FMC_LPC_LA_N_02
FMC_LPC_LA_N_03 FMC_LPC_LA_N_03
FMC_LPC_LA_N_04 FMC_LPC_LA_N_04
FMC_LPC_LA_N_05 FMC_LPC_LA_N_05
FMC_LPC_LA_N_06 FMC_LPC_LA_N_06
FMC_LPC_LA_N_07 FMC_LPC_LA_N_07
FMC_LPC_LA_N_08 FMC_LPC_LA_N_08
FMC_LPC_LA_N_09 FMC_LPC_LA_N_09
FMC_LPC_LA_N_10 FMC_LPC_LA_N_10
FMC_LPC_LA_N_11 FMC_LPC_LA_N_11
FMC_LPC_LA_N_12 FMC_LPC_LA_N_12
FMC_LPC_LA_N_13 FMC_LPC_LA_N_13
FMC_LPC_LA_N_14 FMC_LPC_LA_N_14
FMC_LPC_LA_N_15 FMC_LPC_LA_N_15
FMC_LPC_LA_N_16 FMC_LPC_LA_N_16
FMC_LPC_LA_N_17 FMC_LPC_LA_N_17
FMC_LPC_LA_N_18 FMC_LPC_LA_N_18
FMC_LPC_LA_N_19 FMC_LPC_LA_N_19
FMC_LPC_LA_N_20 FMC_LPC_LA_N_20
FMC_LPC_LA_N_21 FMC_LPC_LA_N_21
FMC_LPC_LA_N_22 FMC_LPC_LA_N_22
FMC_LPC_LA_N_23 FMC_LPC_LA_N_23
FMC_LPC_LA_N_24 FMC_LPC_LA_N_24
FMC_LPC_LA_N_25 FMC_LPC_LA_N_25
FMC_LPC_LA_N_26 FMC_LPC_LA_N_26
FMC_LPC_LA_N_27 FMC_LPC_LA_N_27
FMC_LPC_LA_N_28 FMC_LPC_LA_N_28
FMC_LPC_LA_N_29 FMC_LPC_LA_N_29
FMC_LPC_LA_N_30 FMC_LPC_LA_N_30
FMC_LPC_LA_N_31 FMC_LPC_LA_N_31
FMC_LPC_LA_N_32 FMC_LPC_LA_N_32
FMC_LPC_LA_N_33 FMC_LPC_LA_N_33
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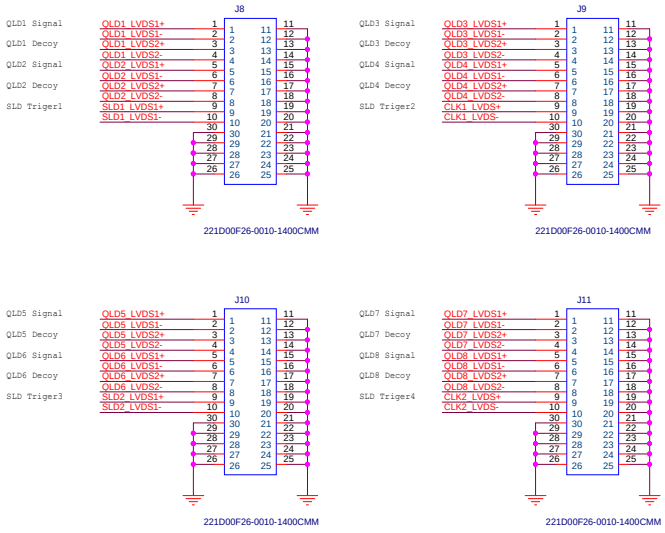
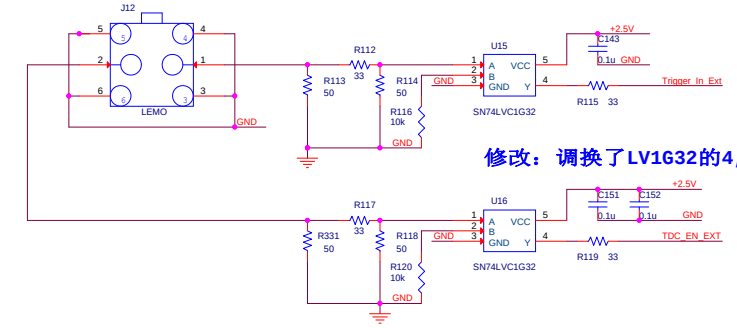
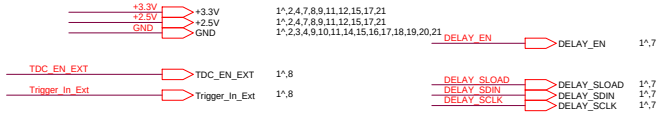
INPUT CH1-16

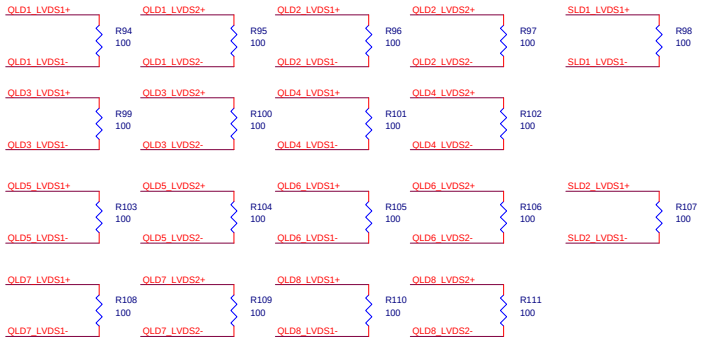


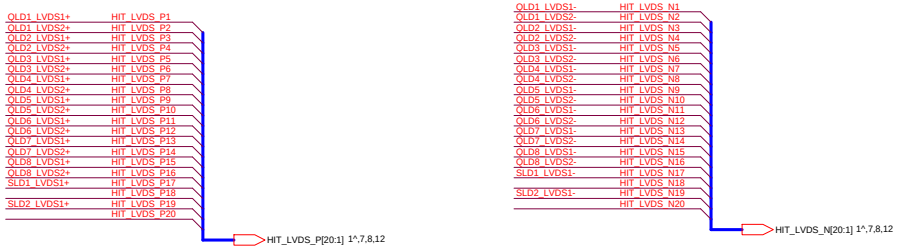


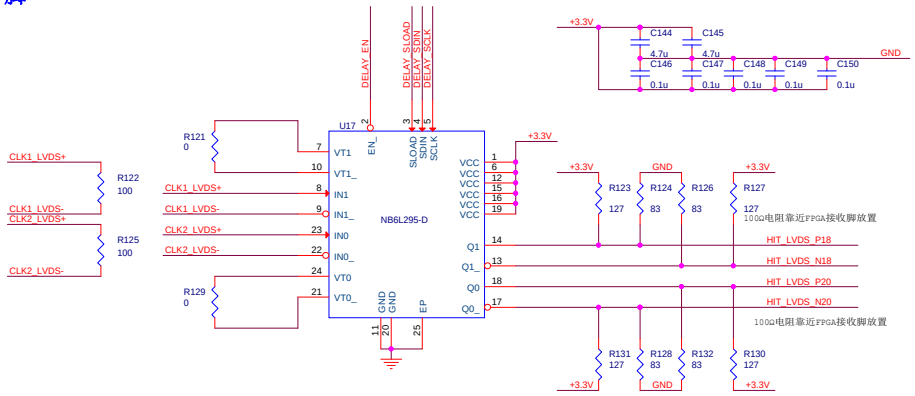
修改：调换了LV1G32的4,5管脚



100Ω电阻靠近FPGA接收脚放置







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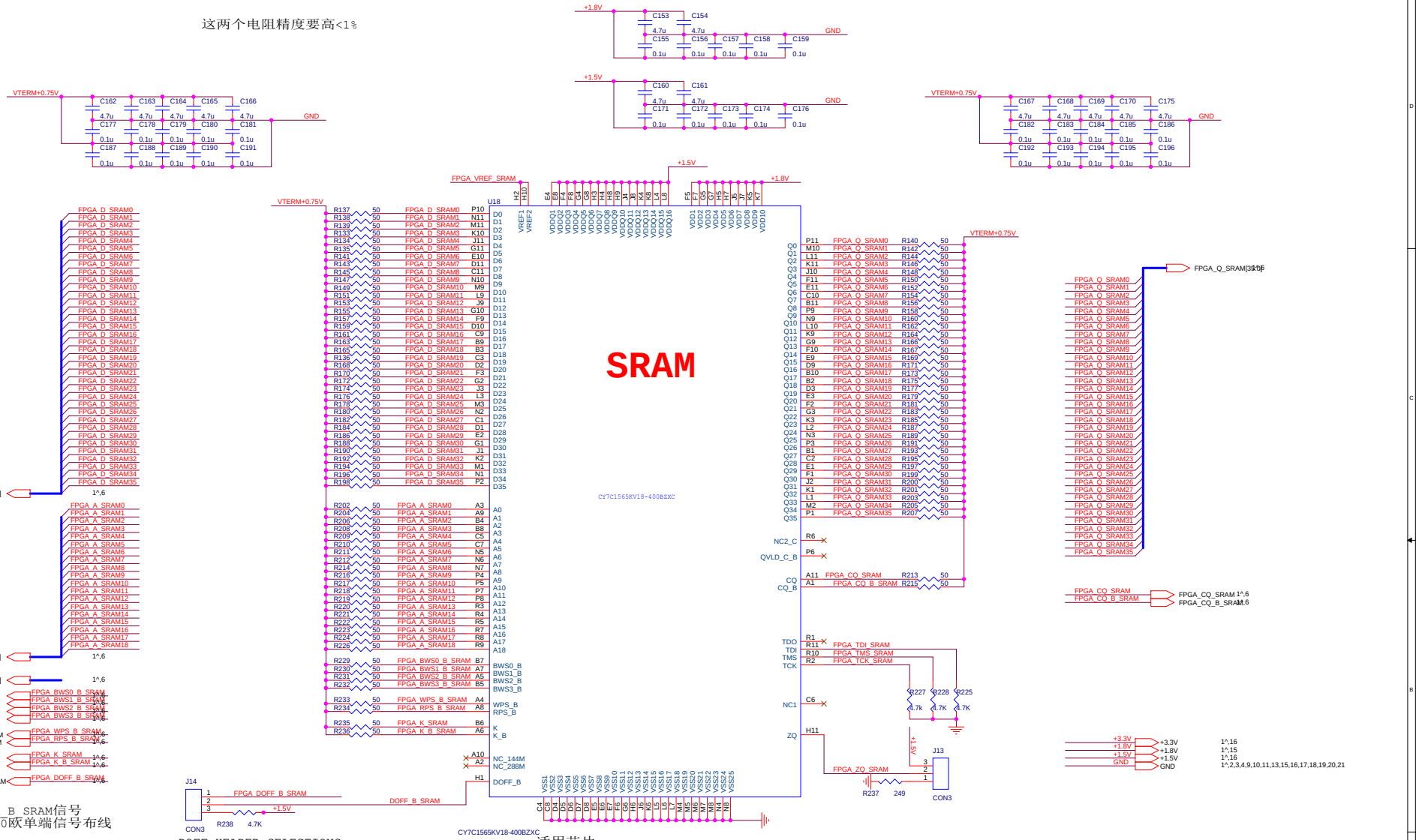
这两个电阻精度要高<1%



FPGA_K_SRAM和FPGA_K_B_SRAM信号
不做差分式布线，做50欧单端信号布线

DOFF HEADER SELECTIONS
1-2 QDR-II+ Mode - PLL ON
2-3 QDR Mode (<167MHz) - PLL OFF

适用芯片
- Cypress QDRII+ CY7C1565V18-375BZXC
- Samsung QDRII+ K7S3236U4C-EC400

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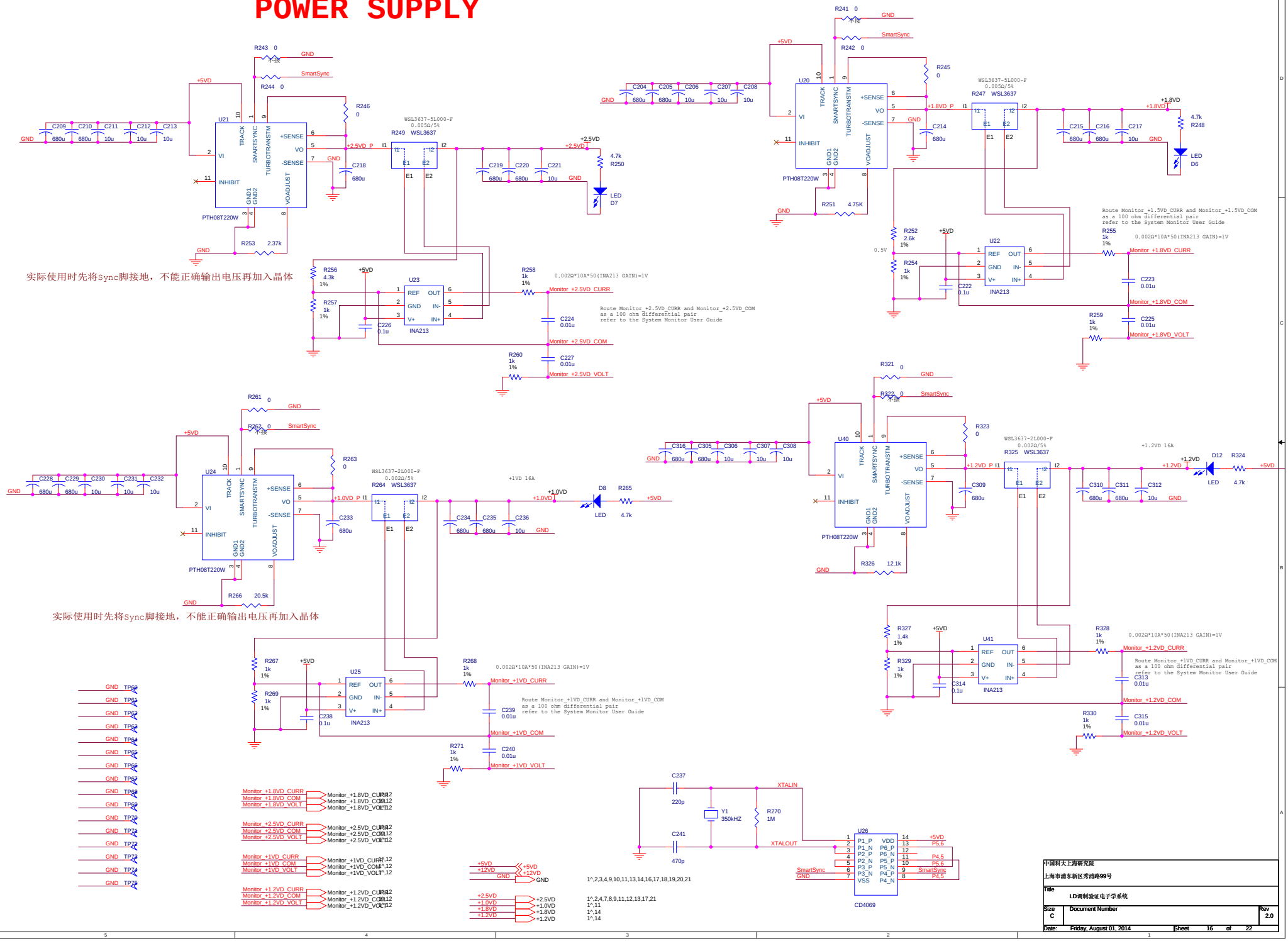
POWER SUPPLY



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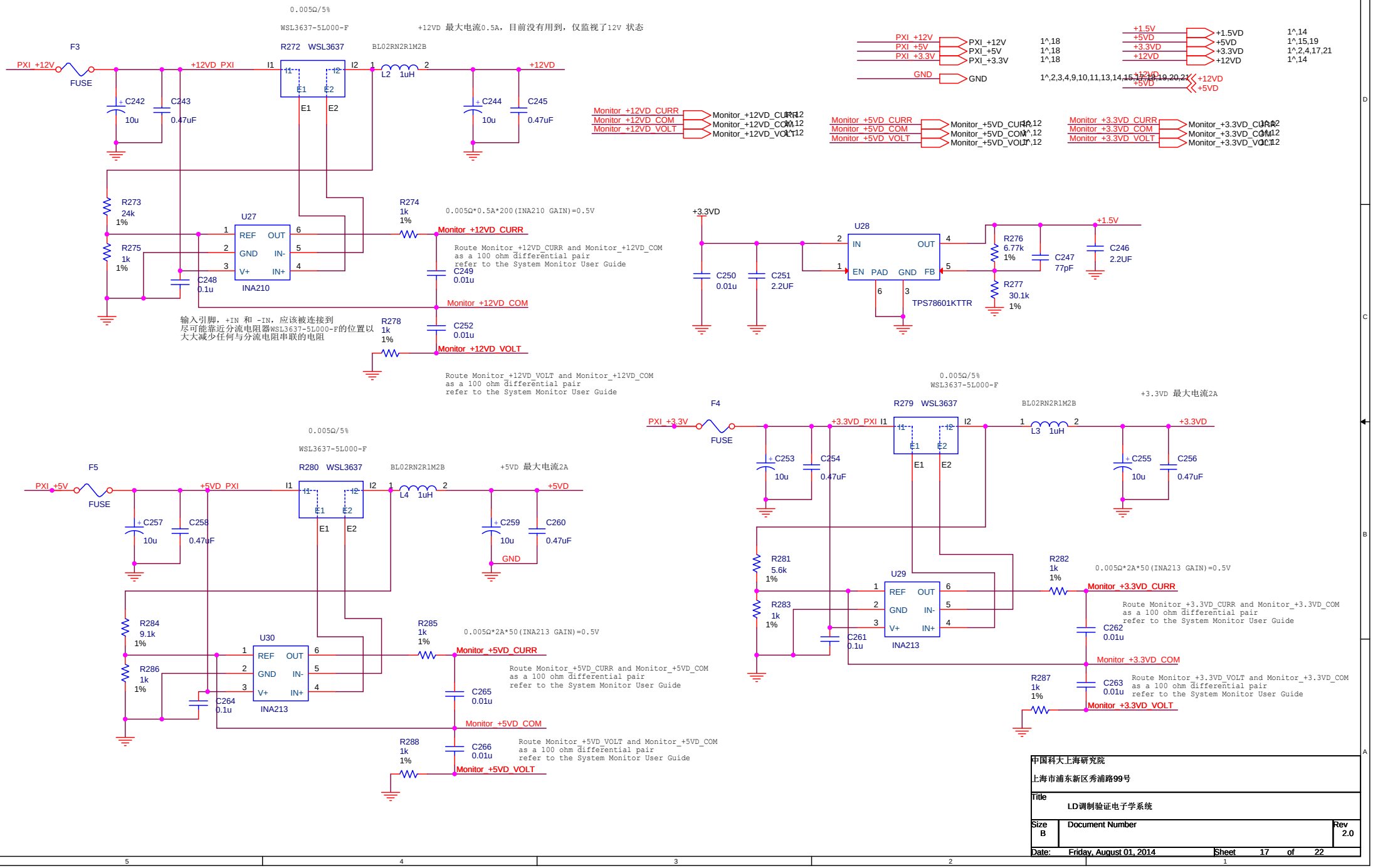
0.005Ω/5%
WSL3637-5L000-F
+12VD 最大电流0.5A，目前没有用到，仅监视了12V 状态
F3
R272 WSL3637
BL02RN2R1M2B
PXI +12V
FUSE
+12VD_PXI
I1
I2
L2 1uH
+12VD
C242 10u
C243 0.47uF
C244 10u
C245 0.47uF
E1
E2
R273 24k 1%
R275 1k 1%
U27
REF
GND
V+
OUT
IN-
IN+
INA210
C248 0.1u
R274 1k 1%
0.005Ω*0.5A*200(INA210 GAIN)=0.5V
Monitor_+12VD_CURR
C249 0.01u
Monitor_+12VD_COM
R278 1k 1%
C252 0.01u
Monitor_+12VD_VOLT
输入引脚，+IN 和 -IN，应该被连接到
尽可能靠近分流电阻器WSL3637-5L000-F的位置以
大大减少任何与分流电阻串联的电阻
Route Monitor_+12VD_CURR and Monitor_+12VD_COM
as a 100 ohm differential pair
refer to the System Monitor User Guide
Route Monitor_+12VD_VOLT and Monitor_+12VD_COM
as a 100 ohm differential pair
refer to the System Monitor User Guide
PXI +12V
PXI +5V
PXI +3.3V
GND
PXI_+12V
PXI_+5V
PXI_+3.3V
GND
1^,18
1^,18
1^,18
1^,2,3,4,9,10,11,13,14,15,17,18,19,20,21
+1.5V
+5VD
+3.3VD
+12VD
+1.5VD
+5VD
+3.3VD
+12VD
1^,14
1^,15,19
1^,2,4,17,21
1^,14
+12VD
+5VD
Monitor_+12VD_CURR
Monitor_+12VD_COM
Monitor_+12VD_VOLT
Monitor_+12VD_CURR
Monitor_+12VD_COM
Monitor_+12VD_VOLT
1^,12
1^,12
1^,12
Monitor_+5VD_CURR
Monitor_+5VD_COM
Monitor_+5VD_VOLT
Monitor_+5VD_CURR
Monitor_+5VD_COM
Monitor_+5VD_VOLT
1^,12
1^,12
1^,12
Monitor_+3.3VD_CURR
Monitor_+3.3VD_COM
Monitor_+3.3VD_VOLT
Monitor_+3.3VD_CURR
Monitor_+3.3VD_COM
Monitor_+3.3VD_VOLT
1^,12
1^,12
1^,12
+3.3VD
U28
IN
OUT
EN
PAD
GND
FB
TPS78601KTTR
C250 0.01u
C251 2.2UF
R276 6.77k 1%
R277 30.1k 1%
C247 77pF
C246 2.2UF
+1.5V
0.005Ω/5%
WSL3637-5L000-F
+3.3VD 最大电流2A
F4
R279 WSL3637
BL02RN2R1M2B
PXI +3.3V
FUSE
+3.3VD_PXI
L3 1uH
+3.3VD
C253 10u
C254 0.47uF
C255 10u
C256 0.47uF
R281 5.6k 1%
R283 1k 1%
U29
C261 0.1u
R282 1k 1%
0.005Ω*2A*50(INA213 GAIN)=0.5V
Monitor_+3.3VD_CURR
C262 0.01u
Monitor_+3.3VD_COM
R287 1k 1%
C263 0.01u
Monitor_+3.3VD_VOLT
Route Monitor_+3.3VD_CURR and Monitor_+3.3VD_COM
as a 100 ohm differential pair
refer to the System Monitor User Guide
Route Monitor_+3.3VD_VOLT and Monitor_+3.3VD_COM
as a 100 ohm differential pair
refer to the System Monitor User Guide
0.005Ω/5%
WSL3637-5L000-F
F5
R280 WSL3637
BL02RN2R1M2B
+5VD 最大电流2A
PXI +5V
FUSE
+5VD_PXI
L4 1uH
+5VD
C257 10u
C258 0.47uF
C259 10u
C260 0.47uF
GND
R284 9.1k 1%
R286 1k 1%
U30
C264 0.1u
R285 1k 1%
0.005Ω*2A*50(INA213 GAIN)=0.5V
Monitor_+5VD_CURR
C265 0.01u
Monitor_+5VD_COM
R288 1k 1%
C266 0.01u
Monitor_+5VD_VOLT
Route Monitor_+5VD_CURR and Monitor_+5VD_COM
as a 100 ohm differential pair
refer to the System Monitor User Guide
Route Monitor_+5VD_VOLT and Monitor_+5VD_COM
as a 100 ohm differential pair
refer to the System Monitor User Guide
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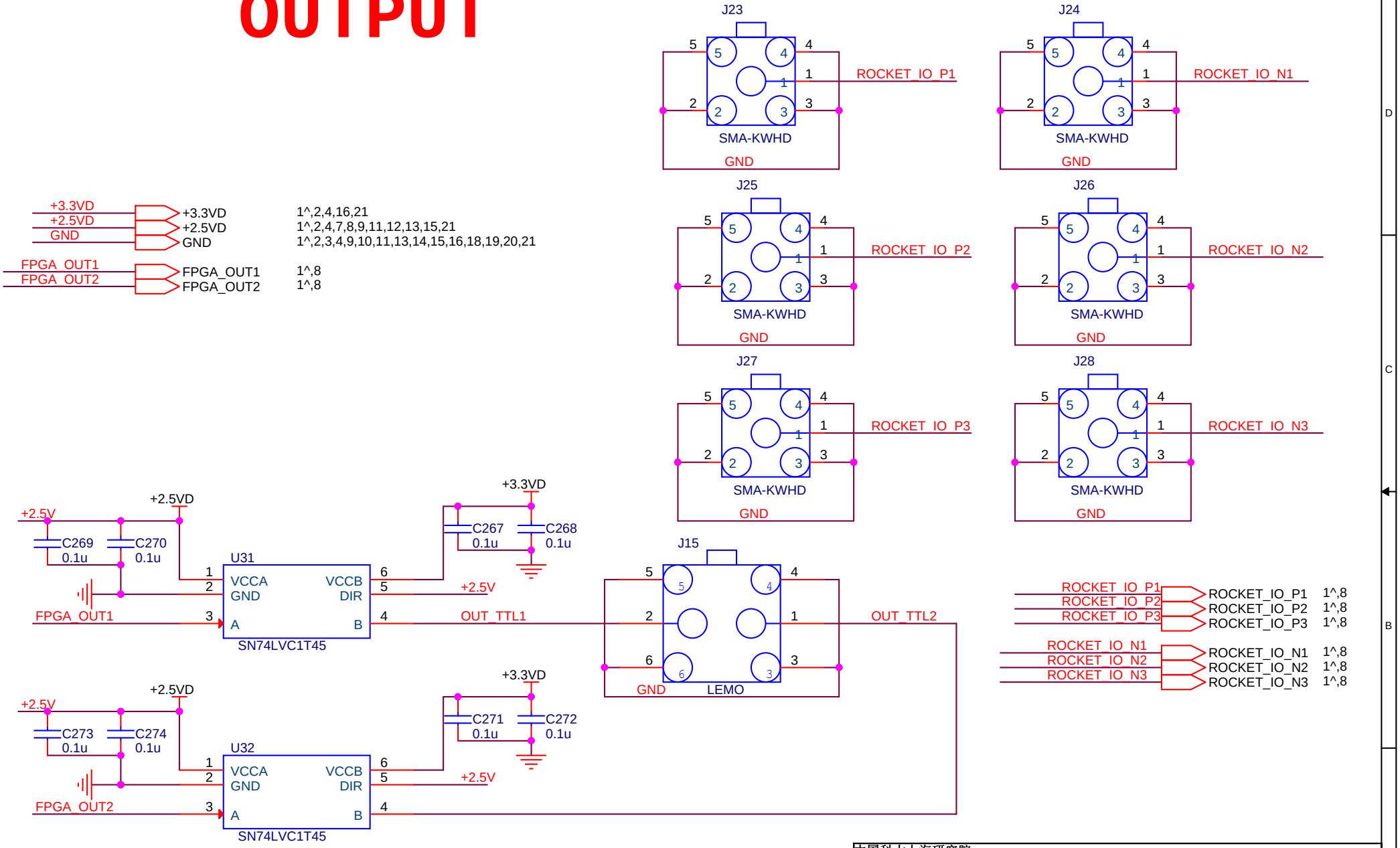
OUTPUT



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J16-1
J16-2
J16-3
J16-4
J16-5
J16-6
CON_PXI_J1
J18-1
J18-2
J18-3
J18-4
J18-5
J18-6
CON-PXI-J2
J19A
J19B
J19C
J19D
J19E
J19F
CON_PXI_J3
J20-1
J20-2
J20-3
J20-4
J20-5
J20-6
CON_PXI_J4
J17A
J17D
J17B
J17E
J17C
J17F
CON_PXI_J5
address and data pins
PXI_AD[31..0]
PXI_PAR
PXI_C/BE[3..0]
system pins
PXI_CLK
PXI_RST
Error Reporting pins
PXI_SERR
PXI_PERR
Interface Control Pins
PXI_FRAME
PXI_IRDY
PXI_TRDY
PXI_STOP
PXI_IDSEL
PXI_DEVSEL
Arbitration Pins (Bus Masters Only)
PXI_GNT
PXI_REQ
Interrupt Pins
PXI_INTA
Trigger Bus and Star Trigger
PXI_TRIG[7..0]
PXI_STAR
system reference clock
PXI_CLK10
PXI Local Bus
PXI_LBR[11..0]
PXI_LBL[11..0]
PXI_LBR12
PXI_LBL12
考虑使用+12V和-12V电源，可缓解+5V
PXI插槽
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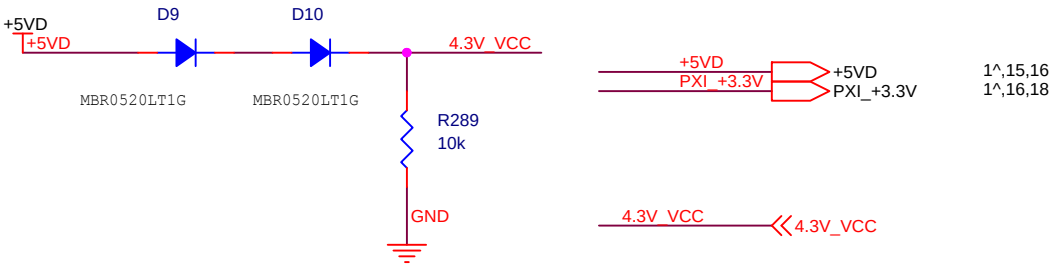
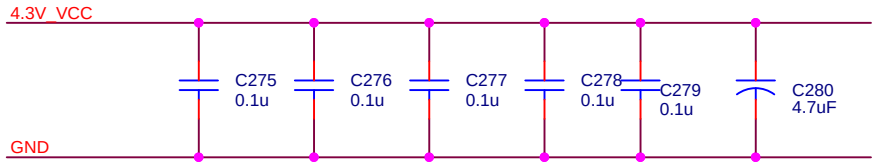
PXI POWER

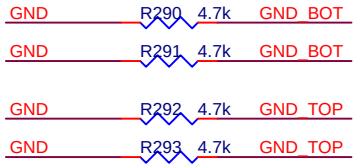
此处D9,D10封装画反。焊接时要注意有标志为正端。





机箱保护地

连到板框边缘



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电平转换

address and data pins

PXI_AD[31..0] — PXI_AD[31..0]
PXI_PAR — PXI_PAR
/PXI_C/BE[3..0] — /PXI_C/BE[3..0]

system pins

PXI_CLK — PXI_CLK
/PXI_RST — /PXI_RST

Error Reporting pins

/PXI_SERR — /PXI_SERR
/PXI_PERR — /PXI_PERR

Interface Control Pins

/PXI_FRAME — /PXI_FRAME
/PXI_IRDY — /PXI_IRDY
/PXI_TRDY — /PXI_TRDY
/PXI_STOP — /PXI_STOP
PXI_IDSEL — PXI_IDSEL
/PXI_DEVSEL — /PXI_DEVSEL

Arbitration Pins (Bus Masters Only)

/PXI_GNT — /PXI_GNT
/PXI_REQ — /PXI_REQ

Interrupt Pins

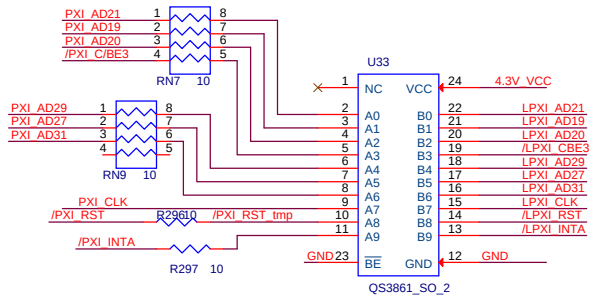
/PXI_INTA — /PXI_INTA

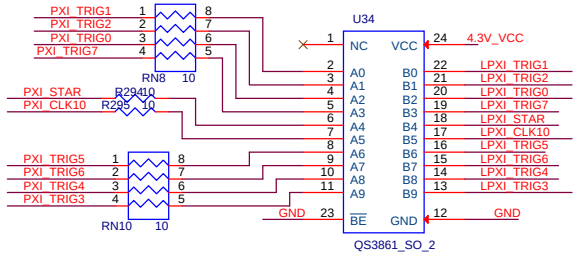
Trigger Bus and Star Trigger

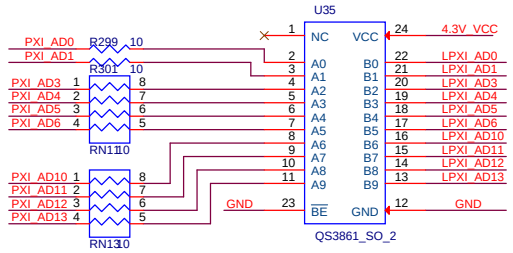
PXI_TRIG[7..0] — PXI_TRIG[7..0]
PXI_STAR — PXI_STAR

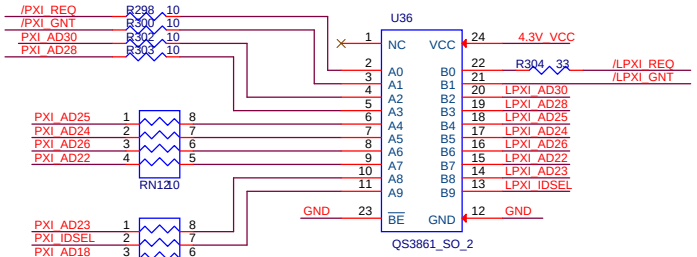
system reference clock

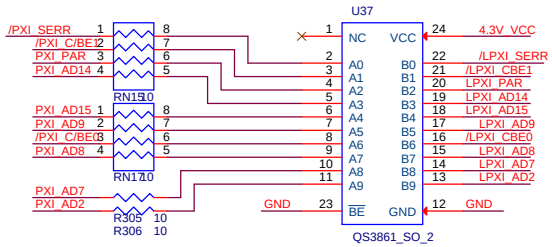
PXI_CLK10 — PXI_CLK10

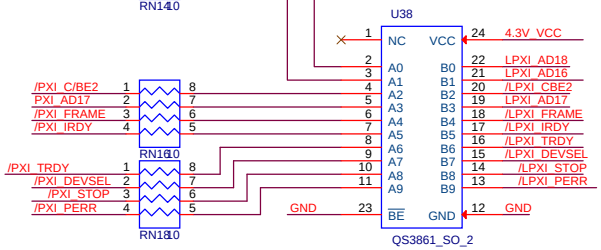












PXI Local Bus

PXI_LBR[11..0] — PXI_LBR[11..0] — PXI_LBR[11..0] — PXI_LBR[11..0] 1^,4,18
PXI_LBL[11..0] — PXI_LBL[11..0] — PXI_LBL[11..0] — PXI_LBL[11..0] 1^,4,18
PXI_LBR12 — PXI_LBR12 — PXI_LBR12 — PXI_LBR12 1^,4,18
PXI_LBL12 — PXI_LBL12 — PXI_LBL12 — PXI_LBL12 1^,4,18

GND

4.3V_VCC — 4.3V_VCC

address and data pins

LPXI_AD[31..0] — LPXI_AD[31..0] 1^,4
LPXI_PAR — LPXI_PAR 1^,4
/LPXI_CBE[3..0] — /LPXI_CBE[3..0] 1^,4

system pins

LPXI_CLK — LPXI_CLK 1^,4
/LPXI_RST — /LPXI_RST 1^,4

Error Reporting pins

/LPXI_SERR — /LPXI_SERR 1^,4
/LPXI_PERR — /LPXI_PERR 1^,4

Interface Control Pins

/LPXI_FRAME — /LPXI_FRAME 1^,4
/LPXI_IRDY — /LPXI_IRDY 1^,4
/LPXI_TRDY — /LPXI_TRDY 1^,4
/LPXI_STOP — /LPXI_STOP 1^,4
LPXI_IDSEL — LPXI_IDSEL 1^,4
/LPXI_DEVSEL — /LPXI_DEVSEL 1^,4

Arbitration Pins (Bus Masters Only)

/LPXI_GNT — /LPXI_GNT 1^,4
/LPXI_REQ — /LPXI_REQ 1^,4

Interrupt Pins

/LPXI_INTA — /LPXI_INTA 1^,4

Trigger Bus and Star Trigger

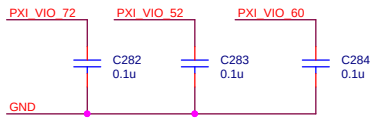
LPXI_TRIG[7..0] — LPXI_TRIG[7..0] 1^,4
LPXI_STAR — LPXI_STAR 1^,4

system reference clock

LPXI_CLK10 — LPXI_CLK10 1^,4

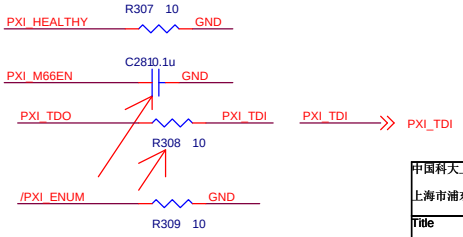
GND — GND

PXI_VIO_72 — PXI_VIO_72
PXI_VIO_52 — PXI_VIO_52
PXI_VIO_60 — PXI_VIO_60



0.1uF 或者0.01uF
线长小与250mil，线宽至少20mil

PXI_HEALTHY — PXI_HEALTHY
PXI_M66EN — PXI_M66EN
PXI_TDO — PXI_TDO
/PXI_ENUM — /PXI_ENUM



PXI_TDI — PXI_TDI

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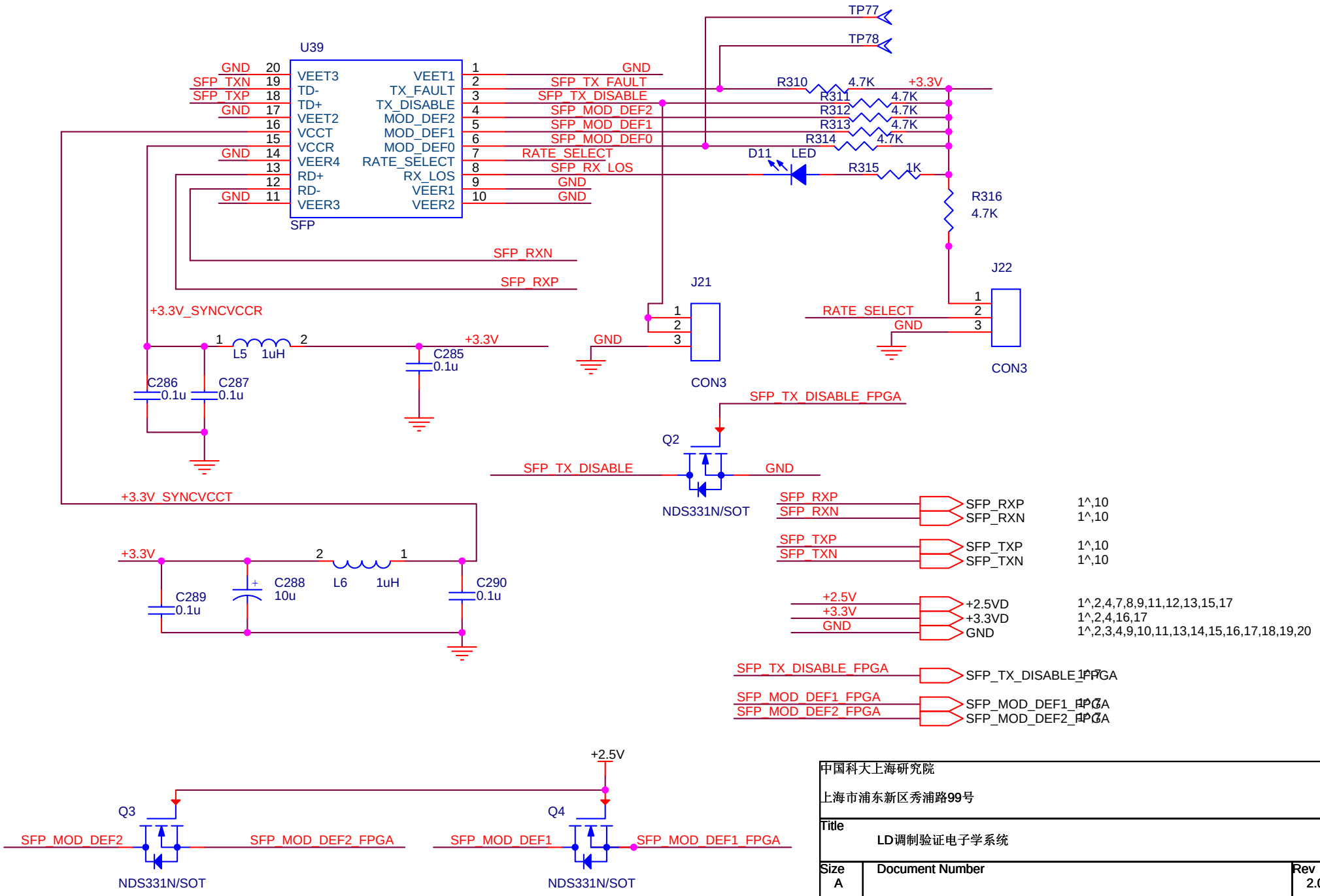
将TX_DISABLE 1K下拉j加上为4.7K上拉可选



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