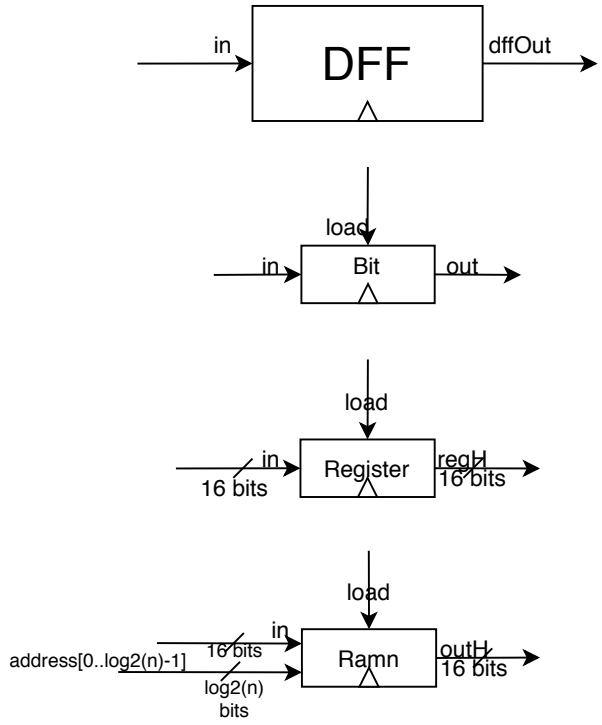
LEGEND:



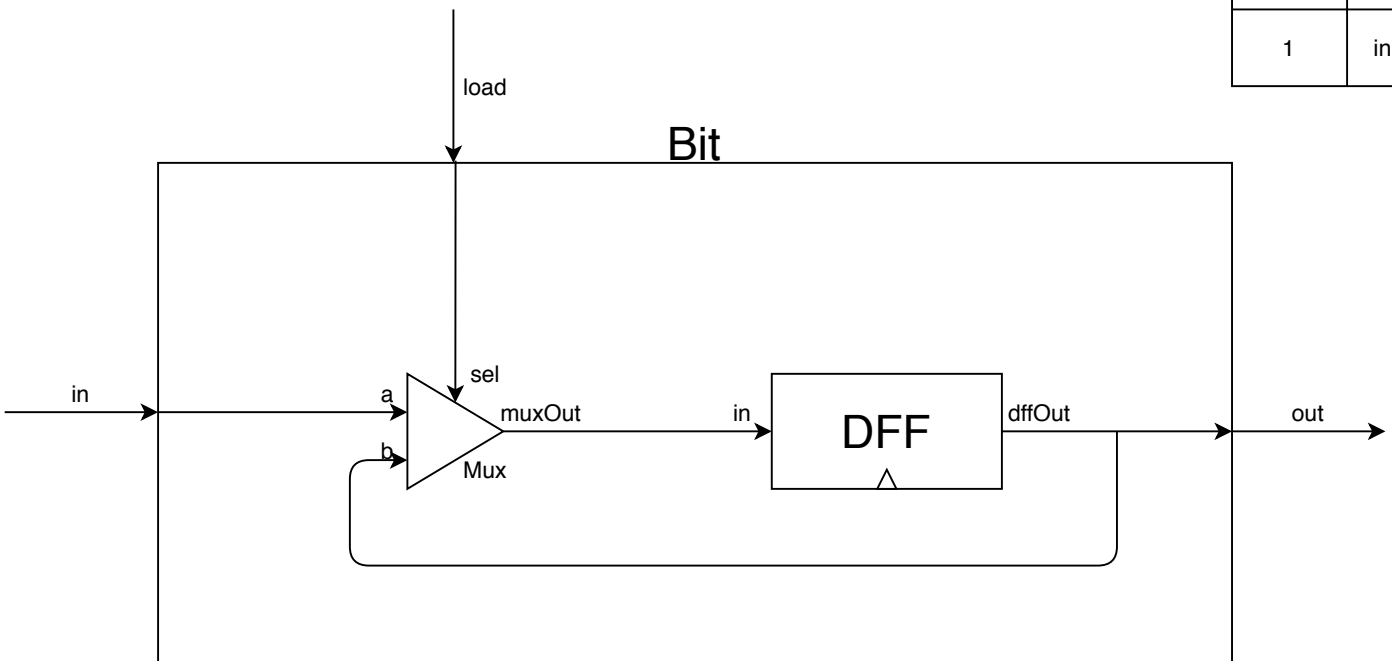
Homework #4

CS220 - Computer Architecture

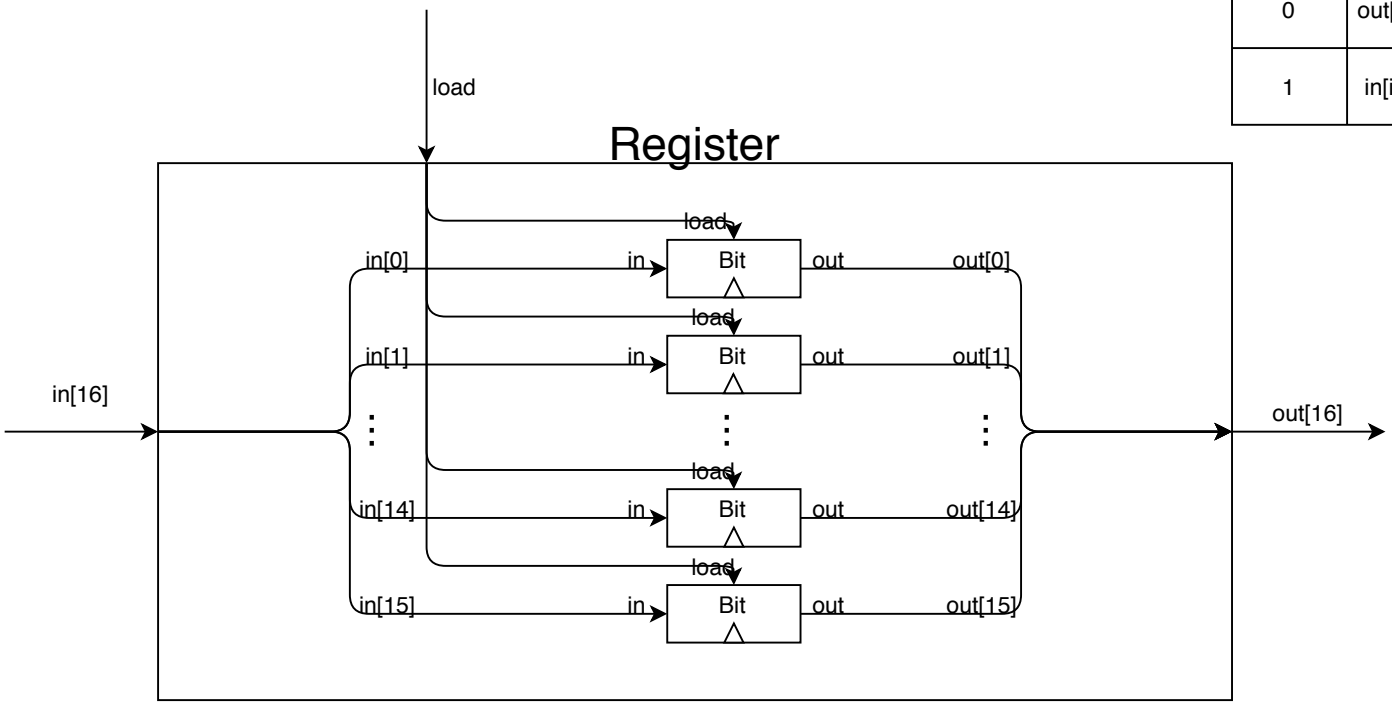
Author: Blake Dowling

Last Modified: 9/26/20

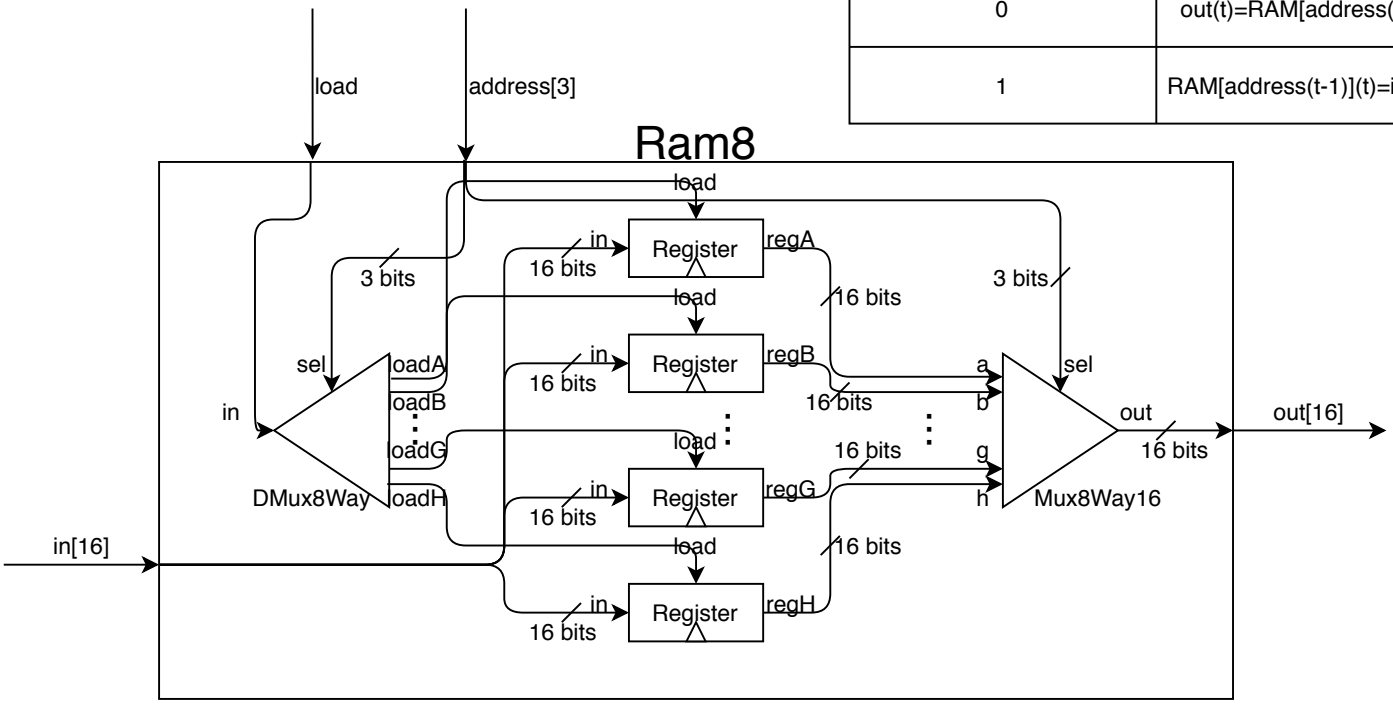
load(t-1)	out(t)
0	out(t-1)
1	in(t-1)



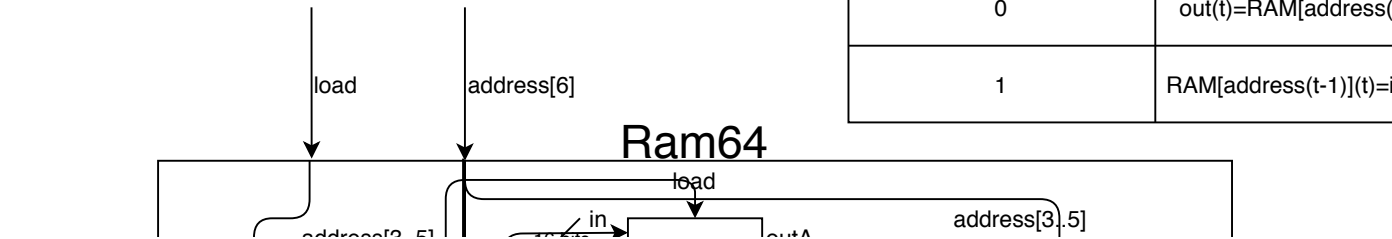
load(t-1)	out[i](t)
0	out[i](t-1)
1	in[i](t-1)

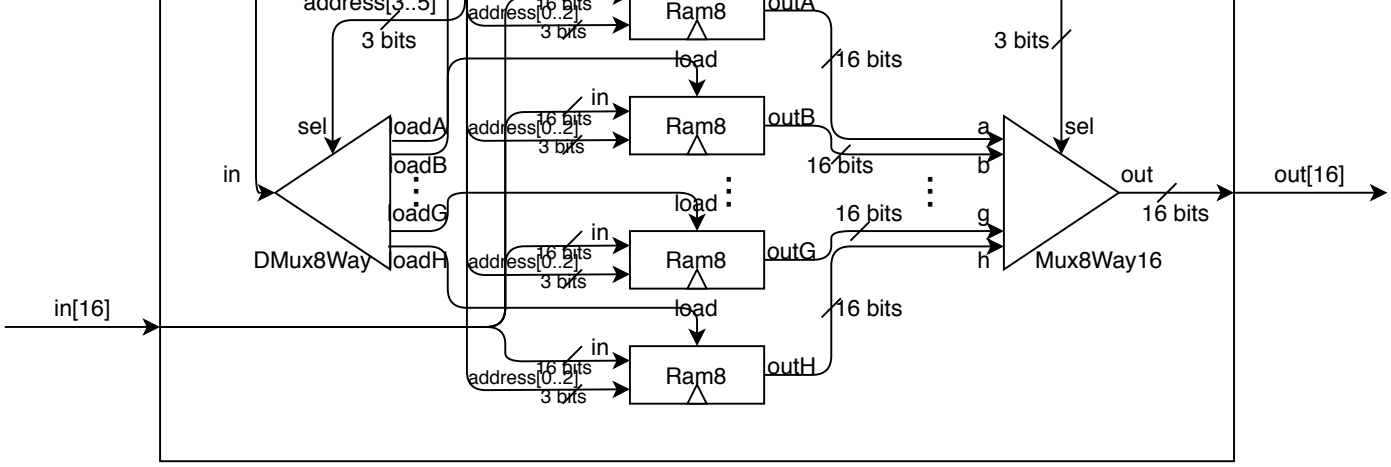


load(t-1)	
0	out(t)=RAM[address(t)](t)
1	RAM[address(t-1)](t)=in(t-1)

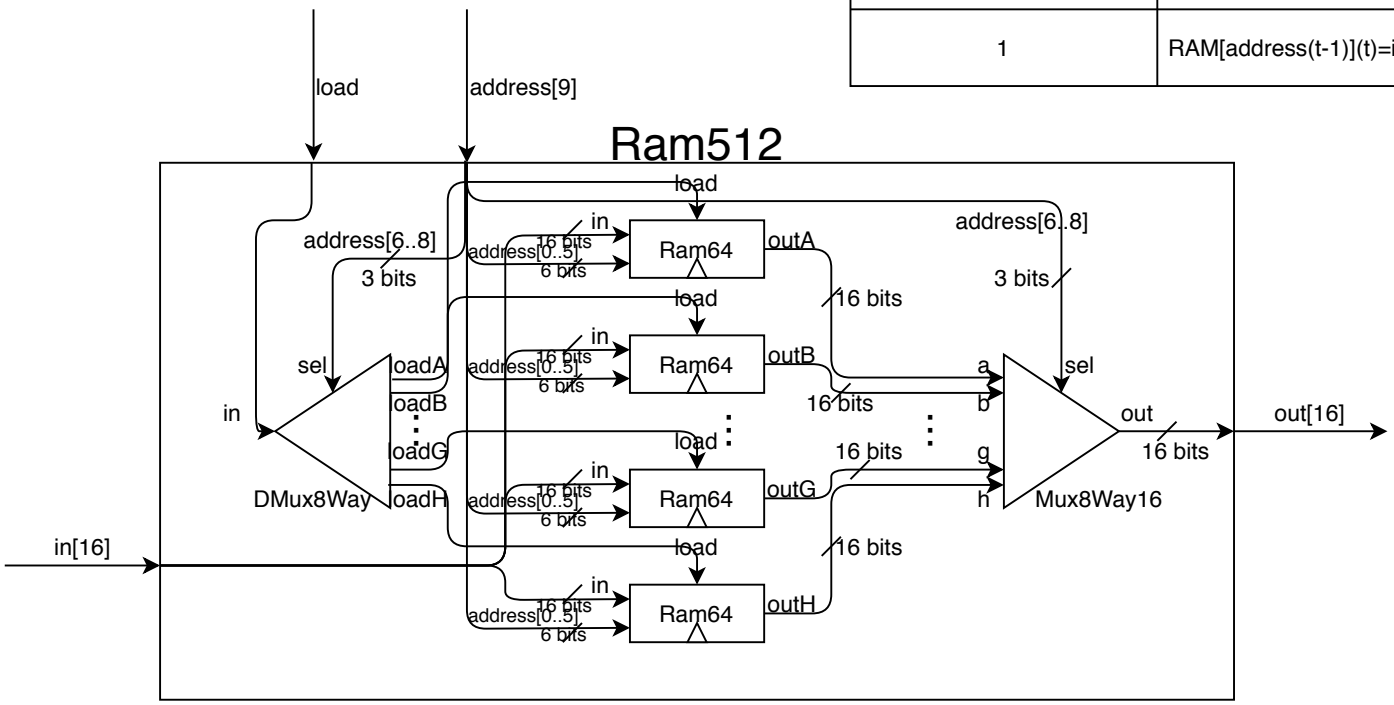


load(t-1)	
0	out(t)=RAM[address(t)](t)
1	RAM[address(t-1)](t)=in(t-1)

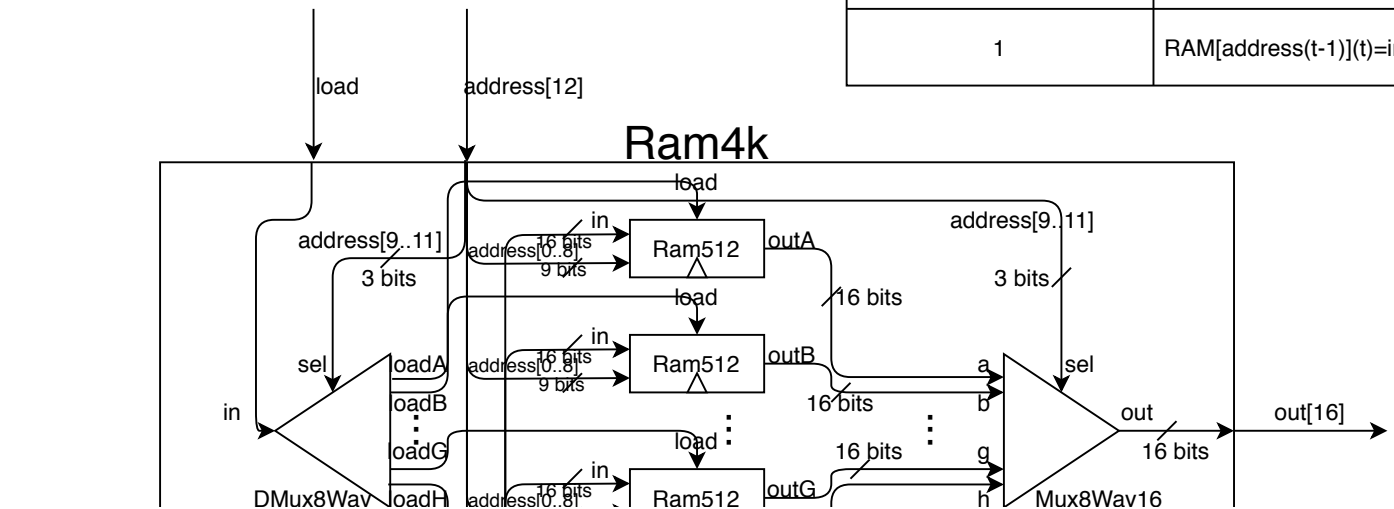


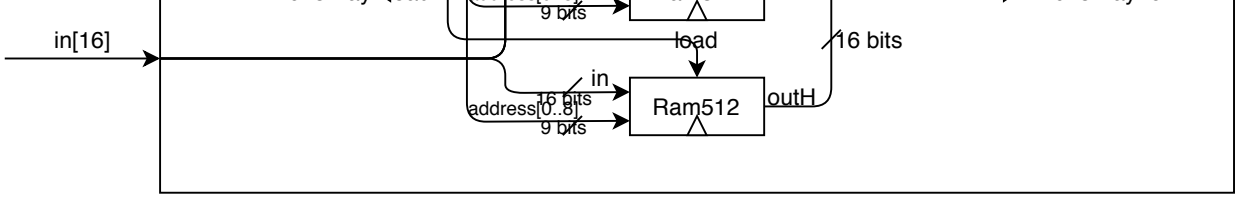


load(t-1)	
0	out(t)=RAM[address(t)](t)
1	RAM[address(t-1)](t)=in(t-1)

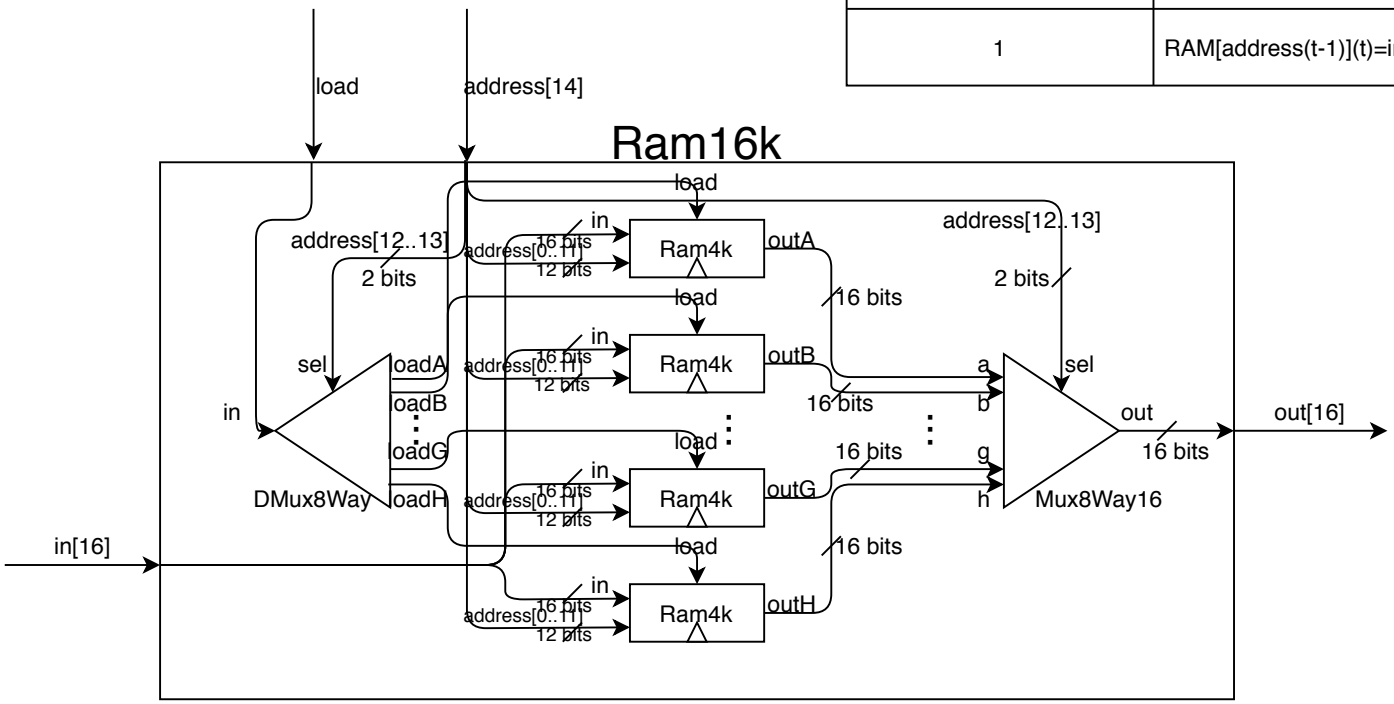


load(t-1)	
0	out(t)=RAM[address(t)](t)
1	RAM[address(t-1)](t)=in(t-1)

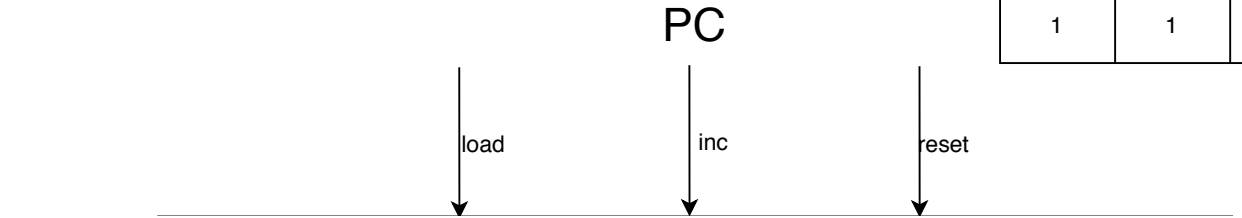


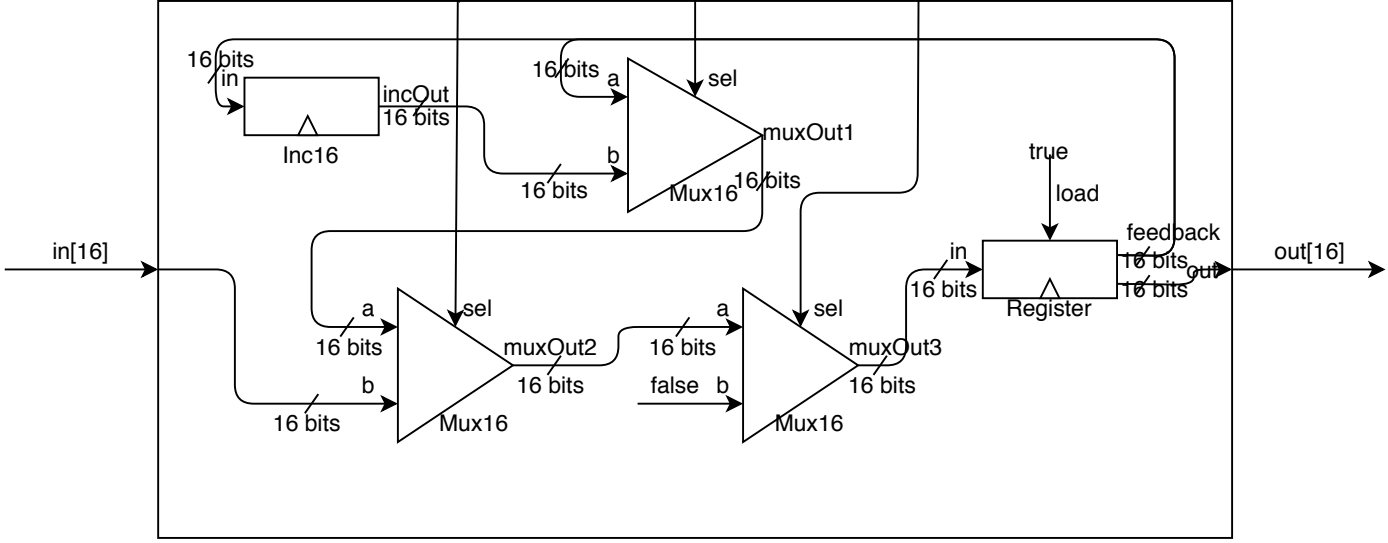


load(t-1)	
0	out(t)=RAM[address(t)](t)
1	RAM[address(t-1)](t)=in(t-1)



reset(t-1)	load(t-1)	inc(t-1)	out(t)
0	0	0	out(t-1)
0	0	1	out(t-1)+1
0	1	0	in(t-1)
0	1	1	in(t-1)
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0




16 bits
in
Inc16
incOut
16 bits
16 bits
a
sel
b
Mux16
muxOut1
16 bits
true
load
in[16]
in
feedback
16 bits
out
16 bits
Register
out[16]
a
sel
16 bits
b
16 bits
Mux16
muxOut2
16 bits
a
sel
16 bits
false
b
Mux16
muxOut3
16 bits