

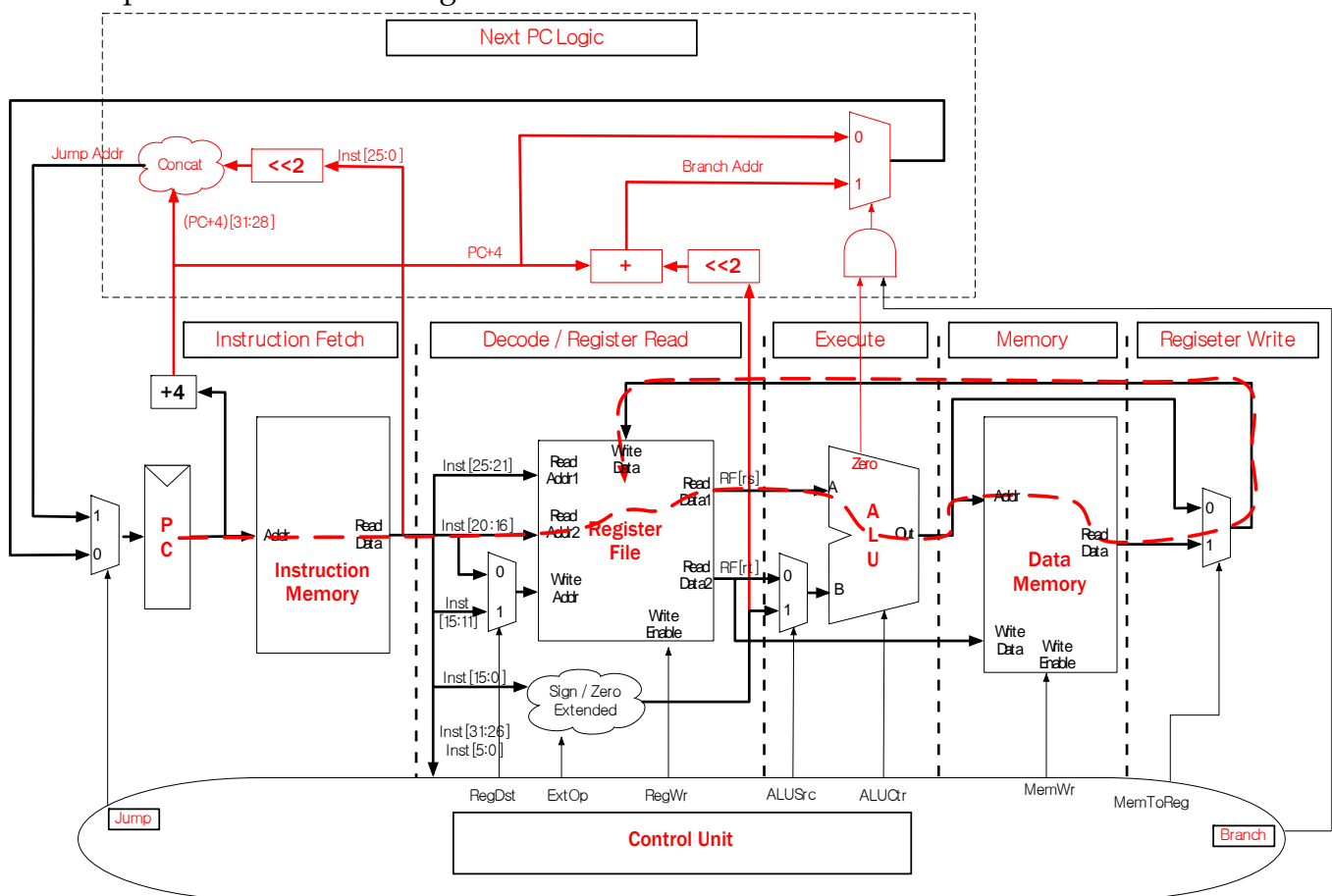
Single Cycle CPU Design

Here we have a single cycle CPU diagram. Answer the following questions:

1. Name each component.
2. Name each datapath stage and explain its functionality.

| Stage | Functionality |
|------------------------|--|
| Instruction Fetch | Send an address to the instruction memory Read the instruction (MEM[PC]) |
| Decode / Register Read | Generate the control signal values using the opcode & funct fields Read the register values with the rs & rt fields Sign / zero extend the immediate |
| Execute | Perform arithmetic / logical operations |
| Memory | Read from / write to the data memory |
| Register Write | Write back the ALU result / the memory load to the register file |

3. Provide data inputs and control signals to the next PC logic.
4. Implement the next PC logic.



Single Cycle CPU Control Logic

Fill out the values for the control signals from the previous CPU diagram.

| Instrs. | Control Signals | | | | | | | | |
|---------|-----------------|--------|--------|-------|--------|--------|-------|----------|-------|
| | Jump | Branch | RegDst | ExtOp | ALUSrc | ALUCtr | MemWr | MemtoReg | RegWr |
| add | 0 | 0 | 1 | X | 0 | 0010 | 0 | 0 | 1 |
| ori | 0 | 0 | 0 | 0 | 1 | 0001 | 0 | 0 | 1 |
| lw | 0 | 0 | 0 | 1 | 1 | 0010 | 0 | 1 | 1 |
| sw | 0 | 0 | X | 1 | 1 | 0010 | 1 | X | 0 |
| beq | 0 | 1 | X | 1 | 0 | 0110 | 0 | X | 0 |
| j | 1 | X | X | X | X | XXXX | 0 | X | 0 |

X: don't care value (either 0 or 1 is ok)

This table shows the ALUCtr values for each operation of the ALU:

| Operation | AND | OR | ADD | SUB | SLT | NOR |
|-----------|------|------|------|------|------|------|
| ALUCtr | 0000 | 0001 | 0010 | 0110 | 0111 | 1100 |

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- $t_{clk} \geq t_{clk-to-q} + t_{CL} + t_{setup}$, where t_{CL} is the critical path in the combinational logic.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers.

Single Cycle CPU Performance Analysis

The delays of circuit elements are given as follows:

| Element | Register clk-to-q | Register Setup | MUX | ALU | Mem Read | Mem Write | RegFile Read | RegFile Setup |
|-----------|-------------------|----------------|-----------|-----------|---------------|----------------|--------------|---------------|
| Parameter | $t_{clk-to-q}$ | t_{setup} | t_{mux} | t_{ALU} | $t_{MEMread}$ | $t_{MEMwrite}$ | t_{RFread} | $T_{RFsetup}$ |
| Delay(ps) | 30 | 20 | 25 | 200 | 250 | 200 | 150 | 20 |

1. What instruction exercises the critical path?

Load Word (lw)

2. What is the critical path in the single cycle CPU?

Red dashed line in the diagram

3. What are the minimum clock cycle, t_{clk} , and the maximum clock frequency, f_{clk} ?

$$t_{clk} \geq t_{PC, clk-to-q} + t_{MEMread} + t_{RFread} + t_{ALU} + t_{DMEMread} + t_{mux} + t_{RFsetup}$$

$$= 30 + 250 + 150 + 200 + 250 + 25 + 20 = 925 \text{ ps}$$

$$f_{clk} = 1/t_{clk} \leq 1/(925 \text{ ps}) = 1.08 \text{ GHz}$$

4. Why is a single cycle CPU inefficient?

Not all instructions exercise the critical path.

It is not parallelized. Each component can be active concurrently.

5. How can you improve its performance?

Pipelining: Put pipeline registers between two datapath stages. → reduce the clock time