pCT Data Acquisition Formats

This report documents the raw binary data format sent to the PC by the pCT data acquisition system (over Ethernet, although for short runs the UART path can be used instead). Note that some details will evolve over time as we gain experience with the system. As presently defined there is some redundant or unnecessary information that is included for convenience in checking and debugging the system.

Data Transfer from the Tracker pCTFE64 ASIC to the FPGA

1. 6-bit Header:

    a. Start bit (1)

    b. Packet type: 0=data

    c. 2-bit trigger tag (also identifies the event processor that was used)

    d. Error bit. If set, read the configuration register to get the error code. This includes the two buffer-control error bits, but not the parity-error bit.

    e. Parity bit (this parity calculation includes the start bit)

2. 6-bit Number of Clusters (0 to 10) (>32 clusters is not possible for the 64-channel chip, but the number is truncated to a maximum of 10). The highest order bit is set if the data list was truncated.

3. 6-bit Cluster 1, number of strips minus 1 (0 to 63)

4. 6-bit Cluster 1, address of the first strip (0 to 63)

5. 6-bit Cluster 2, number of strips minus 1 (0 to 63)

6. 6-bit Cluster 2, address of the first strip (0 to 63)

7. Etc.

This format is hard-wired into the ASIC design, so it will never change. For a typical event with no noise the length will be either 12 bits or 24 bits, easily transmitted on a 100 MHz link from the ASIC to the FPGA for a 1 MHz trigger rate.

Time-Over-Threshold Information from Calibration Events

These data packets are sent from the Tracker boards to the event builder only when calibration data are generated using the internal pulse system of the Tracker ASICs. This is for specialty work only, such as calibration noise scans, never for acquisition of image data. The bits flow into the RAM buffer almost immediately after a calibration strobe command is issued. A subsequent Read command then can be used to get the event data as well. No CRC is attached to the TOT packet. Note that the packet is designed to be structured like a normal event data packet, so that the subsequent DAQ machinery can read it out correctly to the computer by combining the data from all 12 Tracker FPGAs.

1. 6–bit Start Pattern: the receiving event builder looks for the pattern 10xxxx, where xxxx is the address of the tracker FPGA board connected to the given channel, in order to identify the start of the data stream.
    a. 1-bit start bit.
    b. 1-bit packet type (0 for data packet)
    c. 4-bit FPGA board address
2. 12-bit fixed pattern: 111111100001. This looks like an event header with the event number set to the maximum, no error, and just a single chip reporting data.
3. 12-bit fixed pattern: 010011001111. The next-to-highest-order bit differentiates this from a normal event pattern going from Tracker board to the event builder. Otherwise this looks like an ASIC header with the number of clusters equal to 3, corresponding to the following 3 12-bit words, and the chip number equal to 15.
4. 12-bit start time, giving the time elapse in clock cycles from receipt of the calibration strobe to the arrival of the earliest TReq signal.
5. 12-bit time-over-threshold, in clock cycles, of the OR of all 12 TReq signals.
6. 12-bit hit list, one bit for each chip. 0=no TReq signal was received. 1=a TReq signal was received. The TReq signal has to be at least one clock period in length to be registered, but the delay from the calibration pulse to the start of the TReq is not critical. Therefore, these data should be used for doing threshold scans, instead of the event strip data, meaning that only one channel per chip can be scanned at a time.

Data Transfer from Tracker Board FPGA to the Event Builder

This is the format used to transfer data for a single event from tracker boards to the event builder. The Tracker FPGA combines the data streams from the 12 ASICs in order to make this data packet. The cluster information is simply copied from what is sent by the ASICs, so refer to the ASIC data format above in order to decode clusters. Note that if an ASIC has no clusters for the given event, then it simply does not appear in this list. It is possible that there are zero ASICs reporting, but the FPGA must still send this data packet with the header information for every event. The cyclic redundancy code (CRC) attached to the end of the packet is checked by the event builder in order to catch hardware data transmission errors between the FPGAs over the 15-ft DVI cables.

1. 6–bit Start Pattern: the receiving event builder looks for the pattern 10xxxx, where xxxx is the address of the tracker FPGA board connected to the given channel, in order to identify the start of the data stream.
   a. 1-bit start bit.
   b. 1-bit packet type (0 for data packet)
   c. 4-bit FPGA board address
2. 12-bit FPGA Header
   a. 7-bit event tag. The two lowest-order bits are the ASIC trigger tag. The other 5 bits are from the clock counter running in the tracker-board FPGA. The counters are synched at 0 when a reset/synch signal is received by the FPGA.
   b. 1-bit error flag (set in case of a trigger tag mismatch)
   c. 4-bit number of chips reporting cluster data
3. 12-bit ASIC Header (repeated, following the cluster information, if multiple chips are reporting)
   a. 1-bit cluster overflow
   b. Unused bit, set to 0 to differentiate this from a TOT packet
   c. 4-bit number of clusters
   d. Chip error bit
   e. Parity error bit
   f. 4-bit chip address
4. 12-bit Cluster: 12 bits as reported by the ASIC (repeated once for each cluster)
5. Next cluster from the same ASIC, if there is one, etc.
6. Next ASIC header, if there is another one reporting data, etc.
7. 6-bit Trailing CRC

For a "typical" event with 1 track cluster in a layer, this would be 48 bits, or 48 Mbit/s. Or in the worst case, with an additional noise hit per layer in a different ASIC, 72 Mbit/s.

(For register read-back, which only goes via UART, not Ethernet, the same 6-bit start pattern is followed by the 72-bit stream from the chip (6-bit header, 64 bits of register information, and two 1 bits). There is no trailing CRC. Note that only a single chip is allowed to read back register information at one time. While the chips do accept the wildcard address "11111" for all commands, the FPGA program on the readout board does not allow that address to be used for register read-back, to avoid the complications of having to merge the multiple streams.)

The fact that chips without clusters are suppressed in the readout, to preserve bandwidth, may complicate debugging, but we can insert monitoring code in the front-end board FPGA to verify that headers are being received by the tracker board FPGA from all chips for every trigger.

At the receiving end, the event builder has to find an integral packet made up with the correct 6-bit start code, and after clocking in the specified headers and number of clusters, a 6-bit CRC that matches the data. A corrupt transmission from any tracker board will require a reset of the system, accomplished by stopping the trigger and sending a reset/sych signal that resets all of the DAQ counters and buffers. Similarly, there must be a packet from every front-end FPGA, all with matching event tags. If the event

builder receives an event on at least one transmission line but fails to find a matching packet on another, then it stops looking after a specified number of clock cycles and resets everything, to avoid having a hung DAQ.

Data Transmission from the Energy Detector Digitizer Board FPGA to the Event Builder

This packet is sent for every event by each of the two energy detector digitizer board FPGAs. The first FPGA will read the first 3 scintillators, while the second will read only two scintillators. There are two data formats, selected by the user. The normal format is for data reduced in the digitizer board FPGA by adding together all of the samples in each pulse (after subtracting the pedestal). The other format sends the raw digitizations from the 14-bit ADCs for each of up to 16 time samples per channel per event. That format is to be used for debugging and calibration. All of the pedestal and pulse-height information is signed, in 2's complement format.

[1] 6–bit Start Pattern: the receiving event builder looks for the pattern 10xxxx, where xxxx is the address of the tracker FPGA board connected to the given channel, in order to identify the start of the data stream.
    a. 1-bit start bit.
    b. 1-bit packet type (0 for data packet)
    c. 4-bit FPGA board address
[2] 12-bit header
    a. 2-additional bits in the trigger tag for unreduced data or
        i. 1-bit flag = 1 if pedestals are included, 0 if not
        ii. 1 additional bit in the trigger tag
    b. 3-bit tag for the front-end buffer
    c. Data type: 0=samples, 1=reduced
    d. 1-bit error flag. Set if there is a command parity error, a timeout waiting for an event, a trigger error, or a trigger received when not ready.
    e. 5 bits, number of samples for each channel, or Nch,OTR2,OTR1,OTR0 if reduced data, where Nch is 2 bits for the number of channels to write out.
[3] 48-bit data slice in case that samples are read out, followed by the remaining data slices
    a. 3-bit sample count (this wraps around if the number of samples is greater than 7)
    b. 3 15-bit digitizations (each is 14 bits plus MSB=overflow indicator)
[4] 16 or 24-bit channel data reduced (normally 3 of these for the first board; or 2 for the second board)
    a. 8-bit signed pedestal, if pedestal output is specified
    b. 16-bit signed sum of the samples
[5] 4 unused bits IF reduced data AND no pedestals written out AND only 2 channels, to fill out an integer number of 12-bit words.
[6] 6-bit CRC

The number of bits is 6+12+3*24+6=96 (or 84 for the board with 2 channels). This is marginal for our goal of a >1 MHz event rate at 100 Mbit/s data transmission. But after some experience we could eliminate the 8-bit pedestals. That would reduce the number of bits down to 72 (68). Note that in the case of reduced data the system already sends the time difference for only the second energy digitizer board (the one with 2 channels read out), so eliminating it would not help.

Data Transmission from the Event Builder to the Computer

The data stream begins with a run header, as follows:

- 24-bit identifier
  - o Byte 1: 52
  - o Byte 2: 55
  - o Byte 3: 4E
  - o = 1101 0010 0101 0101 0100 1110 = "1RUN" in standard ASCII
- 24-bit run number
- 32-bit run start time, floating point single precision, in seconds
- 7 status bits, currently set to zero
- Status bit, set if event time tags are written out
- 8-bit program version number

The Xilinx ML605 event builder is programmed to put complete events together, so it expects for each event to receive a contribution from all 14 front-end FPGAs (unless a specific mask register is loaded telling it that some boards are not connected). For the most part it builds an event by making a header and then copying the data sent from the front-end FPGAs. So the formats listed above for transmission of data to the event builder should be consulted.

- 24-bit beginning-of-event identifier, used at least temporarily for searching for start-of-events. Once we are confident that the data format doesn't get corrupted, then this can be eliminated.
  - o Byte 1: F0
  - o Byte 2: 43
  - o Byte 3: 54
  - o = 1111 0000 0100 0011 0101 0100 = "1pCT" in standard ASCII
- 36-bit event time tag, in clock cycles
- 12-bit time since the previous trigger, in clock cycles
- 24-bit Event header
  - o Start bits "10"
  - o Four bits error flags:
    - Incorrect FPGA address received
    - Tag mismatch error
    - CRC error
    - TBD

- - 18-bit event number
- 12-bit First Tracker FPGA header
    - 4-bit FPGA address (this is the only difference from the header sent from the Tracker board)
    - 3-bit event tag. The two lowest-order bits are the ASIC trigger tag. The other bit is from the clock counter running in the tracker-board FPGA.
    - 1-bit error flag (set in case of a trigger tag mismatch)
    - 4-bit number of chips reporting cluster data
- First FPGA ASIC hit list
- Repeat for remaining 11 Tracker FPGAs (at least a header is present for all FPGAs, even if no hits)
- Similarly for the energy detector data from the first digitizer board (3 channels), for which the data are identical to what was sent from the digitizer board to the event builder.
- Similarly for the energy detector data from the second digitizer board (2 channels), for which the data are identical to what was sent from the digitizer board to the event builder.

The number of bits would be, using 44 bits per tracker FPGA and 12 FPGAs (2 per T layer), plus two energy detector boards, one with 96 bits and the other with 72 bits: 24+12*12+12*44+96+72=864 bits. For a 1 MHz trigger rate this will exceed the ZestET1 Ethernet capability, but by only 8%. We can eventually reduce it by combining information from the two halves of the T boards and eliminating unnecessary energy detector information.

Here is an example event stream from the beginning of a short cosmic-ray run taken with a single Tracker V layer and all 5 energy detector channels, with the system set to write out the unreduced samples. I parsed it by hand to illustrate the binary format.

IIIIOOOOOIOOOOIIOIOIOIOO   "IpCT" start-of-event identifier

IO OOOO OOOOOOOOOOOOOOOOOO   Event header, event 0

OOOO OOO O OOOI   Header for FPGA-0 (V board), 1 chip reporting

O O OOOI O O OOII   Chip header, 1 cluster, chip 3

OOOOOO OOIIIO   Cluster, 1 strip, first strip=14

OOOI OOO O OOOO   Empty header for FPGA-1 (not attached)

OOIO OOO O OOOO   Empty header for FPGA-2 (not attached)

OOII OOO O OOOO   Empty header for FPGA-3 (not attached)

OIOO OOO O OOOO   Empty header for FPGA-4 (not attached)

OIOI OOO O OOOO   Empty header for FPGA-5 (not attached)

OIIO OOO O OOOO   Empty header for FPGA-6 (not attached)

OIII OOO O OOOO   Empty header for FPGA-7 (not attached)

IOOO OOO O OOOO   Empty header for FPGA-8 (not attached)

IOOI OOO O OOOO   Empty header for FPGA-9 (not attached)

IOIO OOO O OOOO   Empty header for FPGA-10 (not attached)

IOII OOO O OOOO   Empty header for FPGA-11 (not attached)

OOO OO O O IOOOO   FPGA-12 header (energy board), 16 samples per channel

OOIOOOIOOIIO   Time since previous trigger = 550 clock cycles

OOI O IIIIIIIIIOIOOI O IIIIIIIIOIIOOI O IIIIIIOOIOOIOO Samples 1: -23   -39   -220 no overflows

OIO O IIIIIIIIIOIOIO O IIIIIIIIOIIOOO O IIIIIIOOIOOOII Samples 2: -22   -40   -221 no overflows

OII O IIIIIIIIIOIOII O IIIIIIIIIIOIII O IIIIIIOIOOOIOI Samples 3: -21   -9   -187 no overflows

IOO O OOOOOOIOOOOIII O OOOOIOIIOOIIIO O OOOOOIOOIIOIOI Samples 4: 135   718   309 no overflows

IOI O OOOOIOOIIIIIOO O OOOIOIOIIIIIOO O OOOOIOIOIIOOII Samples 5: 636   1404   691 no overflows

IIO O OOOOIOIIIOIOIO O OOOIOOIIIOIOOI O OOOOIOOIOIOOOI Samples 6: 746   1257   593 no overflows

III O OOOOIOOOIIIOOO O OOOOIIOIOIIOOI O OOOOOIOIOIIOOO Samples 7: 568   857   344 no overflows

OOO O OOOOOIOIIIOOOO O OOOOIOOOOOOOOO O OOOOOOIOOOOIIO Samples 8: 368   512   134 no overflows

001 0 00000011011001 0 00000100010111 0 111111111111001 *Samples 9: 217   279   -7 no overflows*

010 0 00000001110101 0 00000010001111 0 111111100111111 *Samples 10: 117   143   -97 no overflows*

011 0 00000000111100 0 00000001000100 0 111111011011100 *Samples 11: 60   68   -146 no overflows*

100 0 00000000011010 0 00000000011000 0 111111010100000 *Samples 12: 26   24   -176 no overflows*

101 0 00000000000110 0 00000000000000 0 111111001111101 *Samples 13: 6   0   -195 no overflows*

110 0 11111111111110 0 11111111110011 0 111111001101000 *Samples 14: -2   -13   -204 no overflows*

111 0 11111111101110 0 11111111101010 0 111111000101111 *Samples 15: -10   -22   -209 no overflows*

000 0 11111111010100 0 11111111001010 1 111111001011101 *Samples 16: -12   -27   -211 no overflows*

000 00 0 0 10000   *FPGA-12 header (energy board), 16 samples per channel*

001000100110   *Time since previous trigger = 550 clock cycles*

001 0 11100011100110 0 00000000111001 0 111101001011100   -1818   57 -724

010 0 11100011101010 0 00000000111011 0 111101001010010   -1814   59 -726

011 0 11100011101110 0 00000001000110 0 111101001010001   -1810   70 -727

100 0 11101000000101 0 00000111011010 0 111101001010000   -1531   474 -728

101 0 11101101101001 0 00001111010000 0 111101001010001   -1175   976 -727

110 0 11101101000010 0 00001110100100 0 111101001010001   -1214   932 -727

111 0 11101010001111 0 00001010101011 0 111101001010000   -1393   683 -728

000 0 11100111101110 0 00000111000100 0 111101001010001   -1554   452 -727

001 0 11100110000100 0 00000100100010 0 111101001010011   -1660   290 -725

010 0 11100101000110 0 00000011000001 0 111101001010010   -1722   193 -726

011 0 11100100011111 0 00000010001001 0 111101001010011   -1761   137 -725

100 0 11100100000111 0 00000011001111 0 111101001010011   -1785   103 -725

101 0 11100011111010 0 00000001010110 0 111101001010010   -1798   86 -726

110 0 11100011110011 0 00000010011101 0 111101001010001   -1805   77 -727

111 0 11100011110001 0 00000001001000 0 111101001010010   -1807   72 -726

000 0 11100011101011 0 00000001000011 0 111101001010001   -1813   67 -727

1111000001000011010100   *"1pCT" start-of-event identifier*

10 0000 000000000000000001   *Event header, event 1*

0000 001 0 0001	*Header FPGA-0, trigger tag 1, 1 chip reporting*
0 0 0010 0 0 0100	*Chip header, 2 clusters, chip 4*
000000 111100	*First cluster, 1 strip, starting at strip 60*
000000 100100	*Second cluster, 1 strip, starting at strip 36*
0001 00100000	*FPGA-1 empty*
0010 00100000	*FPGA-2 empty*
etc. etc.	