LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8619C

HDMI to TTL/LVDS Converter

Datasheet

1. Features

- **HDMI/Dual-mode DP Input Interface**
  - Compliance with DVI V1.0 and HDMI V1.4
  - Support up to 1.65Gbps for DVI
  - Support up to 3.4Gbps for HDMI
  - Support resolution up to 4Kx2K@30Hz for HDMI
  - Support 8/10/12 bit per component (bpc)
  - Support CEC
  - Support HDCP decryption
  - Support On-chip EDID
  - Receiver side equalization up to 25 dB
- **LVDS Output Interface**
  - Compatible with VESA and JEIDA standard
  - 1~2 configurable port
  - Support port swapping
  - Support maximum data rate 1.5Gb/s/lane
  - Resolution up to 4Kx2K@30Hz
  - Supports 6-bit, 8-bit output
- **TTL Output Interface**
  - Support up to 24-bit RGB or BT656/BT1120 output
  - Support both SDR and DDR output
  - Support up to 148.5MHz DDR or 300MHz SDR clock output
  - Support both 1.8V and 3.3V output voltage level
- **Video and Audio Processing**
  - Programmable color space conversion
  - Advanced dithering logic for 6-bit color depth output
  - Optional SPDIF output and 8-channel I2S output
- **Miscellaneous**
  - Support 100KHz and 400KHz I2C slave
  - External 25MHz Crystal Reference Clock
  - Temperature Range: -40°C to +85°C
  - Packaged in QFN76 9mm x 9mm

2. General Description

The Lontium's LT8619C is a high performance HDMI/Dual-mode DP receiver chip based on ClearEdge™ Technology, compliant with the HDMI 1.4 specification. The TTL output can support RGB, BT656, BT1120 and the output resolution can support up to 4Kx2K@30Hz resolution.

For easy implement of a multi-media system, LT8619C supports 8-channel high quality I2S audio or SPDIF audio output.

3. Applications

- Car Entertainment
- TV
- Monitor
- Pico Projector
- Smart Projector
- Etc.

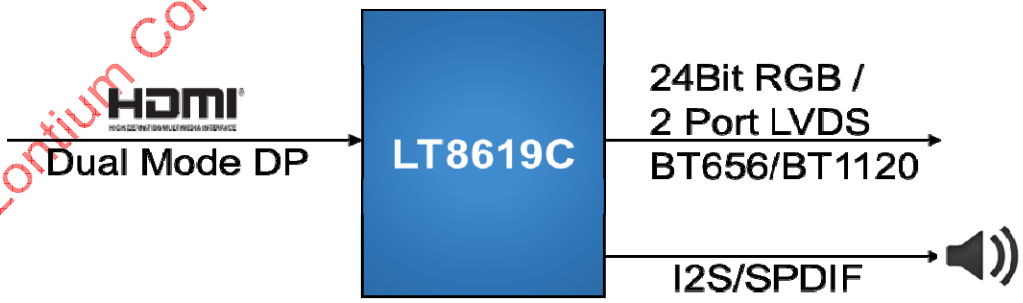

Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8619C	-40° C to +85° C	QFN76(9*9)	Tray

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5. Revision History

Version	Owner	Content	Date
Preliminary	Y S	Initial Release	08/02/2016
R1.1	N W	Update package information	08/08/2016
R1.2	DS R	Modify TTL output pin mapping and block diagram	08/08/2016
R1.3	Bruce Y	Update power consumption data.	03/10/2017
R1.4		Modify the format of the document	04/27/2017

6. Pinning Information

6.1 Pin Configuration

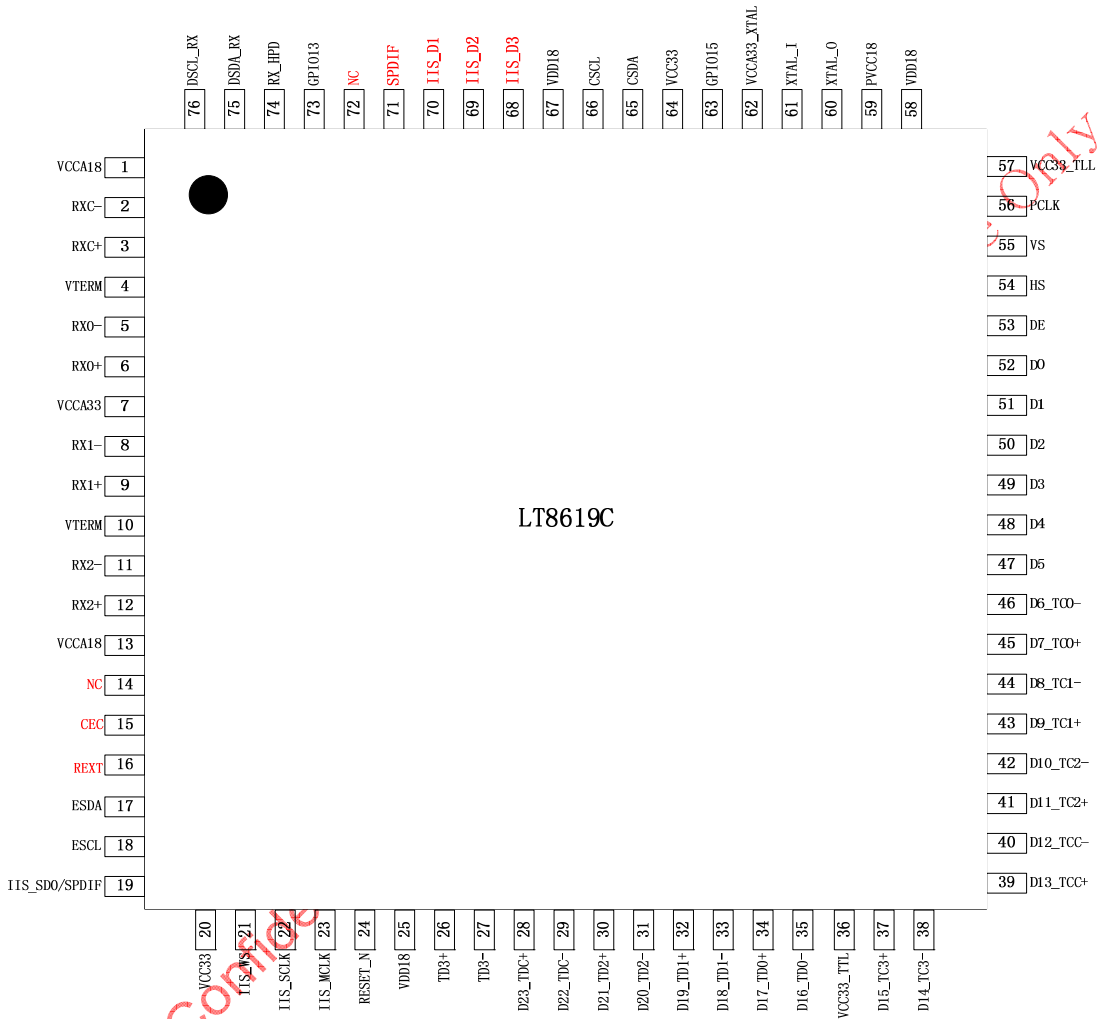


Figure 6.1.1 QFN76 Pin Assignment (Top View)

6.2 Pin Description

(I/O description: A=Analog, I=Input, O=Output, P=Power, G=Ground)

Table 6.2.1 Pin Description

PIN	NAME	I/O	FUNCTION	NOTES
1	VCCA18	AP	1.8V power supply pin for HDMI Receiver	1.8V
2	RXC-	AI	HDMI Receiver clock negative analog input	
3	RXC+	AI	HDMI Receiver clock positive analog input	
4	VTERM	AIO	RX input termination bias, connect to 3.3V power supply	
5	RX0-	AI	HDMI Receiver channel 0 negative analog input	
6	RX0+	AI	HDMI Receiver channel 0 positive analog input	
7	VCCA33	AP	3.3V power supply pin for HDMI Receiver	3.3V
8	RX1-	AI	HDMI Receiver channel 1 negative analog input	
9	RX1+	AI	HDMI Receiver channel 1 positive analog input	
10	VTERM	AIO	RX input termination bias, connect to 3.3V power supply	
11	RX2-	AI	HDMI Receiver channel 2 negative analog input	
12	RX2+	AI	HDMI Receiver channel 2 positive analog input	
13	VCCA18	AP	1.8V power supply pin for HDMI Receiver	1.8V
14，72	NC		No connection. It may be connected to 1.8V power supply.	
15	CEC	IO	HDMI CEC pin	
16	REXT	AIO	External resistor used for accurate current reference, connect 2K 1% resistor to ground. If use internal resistor, this pin may be connected to 1.8V power supply.	
17	ESDA	IO	Master I2C data channel for EEPROM	5V-tolerant
18	ESCL	IO	Master I2C clock channel for EEPROM	5V-tolerant
19	IIS_SD0/SPDIF	O	I2S data0 output/SPDIF audio output	
20	VCC33	P	Power supply pin for IO	3.3V
21	IIS_WS	O	I2S word select output	
22	IIS_SCLK	O	I2S serial clock output	
23	IIS_MCLK	O	I2S audio master clock output	
24	RESET_N	I	Global reset, active low	
25	VDD18	P	Power supply pin for digital	1.8V
26	TD3+	AO	LVDS output	
27	TD3-	AO	LVDS output	
28	D23_TDC+	AO	RGB data23 output(default B7)/LVDS output	
29	D22_TDC-	AO	RGB data22 output(default B6)/LVDS output	
30	D21_TD2+	AO	RGB data21 output(default B5)/LVDS output	
31	D20_TD2-	AO	RGB data20 output(default B4)/LVDS output	
32	D19_TD1+	AO	RGB data19 output(default B3)/LVDS output	
33	D18_TD1-	AO	RGB data18 output(default B2)/LVDS output	
34	D17_TD0+	AO	RGB data17 output(default B1)/LVDS output	
35	D16_TD0-	AO	RGB data16 output(default B0)/LVDS output	

PIN	NAME	I/O	FUNCTION	NOTES
36	VCC33_TTL	AP	3.3V Power supply pins for RGB/LVDS output 3.3V for LVDS output 1.8V or 3.3V for TTL output	3.3V or 1.8V
37	D15_TC3+	AO	RGB data15 output(default G7)/LVDS output	
38	D14_TC3-	AO	RGB data14 output(default G6)/LVDS output	
39	D13_TCC+	AO	RGB data13 output(default G5)/LVDS output	
40	D12_TCC-	AO	RGB data12 output(default G4)/LVDS output	
41	D11_TC2+	AO	RGB data11 output(default G3)/LVDS output	
42	D10_TC2-	AO	RGB data10 output(default G2)/LVDS output	
43	D9_TC1+	AO	RGB data9 output(default G1)/LVDS output	
44	D8_TC1-	AO	RGB data8 output(default G0)/LVDS output	
45	D7_TC0+	AO	RGB data7 output(default R7)/LVDS output	
46	D6_TC0-	AO	RGB data6 output(default R6)/LVDS output	
47	D5	AO	RGB data5 output(default R5)	
48	D4	AO	RGB data4 output(default R4)	
49	D3	AO	RGB data3 output(default R3)	
50	D2	AO	RGB data2 output(default R2)	
51	D1	AO	RGB data1 output(default R1)	
52	D0	AO	RGB data0 output(default R0)	
53	DE	AO	RGB data enable output	
54	HS	AO	RGB horizontal sync output	
55	VS	AO	RGB vertical sync output	
56	PCLK	AO	RGB pixel clock output	
57	VCC33_TTL	AP	3.3V Power supply pins for RGB/LVDS output 3.3V for LVDS output 1.8V or 3.3V for TTL output	3.3V or 1.8V
58	VDD18	P	Power supply pin for digital	1.8V
59	PVCC18	AP	Power supply pin for Audio/Core PLL	1.8V
60	XTAL_O	O	Crystal oscillator output	
61	XTAL_I	I	Crystal oscillator input	
62	VCCA33_XTAL	AP	Power supply pin for XTAL	3.3V
63	GPIO15	IO	GPIO15	
64	VCC33	AP	Power supply pins for IO	3.3V
65	CSDA	IO	Slave I2C data channel	
66	CSCL	I	Slave I2C clock channel	
67	VDD18	P	Power supply pin for digital	1.8V
68	IIS_SD3	O	I2S data3 output	
69	IIS_SD2	O	I2S data2 output	
70	IIS_SD1	O	I2S data1 output	
71	SPDIF	O	SPDIF audio output	
73	GPIO13	IO	GPIO13	
74	RX_HPD	O	HDMI Receiver hot plug detect output	5V-tolerant
75	DSDA_RX	IO	HDMI Receiver DDC data channel	5V-tolerant
76	DSCL_RX	I	HDMI Receiver DDC clock channel	5V-tolerant

7. Functional Block Description

Figure 7.1 is functional block diagram of LT8619C, and the detailed sub-block relationship is also shown in the diagram.

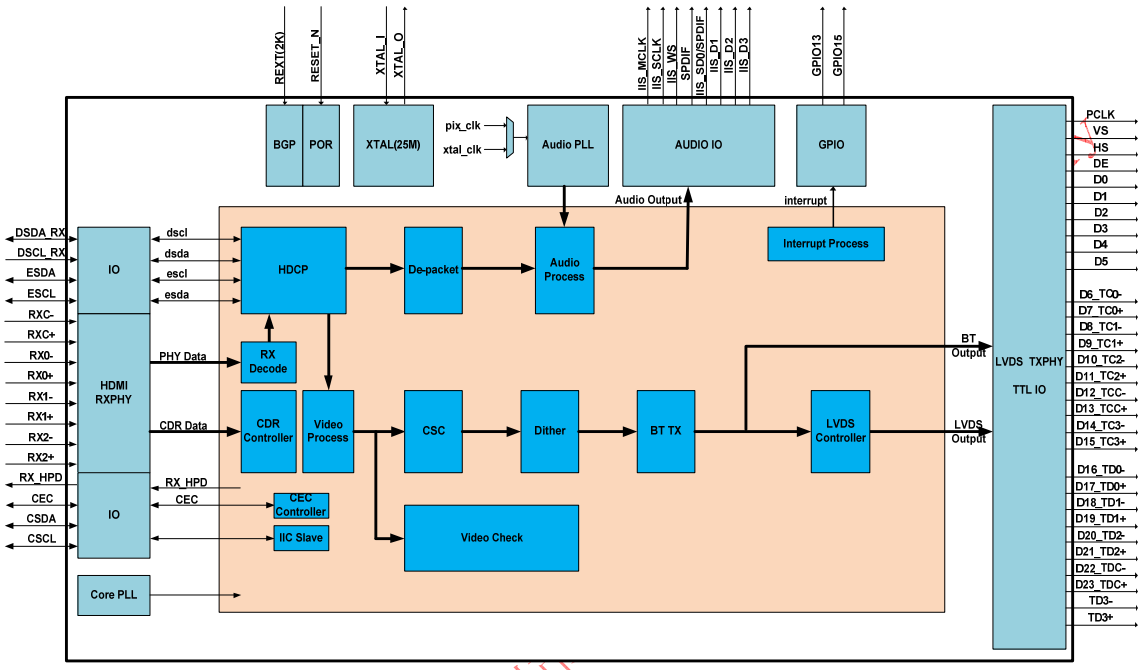


Figure 7.1 Functional Block Diagram

7.1 TTL Output

TTL Output Timing

The TTL output ports send out timing signal PCLK (Pixel Clock), HS (Horizontal Sync), VS (Vertical Sync), DE (Data Enable) and TTL data(RGB or YCbCr or BT656 or BT1120).
For easy PCB layout, LT8619C output data ports D0-D23 can switch RGB data.

Output RGB888/YCbCr data mapping:

Output Port	RGB	YCbCr 4:4:4	16-bit YCbCr 4:2:2	20-bit YCbCr 4:2:2	24-bit YCbCr 4:2:2
D0	R[0]	Cr[0]	C[0]	C[2]	C[4]
D1	R[1]	Cr[1]	C[1]	C[3]	C[5]
D2	R[2]	Cr[2]	C[2]	C[4]	C[6]
D3	R[3]	Cr[3]	C[3]	C[5]	C[7]
D4	R[4]	Cr[4]	C[4]	C[6]	C[8]
D5	R[5]	Cr[5]	C[5]	C[7]	C[9]
D6	R[6]	Cr[6]	C[6]	C[8]	C[10]
D7	R[7]	Cr[7]	C[7]	C[9]	C[11]
D8	G[0]	Y[0]	Y[0]	Y[2]	Y[4]
D9	G[1]	Y[1]	Y[1]	Y[3]	Y[5]

Output Port	RGB	YCbCr 4:4:4	16-bit YCbCr 4:2:2	20-bit YCbCr 4:2:2	24-bit YCbCr 4:2:2
D10	G[2]	Y[2]	Y[2]	Y[4]	Y[6]
D11	G[3]	Y[3]	Y[3]	Y[5]	Y[7]
D12	G[4]	Y[4]	Y[4]	Y[6]	Y[8]
D13	G[5]	Y[5]	Y[5]	Y[7]	Y[9]
D14	G[6]	Y[6]	Y[6]	Y[8]	Y[10]
D15	G[7]	Y[7]	Y[7]	Y[9]	Y[11]
D16	B[0]	Cb[0]			Y[0]
D17	B[1]	Cb[1]			Y[1]
D18	B[2]	Cb[2]		Y[0]	Y[2]
D19	B[3]	Cb[3]		Y[1]	Y[3]
D20	B[4]	Cb[4]			C[0]
D21	B[5]	Cb[5]			C[1]
D22	B[6]	Cb[6]		C[0]	C[2]
D23	B[7]	Cb[7]		C[1]	C[3]

Output RGB666/RGB565 data mapping:

Output Port	RGB666 Mapping 1	RGB666 Mapping 2	RGB666 Mapping 3	RGB565 Mapping 1	RGB565 Mapping 2	RGB565 Mapping 3
D0		R[0]			R[0]	
D1		R[1]			R[1]	
D2	R[0]	R[2]			R[2]	
D3	R[1]	R[3]		R[0]	R[3]	
D4	R[2]	R[4]		R[1]	R[4]	
D5	R[3]	R[5]		R[2]	G[0]	
D6	R[4]	G[0]	R[0]	R[3]	G[1]	
D7	R[5]	G[1]	R[1]	R[4]	G[2]	
D8		G[2]	R[2]		G[3]	R[0]
D9		G[3]	R[3]		G[4]	R[1]
D10	G[0]	G[4]	R[4]	G[0]	G[5]	R[2]
D11	G[1]	G[5]	R[5]	G[1]	B[0]	R[3]
D12	G[2]	B[0]	G[0]	G[2]	B[1]	R[4]
D13	G[3]	B[1]	G[1]	G[3]	B[2]	G[0]
D14	G[4]	B[2]	G[2]	G[4]	B[3]	G[1]
D15	G[5]	B[3]	G[3]	G[5]	B[4]	G[2]
D16		B[4]	G[4]			G[3]
D17		B[5]	G[5]			G[4]
D18	B[0]		B[0]			G[5]
D19	B[1]		B[1]	B[0]		B[1]
D20	B[2]		B[2]	B[1]		B[2]
D21	B[3]		B[3]	B[2]		B[3]
D22	B[4]		B[4]	B[3]		B[4]
D23	B[5]		B[5]	B[4]		B[5]

Output 16/20/24-bit BT1120/BTA-T1004 data mapping:

Output Port	16-bit Mapping 1	16-bit Mapping 2	20-bit Mapping 1	20-bit Mapping 2	24-bit Mapping
D0	C[0]		C[0]		C[0]
D1	C[1]		C[1]		C[1]
D2	C[2]		C[2]		C[2]
D3	C[3]		C[3]		C[3]
D4	C[4]		C[4]	C[0]	C[4]
D5	C[5]		C[5]	C[1]	C[5]
D6	C[6]		C[6]	C[2]	C[6]
D7	C[7]		C[7]	C[3]	C[7]
D8	Y[0]	C[0]	C[8]	C[4]	C[8]
D9	Y[1]	C[1]	C[9]	C[5]	C[9]
D10	Y[2]	C[2]	Y[0]	C[6]	C[10]
D11	Y[3]	C[3]	Y[1]	C[7]	C[11]
D12	Y[4]	C[4]	Y[2]	C[8]	Y[0]
D13	Y[5]	C[5]	Y[3]	C[9]	Y[1]
D14	Y[6]	C[6]	Y[4]	Y[0]	Y[2]
D15	Y[7]	C[7]	Y[5]	Y[1]	Y[3]
D16		Y[0]	Y[6]	Y[2]	Y[4]
D17		Y[1]	Y[7]	Y[3]	Y[5]
D18		Y[2]	Y[8]	Y[4]	Y[6]
D19		Y[3]	Y[9]	Y[5]	Y[7]
D20		Y[4]		Y[6]	Y[8]
D21		Y[5]		Y[7]	Y[9]
D22		Y[6]		Y[8]	Y[10]
D23		Y[7]		Y[9]	Y[11]

Output 8/10/12-bit BT1120/BT656 data mapping:

Output Port	8-bit Mapping	10-bit Mapping 1	10-bit Mapping 2	12-bit Mapping 1	12-bit Mapping 2
D0		Y/C[0]		Y/C[0]	
D1		Y/C[1]		Y/C[1]	
D2		Y/C[2]		Y/C[2]	
D3		Y/C[3]		Y/C[3]	
D4		Y/C[4]		Y/C[4]	
D5		Y/C[5]		Y/C[5]	
D6		Y/C[6]		Y/C[6]	
D7		Y/C[7]		Y/C[7]	
D8	Y/C[0]	Y/C[8]		Y/C[8]	
D9	Y/C[1]	Y/C[9]		Y/C[9]	
D10	Y/C[2]			Y/C[10]	
D11	Y/C[3]			Y/C[11]	

Output Port	8-bit Mapping	10-bit Mapping 1	10-bit Mapping 2	12-bit Mapping 1	12-bit Mapping 2
D12	Y/C[4]				Y/C[0]
D13	Y/C[5]				Y/C[1]
D14	Y/C[6]		Y/C[0]		Y/C[2]
D15	Y/C[7]		Y/C[1]		Y/C[3]
D16			Y/C[2]		Y/C[4]
D17			Y/C[3]		Y/C[5]
D18			Y/C[4]		Y/C[6]
D19			Y/C[5]		Y/C[7]
D20			Y/C[6]		Y/C[8]
D21			Y/C[7]		Y/C[9]
D22			Y/C[8]		Y/C[10]
D23			Y/C[9]		Y/C[11]

7.2 LVDS Output

Display Output Timing

The display output port sends single/double pixel data transfer and synchronized display timing to an external device. The display port also support display panel with 6-bit per color, turn on the dithering function to enhance color depth.

LVDS transmitter supports the following features:

- Programmable single port or dual ports
- Programmable 6 bit or 8 bit output
- Programmable ports swapping

In single port output mode, single pixel data (18/24-bit RGB, 3/4 LVDS data streams) is transferred to display port C on each active edge of LVDS_CLK, the rate of LVDS_CLK is also equal to display pixel clock. The sync & enable signals are also sent to display port on each active edge of LVDS_CLK. Shown on Figure 7.2.1.

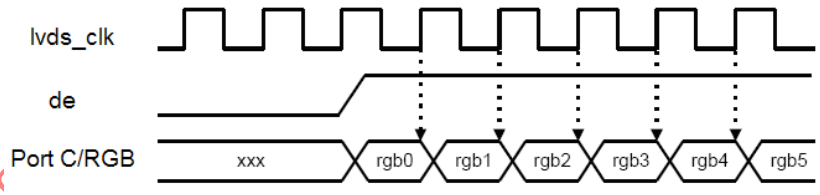


Figure 7.2.1 Single Port Mode Display Data Timing

In dual ports output mode, double pixel data(36/48-bit RGB, 6/8 LVDS data streams) is transferred to display port C & D on each active edge of LVDS_CLK and the rate of LVDS_CLK is equal to half of display pixel clock at this moment. The sync & enable signals are also sent to display port on each active edge of LVDS_CLK. Shown on Figure 7.2.2.

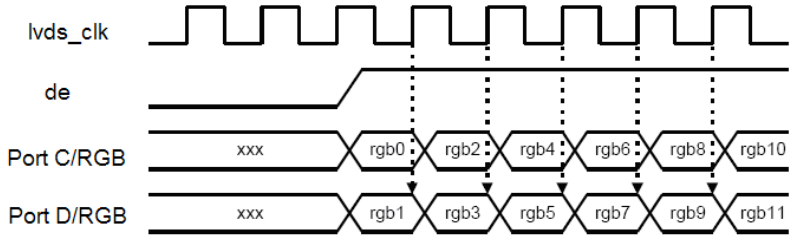


Figure 7.2.2 Dual Ports Mode Display Data Timing

8. DC Electrical Characteristics

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC_{33}	3.3V Supply Voltage	-0.3		4.0	V
VCC_{18}	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		VCC_{33}+0.3	V
Vo	Output Voltage	-0.3		VCC_{33}+0.3	V
T_{STG}	Storage Temperature	-55		125	ºC
DIFF33	Difference between two 3.3V power pins			1.0	V
DIFF18	Difference between two 1.8V power pins			1.0	V
DIFF3318	Difference between any 3.3V power pins and 1.8V power pins	-1.0		2.0	V

Notes:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC_{33}	3.3V Supply Voltage	3.0	3.3	3.6	V
VCC_{18}	1.8V Supply Voltage	1.62	1.8	1.98	V
VCC_N	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	-40	25	85	ºC

8.3 TTL Output Specifications

Digital I/O spec followed LVTTL spec. Under normal operating conditions.

Table 8.3.1 TTL Output Specifications

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{IDI}	Differential input voltage, single ended amplitude			150		700	mV
I_{CC}	Operating current	TMDS clk (27M)	1.8V		104		mA
			3.3V		55		mA
		TMDS clk (74.25M)	1.8V		140		mA
			3.3V		60		mA
		TMDS clk (148.5M)	1.8V		197		mA
			3.3V		72		mA
		TMDS clk (297M)	1.8V		305		mA
			3.3V		80		mA

**Measured under RGB888 output mode. Also can be referred for BT656 and BT1120 output mode.*

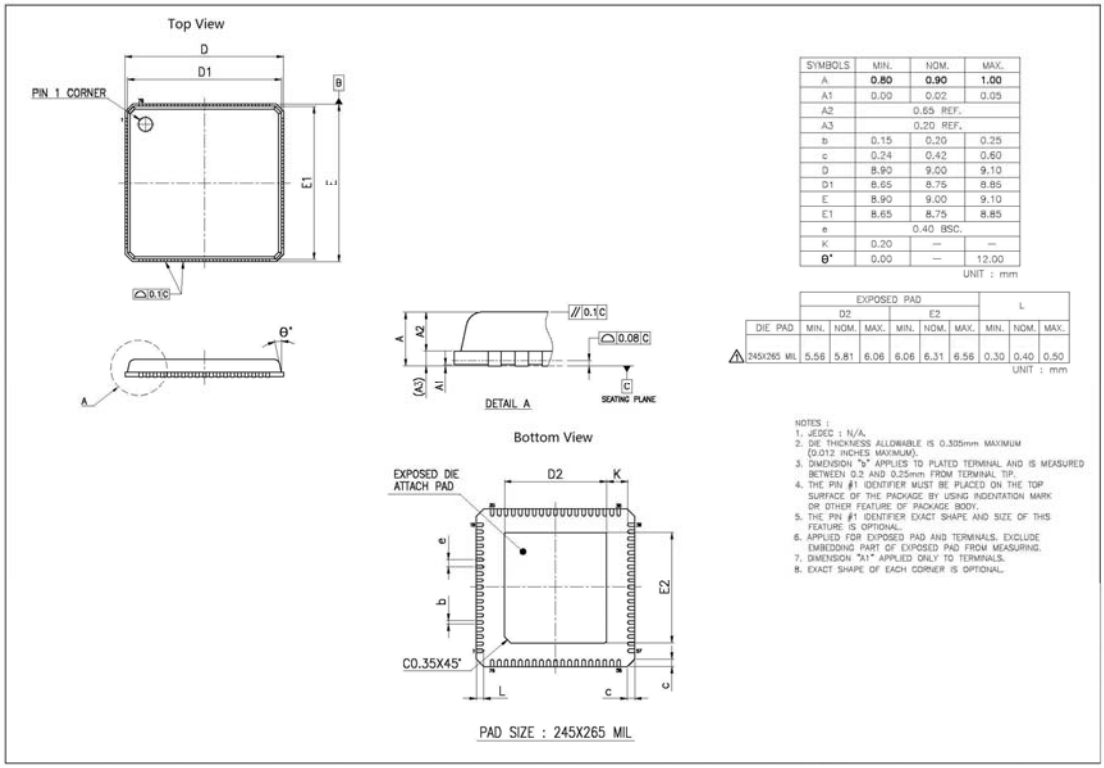
8.4 LVDS Output Specifications

Table 8.4.1 LVDS Output Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	1.8V		176		mA
		3.3V		105		mA

**Measured under dual-port 8bit LVDS output mode and input resolution is 1080P60.*

9. Packaging



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.15	0.20	0.25
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.40 BSC.	
K	0.20	—	—
θ°	0.00	—	12.00

UNIT : mm

	EXPOSED PAD						L		
	D2			E2					
DIE PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
⚠ 245X265 MIL	5.56	5.81	6.06	6.06	6.31	6.56	0.30	0.40	0.50

UNIT : mm

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 9.1 76-pin QFN package

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