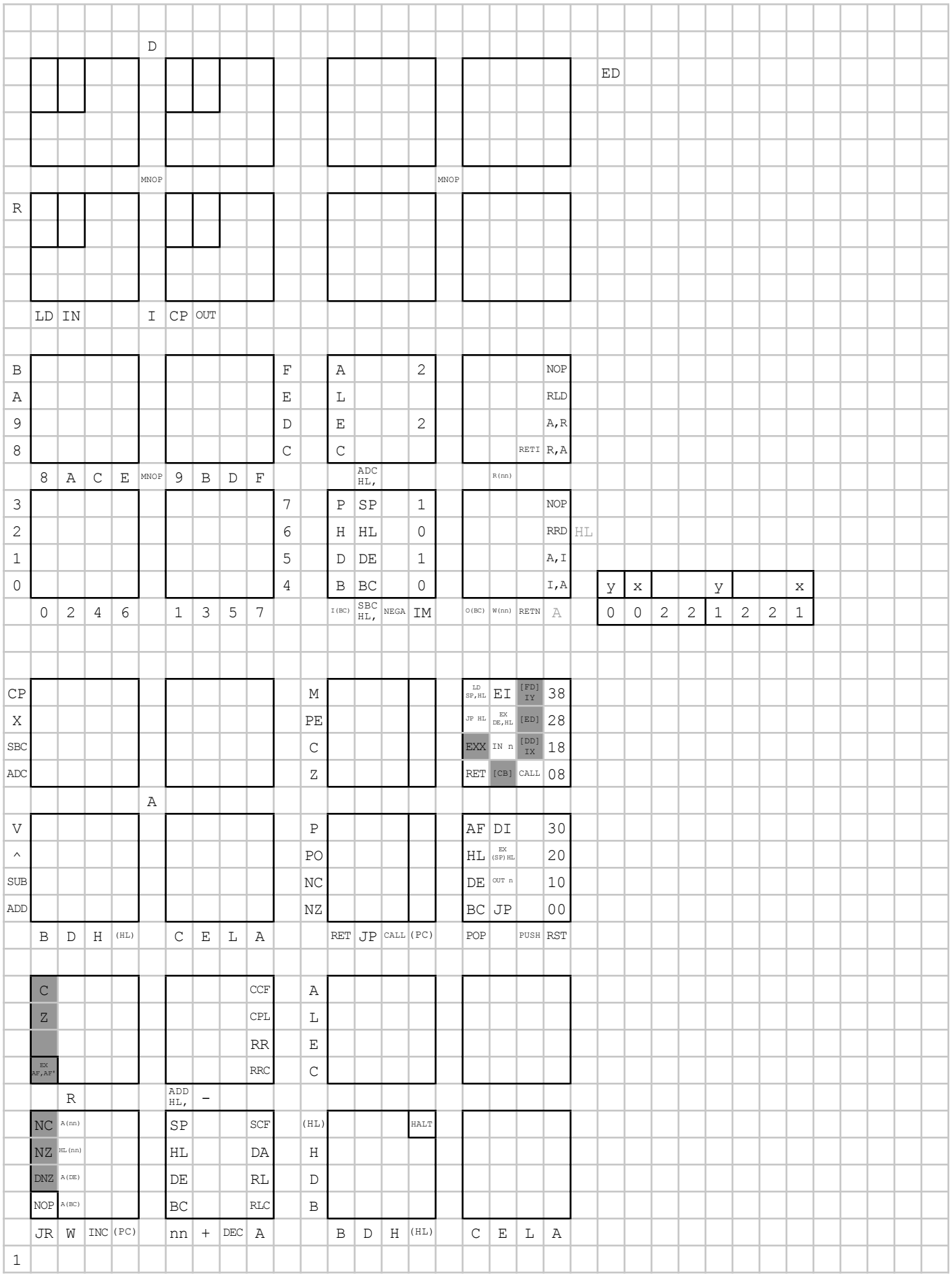
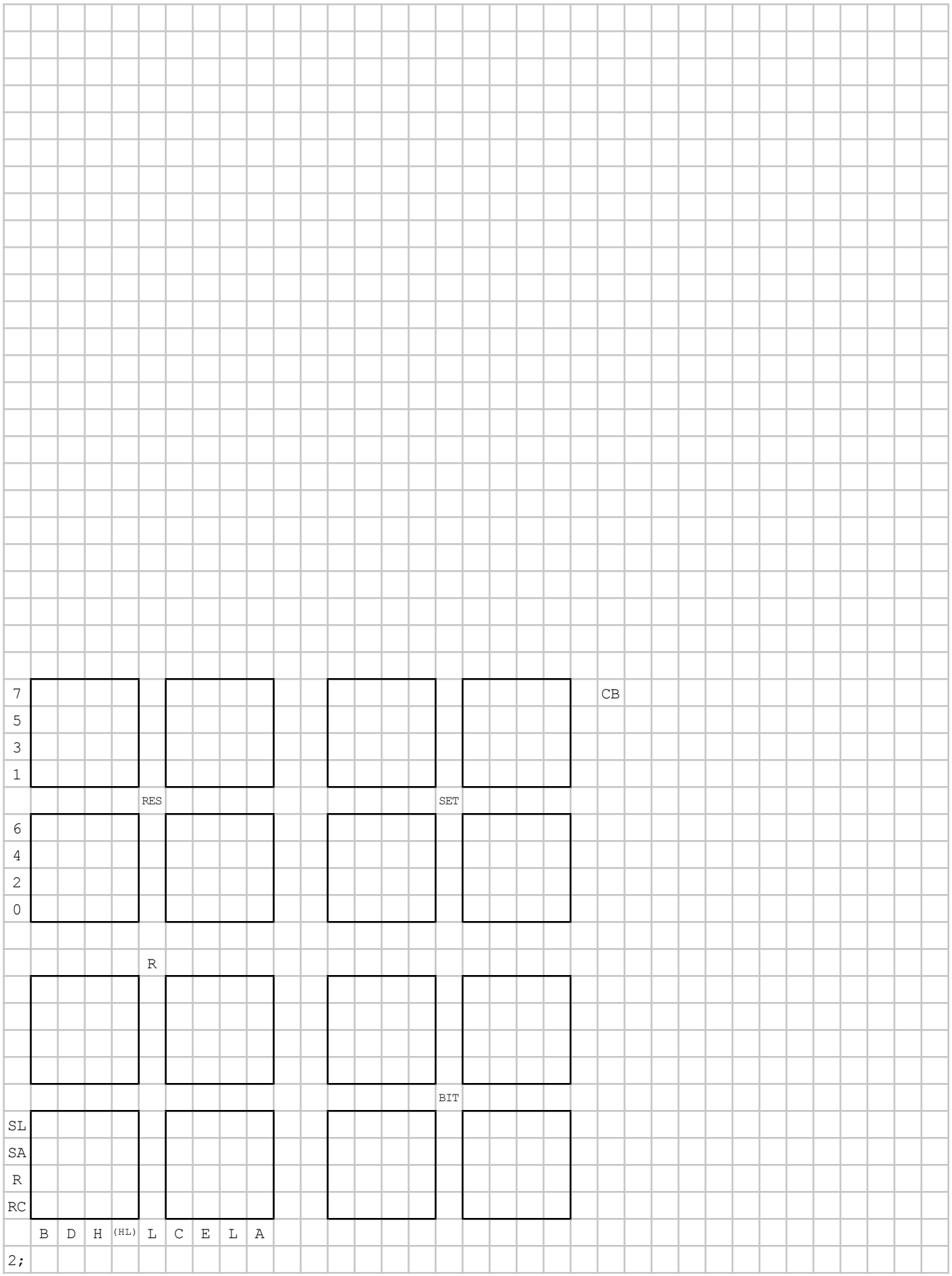
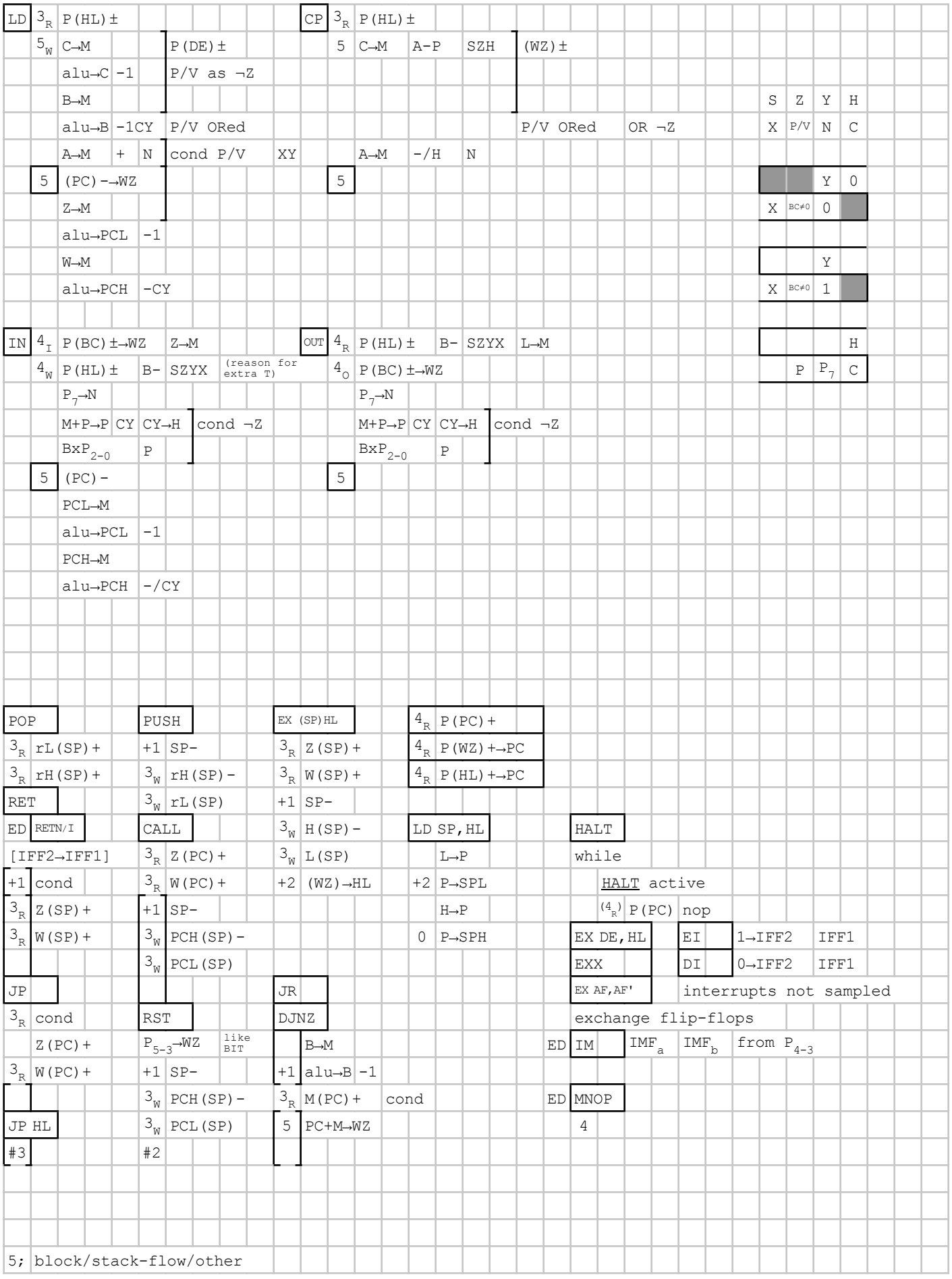

D
ED
MNOP
MNOP
R
LD IN I CP OUT
B F A 2 NOP
A E L RLD
9 D E 2 A,R
8 C C RETI R,A
8 A C E MNOP 9 B D F ADC HL, R(nn)
3 7 P SP 1 NOP
2 6 H HL 0 RRD HL
1 5 D DE 1 A,I
0 4 B BC 0 I,A
0 2 4 6 1 3 5 7 I(BC) SBC HL, NEGA IM O(BC) W(nn) RETN A
y x y x
0 0 2 2 1 2 2 1
CP M LD SP,HL EI [FD] IY 38
X PE JP HL EX DE,HL [ED] 28
SBC C EXX IN n [DD] IX 18
ADC Z RET [CB] CALL 08
A
V P AF DI 30
^ PO HL EX (SP)HL 20
SUB NC DE OUT n 10
ADD NZ BC JP 00
B D H (HL) C E L A RET JP CALL (PC) POP PUSH RST
C CCF A
Z CPL L
RR E
EX AF,AF' RRC C
R ADD HL, -
NC A(nn) SP SCF (HL) HALT
NZ HL(nn) HL DA H
DNZ A(DE) DE RL D
NOP A(BC) BC RLC B
JR W INC (PC) nn + DEC A B D H (HL) C E L A
1


7
5
3
1
CB
RES
SET
6
4
2
0
R
BIT
SL
SA
R
RC
B D H (HL) L C E L A
2;

| | | |

| | | |


LD 3R P(HL)± | 5W C→M | alu→C -1 | B→M | alu→B -1CY | A→M + N | 5 (PC)-→WZ | Z→M | alu→PCL -1 | W→M | alu→PCH -CY
P(DE)± | P/V as ¬Z | P/V ORed | cond P/V XY
CP 3R P(HL)± | 5 C→M A-P SZH | (WZ)± | P/V ORed | OR ¬Z | A→M -/H N | 5
S Z Y H | X P/V N C | Y 0 | X BC≠0 0 | Y | X BC≠0 1
IN 4I P(BC)±→WZ | Z→M | 4W P(HL)± | B- SZYX | (reason for extra T) | P7→N | M+P→P CY | CY→H | cond ¬Z | BxP2-0 | P | 5 (PC)- | PCL→M | alu→PCL -1 | PCH→M | alu→PCH -/CY
OUT 4R P(HL)± | B- SZYX | L→M | 4O P(BC)±→WZ | P7→N | M+P→P CY | CY→H | cond ¬Z | BxP2-0 | P | 5 PC+M→WZ
H | P P7 C
POP 3R rL(SP)+ | 3R rH(SP)+ | RET | ED RETN/I | [IFF2→IFF1] | +1 cond | 3R Z(SP)+ | 3R W(SP)+ | JP | 3R cond | Z(PC)+ | 3R W(PC)+ | JP HL | #3
PUSH +1 SP- | 3W rH(SP)- | 3W rL(SP) | CALL | 3R Z(PC)+ | 3R W(PC)+ | +1 SP- | 3W PCH(SP)- | 3W PCL(SP) | RST | P5-3→WZ | like BIT | +1 SP- | 3W PCH(SP)- | 3W PCL(SP) | #2
EX (SP)HL 3R Z(SP)+ | 3R W(SP)+ | +1 SP- | 3W H(SP)- | 3W L(SP) | +2 (WZ)→HL | JR | DJNZ | B→M | +1 alu→B -1 | cond
4R P(PC)+ | 4R P(WZ)+→PC | 4R P(HL)+→PC
LD SP,HL | L→P | +2 P→SPL | H→P | 0 P→SPH
HALT | while | HALT active | (4R) P(PC) nop | EX DE,HL | EXX | EX AF,AF' | ED IM | IMFa | ED MNOP | 4
EI 1→IFF2 IFF1 | DI 0→IFF2 IFF1 | interrupts not sampled | exchange flip-flops | IMFb | from P4-3
5; block/stack-flow/other

¬	o
1	0

avb

¬(¬a^¬b)

bx(a^¬b)

axbx(a^b)

^		x		v	
0	1	1	0	1	1
0	0	0	1	0	1

							CY
			H				
						N	
		Y		X			
S							
	Z				P/V		

INC A	DAA

should be used if CY is known to be reset...

SUB B		
RLCA	RRCA	
JP PO		CCF

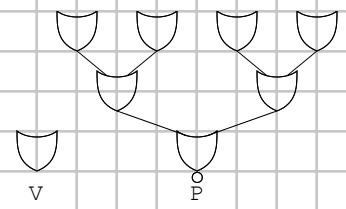
1	M	Z			PE		C
0	P	NZ			PO		NC

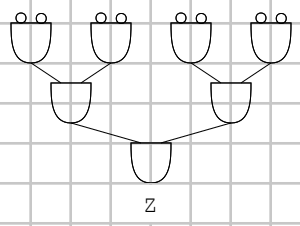
A-B signed→unsigned

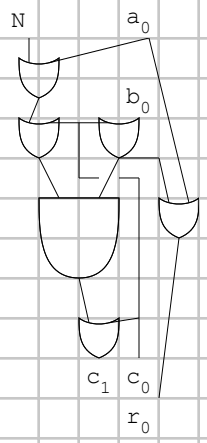
		a_7						a_0	M
-		b_7						b_0	P
-	CY	c_7			H			c_0	
N		S		Y		X		r_0	alu

DB

M







with rising edge of T_L

while BUSREQ active

all high-impedance state

BUSACK active

if M_L

if NMI F/F

0→NMI F/F, IFF1

(4_R) P(PC) 0→W 66→Z push PC sel WZ

if IFF1

if INT active

0→IFF1, IFF2

(6_R) P(PC)

if IMF_a

if IMF_b

I→M push PC sel WZ poMP WZ

else

0→W 38→Z push PC sel WZ

while RESET active (3T MIN to complete)

AB,DB high-impedance state

all other output signals inactive

0→IFF1,IFF2, IMF_a,IMF_b, PC,IR

FFFF→AF,SP note:NMI F/F is not reset

NMI/INT Ack: PC remains stationary for I

INT Ack: IORQ replaces MREQ in M1 and RD not used

two T_W added automatically

IORQ active for 1.5T before rising T_3 (like MREQ)

I MHz/E3*ns=T

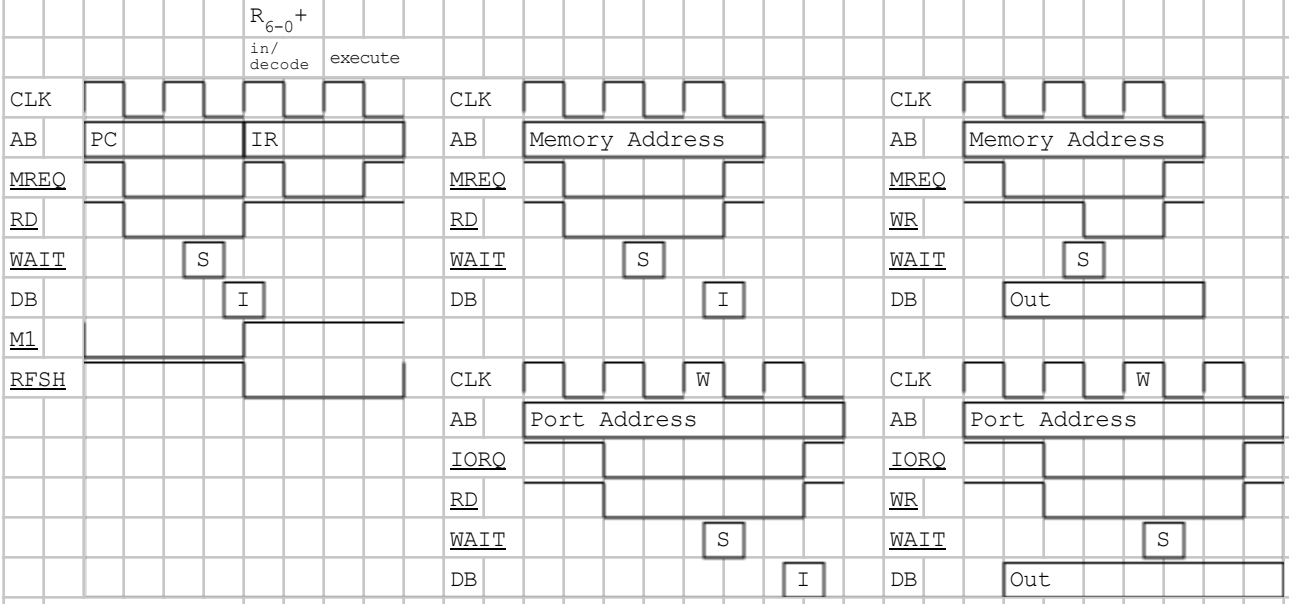
M1 M_x M_L

T_x T_W T_L HALT 1.2T MAX

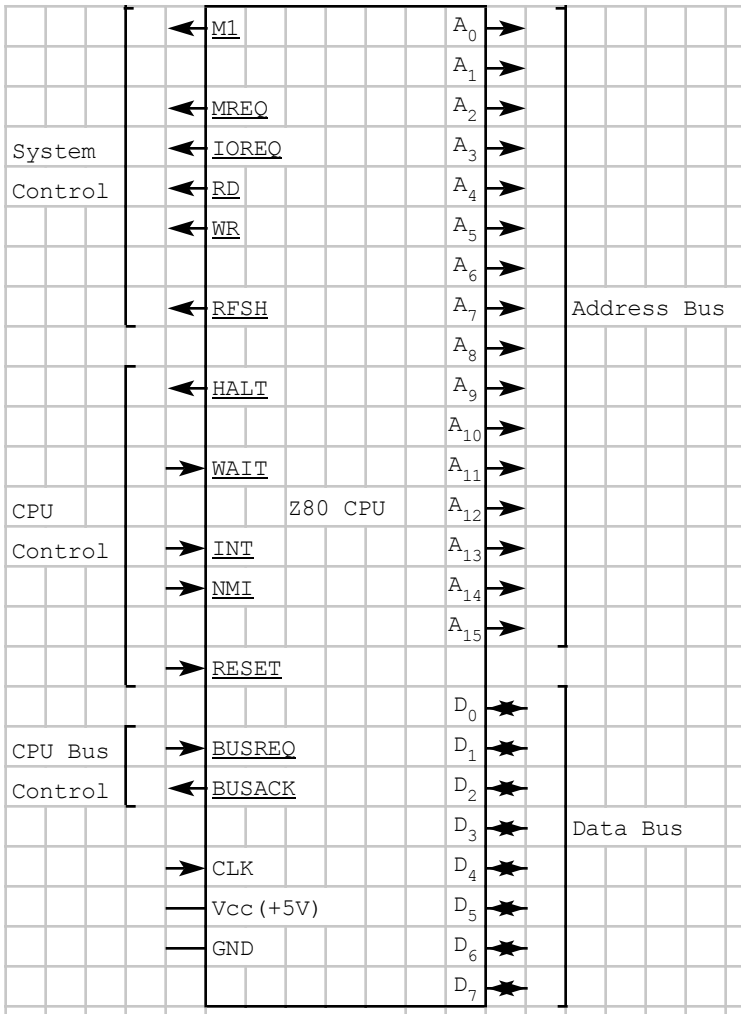
WAIT .28T MIN before sample edge

M1 R W INT .32T MIN before sample edge

I O other delays...



7 timing notes



NMI negative edge-triggered (must remain low for .32T MIN, then 1→NMI F/F)

AB,DB active high

all other signals active low

AB,DB,MREQ,IORQ,RD,WR tristate (high-impedance state/floating for DMA)

single-phase MOS-level/TTL-level clock...

A	F	A	F'
B	C	B	C'
D	E	D	E'
H	L	H	L'

I	R										
I	X										
I	Y		W	Z							
S	P		M	P		ACT	TMP/IR				
P	C		S	T		DE/HL	BCDEHL'	AF'	IMF_a	IMF_b	IFF2	IFF1	NMI F/F

implemented using static RAM

8;