Huawei Mate 10 and Mate 10 Pro Launch on October 16th, More Kirin 970 Details

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by Ian Cutress on September 4, 2017 11:00 AM EST

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Riding on the back of the 'not-announced then announced' initial set of Kirin 970 details, Huawei had one of the major keynote presentations at the IFA trade show this year, detailing more of the new SoC, more into the AI details, and also providing some salient information about the next flagship phone. Richard Yu, CEO of Huawei's Consumer Business Group (CBG), announced that the Huawei Mate 10 and Mate 10 Pro will be launched on October 16th, at an event in Munich, and will feature both the Kirin 970 SoC and a new minimal-bezel display.

Kirin 970 PCB vs Intel Core i7 Laptop Sticker

Suffice to say, that is basically all we know about the Mate 10 at this point: a new display technology, and a new SoC with additional AI hardware under-the-hood to start the process of using AI to enhance the

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We learned that the IP is scalable, but at this time is only going to be limited to Huawei devices. The configuration of the NPU internally is based on multiple matrix multiply units, similar to that shown in Google's TPU and NVIDIA's Tensor core, found in Volta. In Google's first TPU, designed for neural network training, there was a single 256x256 matrix multiply unit doing the heavy lifting. For the TPUv2, as detailed back at the Hot Chips conference a couple of weeks ago, Google has moved to dual 128x128 matrix multiply units. In NVIDIA's biggest Volta chip, the V100, they have placed 640 tensor cores each capable of a 4x4 matrix multiply. The Kirin 970 TPU by contrast, as we were told, uses 3x3 matrix multiply units and a number of them, although that number was not provided.

in efficiency. The 1 TOPS per watt was significant.… https://t.co/I8bAnGHayh

RyanSmithAT: @FSamareanu Oh geeze. I feel like an idiot. Thanks!

ganeshts: MAMR drives will just be like std. PMR drives wrt perf & firmware. SMR / TDMR can optionally be added on top to eke… https://t.co/UkVb3MmkKZ

RyanSmithAT: @FSamareanu Hmm. Not seeing a problem at this second. Could you please go into more detail?

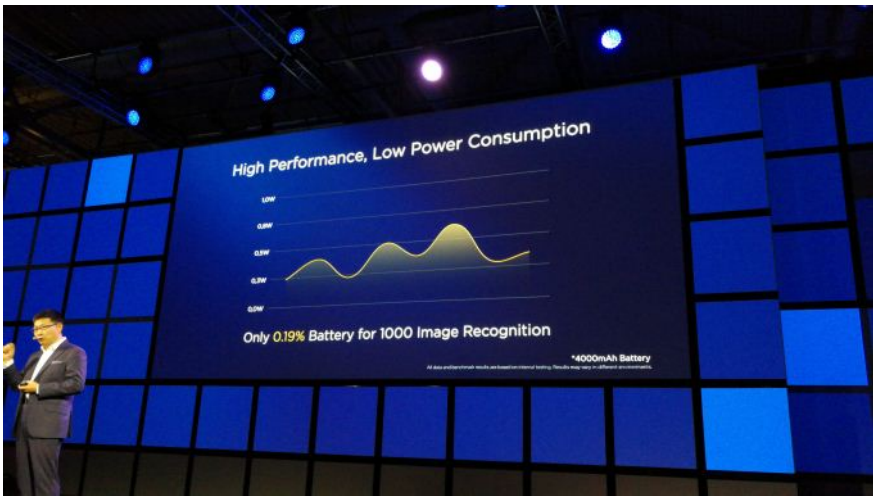
RyanSmithAT: RT @anandtech: Western Digital Stuns Storage Industry with MAMR Breakthrough for Next-Gen HDDs https://t.co/oNt9CqRYD7

RyanSmithAT: RT @IanCutress: Global request for CPU and motherboard reviewers to include which motherboard BIOS versions are used in their reviews. Plea…

ganeshts: @witeken Announced quite some time back - Eye Q5. In ADAS market, TOPS

At the keynote, and confirmed in our discussions after, Huawei stated that the API to use the NPU will be available for developers. The unit as a whole will support the TensorFlow and TensorFlow Lite frameworks, as well as Caffe and Caffe2. The NPU can be accessed via Huawei's own Kirin AI API, or Android's NN API, relying on Kirin's AI Heterogeneous Resource Management tools to split the workloads between CPU, GPU, DSP and NPU. I suspect we'll understand more about this nearer to the launch. Huawei did specifically state that this will be an 'open architecture', but failed to mention exactly what that meant in this context.

time from idle to wake up. Power consumption was not explicitly stated (under 1W), but they did quote that a test of 1000 images being recognized drained a 4000 mAh battery by 0.19%, fluctuating between 0.25W and 0.67W.



for the memory, and the use of a new i7 sensor hub.

HiSilicon High-End Kirin SoC Lineup

SoC	Kirin 970	Kirin 960	Kirin 950/955
CPU	4x A73 @ 2.40 GHz 4x A53 @ 1.80 GHz	4x A73 @ 2.36GHz 4x A53 @ 1.84GHz	4x A72 @ 2.30/2.52GHz 4x A53 @ 1.81GHz
GPU	ARM Mali-G72MP12 ? MHz	ARM Mali-G71MP8 1037MHz	ARM Mali-T880MP4 900MHz
LPDDR4 Memory	2x 32-bit LPDDR4 @ 1833 MHz	2x 32-bit LPDDR4 @ 1866MHz 29.9GB/s	2x 32-bit LPDDR4 @ 1333MHz 21.3GB/s
Interconnect	ARM CCI	ARM CCI-550	ARM CCI-400
Storage	UFS 2.1	UFS 2.1	eMMC 5.0
ISP/Camera	Dual 14-bit ISP	Dual 14-bit ISP (Improved)	Dual 14-bit ISP 940MP/s
Encode/Decode	2160p60 Decode 2160p30 Encode	2160p30 HEVC & H.264 Decode & Encode	1080p H.264 Decode & Encode

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SydneyBlue120d - Monday, September 04, 2017 - link

Are memory, interconnect and ISP inverted in the chart?

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jjj - Monday, September 04, 2017 - link

It was public info that they use Cambricon.

AMD's Ryzen CPU (25m per mm2) on GloFo 14nm vs TSMC 10nm."
Not bad at all. I thought TSMC 10nm had roughly the same transistor density as Intel 14nm (which has 37.5 million transistors per mm^2, with Intel 10nm having reached 100.8 million per mm^2), but it is more likely equivalent to an Intel ~13nm process. As for GloFo, if they managed to quadruple their transistor density in their 7nm node (as the 14 --> 7nm transition implies) it would almost precisely match that of Intel 10nm's, but I highly doubt they will - thought I hope they do. At most I expect they will manage a 3x transistor density, i.e. around 75 million transistors per mm^2.

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