Birla Institute of Technology & Science, Pilani
K K Birla Goa Campus

ACADEMIC UNDER GRADUATE STUDIES DIVISION

First Semester 2025-26
Course Handout Part II

Date: 1st August 2025

In addition to Part-I (General Handout for all courses appended to the timetable) this portion gives specific details regarding the course

Course Number	: ECE/EEE/INSTR F215
Course title	: Digital Design
Instructor-in-charge	: Sarang Dhongdi
Team of Instructors	: Tushar Sakorikar, Akshay Madan, Debasis Das, Souvik Ghosh, Vipin Joshi, Ria Rashid

Course Description : Boolean Algebra & logic minimization; combinational logic circuits: arithmetic circuit design, Design using MSI components; Sequential Logic Circuits : flip flops & latches, registers and counters, Finite state machine ; HDL Implementation of Digital circuits; Digital Integrated Circuits ; Programmable logic devices; Memory organization ; Algorithmic State machine; Introduction to computer organization; The course will also have laboratory component on digital design.

Scope and Objective: This is a foundation course that provides students with a fundamental knowledge of digital systems and their various components. Topics covered include Boolean algebra and logic minimization, digital gates, analysis of basic digital circuits, Combinatorial and Sequential digital circuits, digital ICs, arithmetic operations and algorithms, memories and basic computer organization.

Course learning outcomes:

a. Logic minimization for optimizing gates in digital design
b. Designing and analyzing combinational and sequential circuits in digital domain
c. Hardware implementation on bread-boards/PCBs and simulations using Verilog
d. Understanding memory categorization and organization

Method of conduct of the course – Lectures and tutorials will be conducted as per the timetable from AUGSD. Breadboard based lab experiments will be covered in regular labs. Material for Verilog will be additionally provided. Verilog sessions will be conducted at computer center.

Textbook - M.Morris Mano, "Digital Design", Pearson, 6th ed., 2009

Reference Books:

1) Brian Holdsworth, Clive Woods, "Digital Logic Design", Elsevier, 4th Edition, 2008
2) John.M.Yarbrough, "Digital Logic Design", Cengage Learning, 2009.
3) Ronald.J.Tocci, Neal.S.Widmer, Gregory.L.Moss, "Digital Systems", 2007.
4) Samir Palnitkar, "Verilog HDL", Pearson Education.

Course Plan

Lect. No.	Topic	Learning objectives	Book reference
1	Introduction to Digital systems	Digital systems, Binary logic and Digial logic gates	1.1, 1.9, 2.8
2-3	Boolean Algebra and logic gates	Boolean functions, Canonical forms, Standard forms, conversion between different forms	2.2-2.7
4-5	Code number systems	Number systems and codes	1.2-1.7
6-8	Simplification of Boolean functions	K-maps, QM method, other simplification methods	3
9-11	Combinatorial logic, arithmetic circuits	Adders, subtractors, multipliers	4.1-4.7
12-14	MSI Components	Comparators, Decoders, Encoders, MUXs, DeMUXs	4.8-4.11
15	Simulation basics	Hardware Description language	3.11
16	Simulation of combinational logic	HDL for combinational logic	4.12
17	Digital Integrated circuits	TTL, MOS Logic and their characteristics	10.3-10.5,10.7-10.9, class notes
18-20	Sequential Logic	Flip-flops, latches	5.1-5.4
21-24	Clocked sequential circuits	Analysis of clocked circuits, state diagrams and reduction	5.5, 5.7-5.8
25-26	Registers and counters	Shift registers, synchronous and asynchronous counters	6.1-6.5
27-31	Design of asynchronous circuits	Asynchronous sequential logic	9.1-9.7
32-33	Simulation of Sequential logic	HDL for sequential logic, registers and counters	5.6, 6.6
34-36	Memory and PLD	RAM, ROM, PLA, PAL	7.1-7.8
37-38	Modular approach to CPU design	RTL, HDL description, Algorithmic state machines	8.1-8.2, 8.4-8.7
39-40	Memory organization	Memory hierarchy and different types of memories	Class notes

Evaluation Scheme

No.	Component	Duration	CB/OB	Marks(%)	Date
1	Mid-Sem Exam	90 min	CB	25%	11/10/2025, 4-5:30 PM
2	Quizzes	35 mins	CB	10% (1 best out of 2)	Tentative dates- 15-Sept and 10-Nov
3	Regular Hardware labs*	---	OB	14%	TBA
4	Verilog simulation evaluation	---	OB	8%	Tentative- 15th Nov
5	Lab based projects/assignments	--	OB	8%	TBA
7	Comprehensive Examination	3 hrs	CB	35%	16/12/25 (FN)

Make-up Policy

Application for Make-up will be considered only in Genuine cases. An application in writing with relevant certificates attached (medical from Campus Medical center or SWD) needs to be submitted to the IC of the course at least a day before the scheduled exam. No make-up will be given for components where x best out of y components (built-in make-up) has been incorporated.

Lab Policy

All students are required to be present for all scheduled lab sessions. No make-up for lab sessions will be provided. Students will not be awarded full marks for their lab session if they are late by **more than 10 min** into the scheduled hour.

Grading notice

All students registered in the course are expected to appear for all evaluation components. Per section 4.19 of the BITS, Pilani Academic regulations, NC may be given to students if they fail to provide a chance for the instructor to evaluate their progress in the class. Absence in any evaluation components without prior consent of the instructor or submitting blank or incomplete/incoherent answer books may present grounds for awarding NC in the course.

Announcements

Course management and announcements will be handled through the BITS moodle webpage.

Chamber consultation hours : To be announced in class by individual instructors.

Instructor-in-Charge - ECE/EEE/INSTR F215