FOC Control

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IP Facts

Introduction

The FOC control core provide basic control for FOC system.

Features

- 7 main modes to start and control system
- AXI4-Stream interfaces to data input and output streams
- Register interfaces for mode and settings

teCORE™ IP Facts Table	
Supported Device Family	Zynq® -7000, 7 Series
Supported User Interfaces	AX4-Stream
Resources	
Special Features	
Provided with Core	
Design Files	VHDL Source Code
Constraint Files	Not Provided
Example Design	Not Provided
Test Bench	Not Provided
Simulation Model	Not Provided
Supported S/W Dirver	Not Provided
Tested Design Flows	
Design Entry	Vivado® Design Suite, IP Integrator
Simulation	Vivado Simulator
Synthesis	Vivado Synthesis
Tested Hardware Platforms	
Digilent Arty Z7	
Support	
Provided by Trenz Electronic GmbH	

Overview

Feature Summary

Licensing and Ordering Information

Product Specification

Performance

Resource Utilization

Port Description

Signal name	Direction	Description
Global signals		
axis_aclk	Input	System clock
axis_aresetn	Input	System reset; active low
Registers Interface		
control_in	Input	Mode selection
vd_in	Input	Vd value from register
vq_in	Input	Vq value from register
torque_sp_in	Input	Torque setpoint from register
torque_sp_out	Output	Torque setpoint to Torque PI
RPM Input Stream		
s_rpm_tready	Output	AXI4-Stream interface data ready output.
s_rpm_tvalid	Input	AXI4-Stream interface data valid input.
s_rpm_tdata	Input	Rotation speed information
Flux Input stream		
s_flux_tready	Output	AXI4-Stream interface data ready output.
s_flux_tvalid	Input	AXI4-Stream interface data valid input.
s_flux_tdata	Input	Control information from Flux PI
Torque Input Stream		
s_torque_tready	Output	AXI4-Stream interface data ready output.
s_torque_tvalid	Input	AXI4-Stream interface data valid input.
s_torque_tdata	Input	Control information from Torque PI
Angle Input Stream		
s_angle_tready	Output	AXI4-Stream interface data ready output.
s_angle_tvalid	Input	AXI4-Stream interface data valid input.
s_angle_tdata	Input	Rotor angle information

Signal name	Direction	Description
Output Stream		
m_axis_tready	Input	AXI4-Stream interface data ready input.
m_axis_tvalid	Output	AXI4-Stream interface data valid output.
m_axis_tdata	Output	AXI4-Stream interface data output.

The layout of the output stream is as follows:

Bits	Name	Description
63 ... 48		Unused
47 ... 32	Theta	Encoder angle
31 ... 16	Vd	Vd
15 ... 0	Vq	Vq

The signal "control_in" determines mode of the core. The modes are as follows:

Mode	Description
0	Motor stop
1	Normal mode - Speed loop
2	Output Vd and Vq from registers, rotor position from input stream
3	Output Vq from register, Vd and rotor position from input stream
4	Speed loop, Torque PI bypassed
5	Speed loop, RPM PI bypassed
6	Output Vd and Vq from registers, motor rotates at low constant speed

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Important: In order for the angle encoder to output correct absolute position, the encoder should have passed the index position. One possibility for that is to enable mode 6 long enough for the motor to rotate at least one one full revolution.

Design Flow Steps

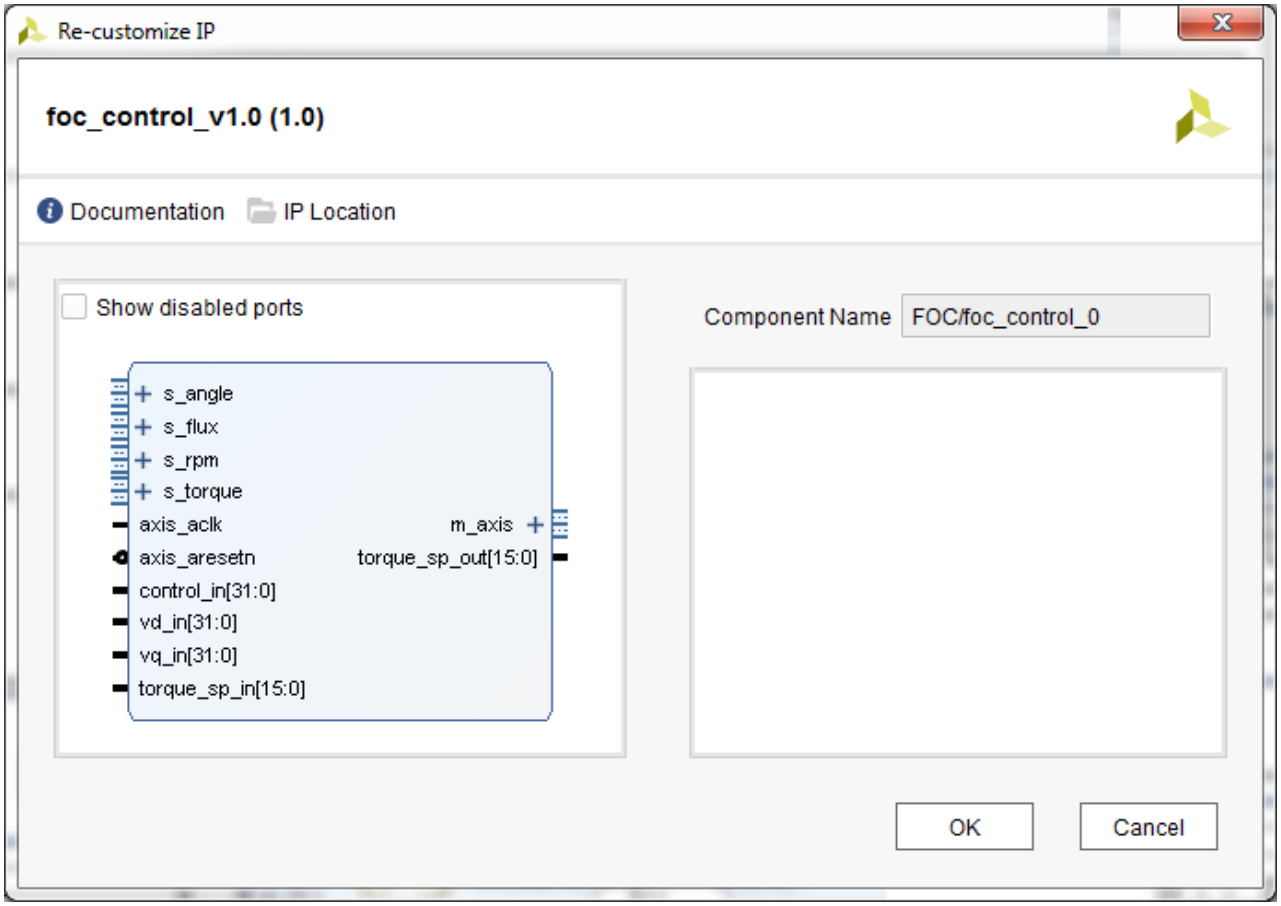
This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

- Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
- Vivado Design Suite User Guide: Designing with IP (UG896)
- Vivado Design Suite User Guide: Getting Started (UG910)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

The re-customization dialogue is as follows:



There are no parameters to be customized.

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the Vivado Design Suite User Guide:

- Designing with IP (UG896)

Example Design

There is no example Design for this IP core release.

Test Bench

There is no test bench for this IP core release.

Appx. A: Change History and Legal Notices

Document Change History

date	revision	authors	description
20xx-xx-xx	v.1	Name	initial release

Legal Notices

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