AXI4-Stream Capture

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IP Facts

Introduction

The AXI4-Stream Capture is an IP core for capturing some data from an AXI4 Stream and forwarding it to the associated Xilinx IP core "AXI DataMover" for storing it in the main memory; it is controlled by a set of registers accessible over AXI Bus.

Features

- Configurable block size.
- Optional trigger input and output.
- Optional pretrigger.

teCORE™ IP Facts Table	
Supported Device Family	Zynq® -7000, 7 Series
Supported User Interfaces	AXI4-Stream
Resources	
Special Features	
Provided with Core	
Design Files	VHDL Source Code
Constraint Files	Not Provided
Example Design	Not Provided
Test Bench	Not Provided
Simulation Model	Not Provided
Supported S/W Dirver	Not Provided
Tested Design Flows	
Design Entry	Vivado® Design Suite, IP Integrator
Simulation	Vivado Simulator
Synthesis	Vivado Synthesis
Tested Hardware Platforms	
Digilent Arty Z7	
Support	
Provided by Trenz Electronic GmbH	

Overview

Feature Summary

Licensing and Ordering Information

Product Specification

The IP core exposes the following set of 32-bit registers on the slave AXI Bus:

Index	Access	Description
0	R/W	Control register bits: Bit 0 - Start transfer when 1 is written after 0 Bit 1 - Data hold; set it to 1 before starting transfer
1	R/W	Transfer size
2	R	Transfer count; incremented at the end of every transfer
3	R/W	Start address
4	R	Last address
5	R/W	Pretrigger, in units of AXI clocks
6	R/W	Status of the associated IP core "AXI DataMover"

Performance

Resource Utilization

Port Description

Signal Name	Direction	Description
Global signals		
axi_aclk	Input	System clock.
axi_aresetn	Input	System reset; active low.
Buses		
S_AXI	Slave	Slave AXI Bus exposing set of control registers
s_axis	Slave	Data stream to be captured
s_axis_s2mm_sts	Slave	Status stream from the associated IP core "AXI DataMover"
m_axis_s2mm	Master	Data stream to the associated IP core "AXI DataMover"
m_axis_s2mm_cmd	Master	Command stream to the asssociated IP core "AXI DataMover"
Trigger input "trig_in"		
s_trig	Input	Trigger data capture
s_ack	Output	Acknowledge data capture trigger
Trigger output "trig_out"		

Signal Name	Direction	Description
m_trig	Output	Trigger data capture
m_ack	Input	Acknowledge data capture trigger

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

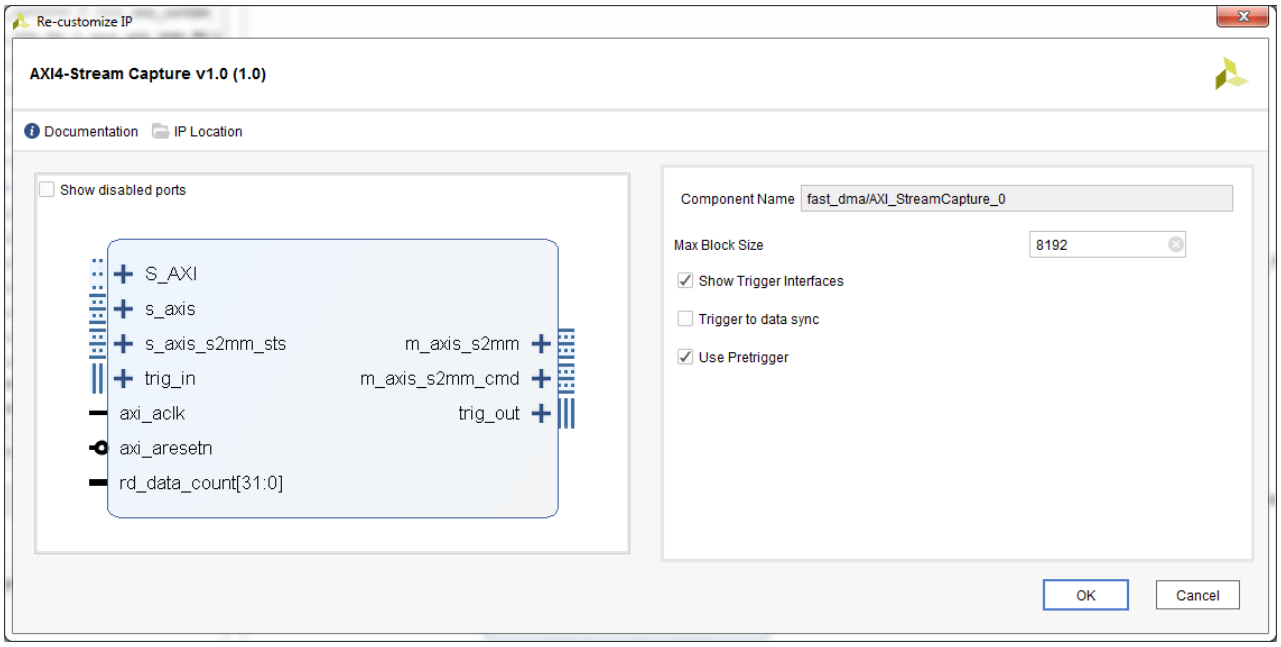
- Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
- Vivado Design Suite User Guide: Designing with IP (UG896)
- Vivado Design Suite User Guide: Getting Started (UG910)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

Core parameters

The re-customization dialog is as follows:



Show Trigger Interfaces

Check to enable trigger input and output.

Trigger to data sync

Use Pretrigger

Check to activate the pretrigger feature.

Constraining the Core

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the Vivado Design Suite User Guide:

- Designing with IP (UG896)

Example Design

There is no example Design for this IP core release.

Test Bench

There is no test bench for this IP core release.

Appx. A: Change History and Legal Notices

Document Change History

date	revision	authors	description
20xx-xx-xx	v.1	Name	initial release

Legal Notices

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