AXI4-Stream Concat

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IP Facts

Introduction

AXI4-Stream Concat core provides simple AXI4-Stream concat function.

Features

- Concat up to 3 AXI Streams
- Flexible AXI Stream data width
- 4 types of tvalid propagation

teCORE™ IP Facts Table	
Supported Device Family	Zynq® -7000, 7 Series
Supported User Interfaces	AXI4-Stream
Resources	
Special Features	
Provided with Core	
Design Files	VHDL Source Code
Constraint Files	Not Provided
Example Design	Not Provided
Test Bench	Not Provided
Simulation Model	Not Provided
Supported S/W Dirver	Not Provided
Tested Design Flows	
Design Entry	Vivado® Design Suite, IP Integrator
Simulation	Vivado Simulator
Synthesis	Vivado Synthesis
Tested Hardware Platforms	
Support	
Provided by Trenz Electronic GmbH	

Overview

Feature Summary

Licensing and Ordering Information

Product Specification

Performance

Resource Utilization

Port Description

Signal Name	Direction	Description
s_axis_aclk	Input	System clock
s_axis_aresetn	Input	System reset (active low)
sa_axis_tready	Output	Slave A AXI4-Stream interface ready
sa_axis_tdata	Input	Slave A AXI4-Stream interface data
sa_axis_tvalid	Input	Slave A AXI4-Stream interface valid
sb_axis_tready	Output	Slave B AXI4-Stream interface ready
sb_axis_tdata	Input	Slave B AXI4-Stream interface data
sb_axis_tvalid	Input	Slave B AXI4-Stream interface valid
sc_axis_tready	Output	Slave C AXI4-Stream interface ready
sc_axis_tdata	Input	Slave C AXI4-Stream interface data
sc_axis_tvalid	Input	Slave C AXI4-Stream interface valid
m_axis_tready	Input	Master AXI4-Stream interface ready
m_axis_tdata	Output	Master AXI4-Stream interface data
m_axis_tvalid	Output	Master AXI4-Stream interface valid

Designing with the Core

Define input AXI4-Stream interfaces quantity width and tvalid type. Output AXI4-Stream interface data will contain concated data from selected interfaces.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

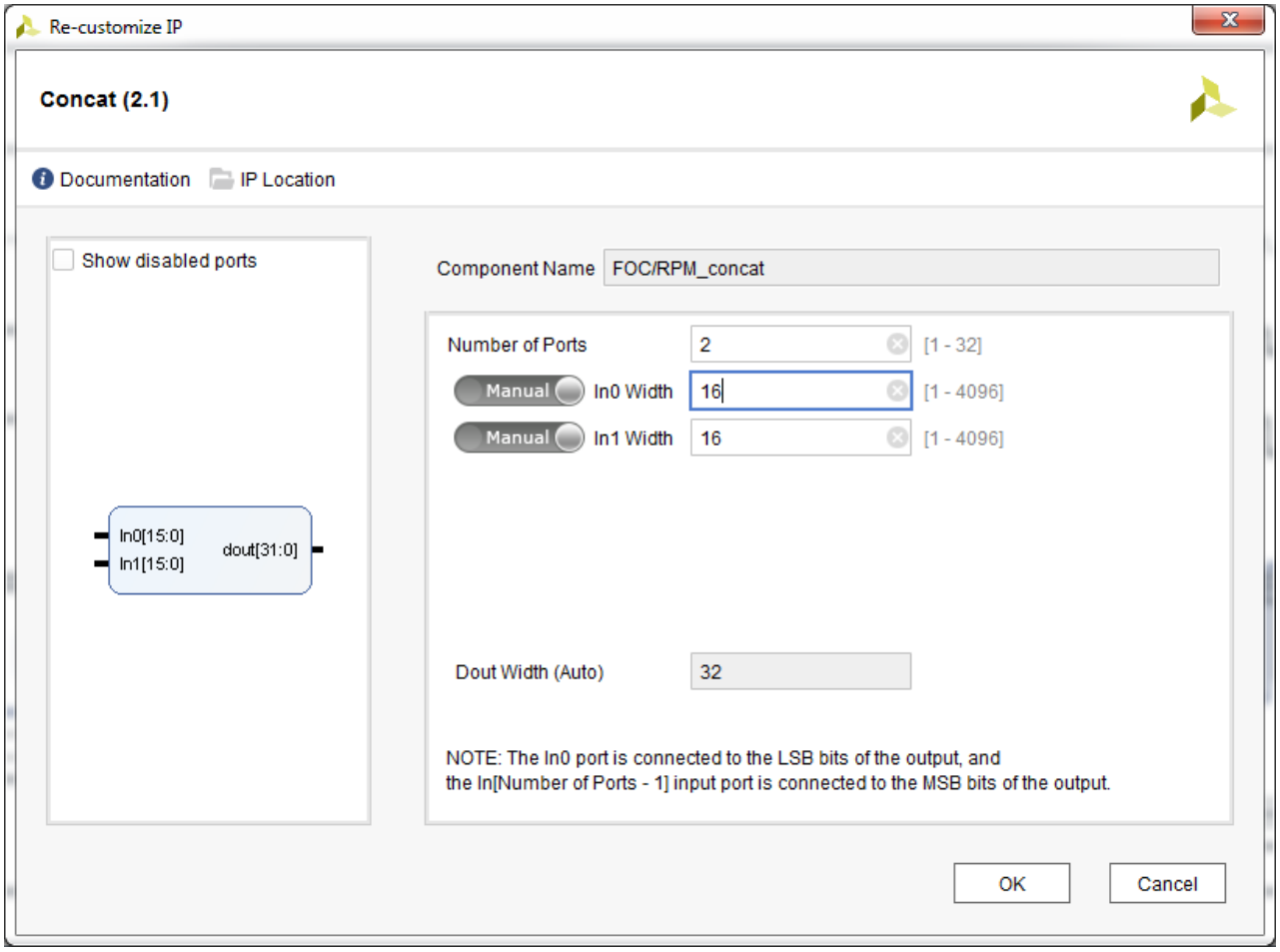
- Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
- Vivado Design Suite User Guide: Designing with IP (UG896)
- Vivado Design Suite User Guide: Getting Started (UG910)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

Core parameters

The re-customization dialogue is as follows:



Number of ports:

Enter the number of input ports.

In0 ... InX width:

Enter the width of the corresponding input port.

Dout Width:

The width of the output port is calculated automatically, no need to enter anything.

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the Vivado Design Suite User Guide:

- Designing with IP (UG896)

Example Design

There is no example Design for this IP core release.

Test Bench

There is no test bench for this IP core release.

Appx. A: Change History and Legal Notices

Document Change History

date	revision	authors	description
20xx-xx-xx	v.1	Name	initial release

Legal Notices

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