FOC with Vivado HLS IP Cores

1.0

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Contents

Chapter 1

Main Page

1.1 Introduction

This project demonstrates a FOC (Field-Oriented Control) motor control design based on IP cores developed with Vivado HLS. In the block design of this project, there is a hierarchy block named "FOC", which includes the FOC-related IP cores. All the IP cores used are listed in the table 1.1. See the chapter Utilization Design Information for the utilization report.

Table 1.1 A complete list of IP cores used

Name	Type	Description
PI Control	HLS Core	PI Contrllers for speed torque and flux
Clarke Direct	HLS Core	Clarke Direct Transform
Clarke Inverse	HLS Core	Clarke Inverse Transform
Park Direct	HLS Core	Park Direct Transform
Park Inverse	HLS Core	Park Inverse Transform
SVPWM	HLS Core	Space Vector Transform
Filters	HLS Core	Filters for input streams
FOC_Control	VHDL Core	FOC System mode control
AXI4-Stream Encoder Interface	VHDL Core	Angle encoder interface and rotate speed calculation
AXI4-Stream Concat	VHDL Core	AXIS buses concat utility core
AXI4-Stream Monitor	VHDL Core	AXIS monitor mux
AXI4-Stream Decimate	VHDL Core	AXIS decimation core
AXI Data Capture	VHDL Core	AXIS adapter core for AXI Datamover
AXI Register Bank 16/16	VHDL Core	AXI Register bank

1.2 Tools

The tools required are listed in the table 1.2.

For the development, only Vivado HLS is needed.

For the documentation Doxygen is used.

Table 1.2 Tools

Tool	Version	Notes
Vivado HLS	2017.1	HLS Development Environment
Doxygen	1.8.11	Documentation extraction
MiKTeX	2.9	PDF generation

Chapter 2

Utilization Design Information

Tool Version	Vivado v.2017.1 (win64) Build 1846317 Fri Apr 14 18:55:03 MDT 2017
Date	Wed Sep 27 21:21:30 2017
Host	W7-64-12 running 64-bit Service Pack 1 (build 7601)
Command	report_utilization -file zsys_wrapper_utilization_placed.rpt -pb zsys_wrapper_utilization_placed.pb
Design	zsys_wrapper
Device	7z010clg400-1
Design State	Fully Placed

Table 2.2 Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	5697	0	17600	32.37
LUT as Logic	5483	0	17600	31.15
LUT as Memory	214	0	6000	3.57
LUT as Distributed RAM	32	0		
LUT as Shift Register	182	0		
Slice Registers	9180	0	35200	26.08
Register as Flip Flop	9180	0	35200	26.08
Register as Latch	0	0	35200	0.00
F7 Muxes	130	0	8800	1.48
F8 Muxes	0	0	4400	0.00

Table 2.3 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
126	Yes	-	Set
143	Yes	-	Reset
322	Yes	Set	-
8589	Yes	Reset	-

Table 2.4 Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	2892	0	4400	65.73
SLICEL	1875	0		
SLICEM	1017	0		
LUT as Logic	5483	0	17600	31.15
using O5 output only	28			
using O6 output only	4316			
using O5 and O6	1139			
LUT as Memory	214	0	6000	3.57
LUT as Distributed RAM	32	0		
using O5 output only	0			
using O6 output only	16			
using O5 and O6	16			
LUT as Shift Register	182	0		
using O5 output only	1			
using O6 output only	76			
using O5 and O6	105			
LUT Flip Flop Pairs	2865	0	17600	16.28
fully used LUT-FF pairs	413			
LUT-FF pairs with one unused LUT output	2276			
LUT-FF pairs with one unused Flip Flop	2131			
Unique Control Sets	408			

Note: Review the Control Sets Report for more information regarding control sets.

Table 2.5 Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	14	0	60	23.33
RAMB36/FIFO∗	11	0	60	18.33
RAMB36E1 only	11			
RAMB18	6	0	120	5.00
RAMB18E1 only	6			

Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

Table 2.6 DSP

Site Type	Used	Fixed	Available	Util%
DSPs	30	0	80	37.50
DSP48E1 only	30			

Table 2.7 IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	22	22	100	22.00
IOB Master Pads	11			
IOB Slave Pads	11			

Site Type	Used	Fixed	Available	Util%
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	130	130	130	100.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	96	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	100	0.00
OLOGIC	1	1	100	1.00
OUTFF_ODDR_Register	1	1		

Table 2.8 Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	4	0	32	12.50
BUFIO	0	0	8	0.00
MMCME2_ADV	1	0	2	50.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

Table 2.9 Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

Table 2.10 Primitives

Ref Name	Used	Functional Category
FDRE	8589	Flop & Latch
LUT3	2051	LUT
LUT2	1702	LUT
LUT6	1060	LUT
LUT4	900	LUT
CARRY4	698	CarryLogic
LUT5	491	LUT
LUT1	418	LUT
FDSE	322	Flop & Latch
SRL16E	240	Distributed Memory

Ref Name	Used	Functional Category
FDCE	143	Flop & Latch
MUXF7	130	MuxFx
BIBUF	130	IO
FDPE	126	Flop & Latch
SRLC32E	47	Distributed Memory
DSP48E1	30	Block Arithmetic
RAMS32	24	Distributed Memory
RAMD32	24	Distributed Memory
RAMB36E1	11	Block Memory
OBUF	11	IO
IBUF	11	IO
RAMB18E1	6	Block Memory
BUFG	3	Clock
PS7	1	Specialized Resource
ODDR	1	IO
MMCME2_ADV	1	Clock
BUFGCTRL	1	Clock

Table 2.11 Black Boxes

Ref Name	Used

Table 2.12 Instantiated Netlists

Ref Name	Used
zsys_zero_16_0	1
zsys_xlslice_6_0	1
zsys_xlslice_5_0	1
zsys_xlslice_4_0	1
zsys_xlslice_3_0	1
zsys_xlslice_2_0	1
zsys_xlslice_1_0	1
zsys_xlconcat_2_0	1
zsys_xlconcat_1_0	1
zsys_xlconcat_0_0	1
zsys_xbar_0	1
zsys_tx_fifo_0	1
zsys_rx_fifo_0	1
zsys_rpm_check_0_0	1
zsys_processing_system7_0↩ _0	1
zsys_proc_sys_reset_1_0	1
zsys_proc_sys_reset_0_0	1
zsys_mode_slice_0	1
zsys_mode_concat_0_0	1
zsys_foc_control_0_0	1
zsys_clk_wiz_0_0	1
zsys_clk_mux_0_0	1
zsys_axis_pwm_0_0	1
zsys_axis_monitor_0_0	1

Ref Name	Used
zsys_axis_encoder_0_0	1
zsys_axis_decimate_0_0	1
zsys_axis_data_fifo_1_0	1
zsys_axis_data_fifo_0_0	1
zsys_axis_broadcaster_0_1	1
zsys_axis_broadcaster_0_0	1
zsys_axis_AD7403_0_0	1
zsys_axi_reg32_0_0	1
zsys_axi_datamover_0_0	1
zsys_auto_pc_1	1
zsys_auto_pc_0	1
zsys_Torque_Sp_slice_0	1
zsys_Torque_PI_Control_0	1
zsys_Torque_Kp_slice_0	1
zsys_Torque_Ki_slice_0	1
zsys_SVPWM_0_0	1
zsys_RPM_Sp_slice_0	1
zsys_RPM_PI_Control_0	1
zsys_RPM_Kp_slice_0	1
zsys_RPM_Ki_slice_0	1
zsys_Park_Inverse_0_0	1
zsys_Park_Direct_0_0	1
zsys_Ib_Ia_0	1
zsys_Flux_Sp_slice_0	1
zsys_Flux_PI_Control_0	1
zsys_Flux_Kp_slice_0	1
zsys_Flux_Ki_slice_0	1
zsys_Filters_0_0	1
zsys_Clarke_Inverse_0_0	1
zsys_Clarke_Direct_0_0	1
zsys_Angle_concat_0	1
zsys_Angle_Shift_slice_0	1
zsys_Angle_RPM_Ib_Ia_0	1
zsys_AXI_StreamCapture_0↩ _0	1