SDSoC Hardware Platform ARTY-Z7

1.0

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Contents

Chapter 1

Main Page

1.1 Introduction

TODO: Introduction Project is used to demonstrate FOC system build based on Vivado HLS blocks. Block design contain FOC hierarchy block, this block include main IP cores used to build motor control system. Cores used:

Name	Type	Desctiption
PI Control	HLS Core	PI Contrllers for speed torque and flux
Clarke Direct	HLS Core	Clarke Direct Transform
Clarke Inverse	HLS Core	Clarke Inverse Transform
Park Direct	HLS Core	Park Direct Transform
Park Inverse	HLS Core	Park Inverse Transform
SVPWM	HLS Core	Space Vector Transform
Filters	HLS Core	Filters for input streams
FOC_Control	VHDL Core	FOC System mode control
AXI4-Stream Encoder Interface	VHDL Core	Angle encoder interface and rotate speed calculation
AXI4-Stream Concat	VHDL Core	AXIS buses concat utility core
AXI4-Stream Monitor	VHDL Core	AXIS monitor mux
AXI4-Stream Decimate	VHDL Core	AXIS decimation core
AXI Data Capture	VHDL Core	AXIS adapter core for AXI Datamover
AXI Register Bank 16/16	VHDL Core	AXI Register bank

1.2 Tools

The tools required are listed in the table 1.2.

For the development, only Vivado HLS is needed.

For the documentation Doxygen is used.

Table 1.2 Tools

Tool	Version	Notes
Vivado HLS	2017.1	HLS Development Environment
Doxygen	1.8.11	Documentation extraction
MiKTeX	2.9	PDF generation

Chapter 2

Utilization Design Information

Tool Version	Vivado v.2017.1 (win64) Build 1846317 Fri Apr 14 18:55:03 MDT 2017
Date	Thu Jul 6 21:50:21 2017
Host	W7-64-12 running 64-bit Service Pack 1 (build 7601)
Command	report_utilization -file zsys_wrapper_utilization_placed.rpt -pb zsys_wrapper_utilization_placed.pb
Design	zsys_wrapper
Device	7z020clg400-1
Design State	Fully Placed

Table 2.2 Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	5191	0	53200	9.76
LUT as Logic	5012	0	53200	9.42
LUT as Memory	179	0	17400	1.03
LUT as Distributed RAM	32	0		
LUT as Shift Register	147	0		
Slice Registers	8516	0	106400	8.00
Register as Flip Flop	8516	0	106400	8.00
Register as Latch	0	0	106400	0.00
F7 Muxes	98	0	26600	0.37
F8 Muxes	0	0	13300	0.00

Table 2.3 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
105	Yes	-	Set
62	Yes	-	Reset
420	Yes	Set	-
7929	Yes	Reset	-

Table 2.4 Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	3215	0	13300	24.17
SLICEL	2097	0		
SLICEM	1118	0		
LUT as Logic	5012	0	53200	9.42
using O5 output only	0			
using O6 output only	3909			
using O5 and O6	1103			
LUT as Memory	179	0	17400	1.03
LUT as Distributed RAM	32	0		
using O5 output only	0			
using O6 output only	16			
using O5 and O6	16			
LUT as Shift Register	147	0		
using O5 output only	2			
using O6 output only	76			
using O5 and O6	69			
LUT Flip Flop Pairs	2461	0	53200	4.63
fully used LUT-FF pairs	348			
LUT-FF pairs with one unused LUT output	1948			
LUT-FF pairs with one unused Flip Flop	1879			
Unique Control Sets	394			

Note: Note: Review the Control Sets Report for more information regarding control sets.

Table 2.5 Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	13	0	140	9.29
RAMB36/FIFO∗	10	0	140	7.14
RAMB36E1 only	10			
RAMB18	6	0	280	2.14
RAMB18E1 only	6			

Note: Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

Table 2.6 DSP

Site Type	Used	Fixed	Available	Util%
DSPs	27	0	220	12.27
DSP48E1 only	27			

Table 2.7 IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	12	12	125	9.60
IOB Master Pads	7			

Site Type	Used	Fixed	Available	Util%
IOB Slave Pads	5			
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	130	130	130	100.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00
IDELAYCTRL	0	0	4	0.00
IBUFDS	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	125	0.00
OLOGIC	1	1	125	0.80
OUTFF_ODDR_Register	1	1		

Table 2.8 Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	16	0.00
MMCME2_ADV	0	0	4	0.00
PLLE2_ADV	0	0	4	0.00
BUFMRCE	0	0	8	0.00
BUFHCE	0	0	72	0.00
BUFR	0	0	16	0.00

Table 2.9 Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

Table 2.10 Primitives

Ref Name	Used	Functional Category
FDRE	7929	Flop & Latch
LUT3	1865	LUT
LUT2	1343	LUT
LUT4	1049	LUT
LUT6	974	LUT
CARRY4	560	CarryLogic
LUT5	528	LUT
FDSE	420	Flop & Latch
LUT1	356	LUT

Ref Name	Used	Functional Category
SRL16E	169	Distributed Memory
BIBUF	130	IO
FDPE	105	Flop & Latch
MUXF7	98	MuxFx
FDCE	62	Flop & Latch
SRLC32E	47	Distributed Memory
DSP48E1	27	Block Arithmetic
RAMS32	24	Distributed Memory
RAMD32	24	Distributed Memory
RAMB36E1	10	Block Memory
OBUF	7	IO
RAMB18E1	6	Block Memory
IBUF	5	IO
PS7	1	Specialized Resource
ODDR	1	IO
BUFG	1	Clock

Table 2.11 Black Boxes

Ref Name	Used

Table 2.12 Instantiated Netlists

Ref Name	Used
zsys_xlslice_1_0	1
zsys_xlslice_0_0	1
zsys_xlconcat_0_0	1
zsys_xbar_0	1
zsys_tx_fifo_0	1
zsys_rx_fifo_0	1
zsys_processing_system7_0_0	1
zsys_proc_sys_reset_0_0	1
zsys_foc_control_0_0	1
zsys_axis_pwm_0_0	1
zsys_axis_monitor_0_0	1
zsys_axis_encoder_0_0	1
zsys_axis_decimate_0_0	1
zsys_axis_data_fifo_0_0	1
zsys_axis_broadcaster_0_1	1
zsys_axis_broadcaster_0_0	1
zsys_axis_AD7403_0_0	1
zsys_axi_reg32_0_0	1
zsys_axi_datamover_0_0	1
zsys_auto_pc_1	1
zsys_auto_pc_0	1
zsys_Torque_Sp_slice_0	1
zsys_Torque_PI_Control_0	1
zsys_Torque_Kp_slice_0	1
zsys_Torque_Ki_slice_0	1

Ref Name	Used
zsys_SVPWM_0_0	1
zsys_RPM_Sp_slice_0	1
zsys_RPM_PI_Control_0	1
zsys_RPM_Kp_slice_0	1
zsys_RPM_Ki_slice_0	1
zsys_Park_Inverse_0_0	1
zsys_Park_Direct_0_0	1
zsys_Ib_Ia_0	1
zsys_Flux_Sp_slice_0	1
zsys_Flux_PI_Control_0	1
zsys_Flux_Kp_slice_0	1
zsys_Flux_Ki_slice_0	1
zsys_Filters_0_0	1
zsys_Clarke_Inverse_0_0	1
zsys_Clarke_Direct_0_0	1
zsys_Angle_concat_0	1
zsys_Angle_Shift_slice_0	1
zsys_Angle_RPM_Ib_Ia_0	1
zsys_AXI_OldData_Capture_0↩ _0	1