XILINX, INC.
DEVELOPMENT AND MARKETING AGREEMENT

THIS DEVELOPMENT AND MARKETING AGREEMENT ("**Agreement**") is made and entered into as of the 22 December 2016 (the "**Effective Date**") by and between Xilinx, Inc., a Delaware corporation with a place of business at 2100 Logic Drive, San Jose, California, 95124 ("**Xilinx**") and Trenz Electronic GmbH, a legal entity organized under the laws of Germany with principal offices at Holzweg 19A 32257 Bunde, Germany ("**Developer**").

RECITALS

A. Xilinx desires to have Developer design, develop and deliver certain Deliverables (as defined below), and to promote such Deliverables for use with Xilinx devices, as further specified in this Agreement.

B. Developer has expertise in the design and development of such Deliverables, and desires to design, develop, deliver and promote such Deliverables, as further specified in this Agreement.

C. Developer desires to permit Xilinx to also market and promote such Deliverables, as further specified in this Agreement.

AGREEMENT

NOW, THEREFORE, in consideration of the mutual covenants and obligations set out herein, and for other good and valuable consideration the receipt and sufficiency of which the parties acknowledge, the parties agree as follows:

1. **Definitions and Interpretation**

1.1 **"Affiliate"** means an entity that (i) controls or is controlled by a party, or (ii) is under common control with a party; where "control" means that more than fifty percent (>50%) of the controlled entity's shares or ownership interest representing the right to make decisions for such entity are owned or controlled, directly or indirectly, by the controlling entity.

1.2 **"Background Technology"** means any Technology that is owned by Developer prior to or independent of any work performed by Developer in connection with this Agreement.

1.3 **"Covered Technology"** means (i) with respect to Developer, the Deliverables, and (ii) with respect to Xilinx, the Xilinx Technology.

1.4 **"Deliverables"** means (i) all Technology to be developed by Developer hereunder, and (ii) all Technology delivered by Developer hereunder; as such may be more fully described in the SOW, excluding Xilinx Technology.

1.5 **"Excluded License"** means any license that requires, as a condition of use, modification

and/or distribution of any Technology subject to such license, that such Technology and/or other Technology combined and/or distributed with such Technology be: (a) disclosed or distributed in source code form; (b) licensed for the purpose of making derivative works; or (c) redistributable at no charge.

1.6 **"Foreground Technology"** means any Technology that is conceived, discovered, created, derived, invented, reduced to practice, made or developed by Developer (whether solely, or by a subcontractor, or jointly with any subcontractor, as applicable) in the course of performing work under this Agreement.

1.7 **"Intellectual Property Rights"** means all intellectual property and industrial rights of any nature, now or hereafter existing, and all renewals and extensions thereof, under the laws of any state, country or jurisdiction in the world, including without limitation rights afforded under laws related to trade secrets, copyrights, moral rights, rights of publicity, trademarks and service marks and other designations of source or origin, patents (including existing patents and patent applications, and any continuations, continuations-in-part, divisionals, re-examinations, reissues and the like with respect thereto) and goodwill and, in each case, whether or not any of the foregoing are registered, unregistered or unregistrable.

1.8 **"Modifications"** means all modifications, changes, alterations, improvements and enhancements made to Xilinx Technology owned now or in the future by Xilinx.

1.9 **"Open Source Technology"** means any Technology for which the copyright is owned by a third party and which is commonly available, typically free of charge, under various licenses such as without limitation the Apache Software License, Artistic License, BSD License, Common Public License, GNU General Public License, GNU Library General Public License, GNU Lesser General Public License, or Mozilla Public License.

1.10 **"Residual Information"** means information in non-tangible form of knowledge, know-how, concepts, ideas or techniques that is retained in unaided memory by Xilinx personnel who have received the Deliverables or Confidential Information under this Agreement**.**

1.11 **"SOW"** means the statement of work attached hereto as *Exhibit A*.

1.12 **"Specifications**" means all functional, performance and similar technical descriptions, specifications, requirements and acceptance criteria regarding a Deliverable, as such may be more fully described in this Agreement or the SOW or documents referenced in the SOW or as otherwise mutually agreed by the parties in writing.

1.13 **"Technology"** means any and all products, materials, data, information, technology or other property of a scientific, technical or artistic nature, whether tangible or intangible, whether oral, visual, electronic or recorded in any form of medium, including but not limited to inventions (whether or not protectable under patent laws), processes, techniques, methodologies, sketches, drawings, models, apparatus,

equipment, machines, devices, integrated circuits, hardware, design tools, software, formulae, algorithms, designs, design files, source code (in any language), documentation, specifications, plans, reports, and other subject matter protectable under Intellectual Property Rights including but not limited to know-how, ideas, works of authorship, new or useful art, combinations, developments and discoveries.

1.14 "**Term**" means the term of this Agreement.

1.15 **"Third-Party Technology"** means any Technology not owned by Xilinx or Developer.

1.16 **"Time Schedule"** means the working timetable identified in the SOW as the same may be amended in writing by both parties from time to time during the Term.

1.17 **"Xilinx Competitor"** means any company that designs, makes (or has made for it) and sells programmable semiconductor devices, including without limitation Altera, Cypress, Lattice, Microsemi and QuickLogic and any of their respective successors.

1.18 **"Xilinx Technology"** means Technology owned by Xilinx and provided by Xilinx to Developer pursuant to this Agreement.

1.19 Unless otherwise provided, references to sections, paragraphs, schedules and exhibits are to sections, paragraphs, schedules and exhibits contained in this Agreement and reference to this Agreement includes reference to its exhibits.

1.20 Headings are inserted for convenience only and do not affect the construction of this Agreement.

1.21 Unless expressly stated in this Agreement or the context otherwise admits or requires, any reference in this Agreement to: (i), any other document or any specified provision of this Agreement or any other document is a reference to this Agreement, to such other document or to such provision as in force for the time being and as amended, extended, varied, assigned, novated, restated or supplemented from time to time; and (ii) words such as "hereby", "hereunder", "hereto", "hereof" and "herein" and other words commencing with "here" shall (unless the context clearly indicates to the contrary) refer to the whole of this Agreement and not to any particular section, clause, paragraph or schedule of this Agreement.

2. Development

2.1 **SOW Preparation.** Developer shall be responsible for identifying in the SOW: (i) all Background Technology; and (ii) all Third-Party Technology that Developer requires to develop the Deliverables.

2.2 **Obligation.** Developer shall develop the Deliverables in accordance with the agreed upon Specifications and the Time Schedule, and all other provisions of this Agreement and the SOW.

2.3 **Communication.** Xilinx and Developer shall each designate a technical contact (each, a "**Technical Contact**") in the SOW, which Technical Contacts shall serve as the primary individuals responsible for facilitating communication between Xilinx and Developer and for coordinating any meetings or other joint activities contemplated in connection with this Agreement. Each party may change its Technical Contact upon written notice to the other party and shall notify the other party as soon as practicable in the event that its current Technical Contact is no longer available.

2.4 **Changes.** The Technical Contacts shall arrange and facilitate appropriate discussions from time to time regarding any changes to the Deliverables, the Specifications or the Time Schedule perceived as necessary or desirable by either party. No such changes shall be effective unless agreed upon by both parties in writing.

2.5 **Delivery.** Developer shall deliver all Deliverables to Xilinx when and in the form designated in the SOW or as otherwise expressly agreed to by Xilinx.

2.6 **Acceptance.** Upon delivery of each Deliverable to Xilinx as required under the mutually agreed schedule in the SOW, Xilinx will test and evaluate the Deliverable to determine if it conforms to the Specifications. If in its opinion, such Deliverable fails to conform to the Specifications, Xilinx will deliver to Developer a written report describing the nonconformity. If no report is delivered to Developer within the thirty (30) days following delivery to Xilinx, such Deliverable will be deemed accepted. Developer will have a maximum of ten (10) days, unless the parties agree that a longer period of time is appropriate due to the nature of the non-conformity, from receipt of each report and non-conforming Deliverable to correct the nonconformity and deliver a corrected Deliverable to Xilinx. If Xilinx determines (acting reasonably) that the nonconformance has not been remedied in a manner consistent with the Specifications, Xilinx may at its option either (a) again reject the Deliverable and repeat the procedure set forth in this Section 2.6, or (b) at Xilinx's discretion, terminate this Agreement upon written notice and withhold additional payments, if any.

3. **Ownership of Intellectual Property Rights**

3.1 **By Developer.**

3.1.1 Developer shall retain ownership of its Intellectual Property Rights to Background Technology to the same extent that Developer has ownership of the same.

3.1.2 Except as otherwise provided in Sections 3.1.3 and 3.2.2, Developer shall retain ownership of its Intellectual Property Rights to all Foreground Technology.

3.1.3 **Exclusivity.** Notwithstanding Section 3.1.2 above, Developer agrees for a period of three (3) years following final acceptance by Xilinx (per Section 2.6 above) of the last Deliverable hereunder, to refrain from (a) granting permission to any third party (other than Xilinx or Affiliates of Xilinx) to use, reproduce, distribute or otherwise exploit the Foreground Technology for any purpose other than the

programming or interoperating with a Xilinx semi-conductor device; and (b) providing the Foreground Technology to any Xilinx Competitor. Developer shall consult Xilinx in advance in a timely manner to the extent that there is any reasonable doubt as to whether a party constitutes a Xilinx Competitor.

3.2 **By Xilinx**:

3.2.1 Xilinx shall retain ownership of its Intellectual Property Rights to the Xilinx Technology.

3.2.2 To the extent that Foreground Technology includes any Modifications, Developer hereby unconditionally agrees to and hereby does assign to Xilinx exclusive ownership of all such Modifications and all rights, title and interest, including without limitation all Intellectual Property Rights, related thereto.

3.2.3 Developer agrees to cooperate with and assist Xilinx upon request in actions to obtain, perfect, maintain, enforce, give effect to or transfer Xilinx's rights under Section 3.2.2, including without limitation executing documents associated therewith. If called upon to render assistance under this Section 3.2.3, Developer shall be entitled to a fair and reasonable fee for such services, including reimbursement of expenses pre-approved by Xilinx.

4. **License Grants from Xilinx.** Xilinx hereby grants to Developer, during the term of this Agreement, a personal, world-wide, royalty-free, limited, revocable (in the event of a breach of this Agreement or Developer's failure to develop the Deliverables pursuant to section 2.2 above), non-exclusive, non-transferable, non-sublicensable license to use the Xilinx Technology on an internal basis solely for reference purposes in developing the Deliverables for the benefit of Xilinx under this Agreement.

5. **License Grants from Developer**

5.1 Deliverables. Developer hereby grants to Xilinx a worldwide, non-exclusive, perpetual, irrevocable, royalty-free, fully-paid-up license:

5.1.1 to use, market, reproduce, promote and demonstrate the Deliverables; and

5.1.2 to grant to third parties non-exclusive licenses to internally test and evaluate the Deliverables and Xilinx may reproduce and distribute the Deliverables for such purposes.

5.2 Foreground Technology. Developer hereby grants to Xilinx a worldwide, non-exclusive, perpetual, irrevocable, transferable, sublicensable, royalty-free, fully-paid-up license, under its Intellectual Property Rights in and to all Foreground Technology, to make, have made, use, sell, offer for sale, import, copy, reproduce, distribute, modify, create derivative works of, publicly perform, publicly display, market, promote, license, transfer, disclose, rent, lease, and lend such Foreground Technology in any manner that Xilinx may now or hereafter desire.

5.3 Background Technology. With respect to any Background Technology which are necessary to use, sell or otherwise exploit a Deliverable and/or to give effect to the rights granted to Xilinx under Sections 5.1 and 5.2 above, Developer hereby grants to Xilinx a worldwide, non-exclusive, perpetual, irrevocable, transferable, sub-licensable, royalty-free, fully-paid-up license, under its Intellectual Property Rights in and to such Background Technology. Xilinx shall not grant to customers a license regarding any Background Technology which allows customers to use the Background Technology in products sold on a commercial basis.

5.4 To the extent that any Third-Party Technology is included in or constitutes all or part of a Deliverable, Developer agrees to and hereby does convey to Xilinx all rights necessary for Xilinx to exploit the same, which shall not be less than those rights granted elsewhere in this Section 5. Developer represents and warrants that: (i) it will not provide or include in any Deliverable any Third Party Technology without Xilinx's prior written consent; and (ii) if and to the extent that Developer does include Third Party Technology, Developer has obtained all necessary permissions, licenses, consents and has the authority to deliver such Third-Party Technology to Xilinx and to grant such rights.

5.5 All rights and licenses granted to Xilinx hereunder may be exercised by Affiliates of Xilinx.

5.6 Except as otherwise expressly set forth in this Agreement, no licenses are granted, whether by implication, estoppel or otherwise, with respect to the Intellectual Property Rights of either party.

6. Payment Terms

6.1 **Expenses.** Except as otherwise expressly agreed by Xilinx in the SOW, Developer will be solely responsible for all costs and expenses incurred by it in developing the Deliverables and in performing all of its obligations in connection with this Agreement, including without limitation paying for any software, hardware, equipment, tools or other Technology, all licenses to Intellectual Property Rights, and all personnel, materials and facilities, that Developer needs to develop the Deliverables.

6.2 **Payments.** Subject to the terms and conditions of this Agreement, Xilinx agrees to pay to Developer the amounts set forth in the SOW hereto as full compensation for meeting all requirements of this Agreement and the SOW, net forty-five (45) days following receipt of Developer's invoices for same (which invoices may not be sent prior to satisfying all applicable criteria specified for such milestone or other invoicing criteria). All amounts shall be listed and all payment shall be made in U.S. Dollars.

6.3 **Taxes.**

6.3.1 **Xilinx Taxes**: Prices set forth in the SOW are exclusive of all federal, state,

municipal or other government sales, use, value added or like taxes or duties now in force or enacted in the future that Developer may be required to collect from Xilinx or pay on behalf of Xilinx on invoice or delivery of the Deliverables under this Agreement ("**Transaction Taxes**"). Any such applicable Transaction Taxes that Developer seeks to collect from Xilinx shall be separately itemized on Developer's invoices. Xilinx agrees to pay such Transaction Taxes unless Xilinx is exempt therefrom. If Xilinx claims that it is exempt from such Transaction Taxes, Xilinx will provide Developer with an exemption resale certificate or other appropriate evidence to show that it is exempt from the relevant taxes.

6.3.2 **Developer Taxes**: Developer shall be solely responsible for taxes on income arising from amounts Xilinx pays to Developer under this Agreement. In addition, all payments by Xilinx to Developer pursuant to this Agreement shall be made net of any applicable withholding tax. If a tax authority takes an action against Xilinx in connection with the withholding taxes applicable under this Agreement, Xilinx will promptly notify Developer thereof, and Xilinx will, upon Developer's reasonable request and at Developer's expense, take such actions as may be customary, reasonable, and lawful to assist Developer in reducing such withholding tax liability. If Xilinx is required to pay any withholding tax after making its payment to Developer, Xilinx will provide to Developer evidence of such payments, and Developer shall reimburse such amount to Xilinx within 30 days thereof.

7. **Marketing.**

7.1 **Developer Obligations.** Developer shall comply with all obligations as set forth in marketing plan set forth in Exhibit B attached hereto, pursuant to the terms and conditions of this Agreement and the terms and conditions set forth in the plan.

7.2 **Publicity.** Neither party shall, without the other party's prior written approval, make any public announcement or disclosure as to the existence or matters set forth in this Agreement.

8. **Warranties.** Developer represents and warrants that:

8.1 the Deliverables shall conform to the Specifications for a period of twelve (12) months after delivery;

8.2 it shall: (i) perform all services provided to Xilinx hereunder in a professional and workmanlike manner with all due skill, care and diligence and in accordance with all applicable laws and legal requirements; and (ii) dedicate sufficient resources as determined in its reasonable discretion to fulfill all services provided to Xilinx hereunder in an adequate and timely manner using personnel who are appropriately experienced and qualified;

8.3 it has all rights, powers and authority to grant the rights and licenses granted hereunder

and is under no disability, restriction or prohibition, whether contractual or otherwise, with respect to the execution and entry into this Agreement and performance of its obligations under this Agreement;

8.4 the Background Technology and its contribution to the Deliverables does not and will not, to the best of Developer's knowledge, at the time of delivery to Xilinx, infringe any Intellectual Property Right of any third party;

8.5 as of the Effective Date, Developer has received no claims and has no knowledge of any claims related to the actual or alleged infringement of any Intellectual Property Rights with respect to the Deliverables;

8.6 except with Xilinx's prior written agreement in strict compliance with Section 5.4 above, the Deliverables will be the original work product of Developer and shall not, in whole or in part, contain or be comprised of any Third-Party Technology including, without limitation, any Open Source Technology, or any Technology governed by an Excluded License;

8.7 except unless otherwise expressly agreed by Xilinx in the SOW, no portion of the Deliverables shall contain, at the time of delivery, any virus, "back door," "time bomb," "Trojan horse," "worm," "drop-dead device" or other feature designed to (i) permit unauthorized access to, or use of, the Deliverables or computer systems on which the Deliverables are loaded, (ii) disable, damage or erase the Deliverables or data, or (iii) perform any other similar actions that would preclude full use of the Deliverables by Xilinx or other applicable third parties; and

8.8 it has entered into all necessary agreements in order to ensure that all Intellectual Property Rights created by its personnel or sub-contractors in connection with this Agreement and the SOW will vest in the Developer and not the relevant personnel or sub-contractors;

8.9 it shall strictly abide by, and have its personnel and subcontractors abide by any and all applicable laws, regulations, ordinances, or statutes with respect to the development of the Deliverables hereunder.

8.10 **Disclaimer.** THE FOREGOING WARRANTIES ARE IN LIEU OF ALL OTHER WARRANTIES OR CONDITIONS, AND EXCEPT FOR THE EXPRESS WARRANTIES OR CONDITIONS STATED IN THIS AGREEMENT, NEITHER PARTY MAKES ANY ADDITIONAL WARRANTIES OR CONDITIONS, EXPRESS OR IMPLIED, AS TO ANY MATTER WHATSOEVER. IN PARTICULAR, ANY AND ALL WARRANTIES AND CONDITIONS OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE EXPRESSLY EXCLUDED TO THE FULLEST EXTENT PERMITTED BY LAW AND THE PARTIES AGREE THAT THIS IS FAIR AND REASONABLE.

9. **Indemnification.** Each party (an "**Indemnitor**") shall, at its expense, indemnify, defend and hold harmless the other party and its Affiliates (an "**Indemnitee**") from and against any

claims, suits, losses, liabilities, damages, court judgments or awards and the associated costs and expenses (including reasonable attorneys' fees) incurred as a result of the actual or alleged misappropriation or infringement of any third party Intellectual Property Rights or Third-Party Technology by the Indemnitee's possession, use, distribution or other exploitation (to the extent so authorized under this Agreement) of the Indemnitor's Covered Technology and/or its Background Technology (if applicable). In such case, the Indemnitee shall (a) provide the Indemnitor with prompt notice of such claim, (b) tender control of the defense and settlement of such claim to the Indemnitor, and (c) assist and cooperate with the Indemnitor as requested, at Indemnitor's expense. Should the possession, use, distribution or other exploitation (to the extent so authorized under this Agreement) of the Indemnitor's Covered Technology and/or its Background Technology subject to a claim be enjoined, or, in the event the Indemnitor reasonably believes such use may be enjoined, Indemnitor may, at its option, either: (i) substitute a fully equivalent non-infringing unit of the Covered Technology and/or its Background Technology (if applicable); (ii) modify the infringing Covered Technology and/or its Background Technology (if applicable), so that it no longer infringes but remains functionally equivalent; or (iii) if neither (i) nor (ii) is commercially feasible, obtain for the other party the right to continue use thereof. The Indemnitee shall not be entitled to be indemnified by the Indemnitor under this Section 9 to the extent that the infringement arises from changes or modifications by the Indemnitee or has resulted from the combination of the Indemnitor's Covered Technology (as applicable) with the Technology of the Indemnitee.

10. **Confidentiality.**

10.1 **Confidential Information.** "**Confidential Information**" shall mean information disclosed by one party (the "**Disclosing Party**") to the other party (the "**Recipient**"), subject to the provisions of this Section 10 below, and may include, but is not limited to, information relating to products, product specifications, product roadmaps, product design and manufacturing, business strategies and plans, customer lists, research and development, and such other information disclosed either (i) in written or other tangible form and marked "Confidential" or with words of similar import, or (ii) under circumstances by which the Recipient should reasonably understand such information is to be treated as confidential, whether or not marked "Confidential" or otherwise. Confidential Information of Xilinx includes, without limitation, the Xilinx Technology and the terms and conditions of this Agreement.

10.2 **Exceptions.** The obligations of confidentiality under this Agreement shall not apply to information that: (a) is already known to the Recipient at the time of disclosure without obligation of confidentiality, (b) is or becomes publicly known through no wrongful act or omission of the Recipient; (c) is rightfully received by the Recipient from a third party without obligation of confidentiality; (d) is approved for release by written authorization of the Disclosing Party; or (e) was developed by the Recipient independently and without the use or benefit of any of the Confidential Information. A disclosure of Confidential Information that is required to be made by the Recipient pursuant to any order or requirement of a court, administrative agency, or any other

governmental agency shall not be deemed a breach of this Agreement, provided that the Recipient shall: (i) immediately notify the Disclosing Party in writing of such order or requirement, (ii) give the Disclosing Party an opportunity to contest disclosure or seek an appropriate protective order, and (iii) cooperate with Disclosing Party to narrow the scope of such disclosure to only that portion of the Confidential Information which is necessary to fulfill the order or requirement.

10.3 **Duties.** Recipient agrees, for a period of five (5) years from the date of last disclosure, (but perpetually for Xilinx's source code), not to: (i) use Disclosing Party's Confidential Information for any reason, other than to exercise the rights and licenses granted to it in this Agreement and to fulfill its obligations under this Agreement (the "**Purpose**"); and (ii) disclose the Disclosing Party's Confidential Information to any third party except its employees, consultants, independent sales representatives and Affiliates, and employees and consultants, independent sales representatives of Affiliates that (a) have a legitimate "need to know" for furtherance of the Purpose, and (b) are subject to confidentiality obligations no less restrictive than those set forth herein. Recipient shall exercise the same degree of care in protecting Disclosing Party's Confidential Information that it uses for its own confidential information of a similar nature, but in no event less than reasonable care.

10.4 **Other Rights.** Nothing herein shall be deemed to restrict Xilinx's rights to the Deliverables, Foreground Technology and Background Technology to the extent set forth in Sections 3 or 5 above.

10.5 **Use of Residual Information.** Developer acknowledges and agrees that Xilinx and its personnel may utilize for any purpose and the restrictions of this Section 10 shall not apply to any Residual Information. However, the foregoing shall not be deemed a license or waiver under any valid patents or copyrights of the Developer.

10.6 **Current and Future Development.** Developer understands that Xilinx may currently or in the future be developing information internally, or receiving information from other parties that may be similar to Developer's information. Nothing in this Agreement will be construed as a representation or inference that Xilinx will not develop, or have developed, products or services that, without violation of this Agreement, compete with the products or services of Developer.

11. **Limitation of Liability**

EXCEPT FOR ANY LIABILITY UNDER SECTIONS 8 (WARRANTIES), 9 (INDEMNIFICATION) OR 10 (CONFIDENTIALITY):

(A) NEITHER PARTY SHALL HAVE ANY LIABILITY FOR INCIDENTAL, CONSEQUENTIAL, INDIRECT, SPECIAL OR PUNITIVE DAMAGES ARISING OUT OF OR IN CONNECTION WITH THIS AGREEMENT; AND

(B) IN NO EVENT SHALL EITHER PARTY'S AGGREGATE LIABILITY ARISING OUT OF OR IN

CONNECTION WITH THIS AGREEMENT EXCEED THE AMOUNTS PAID BY XILINX TO DEVELOPER UNDER THIS AGREEMENT.

12. **Term and Termination**

12.1 **Term.** This Agreement shall commence on the Effective Date and shall continue in effect until terminated as specified below.

12.2 **Termination for Bankruptcy.** This Agreement shall automatically terminate without notice immediately upon either party (i) becoming insolvent; (ii) voluntarily filing a petition under applicable bankruptcy or insolvency laws; (iii) having filed against it a petition under applicable bankruptcy or insolvency laws which such party fails to have released within sixty (60) days after filing; (iv) proposing any dissolution, composition or financial reorganization with creditors or if a receiver, trustee, custodian, administrator, examiner or similar agent is appointed or takes possession with respect to all or substantially all property or business of such party; or (v) making a general assignment for the benefit of creditors.

12.3 **Termination for Breach.** Either party shall have the right to terminate this Agreement if the other party is in material breach of any term or condition of this Agreement and fails to remedy such breach within ten (10) business days after written notice.

12.4 **Termination for Convenience**. Xilinx may terminate this Agreement for any or no reason upon not less than thirty (30) days prior written notice to the other party. Upon notice of any such termination, Developer shall, unless otherwise mutually agreed, endeavor to wind-down future activities hereunder as promptly as possible.

12.5 **Obligations; Survival.** In the event of termination for convenience by Xilinx, Xilinx shall pay Developer for all Deliverables accepted and a prorated potion of uncompleted Deliverables based on the percentage of work completed. In the event of termination under Section 12.2 (Termination for Bankruptcy) or 12.3 (Termination for Breach), Xilinx shall have no obligation to pay Developer any fees beyond the last Deliverable accepted. Upon the expiration or termination of this Agreement (i) each party shall, within ten (10) business days thereof, return to the other party (or, if approved, destroy) all copies of all materials in such party's possession which are owned by the other party, except as otherwise remaining validly licensed to the other party hereunder following such expiration or termination, and (ii) the following provisions of this Agreement shall survive:

Section 1 (Definitions and Interpretation) and all defined terms
Section 3 (Ownership of Intellectual Property Rights)
Section 5 (License Grants from Developer)
Section 6 (Payment Terms) for all unpaid amounts
Section 7.2 (Publicity)
Section 8 (Warranties)
Section 9 (Indemnification)

Section 10 (Confidentiality)
Section 11 (Limitation of Liability)
Section 12.5 (Obligations; Survival)
Section 13 (Miscellaneous)
Paragraphs 3 and 4 of Exhibit B (Marketing Plan)

12.6 **Consequences of Termination.** Upon termination (or expiry) of this Agreement for any reason: (i) all rights and obligations of the parties under this Agreement shall automatically terminate except for any rights of action which may have accrued prior to termination and any obligations which expressly or by implication are intended to commence or continue in effect on or after termination (or expiry); and (ii) each party shall promptly destroy all copies of the relevant Confidential Information (excluding Foreground Technology) in whatever form in its possession, custody or control and to the extent that the Confidential Information or any part thereof are contained or stored on any computer, data processing equipment or other IT equipment (including CD-ROMs and USB flash devices), shall procure that the Confidential Information is expunged from any such computer, data processing equipment or other IT equipment.

13. **Miscellaneous**

13.1 **Export Compliance.** Developer shall adhere to all applicable import and export laws and regulations of Developer's country and of the United States, without limitation. This Agreement may involve items and information that are subject to the International Traffic in Arms Regulations (ITAR) or Export Administration Regulations (EAR). The importer/exporter of record shall not export, reexport, resell, transfer, or disclose, directly or indirectly, any products or technical data, to any proscribed person, entity, or country, or foreign persons thereof, unless properly authorized by the U.S. government and/or any other applicable or relevant government or regulatory body.

13.2 **No Waiver.** No waiver of any term or condition of this Agreement will be valid or binding on either party unless the same will have been mutually agreed in writing by both parties. The failure of either party to enforce at any time any of the provisions of the Agreement, or the failure to require at any time performance by the other party of any of the provisions of this Agreement, will in no way be construed to be a present or future waiver of such provisions, nor in any way affect the validity of either party to enforce each and every such provision thereafter

13.3 **Severability.** If any provision of this Agreement is held to be unlawful, unenforceable or invalid by a court of competent jurisdiction, then the remaining provisions will nevertheless remain in full force and effect to the maximum extent permissible under applicable law.

13.4 **Governing Law.** This Agreement and any dispute or claim arising out of or in connection with this Agreement shall be governed by, subject to, and construed in accordance with the laws of Ireland and the parties irrevocably agree that the Irish courts will have exclusive jurisdiction to settle any such dispute or claim**.**

13.5 **Force Majeure.** Neither party shall be liable hereunder by reason of any failure or delay in the performance of its obligations hereunder to the extent caused by an event that is beyond the reasonable control of such party including without limitation strikes, shortages, riots, insurrection, fires, flood, storm, explosions, acts of God, war, governmental action, labor conditions, acts of terrorism, power shortage or outage, or earthquakes.

13.6 **Assignment.** Xilinx may assign this Agreement, in whole or in part, to any Affiliate or to any person or entity to whom it transfers all or substantially all of its assets to which this Agreement relates, provided assignee agrees in writing to be bound by the terms of this Agreement. Developer agrees that its rights and obligations under this Agreement may not be transferred or assigned directly or indirectly without the prior written consent of Xilinx except as provided herein. Subject to the foregoing, this Agreement will be binding upon and inure to the benefit of the parties hereto, their successors and permitted assigns.

13.7 **Independent Contractors.** The relationship of Xilinx and Developer established by this Agreement is that of independent contractors, and nothing contained in this Agreement will be construed to (i) give either party the power to direct and control the day-to-day activities of the other, (ii) constitute the parties as agents, partners, fiduciaries, joint venturers, or otherwise as participants in a joint or common undertaking, or (iii) allow Developer to create or assume any obligation on behalf of Xilinx for any purpose whatsoever.

13.8 **Order of Precedence.** In the event of a conflict between the terms of this Agreement and the terms of an SOW or other Exhibit or Schedule, then the terms of this Agreement shall take precedence.

13.9 **Entire Agreement.** This Agreement and the Exhibits attached hereto, which are hereby incorporated by reference, sets forth the entire agreement and understanding of the parties relating to the subject matter herein and merges all prior discussions between them. No modification of or amendment to this Agreement will be effective unless in writing signed by both parties.

13.10 **Notices**. Any notices required or permitted by this Agreement shall be in writing and shall be delivered as follows, with notice deemed given as indicated: (i) by personal delivery, when delivered personally; (ii) by overnight courier, upon written verification of receipt; (iii) by fax transmission, upon acknowledgment of receipt of electronic transmission, provided that notice is also provided by one of the other methods herein within five days thereafter; or (iv) by registered post, return receipt requested, upon verification of receipt. Notice shall be sent to the addresses set forth above or to such other address as either party may specify in writing. Notices to Xilinx shall be addressed to the attention of: Legal Department, Attn: General Counsel, 2100 Logic Drive, San Jose, CA 95124.

13.11 **Counterparts.** This Agreement may be executed in any number of counterparts, and

by the several parties to it on separate counterparts, each of which when so executed will constitute an original but all of which together will evidence the same agreement.

EXHIBIT A – STATEMENT OF WORK

(attached after this page)

Trenz Electronic GMBH
Holzweg 19A
32257 Bunde
Germany

Statement of Work - For: Xilinx -

-

Document title: **Tegernsee Electric Drive Development Platform (EDDP) - Design & Development of Reference Design & IP Cores**

Document number: 009

Date of Issue: December 20, 2016

Author:

Authorized by:

Abstract

The purpose of this Statement of Work (SOW) is to describe the development of an open source, SDSoC-based, HLS-used Motor Controller with a complete Reference Design, the details of which are outlined in relevant sections. It also includes the business models corresponding to the EDDP.

-

Keywords

Zynq,

-

Distribution list

Name	Function	Name	Function
Christoph Fritsch, Xilinx	ISM Director	Antti Lukats	Trenz Electronic GmbH
Ganesh Narayanaswamy, Xilinx	Sr Marketing Manager		
Giulio Corradi, Xilinx	Staff System Architect		
Bill Klingler, Xilinx	Program Manager		

1 ABOUT THIS DOCUMENT

1. Change control

2. Current status and anticipated changes

- None

3. Change history

- ssue	- Date	- By	- Change
- 1	- October 12, 2016	- Antti Lukats	- Created the SOW
- 2	- October 28, 2016	- Gane sh N - Giuli o C	- Updated version of the document
- 3	- November 15, 2016	- Gane sh N - Giuli o C	- Updated, removed non-pertinent content, modified 5.1.1.a; - Doc now at V0.5
- 4	- November 18, 2016	- Gane sh N	- After discussions with Giulio, & Trenz – few adds
- 5	- November 28, 2016	- Gane sh N - Lorra ine L	- Legal inputs - Additional elaborations & changes
- 6	- December 06, 2016	- Giuli o C - Gane sh N	- Acceptance criteria added - Add Business Model
- 7	- December 09, 2016	- Antti L - Gane sh N	- Added CE Compliance related activities & quote
- 8	- December 13, 2016	- Gane sh N	- Minor cleanup & updates
- 9	- December 20, 2016	- Gane sh N	- Few business terms added in Sections 7 & 8

4. References

- This document refers to the following documents.

- ef	-	**Doc No**	-	**Author(s)**	-	**Title**
-	- -	LIGHT MOTOR PHYSICAL 1.0	-	QDESYS	- 1.0 -	LIGHT MOTOR PHYSICAL VERSION
-	-	Tegernsee EDDP SRD Final	-	Xilinx Inc.	-	Tegernsee Electric Driver Development Platform (EDDP)
-	-	Tegernsee EDDP PPT	-	Xilinx Inc.	-	Tegernsee EDDP (Presentation)
-	-	EDPS BOM Final	-	QDESYS	-	EDPS – BOM Dec2016
			-	Trenz		
-	-	Mangfall EDPS Trenz SoW	-	Trenz	-	

-

2 RESPONSIBILITIES/ CONTACT LIST

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3 INTRODUCTION – TEGERNSEE ELECTRIC DRIVE DEVELOPMENT PLATFORM (EDDP)

- The Tegernsee EDDP consists of the following:
  a. ARTY-Z7 Zynq Platform which is a small form factor development board aimed to low cost applications and equipped with the ZYNQ7010 device.
  b. Mangfall Electric Drive Power Stage (EDPS) is a power stage module that can be interfaced with the ARTY-Z7 via two (2x6) PMOD connectors to support a single motor.
  c. Alpbach IP cores is a set of cores, some of which are partly supported by the Vivado HLS tool and/or SDSoC environment & satisfy the basic functionality & demonstrability of simple to understand FOC (Field Oriented Control) running on Zynq-7000 device.
  d. Rottach Electric Drive Reference Design consists of a full featured electric drive platform Bitstream and GUI. Supports Hardware in the Loop using Matlab and Scilab and incorporates the Alpbach IP cores.
- This SOW corresponds to 3.c & 3.d of the above Electric Drive Development Platform (EDDP) and will be implemented by Trenz Electronic GMBH (Developer).
-

4 DEVELOPMENT CONSIDERATIONS

4.1 Project requirements

4.1.1 The Alpbach IP Cores

- Will delivered in their respective source code formats. The following IPs will be developed:

- Pulse Width Modulator (PWM), delivering a 3-phase space vector input. PWM frequency is fixed at 20KHz
- Sigma-Delta ADC; Ia, Ib & Ic Sigma-Delta acquisition at fixed rate
- HLS synthesizable Field Oriented Control (FOC); FOC & interface run on 1 ARM core
- Encoder IP; encoder is acquired on the 4 input edges bidirectional, there is no interpolation
- Simple GUI

4.1.2 The Rottach Reference Design

- The Alpbach IP cores developed will be incorporated as part of a reference design to demonstrate multiple use cases as described in 4.3.1

4.1.3 Accessibility Requirements

- All designs mentioned in the above 4.1.1 & 4.1.2 will be provided as Open Source Technology.

4.2 Implementation Proposal

4.2.1 The Alpbach IP Cores will functionally satisfy the following Use Cases as implemented in a reference design named Rottach Reference Design. The IP Cores should conform to the requirements of adding these cores to the IP Catalog.

- The source code will have needed descriptions & comments for the user to have an understanding of the operation.

4.2.1.1 C-based Design

- The motor controller (torque control only) will be designed using C-language & will be synthesizable using Vivado. This will guide the customer to familiarize designing a motor

controller in C, introducing the basic functions like the PWM and Encoder in RTL, and explaining the FOC at C level.

4.2.1.2 Use Case #1 – Vivado HLS-based flow – Torque Control

- Design of a motor controller (Torque control only). This use case guides the customer to familiarize with C to HLS in the context of motor control, explaining the steps involved in synthesizing the FOC in C with HLS
- Taking Use Case #1, the implementation will:
  - Synthesize C-based FOC using HLS
  - Network interface run in the ARM core – 1 core

4.2.1.3 Use Case #2 - Vivado SDSoC-based flow – Torque Control

- Design of a motor controller (Torque control only). This use case guides the customer to familiarize with C to HLS in the context of motor control, explaining the steps involved in synthesizing the FOC in C with SDSoC
- Taking Use Case #2, the implementation will:
  - Use SDSoC to transform the C-based FOC for synthesis using HLS
  - Create Bare Metal application drivers using SDSoC
  - Network interface run in the ARM core – 1 core

4.2.1.4 Use Case #3 - Vivado SDSoC flow – Speed Loop

- Design of a speed loop in a motor controller. This use case guides customer for speed loop implementation based on encoder readout
- Taking Use Case #3, the implementation will add:
  - Numerical speed set in RPM into the GUI.
  - Speed loop implemented by the ARM core as PI controller

4.2.2 Graphical User Interface (GUI)

- Designed as a program or web interface residing in a host PC allowing:
- Motor on/off,
- Motor Is current set up via numerical input,
- Ia, Ib, Id, Iq, Is currents and encoder speed as graphical readout.
- PI values, PWM frequency, and filters cutoff programmable
- All other parameters like scaling factors, motor data, etc. are embedded in the C code. The GUI does not allow changes.

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5 DESIGN SERVICES

5.1 Alpbach IP Cores Design & Development

- The IP cores are Open Source Technology & will be written using high-quality coding style with adequate comments. Further, the code should be made as much as possible independent of the synthesis tools to support version independency.

5.1.1 Deliverables

a. Pulse Width Modulator (PWM) implementing Space Vector Modulation and DC_link compensation in RTL as Vivado Catalog ready IP Core

b. Incremental Encoder IP in RTL as Vivado Catalog ready IP Core

c. Sigma Delta acquisition module in RTL as Vivado Catalog ready IP Core

d. HLS synthesizable Field Oriented Control (FOC) in C as HLS project file
e. SDSoC platform for the ARTY-Z7 adopted for EDDP
f. SDSoC synthesizable Field Oriented Control (FOC) in C as SDSoC project file
g. Zynq Vivado Design as Vivado Project or TCL script(s) to re-create the project
h. GUI App for receiving and transmitting commands and variables including all source code
i. 1 day tutorial for Xilinx SME
j. User Guides corresponding to the different Use Cases listed in Section 4.2

5.1.2 Acceptance Criteria

- Verification from Xilinx of the delivered documents.
- Demonstration of the running prototype by Developer to Xilinx showing running motor with the Alpbach IP and Alpbach GUI
  - Witnessed by Xilinx ISM System Architect
  - Witnessed by Xilinx ISM Marketing Manager
  - Evidence that the [IP Cores] are capable of being provided as Open Source Technology.

5.1.3 Compliance – Conformance Test

The Alpbach IP, Alpbach GUI & the Rottach Reference Design shall pass the validation specified in the table below.

N.	Test Case for Use Cases #1, #2	Set-up	Pass criteria
1	Startup motor @25% max motor current +90 degrees FOC angle	Motor powered nominal supply, no shaft load. Commanding a set-point of 25% rated motor current. Measurement point encoder feedback on GUI	The motor shall start, spin regularly, fluid without vibration or hang-up. Measured Alpha and Beta currents of the FOC shall create 25% +/- 2% Is (Stator Current)
2	Startup motor @50% max motor current +90degrees angle	Motor powered, nominal supply no shaft load. Commanding a set-point of 50% rated motor current. Measurement point encoder feedback on GUI	The motor shall start, spin regularly, fluid without vibration or hang-up. Measured Alpha and Beta currents of the FOC shall create 50% +/- 2% Is (Stator Current)

3	Startup motor @75% max motor current +90degrees angle	Motor powered, nominal supply no shaft load. Commanding a set-point of 75% motor current. Measurement point encoder feedback on GUI	The motor shall start, spin regularly, fluid without vibration or hang-up. Measured Alpha and Beta currents of the FOC shall create 75% +/- 2% Is (Stator Current)
4	Startup motor @90% max motor current +90degrees angle	Motor powered, nominal supply no shaft load. Commanding a set-point of 90% motor current. Measurement point encoder feedback on GUI	The motor shall start, spin regularly, fluid without vibration or hang-up. Measured Alpha and Beta currents of the FOC shall create 90% +/- 2% Is (Stator Current)
5	Repeat tests 1..4 with -90degrees	Motor powered, nominal supply no shaft load.	The motor shall spin instantaneously as in 1...4 in opposite direction
6	Startup motor @50% max motor current +90degrees angle Change angle between +90 and -90 for a minimum of 6 times	Motor powered, nominal supply no shaft load. Commanding a set-point of 50% motor current	The motor shall spin instantaneously in opposite direction any time the sign of the input angle is changed.

- ***Table 1- Compliance Motor Control***

The following table shows the validation test cases.

N.	Test Case for Use Case #3	Set-up	Pass criteria

1	Startup motor @25% nominal motor **no-load** speed +90degrees angle	Motor powered nominal supply, no shaft load. Commanding a set-point of 25% rated speed. Measurement point encoder feedback on GUI	The motor shall spin at rated speed and maintain speed with 1%
2	Startup motor @50% nominal motor **no-load** speed +90degrees angle	Motor powered, nominal supply no shaft load. Commanding a set-point of 50% rated speed. Measurement point encoder feedback on GUI	The motor shall spin at rated speed and maintain speed with 1%
3	Startup motor @75% max motor **no-load** speed +90degrees angle	Motor powered, nominal supply no shaft load. Commanding a set-point of 75% rated speed. Measurement point encoder feedback on GUI	The motor shall spin at rated speed and maintain speed with 1%
4	Startup motor @90% max motor **no-load** speed +90degrees angle	Motor powered, nominal supply no shaft load. Commanding a set-point of 50% rated speed. Measurement point encoder feedback on GUI	The motor shall spin at rated speed and maintain speed with 1%
5	Repeat tests 1..4 with -90degrees	Motor powered, nominal supply no shaft load.	The motor shall spin as in 1…4 in opposite direction rated speed and maintain speed with 1%
6	Repeat tests with direction change +90, -90 for 5 times @50% nominal motor **no-load** speed		

Table 2 - Speed Control Acceptance Criteria

5.2 Alpbach GUI Design & Development

- This GUI is a simple interface residing in a PC allowing basic control and monitoring of the EDDP. The GUI will run on Windows 10 operating system. The GUI will use Ethernet UDP protocol to connect to the ARTY-Z7 board for sending and receiving the inputs and outputs. ARTY-Z7 will implement a simple receiving and transmitting loop to transfer commands to the Alpbach IP and reading variables from the Alpbach IP.

5.2.1 Deliverables

- Commented (formatting: Doxygen) Source code for the GUI
- User guide, as original source and PDF file (or HTML)

5.2.2 Acceptance Criteria

- Demonstration of the running prototype by Developer to Xilinx showing running motor with the Alpbach IP and Alpbach GUI, based on Section 5.1.3
  - Witnessed by Xilinx ISM System Architect
  - Witnessed by Xilinx ISM Marketing Manager
  - Evidence that the Deliverable is made available as Open Source Technology

5.3 Rottach Reference Design & Development

- The Rottach Reference Design will incorporate all the use cases detailed in 4.3 thereby demonstrating the functionality of the Alpbach IP cores in actual electric drive examples with the described design methodologies.

5.3.1 Deliverables

- Complete reference design with design files for each use case detailed in 4.3
- User Guide, as original source and PDF file (or HTML) for each use case

5.3.2 Acceptance Criteria

- Demonstration of the running prototype by Developer to Xilinx using the reference design per the criteria outlined in Section 5.1.3
  - Witnessed by Xilinx ISM System Architect
  - Witnessed by Xilinx ISM Marketing Manager
- High-quality User Guide for each use cases listed in 4.3
- Evidence that Deliverable is made available as Open Source Technology.

5.4 CE Compliance

- Xilinx is agreeing to fund a certain amount in accordance with Section 10 of this SOW for CE compliance testing of the EDDP Platform.

- Developer shall be responsible for ensuring that the EDDP platform is CE compliant within the meaning of Directive 2004/108/EC and any applicable national implementing legislation.

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6 INTENTIONALLY BLANK

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7 MAINTENANCE & SUPPORT

7.1 Alpbach IP Cores

- Design Maintenance & Support – Developer is not envisaging any support for Alpbach, the design can be supported by Xilinx as per application note.
- However, the IP Cores will be designed to support usage with Vivado HLS 2017.1 & SDSoC 2017.1.

7.2 Alpbach GUI

- Design Maintenance & Support – Developer is not envisaging any support for Alpbach GUI, the design can be supported by Xilinx as per application note.

7.3 Rottach Reference Design & Development

- Design Maintenance & Support – Developer is not envisaging any support for Rottach Reference Design, the design can be supported by Xilinx as per application note.
- However, the Reference Design along with the various Use Cases will be designed to support usage with Vivado HLS 2017.1 & SDSoC 2017.1.

7.4 Mangfall EDPS Board

- If Developer sells the EDPS Boards (Part # 7) directly, Developer agrees to provide the support needed related to these boards.

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8 BUSINESS MODEL

8.1 Online Access of EDDP Design Data

As detailed in the respective sections, the Developer will provide Open Source access to the entire design database.

- This database will be hosted on github.xilinx.com by the Developer. Developer will use BSD – 3 Clause as the license for sourcing this database

8.2 HW & SW Commercial Availability

- Developer will make available the below options for sale to Xilinx's Distributors):

-

- Part #s	- Product	- Description
- Part # 1	- Control Kit	- ARTY-Z7 board + PMOD cables + power supplies + USB cable + SD Card

- Part # 2	- EDPS Kit	- EDPS board + power supplies
- Part # 3	- Mezzanine Kit	- Mezzanine board + PMOD cables
- Part # 4	- EDDP 1-axis	- Control Kit + EDPS Kit + motor
- Part # 5	- EDDP 2-axis	- Control Kit + EDPS Kit (2 #s) + Mezzanine Kit (1) + motors (2 #s)
- Part # 6	- EDDP 3-axis	- Control Kit + EDPS Kit (3 #s) + Mezzanine Kit (1) + motors (3 #s)
- Part # 7	- EDPS Board	- EDPS Board alone; no power supplies are included

- Developer will validate the systems (Part # 4, Part # 5, and Part # 6) prior to shipping them to the Xilinx Distributors.
- Developer will define the Diagnostic Test & obtain Xilinx approval for sufficiency. This Diagnostic Test will be run on every box prior shipment.
- Developer will make Part # 7 available for sale for Xilinx Distributors.

-

9 PROJECT SCHEDULE

9.1 Alpbach IP Cores Design & Development

- For every item in Alpbach IP cores there are the following steps:

(1) Functional Design, this is the phase required to create the specific module
(2) Implementation of the Function in C or RTL
(3) Creation Test bench in RTL or C
(4) Simulation of the Function in RTL or C
(5) Integration of the Function in the target
(6) Validation of the Function in the target
(7) Design Documentation writing

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- Ref	- Item	- Delivery	- Notes	- Responsible
- 1	- SOW Complete	-	-	- Developer, Xilinx
- 2	- Zynq project and Drivers for ARTY-Z7 to control EDPS in SDSoC	- 20 working days after SoW closure	-	- Developer
- 3	- Base ARTY-Z7 SDSoC Platform for EDDP	- 20 working days after SoW closure	-	- Developer

- 4	- Sigma Delta acquisition module in RTL as Vivado Catalog ready IP Core	- 20 working days after SoW closure	-	- Developer
- 5	- Encoder IP in RTL as Vivado Catalog ready IP Core	- 20 working days after SoW closure	-	- Developer
- 6	- Pulse Width Modulator (PWM) in RTL as Vivado Catalog ready IP Core	- 20 working days after SoW closure	-	- Developer
- 7	- Clark Transform and Inverse Clark in C for HLS	- 5 working days after Ref. 1-6	-	- Developer
- 8	- Park Transform and Inverse Park in C for HLS	- 2 working days after Ref. 7	-	- Developer
- 9	- PI controller in C for HLS	- 10 working days after Ref. 8	-	- Developer
- 10	- Integrating modules 4,5,6,7,8,9	- 5 working days after Ref. 9	-	- Developer
- 11	- UDP protocol for PC connectivity in C for ARM	- 3 working days after Ref. 10	-	- Developer
- 12	- Logging module; it logs Ia, Ib, Id, Iq and encoder values in RTL or C for HLS if convenient	- 10 working days after Ref. 4-9	-	- Developer
- 13	- GUI Commands interpreter in C for ARM	- 10 working days after Ref. 11	-	- Developer
- 14	- Add technical documents, User Guides, Reference Designs, IP Cores to webpages	- 1 working day after 10	- To be added in the same webpages created for EDPS.	- Developer

9.2 Alpbach GUI Design & Development

- **Ref**	- **Item**	- **Delivery**	- **Notes**	- **Responsible**
- 14	- GUI Socket for Ethernet UDP	- 3 working days after Ref. 13	-	- Developer

- 15	- GUI user interface	- 10 working days after Ref. 14	-	- Developer

9.3 Rottach Reference Design & Development

- Ref	- Item	- Delivery	- Notes	- Responsible
- 16	- Retargeting of Alpbach IP Cores with SDSoC (modules 7, 8, 9)	- 15 working days after Ref. 7-9	-	- Developer
- 17	- Full platform test and validation Use Case #1	- 10 working days after Ref. 16 and validated EDPS HW	-	- Developer
- 18	- Full platform test and validation Use Case #2		-	
- 19	- Full platform test and validation Use Case #3		-	

9.4 Full System Certification Tests for CE Compliance

- Ref	- Item	- Delivery	- Notes	- Responsible
- 20	- Full system setup for EMI/EMC testing in certified laboratory as required for the CE Certification.	- 5 working days after 19	-	- Developer
- 21	- Testing in the EMC/EMI lab – 2 days	- After 20, may have to wait for available time	- If 2 days are insufficient extra lab days may be needed	- Developer
- 22	- Additional test in the lab if required per day	-	- 2500EUR/Day	- Developer

10 FINANCIALS

10.1 Pricing and payment terms

- Ref WPn	- Item	- Working Days -	- Price in EUR	- Notes
- 2	- Zynq project and Drivers for ARTY-Z7 to control EDPS in SDSoC	- 1	- 520	-

-	3	-	Base ARTY-Z7 SDSoC Platform for EDDP	-	1	-	520	-	
-	4	-	Sigma Delta acquisition module in RTL as Vivado Catalog ready IP Core	-	3	-	1560	-	
-	5	-	Encoder IP in RTL as Vivado Catalog ready IP Core	-	3	-	1560	-	
-	6	-	Pulse Width Modulator (PWM) in RTL as Vivado Catalog ready IP Core	-	3	-	1560	-	
-	7	-	Clark Transform and Inverse Clark in C for HLS	-	1	-	520	-	
-	8	-	Park Transform and Inverse Park in C for HLS	-	1	-	520	-	
-	9	-	PI controller in C for HLS	-	1	-	520	-	
-	10	-	Integrating modules 4,5,6,7,8,9	-	1	-	520	-	
-	11	-	UDP protocol for PC connectivity in C for ARM	-	1	-	520	-	
-	12	-	Logging module; it logs Ia, Ib, Id, Iq and encoder values in RTL or C for HLS if convenient	-	1	-	520	-	
-	13	-	GUI Commands interpreter in C for ARM	-	1	-	520	-	
-	14	-	GUI Socket for Ethernet UDP	-	2	-	1040	-	
-	15	-	GUI user interface	-	6	-	3120	-	
-	16	-	Retargeting of Alpbach IP Cores with SDSoC (modules 7, 8, 9)	-	4	-	2080	-	
-	17	-	Full platform test and validation for all Use Cases - User Guide for IP Cores & Reference Design with all Use Cases	-	3	-	1560	-	
-	18	-	Test system preparation	-	2	-	1360	-	
-	19	-	EMC Tests in lab, total 2 days	-	2	-	5000	-	
-	20	-	Additional EMC Lab test, per day	-	1	-	2500	-	If needed, not

				included in total
-	- **Total**	- **37**	- **23,520**	-

10.2 Payment Schedule

-

- **PPn**	- **Items (Ref to Table 10.1)**	- **Payable**	- **Notes**
- 1	- Ref 1-11 (IP Cores, HLS)	- After completion of Ref 11	-
- 2	- Ref 12-17 (SdSoC, GUI)	- After Ref 17 + tutorial day	-
- 3	- Ref 18-20	- After 19(20)	- 20 is optional may not be needed

EXHIBIT B – MARKETING PLAN

1. Following Xilinx' acceptance of the last Deliverable under the SOW, for a period of no less than 24 months, Developer shall use reasonable efforts to market and promote the Deliverables and to negotiate agreements that grant non-exclusive licenses for the Deliverables to third-party customers referred to Developer by Xilinx, and to negotiate agreements for related support, maintenance and design services as may be requested by Xilinx or by such customers. In doing so, Developer shall abide by all of the following:

   A. Xilinx may supply Developer with one or more sample license agreements (e.g., "SignOnce" templates) that Developer may consider using for its licensing activities. Developer agrees that it shall be solely responsible for ensuring any such sample agreement protects Developer's interests. Developer agrees to use reasonable efforts to negotiate changes to any such license agreement in the normal course of negotiations with customers, such as by offering commercially reasonably warranty, indemnity and liability terms and conditions, or to negotiate based on a customer's form of license agreement. In no event shall any such agreement impose upon Xilinx any obligation or liability of any nature.

   B. Developer shall negotiate its own customer support terms including price.

   C. Developer must use its own branding (trademarks, etc.) when marketing the Deliverables.

   D. Developer will provide to Xilinx, on a quarterly basis, a list of every customer to whom Developer has granted a license to the Deliverables in such quarter.

2. Xilinx will, for the duration of the 24 month period referred to above in paragraph 1 of this Exhibit, use reasonable efforts to refer its customers to Developer in promoting the Deliverables.

3. In no event shall Xilinx have any liability whatsoever for (and Developer assumes all risks for and shall indemnify Xilinx from and against any third party claims, suits, losses, liabilities, damages, court judgments or awards and the associated costs and expenses (including reasonable attorneys' fees) incurred as a result of) arising out of or in relation to the marketing efforts of Developer as set forth in this Exhibit including with respect to all warranty, indemnity, breach of contract and other matters which may arise in connection therewith.

4. XILINX DOES NOT GUARANTY THAT ANY PARTICULAR AMOUNT OR LEVEL OF FINANCIAL BENEFIT TO DEVELOPER WILL ARISE AS A RESULT OF THE ACTIVITIES DESCRIBED IN THIS EXHIBIT.

IN WITNESS WHEREOF, the parties hereto have executed this Agreement on the dates set forth below.

XILINX, INC.

Signature: DocuSigned by: DC998732BF4E433...

Print Name: Arun Iyengar

Title: VP GlobalMarkets Group

Date: 12/30/2016

DEVELOPER

Signature: DocuSigned by: Thorsten Trenz 0186C6ED202B47C...

Print Name: Thorsten Trenz

Title: CEO

Date: 12/22/2016

Xilinx Legal L C L Approved