AXI4-Stream AD7403

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IP Facts

Introduction

The AXI4-Stream AD7403 IP core filters the delta-sigma bitstream read from one or more ADC-s of type of AD7403 and outputs a stream of samples.

Features

- Sample width in the output stream fixed to 16 bits.
- The decimation rate of the Sinc^3 filter is one of 32, 64, 128 or 256. This can be either configured to a fixed value or externally set during runtime.
- Configurable ratio of ADC clock to system clock of 1:1, 1:2, 1:3, 1:4 or 1:5.
- Samples can be output either in parallel or in serial. In serial mode one sample is output after another, with TDEST signal corresponding to channel number.

teCORE™ IP Facts Table	
Supported Device Family	Zynq® -7000, 7 Series
Supported User Interfaces	AXI4-Stream
Resources	
Special Features	
Provided with Core	
Design Files	VHDL Source Code
Constraint Files	Not Provided
Example Design	Not Provided
Test Bench	Not Provided
Simulation Model	Not Provided
Supported S/W Dirver	Not Provided
Tested Design Flows	
Design Entry	Vivado® Design Suite, IP Integrator
Simulation	Vivado Simulator
Synthesis	Vivado Synthesis
Tested Hardware Platforms	
Digilent Arty Z7	
Support	
Provided by Trenz Electronic GmbH	

Overview

Feature Summary

Licensing and Ordering Information

Product Specification

The ADC serial clock (signal clkout) is generated from the system clock (signal m_axis_aclk).

The delta-sigma bitstream from the ADC-s is filtered by a $Sinc^3$ filter to obtain 16-bit samples. The output sample rate is the ADC serial clock divided by the decimation ratio.

In the case parallel mode has been selected, the samples of all channels are output simultanously. The AXI Stream data width will be 16 times the number of channels and the TDEST signal will not be used.

In the case serial mode has been selected, the samples are output sequentially, one after another. The AXI Stream data width will be 16 and the TDEST signal corresponds to the channel index.

Performance

Resource Utilization

Port Description

Signal Name	Direction	Description
ADC interface		
din[C_CHANNELS:0]	Input	ADC serial data inputs.
clkout	Output	ADC serial clock output, common for all ADC-s.
Global signals		
m_axis_aclk	Input	System clock.
m_axis_aresetn	Input	System reset; active low.
AXI4-Stream output signals		
m_axis_tdata	Output	AXI4-Stream interface data output.
m_axis_tvalid	Output	AXI4-Stream interface data valid output.
m_axis_tready	Input	AXI4-Stream interface data ready input. This is not used.
m_axis_tdest	Output	AXI4-Stream interface channel definition. Used in serial mode only.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

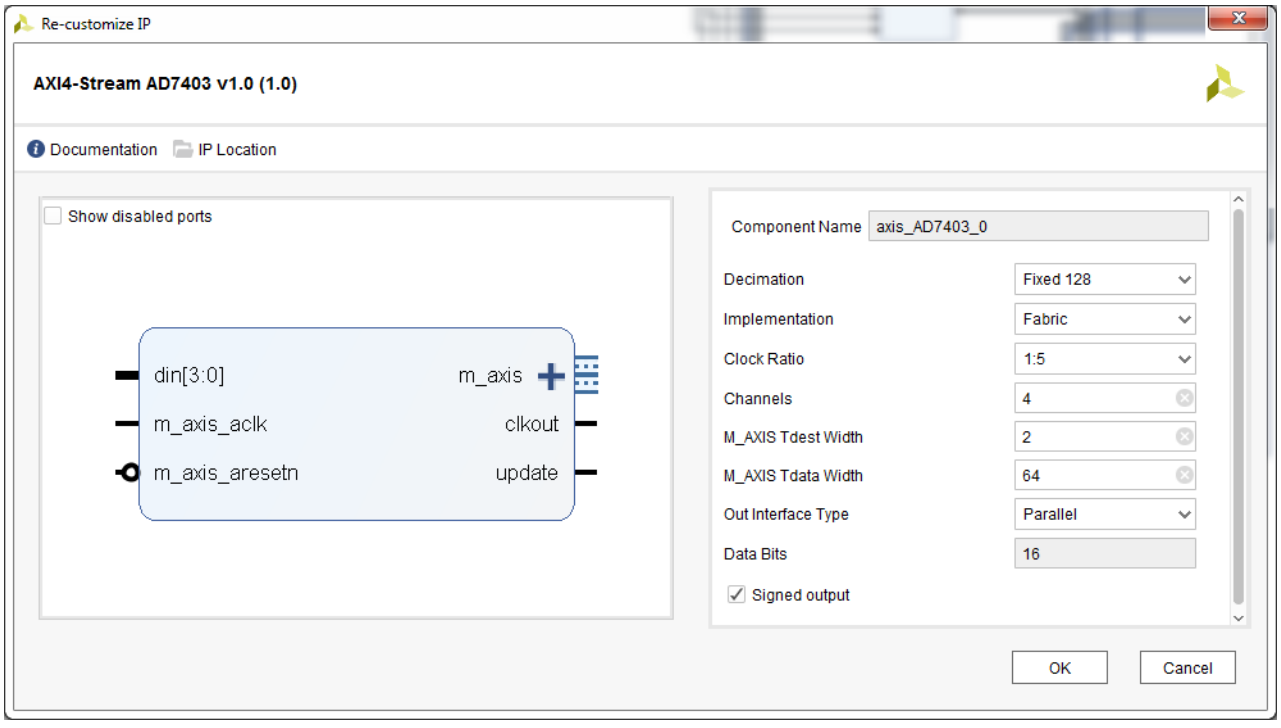
- Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
- Vivado Design Suite User Guide: Designing with IP (UG896)
- Vivado Design Suite User Guide: Getting Started (UG910)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

Core parameters

The re-customization dialog is as follows:



Decimation

Select the decimation rate, or, Variable. The output sample rate will be ADC serial clock divided by decimation rate.

Clock ratio

Select the clock ratio such that the frequency of the signal clkout will be in the acceptable range for the ADC chip. The AD7403 requires clock frequency in the range from 5 MHz to 20 MHz.

Channels

Enter the number of ADC chips to be interfaced to.

M_AXIS TDEST width

Number of the channel.

Only in use when the output interface type is serial.

M_AXIS TDATA width

Number of bits in the TDATA signal of the output data stream. When the output data type is parallel, it should be set to the number of channels times the bit width. In the serial mode, it should be set to the width of a single channel.

Output Interface Type

Select either parallel or serial. The serial mode might be useful in a multichannel system when there is more than one consumer of the sample stream. The parallel mode is simpler to use, especially by the IP Cores written with Xilinx HLS.

Signed output

Check if the output of the ADC is signed.

Constraining the Core

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the Vivado Design Suite User Guide:

- Designing with IP (UG896)

Example Design

There is no example Design for this IP core release.

Test Bench

There is no test bench for this IP core release.

Appx. A: Change History and Legal Notices

Document Change History

date	revision	authors	description
20xx-xx-xx	v.1	Name	initial release

Legal Notices

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