AXI4-Stream Encoder

Revision:	v.1
Date:	28.10.2017 22:10

Table of Contents

IP Facts

Introduction

AXI4-Stream Encoder Interface core provides interface to relative rotation encoders with index signal.

Features

Input signal filtering.

AXI4-Stream and bus interface.

Angle shift correction.

Optional period and RPM outputs.

Forward and inverse direction settings.

teCORE™ IP Facts Table	
Supported Device Family	Zynq® -7000, 7 Series
Supported User Interfaces	AXI4-Stream
Resources	
Special Features	
Provided with Core	
Design Files	VHDL Source Code
Constraint Files	Not Provided
Example Design	Not Provided
Test Bench	Not Provided
Simulation Model	Not Provided
Supported S/W Dirver	Not Provided
Tested Design Flows	
Design Entry	Vivado® Design Suite, IP Integrator
Simulation	Vivado Simulator
Synthesis	Vivado Synthesis
Tested Hardware Platforms	
Digilent Arty Z7	
Support	
Provided by Trenz Electronic GmbH	

Overview

Feature Summary

Licensing and Ordering Information

Product Specification

Performance

Resource Utilization

Port Description

Signal name	Direction	Description
A	Input	Encoder A signal
B	Input	Encoder B signal
I	Input	Encoder Index signal
angle_data	Output	Current angle data
period_data	Output	Current perod data
rpm_data	Output	Current RPM data
angle_shift	Input	Angle correction input
axis_aclk	Input	System clock
axis_aresetn	Input	System reset (active low)
m_angle_tdata	Output	Angle AXI4-Stream interface data
m_angle_tvalid	Output	Angle AXI4-Stream interface valid
m_angle_tready	Input	Angle AXI4-Stream interface ready (not used)
m_rpm_tdata	Output	RPM AXI4-Stream interface data
m_rpm_tvalid	Output	RPM AXI4-Stream interface valid
m_rpm_tready	Input	RPM AXI4-Stream interface ready (not used)
m_period_tdata	Output	Period AXI4-Stream interface data
m_period_tvalid	Output	Period AXI4-Stream interface valid
m_period_tready	Input	Period AXI4-Stream interface ready (not used)

Designing with the Core

Encoder signals A, B and I should be routed to core inputs. User can select needed AXIS interfaces or use output vectors. User should define encoder "Codes Per Revolution" (CPR) parameter and input filter width to get correct angle and speed information. Angle information updates by edge of encoder signal A. Speed information updated by user defined period. Angle shift input can be used to apply correction value to be substracted from encoder angle information.

Note: Core provide absolute angle value only after receiving first index impulse, before first index angle information is not valid.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

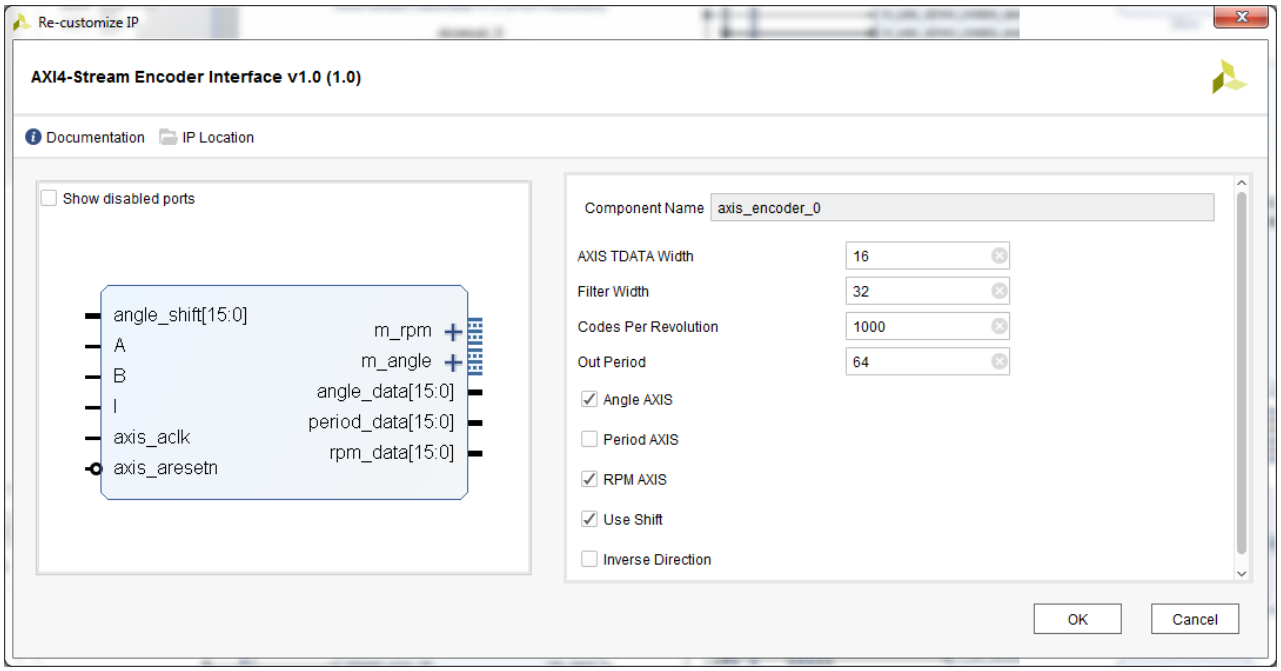
- Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
- Vivado Design Suite User Guide: Designing with IP (UG896)
- Vivado Design Suite User Guide: Getting Started (UG910)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

Core parameters

The re-customization dialogue is as follows:



AXIS TDATA width

Enter width for all the output data streams.

Filter width

Enter width of the input filter. The higher the number, the better filtering, however, the less bandwidth, too.

Codes per revolution

Enter number of encoder codes per one revolution

Out period

Enter the period after of the output data, in terms of clock cycles. This has effect on the period and rpm data only.

Angle AXIS

Check to enable the angle output AXI4-Stream.

Period AXIS

Check to enable period output AXI4-Stream.

RPM AXIS

Check to enable speed output AXI4-Stream.

Use shift

Check to add the input "angle_shift" to the output angle.

Inverse direction

Check to reverse the direction of rotation.

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the Vivado Design Suite User Guide:

- Designing with IP (UG896)

Example Design

There is no example Design for this IP core release.

Test Bench

There is no test bench for this IP core release.

Appx. A: Change History and Legal Notices

Document Change History

date	revision	authors	description
20xx-xx-xx	v.1	Name	initial release

Legal Notices

Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

3. Neither the name of the copyright holder nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission.

THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.