AXI4-Stream PWM

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IP Facts

Introduction

AXI4-Stream PWM core provides PWM encoding of input AXI4-Stream in unipolar or bipolar modes.

Features

- Unipolar and Bipolar modes.
- Configurable output PWM frequency.
- Parallel or serial input AXIS interface type.
- Deadtime Cycles for Bipolar mode.

teCORE™ IP Facts Table	
Supported Device Family	Zynq® -7000, 7 Series
Supported User Interfaces	AXI4-Stream
Resources	
Special Features	
Provided with Core	
Design Files	VHDL Source Code
Constraint Files	Not Provided
Example Design	Not Provided
Test Bench	Not Provided
Simulation Model	Not Provided
Supported S/W Dirver	Not Provided
Tested Design Flows	
Design Entry	Vivado® Design Suite, IP Integrator
Simulation	Vivado Simulator
Synthesis	Vivado Synthesis
Tested Hardware Platforms	
Support	
Provided by Trenz Electronic GmbH	

Overview

Feature Summary

Licensing and Ordering Information

Product Specification

Performance

Resource Utilization

Port Description

Signal name	Direction	Description
pwm	Output	PWM Output for unipolar mode
pwm_l	Output	Low PWM output for bipolar mode
pwm_h	Output	High PWM output for bipolar mode
s_axis_aclk	Input	System clock
s_axis_aresetn	Input	System reset (active low)
s_axis_tready	Output	AXI4-Stream interface ready
s_axis_tdata	Input	AXI4-Stream interface data
s_axis_tdest	Input	AXI4-Stream interface channel
s_axis_tvalid	Input	AXI4-Stream interface valid

Designing with the Core

Core can receive input data stream in two formats. In parallel format data for all channels received simultaneous in serial format consequent (channel defined by tdest). Core ganerate PWM signals based on input data system frequency and PWM frequency. For bipolar mode deadtime cycles should be defined to prevent a short circuit.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the Vivado IP integrator can be found in the following Vivado Design Suite user guides:

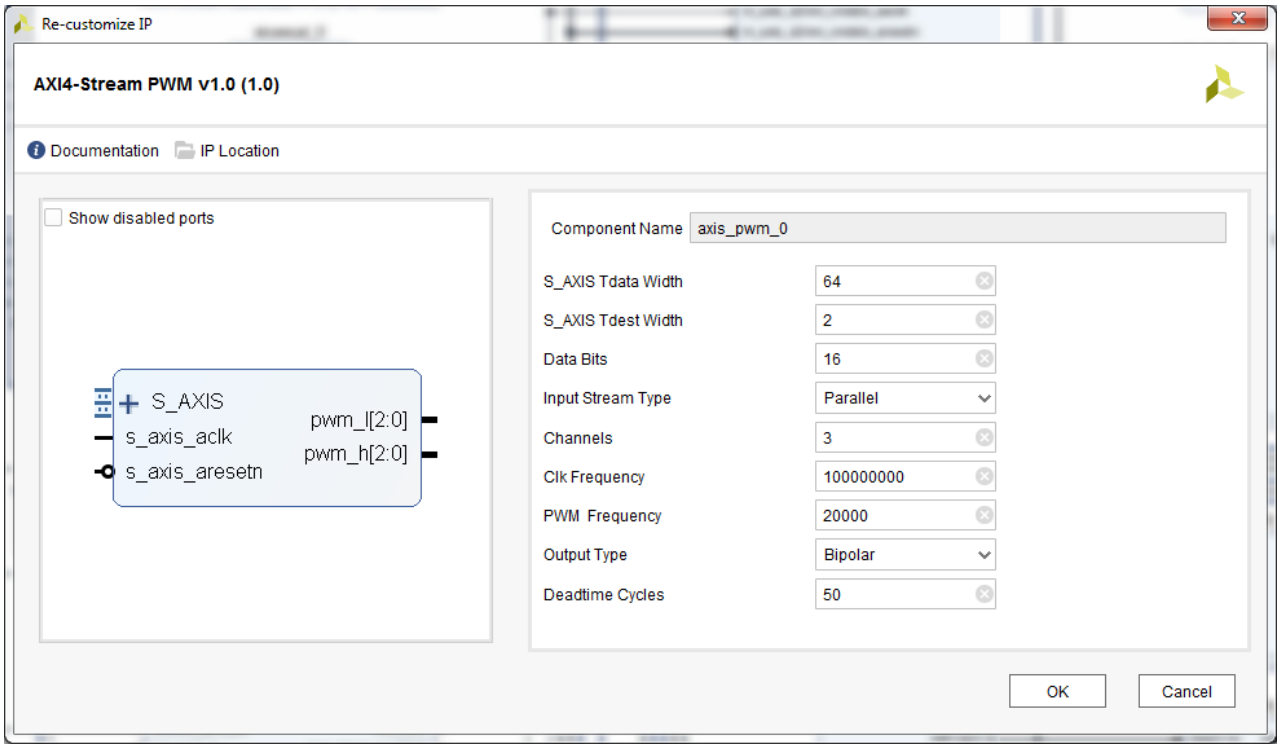
- Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994)
- Vivado Design Suite User Guide: Designing with IP (UG896)
- Vivado Design Suite User Guide: Getting Started (UG910)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado Design Suite.

Core parameters

The re-customization dialogue is as follows:



S_AXIS TDATA width

Width of the TDATA signal of the input AXI4-Stream. In the case of parallel input stream, it has to be at least as wide as the number of channels times data bits. In the case of serial input stream it has to be at least the number of data bits of one channel.

Important: Vivado might have problems debugging when the stream width is not a power of two times 8 (e. g. one of 8,16,32 etc.). Let us note that the unused signals will be optimized away during synthesis.

S_AXIS TDEST width

Width of the TDEST signal of the input AXI4-Stream.

Data bits

Number of data bits per one channel in the input data stream.

Input stream type

Either "Parallel" or "Serial".

Channels

Number of PWM channels.

Clock frequency

Frequency of the clock.

PWM frequency

Frequency of the output PWM.

Output type

Either "Bipolar" or "Unipolar".

Deadtime cycles

Number of deadtime cycles, in terms of input clock cycles. This is valid only in the case of bipolar PWM.

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

This core does not support simulation.

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the Vivado Design Suite User Guide:

- Designing with IP (UG896)

Example Design

There is no example Design for this IP core release.

Test Bench

There is no test bench for this IP core release.

Appx. A: Change History and Legal Notices

Document Change History

date	revision	authors	description
20xx-xx-xx	v.1	Name	initial release

Legal Notices

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