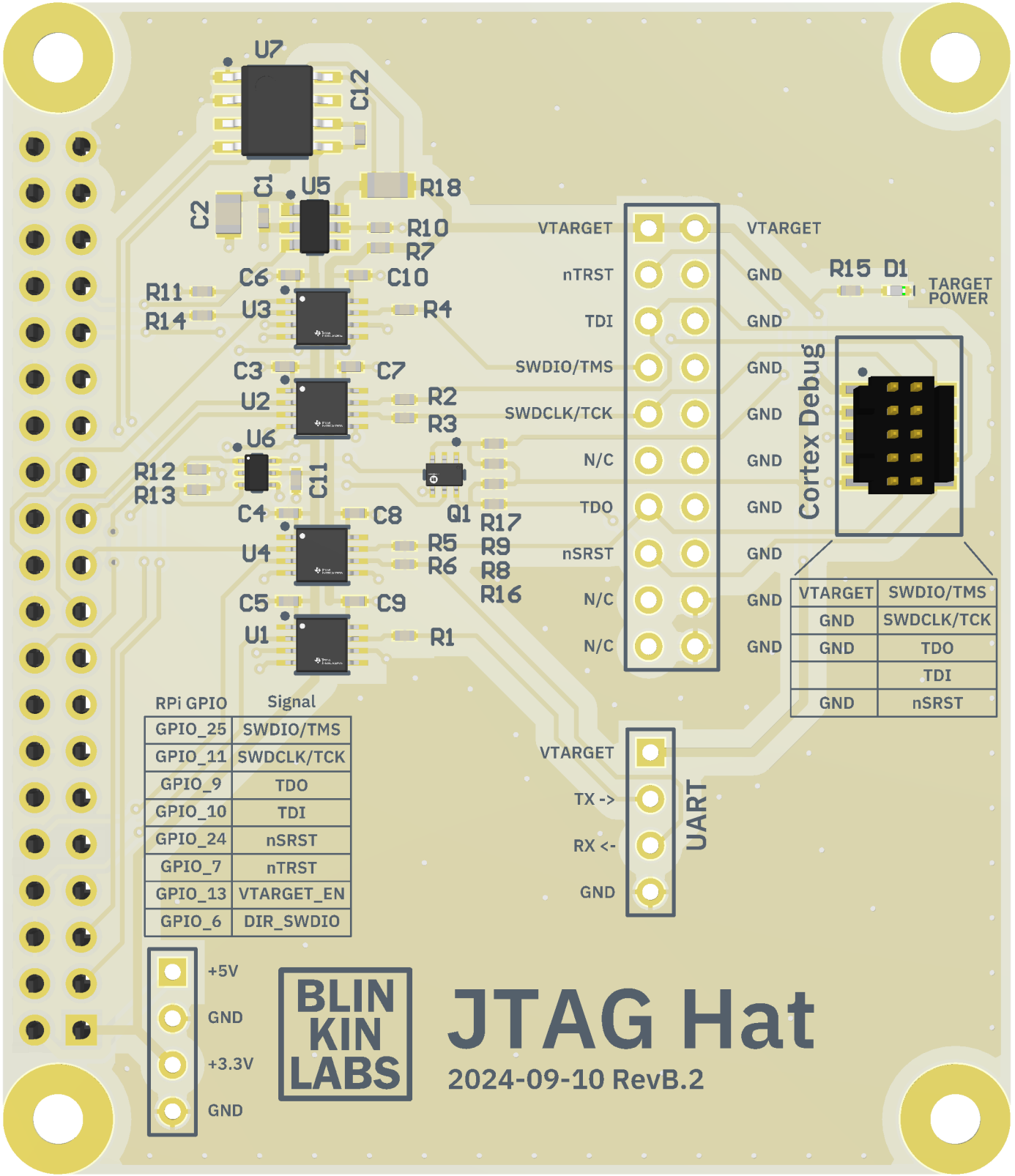
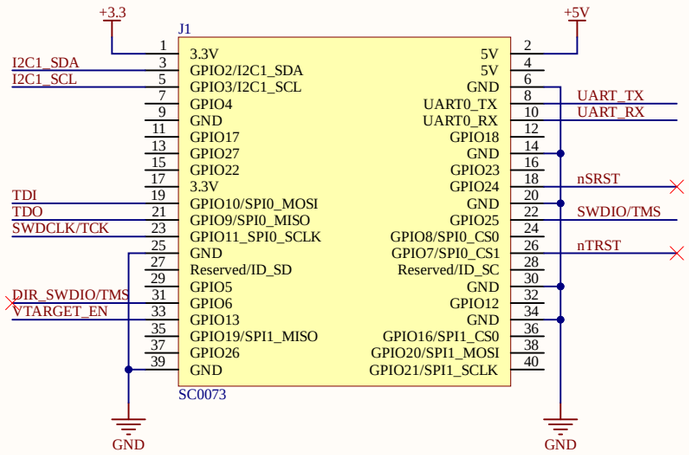

U7
C12
C1
U5
R18
C2
R10
R7
C6
C10
R11
R14
U3
R4
C3
C7
U2
R2
R3
U6
R12
R13
C11
C4
C8
Q1
R17
R9
R8
R16
U4
R5
R6
C5
C9
U1
R1
VTARGET
nTRST
TDI
SWDIO/TMS
SWDCLK/TCK
N/C
TDO
nSRST
N/C
N/C
VTARGET
GND
GND
GND
GND
GND
GND
GND
GND
R15
D1
TARGET POWER
Cortex Debug
VTARGET SWDIO/TMS
GND SWDCLK/TCK
GND TDO
TDI
GND nSRST
RPi GPIO Signal
GPIO_25 SWDIO/TMS
GPIO_11 SWDCLK/TCK
GPIO_9 TDO
GPIO_10 TDI
GPIO_24 nSRST
GPIO_7 nTRST
GPIO_13 VTARGET_EN
GPIO_6 DIR_SWDIO
VTARGET
TX ->
RX <-
GND
UART
+5V
GND
+3.3V
GND
BLIN KIN LABS
JTAG Hat
2024-09-10 RevB.2

JTAG Hat

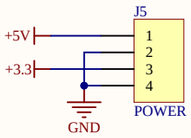
OpenOCD JTAG board for Raspberry Pi 2/3/4, with target voltage isolation

Raspberry Pi header

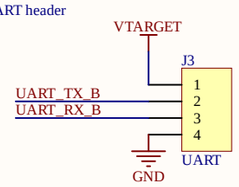



```
# Each of the JTAG lines need a gpio number set: tck tms tdi tdo
# Header pin numbers: 23 22 19 21
bcm2835gpio_jtag_nums 11 25 10 9

# Each of the SWD lines need a gpio number set: swclk swdio
# Header pin numbers: 23 22
bcm2835gpio_swd_nums 11 25

# If you define trst or srst, use appropriate reset_config
# Header pin numbers: TRST - 26, SRST - 18
```

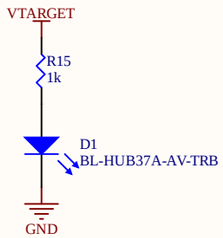
Extra Power



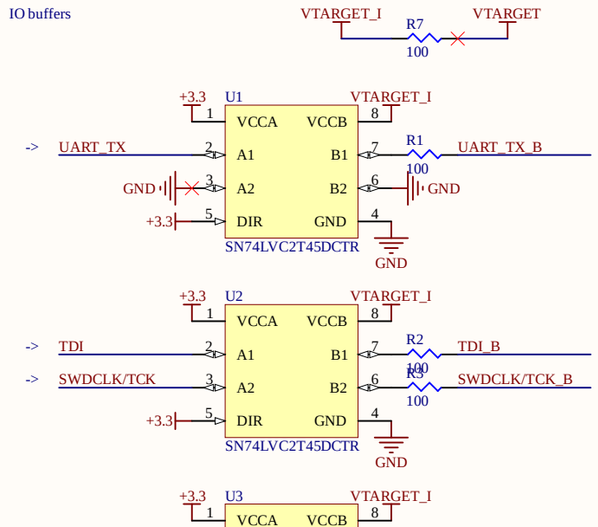
UART header

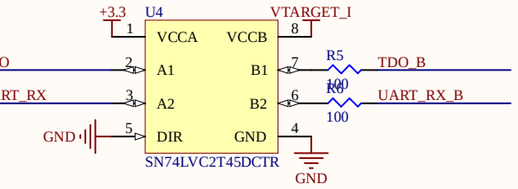


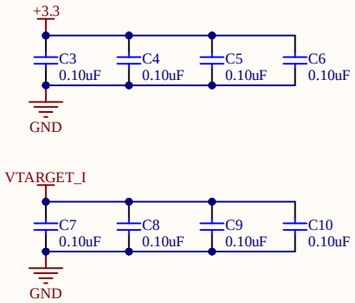
Target power indication



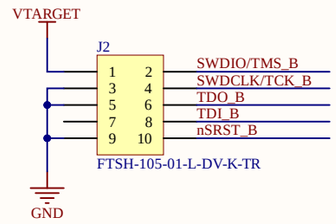
IO buffers

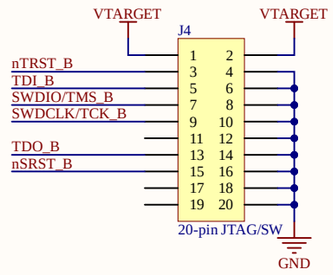




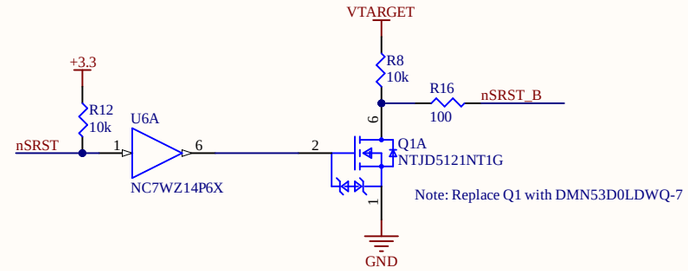


JTAG headers

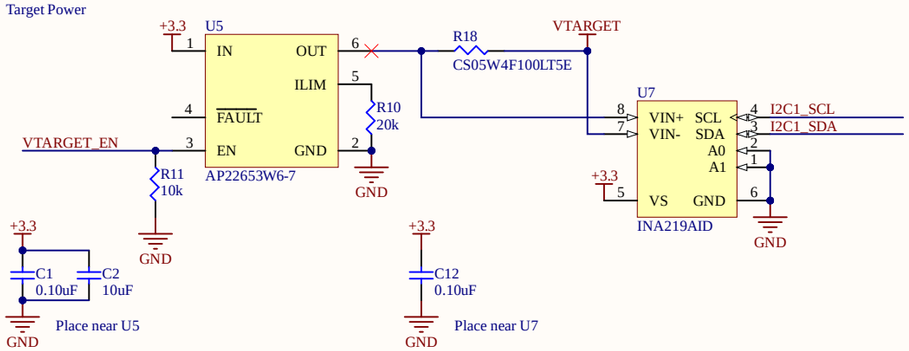




Reset



Target Power



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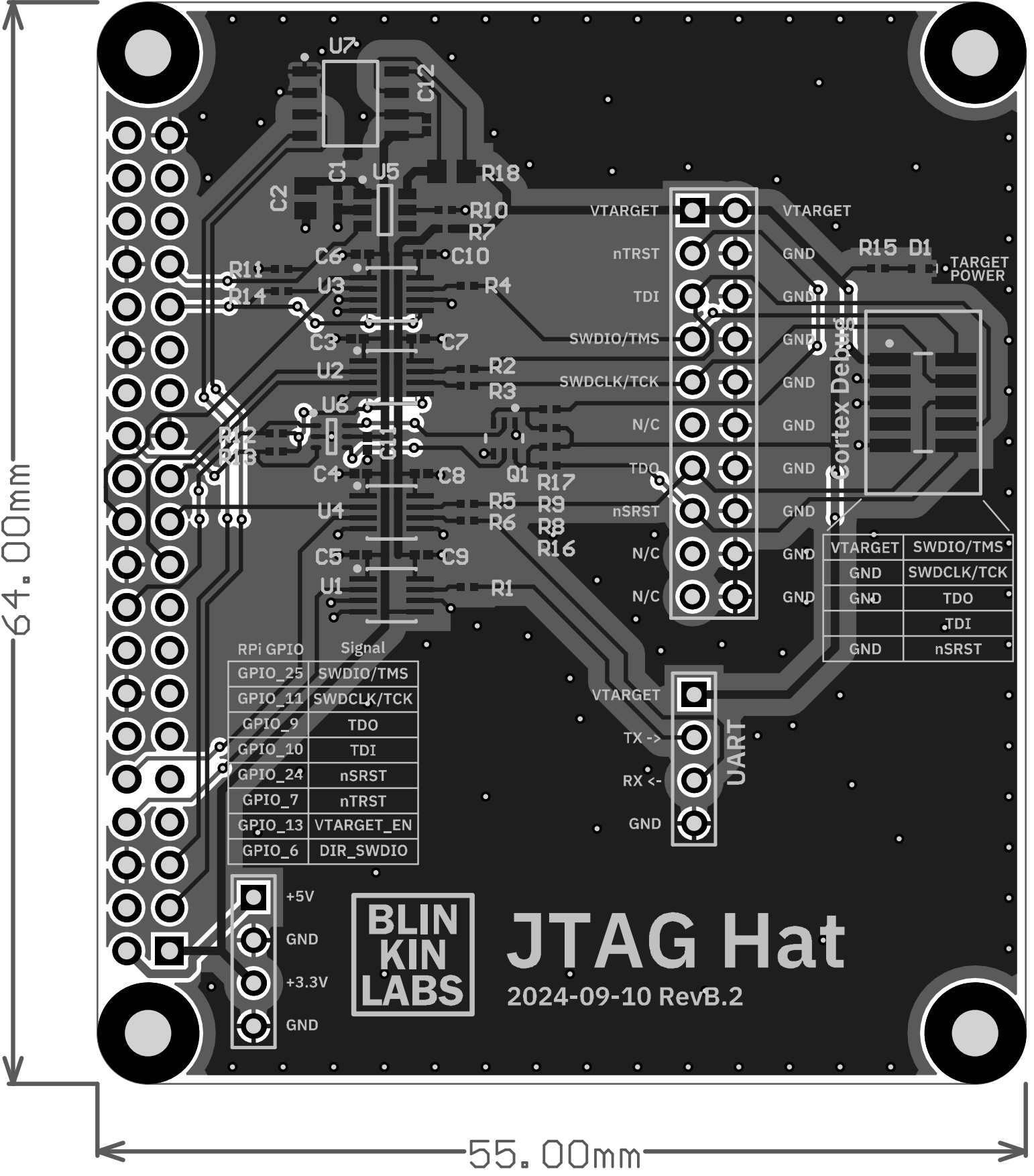
Title: Schematic		
Project: JTAG Hat		Revision: RevB.2
Date: 9/10/2024	Time: 5:22:54 PM	Sheet 1 of 1



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	Solder Resist	0.40mil	3.5	GTS
1	Top Layer		1.40mil		GTL
	Dielectric 1	FR-4	12.60mil	4.8	
2	Bottom Layer		1.40mil		GBL
	Bottom Solder	Solder Resist	0.40mil	3.5	GBS
	Bottom Overlay				GBO
Total board thickness:			16.20mil		

Design Rules Verification Report

Filename : C:\Users\matt\reference\JTAG_hat\pcb\PCB1.PcbDoc

Warnings 0
Rule Violations 74

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Clearance Constraint (Gap=1mm) (InNamedPolygon('pg_gnd_fill')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.508mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=6mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	36
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	29
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	9
Room Sheet1 (Bounding Region = (104.14mm, 41.656mm, 174.625mm, 122.301mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	74

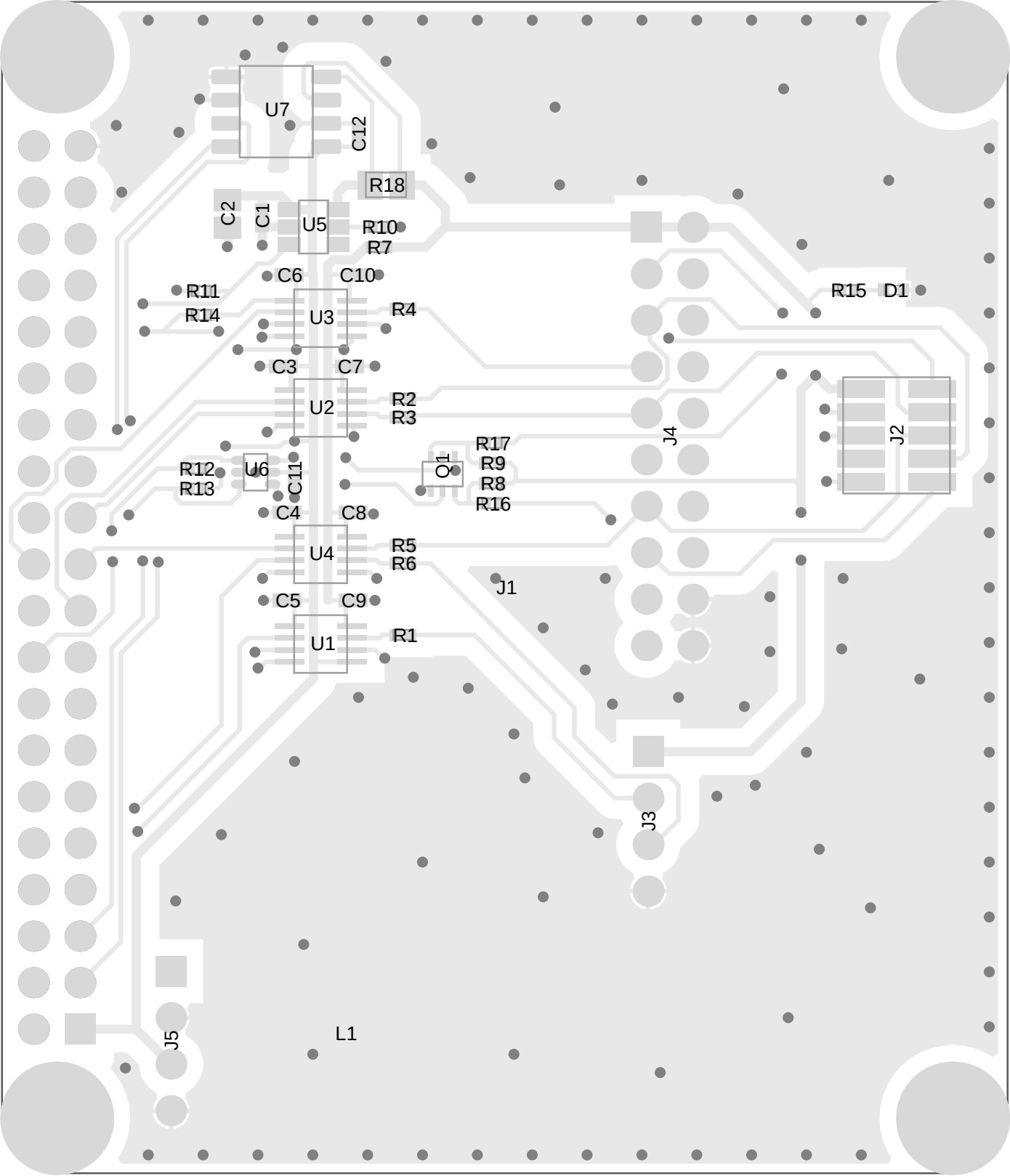
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C10-1(19.79mm,49.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(14.235mm,51.812mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C11-1(16mm,37.51mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C12-1(19.5mm,57.14mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C3-1(15.01mm,44.1mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(15.21mm,36.1mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C5-1(15.21mm,31.3mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C6-1(15.31mm,49.1mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C7-1(19.39mm,44.1mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C8-1(19.59mm,36.1mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C9-1(19.59mm,31.3mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R10-1(21mm,51.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R1-1(21.527mm,29.415mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R11-1(10.5mm,48.2mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R12-1(11mm,38.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R13-1(11mm,37.4mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R14-1(10.5mm,46.9mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R15-1(46.65mm,48.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R16-1(26.4mm,36.6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R17-1(26.4mm,39.9mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R2-1(21.527mm,42.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R3-1(21.527mm,41.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R4-1(21.527mm,47.215mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R5-1(21.527mm,34.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R6-1(21.527mm,33.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R7-1(20.2mm,50.6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R8-1(26.4mm,37.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R9-1(26.4mm,38.8mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(15.71mm,52.652mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(15.71mm,51.702mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-4(18.36mm,50.752mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-5(18.36mm,51.702mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-1(12.946mm,38.95mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-2(12.946mm,38.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-4(14.796mm,37.65mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-5(14.796mm,38.3mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (15.395mm,30.49mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (15.395mm,35.39mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (15.395mm,35.39mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.212mm < 0.254mm) Between Arc (15.395mm,43.39mm) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (15.395mm,43.39mm) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (15.395mm,43.39mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (15.395mm,48.29mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad D1-2(49.275mm,48.25mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-1(46.977mm,42.855mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-1(46.977mm,42.855mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-10(50.877mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-10(50.877mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-2(50.877mm,42.855mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-2(50.877mm,42.855mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-3(46.977mm,41.585mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-4(50.877mm,41.585mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-5(46.977mm,40.315mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-6(50.877mm,40.315mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-7(46.977mm,39.045mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-8(50.877mm,39.045mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-9(46.977mm,37.775mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-9(46.977mm,37.775mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.094mm < 0.254mm) Between Pad U2-4(15.727mm,40.84mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad U6-1(12.946mm,38.95mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad U6-2(12.946mm,38.3mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad U6-3(12.946mm,37.65mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad U6-4(14.796mm,37.65mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad U6-5(14.796mm,38.3mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad U6-6(14.796mm,38.95mm) on Top Layer
And

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(3mm,3mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(3mm,61mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(52mm,3mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(52mm,61mm) on
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.373mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.373mm < 0.508mm) Between Board Edge And Track

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for JTAG_hat.PrjPcb


U7
C12
R18
C2
C1
U5
R10
R7
C6
C10
R11
R14
U3
R4
C3
C7
U2
R2
R3
R12
R13
U6
C11
Q1
R17
R9
R8
R16
C4
C8
U4
R5
R6
J1
C5
C9
U1
R1
J4
J2
R15
D1
J3
J5
L1