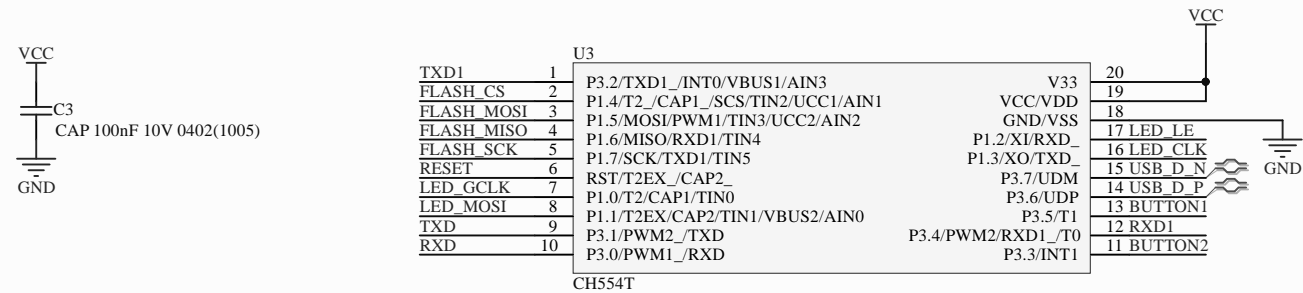
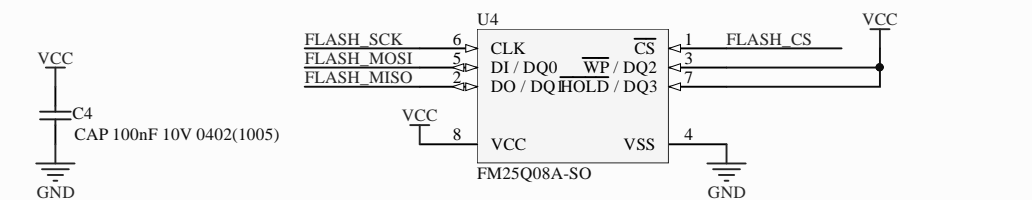


# MCU

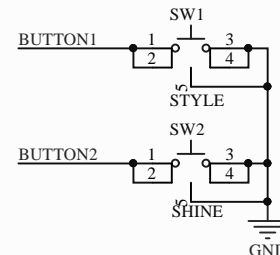


# SPI Flash

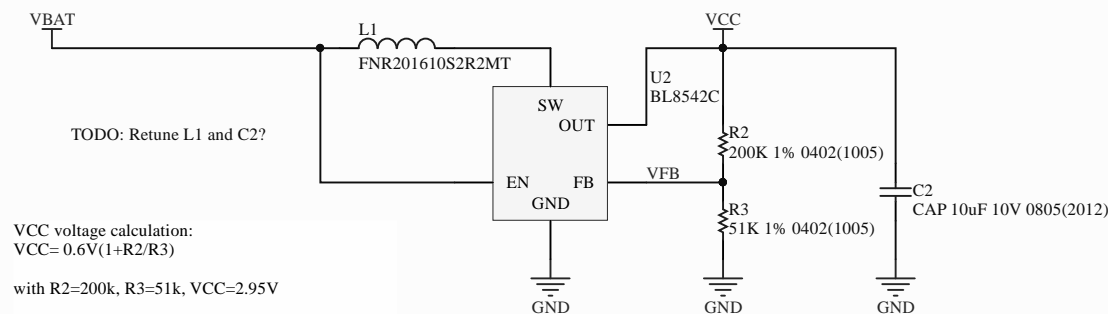


Note: Generic 8mBit flash, use a cheaper one.

# Buttons

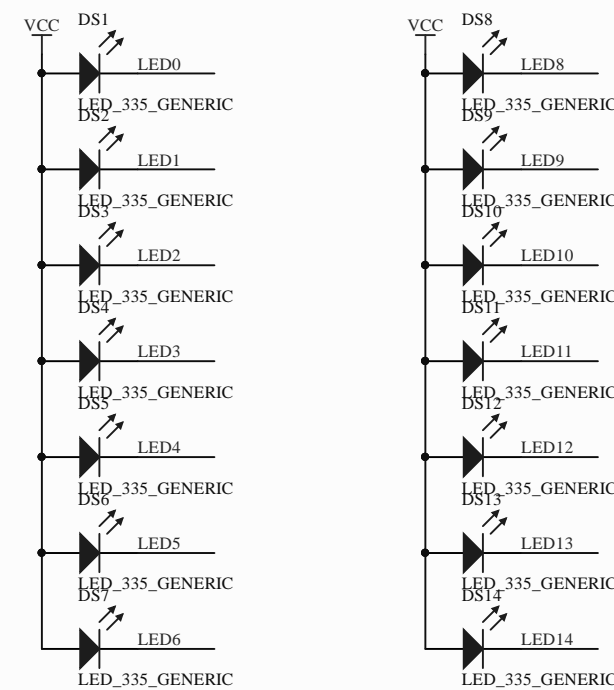


# Boost circuit for system power

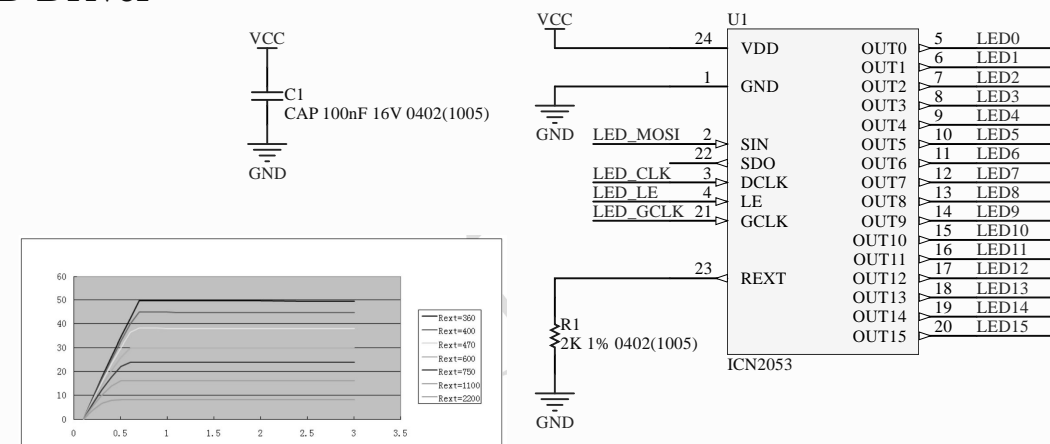


VCC voltage calculation:  
 $VCC = 0.6V(1 + R2/R3)$   
with  $R2=200k$ ,  $R3=51k$ ,  $VCC=2.95V$

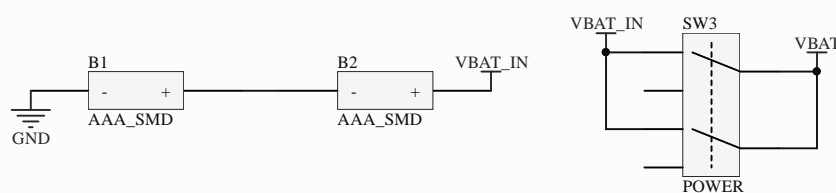
# LED Array



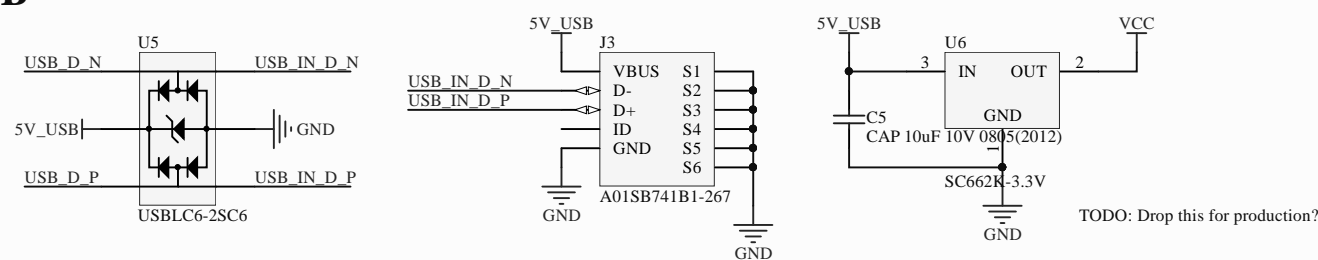
# LED Driver



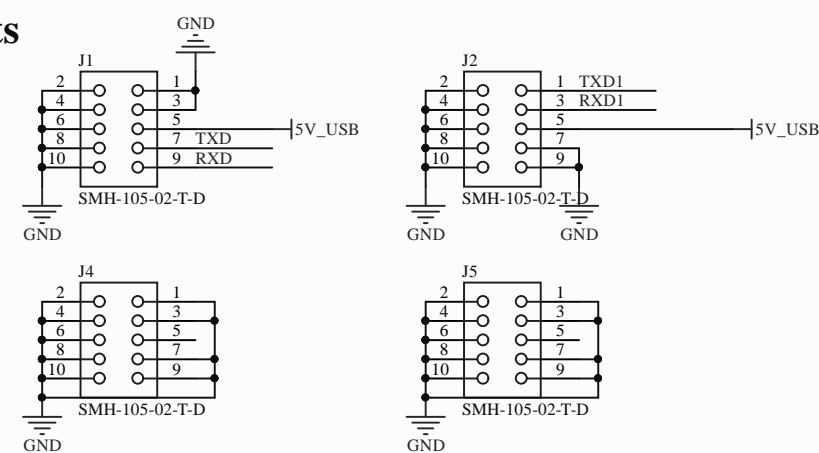
# Battery

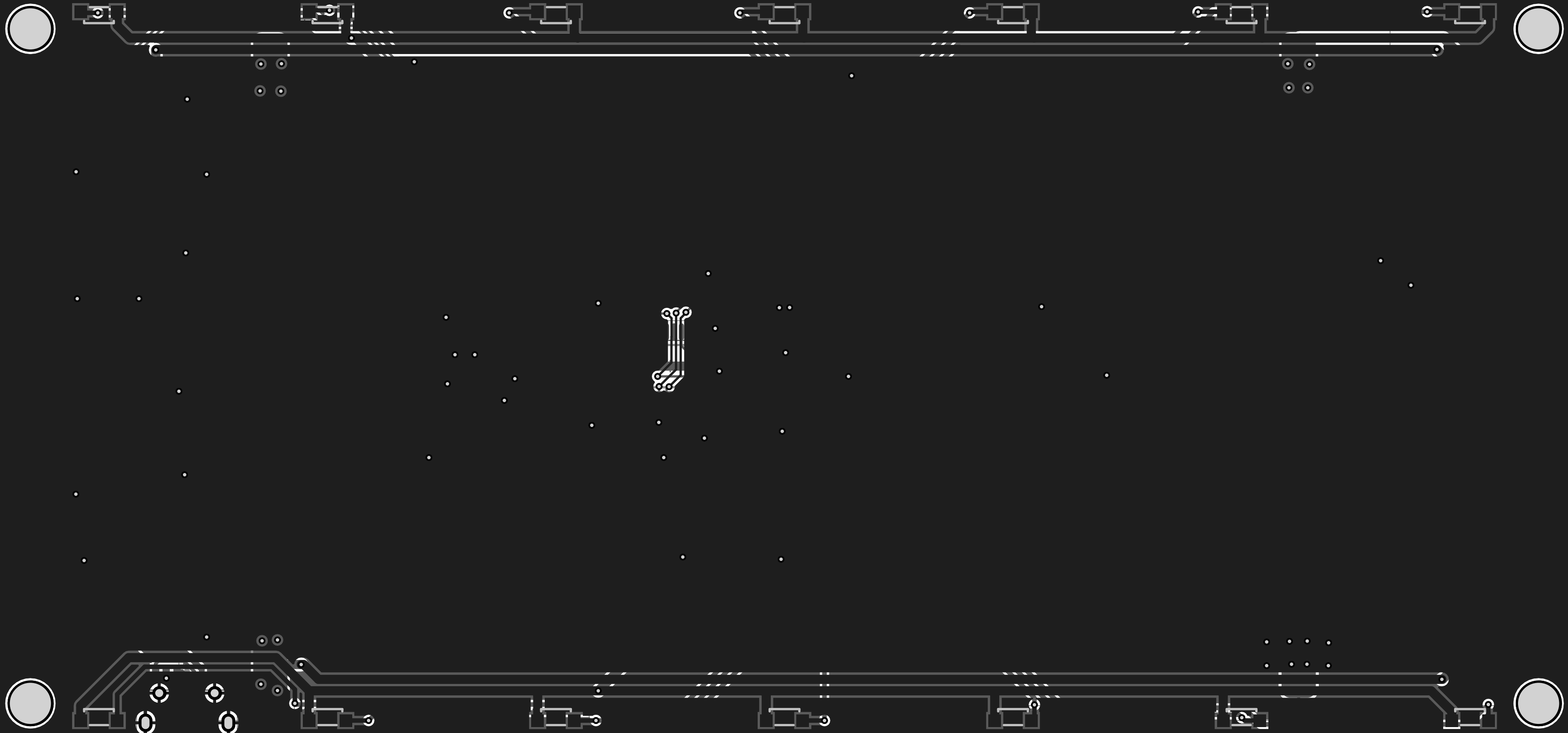


# USB



# Sync ports





## Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Blinkinlabs-Repos\LeoBlinky2018\pcb\LeoBlinky2018.PcbD

Warnings 0  
Rule Violations 164

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	22
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=2mm) (Preferred=0.4mm) (All)	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.711mm) (PreferredHoleWidth=0.711mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.2mm) (Max=0.2mm)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor	0
Hole Size Constraint (Min=0.025mm) (Max=3.6mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	18
Minimum Solder Mask Sliver (Gap=0mm) (OnLayer('Top Solder') and isfree),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	97
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	12
Room LeoBlinky2018 (Bounding Region = (187.45mm, 146.5mm, 333.45mm, 219.5mm)	0
Component Clearance Constraint ( Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm )	15
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	164

Clearance Constraint (Gap=0.2mm) (All),(All)	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-1(72.565mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-10(78.28mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-10(78.28mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-11(78.915mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-13(79.55mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-14(78.915mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-15(78.28mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-16(77.645mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-17(77.01mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-18(76.375mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-19(75.74mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-2(73.2mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-20(75.105mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-21(74.47mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-22(73.835mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-23(73.2mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-3(73.835mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-4(74.47mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-5(75.105mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-6(75.74mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-7(76.375mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-8(77.01mm,36.225mm) on Bottom Layer And Pad	

**Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)**

Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C1-1(69.55mm,30.425mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C3-1(50.895mm,28.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C4-1(57.9mm,28.45mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-D-(18.35mm,4.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-D-(18.35mm,4.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-D+(17.7mm,4.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-GND(16.4mm,4.9mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm) Between Pad J3-GND(16.4mm,4.9mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm) Between Pad J3-S4(20.125mm,4.9mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-1(69.5mm,31.95mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R2-1(44.675mm,34.25mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R3-1(44.675mm,32.225mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-1(43.061mm,33.125mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-2(42.111mm,33.125mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(16.85mm,6.825mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(15.9mm,6.825mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-4(14.95mm,9.575mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-5(15.9mm,9.575mm) on Bottom Layer

And

**Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)**

[illegible]



**Net Antennae (Tolerance=0mm) (All)**

Net Antennae: Via (114.05mm,59.95mm) from Top Layer to Bottom Layer
Net Antennae: Via (114.15mm,57.85mm) from Top Layer to Bottom Layer
Net Antennae: Via (115.8mm,57.85mm) from Top Layer to Bottom Layer
Net Antennae: Via (115.95mm,59.9mm) from Top Layer to Bottom Layer
Net Antennae: Via (24.175mm,5.675mm) from Top Layer to Bottom Layer
Net Antennae: Via (24.175mm,59.925mm) from Top Layer to Bottom Layer
Net Antennae: Via (24.1mm,57.575mm) from Top Layer to Bottom Layer
Net Antennae: Via (24.275mm,9.475mm) from Top Layer to Bottom Layer
Net Antennae: Via (25.625mm,5.123mm) from Top Layer to Bottom Layer
Net Antennae: Via (25.625mm,9.55mm) from Top Layer to Bottom Layer
Net Antennae: Via (25.925mm,57.55mm) from Top Layer to Bottom Layer
Net Antennae: Via (25.975mm,59.95mm) from Top Layer to Bottom Layer

**Component Clearance Constraint ( Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm ) (All),(All)**

Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic ORI RevC
Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic ORI RevC
Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic ORI RevC
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Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic ORI RevC
Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic ORI RevC
Component Clearance Constraint: (Collision < 0.254mm) Between SMT Small Component B2-AAA_SMD (25mm,33.5mm)

on



## Electrical Rules Check Report

Class	Document	Message
Warning	LeoBlinky2018.SchDoc	Net FLASH_CS has no driving source (Pin U3-2,Pin U4-1)
Warning	LeoBlinky2018.SchDoc	Net FLASH_SCK has no driving source (Pin U3-5,Pin U4-6)
Error	LeoBlinky2018.SchDoc	Net LED7 has only one pin (Pin U1-12)
Error	LeoBlinky2018.SchDoc	Net LED15 has only one pin (Pin U1-20)
Warning	LeoBlinky2018.SchDoc	Net LED_CLK has no driving source (Pin U1-3,Pin U3-16)
Warning	LeoBlinky2018.SchDoc	Net LED_GCLK has no driving source (Pin U1-21,Pin U3-7)
Warning	LeoBlinky2018.SchDoc	Net LED_LE has no driving source (Pin U1-4,Pin U3-17)
Warning	LeoBlinky2018.SchDoc	Net LED_MOSI has no driving source (Pin U1-2,Pin U3-8)
Error	LeoBlinky2018.SchDoc	Net RESET has only one pin (Pin U3-6)

