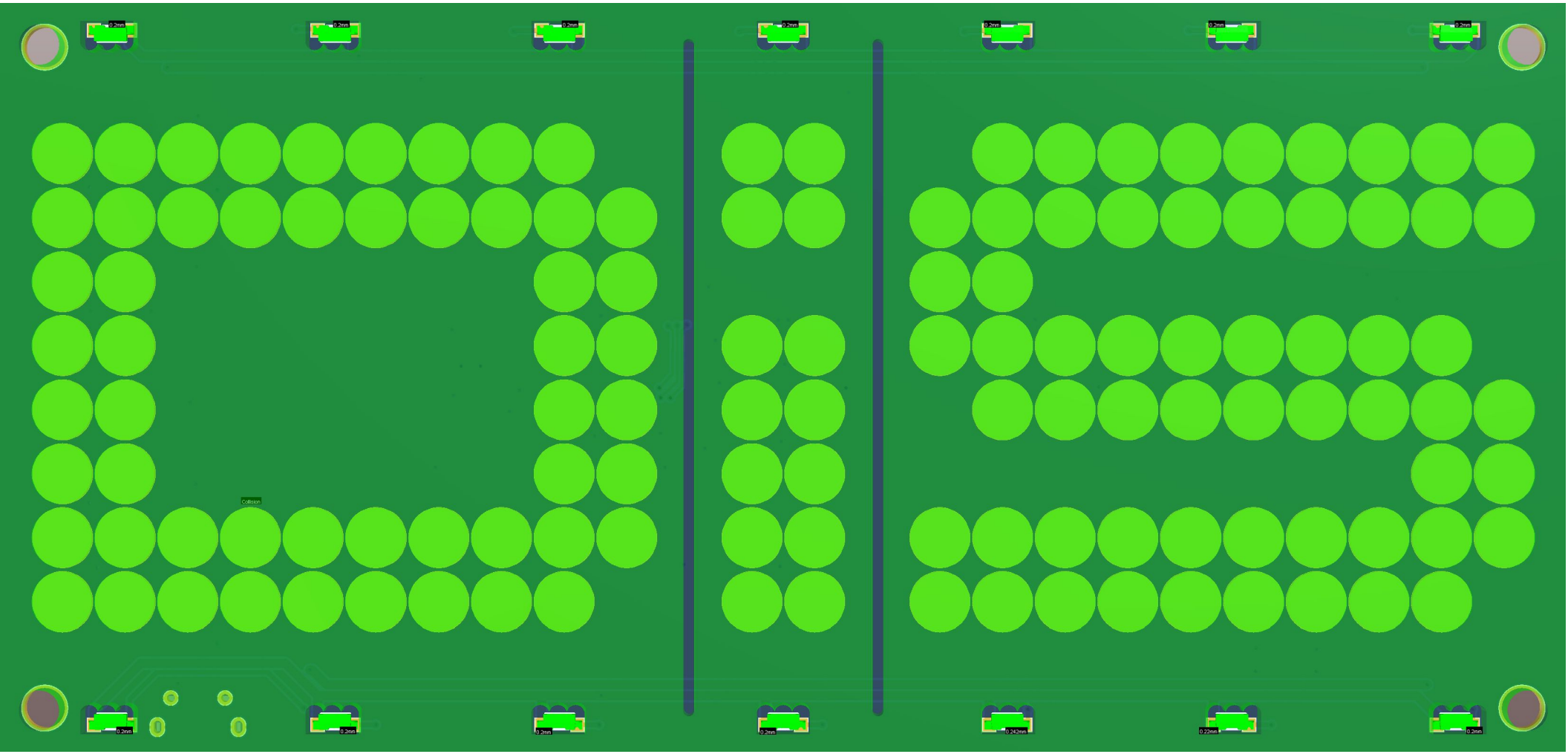
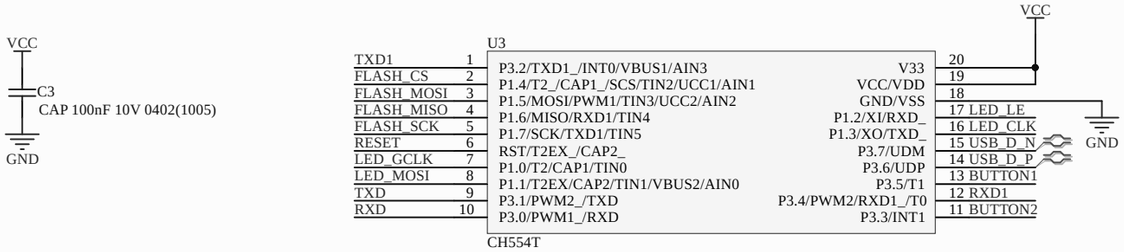
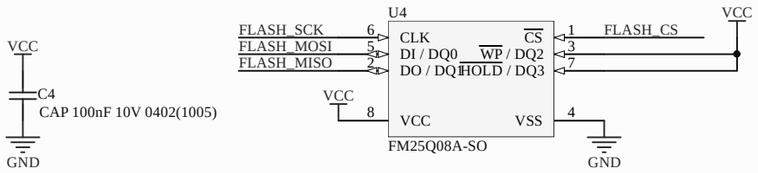

Collision

MCU

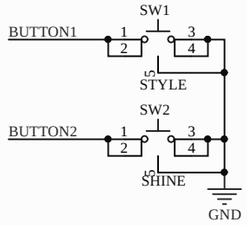


SPI Flash

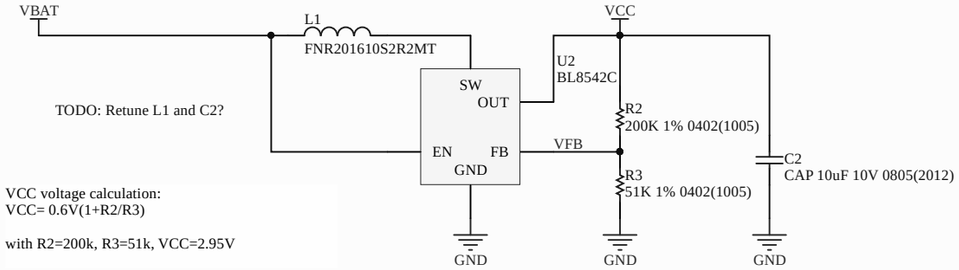


Note: Generic 8mBit flash, use a cheaper one.

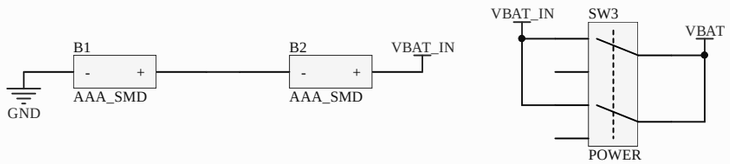
Buttons



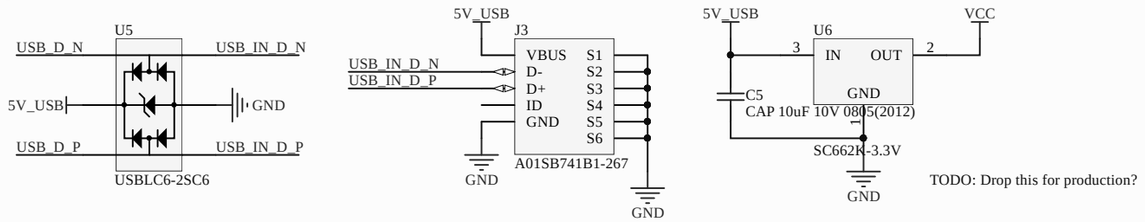
Boost circuit for system power



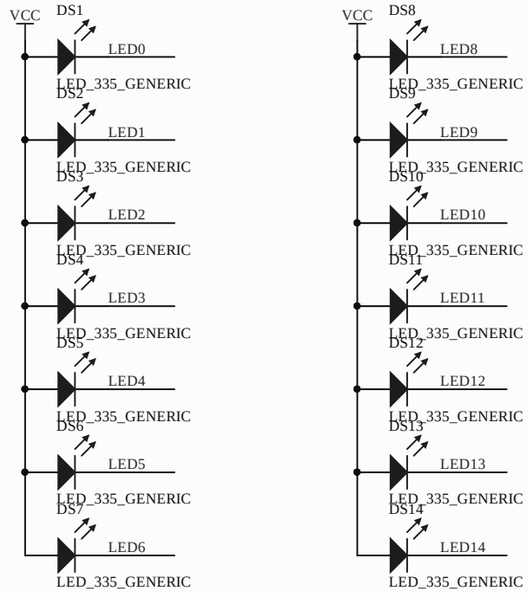
Battery



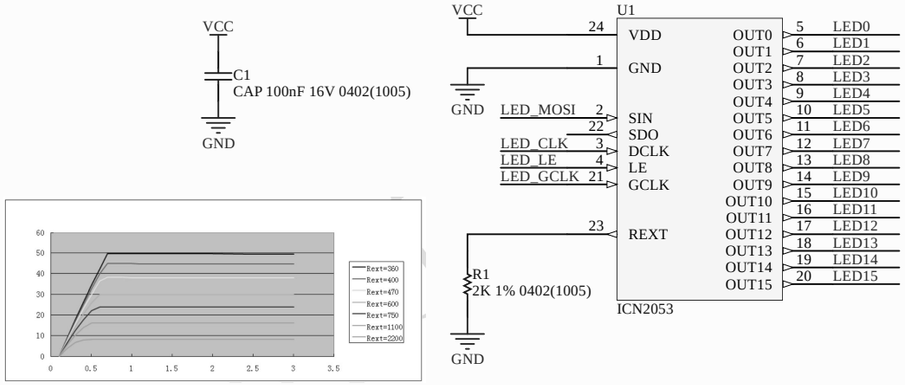
USB



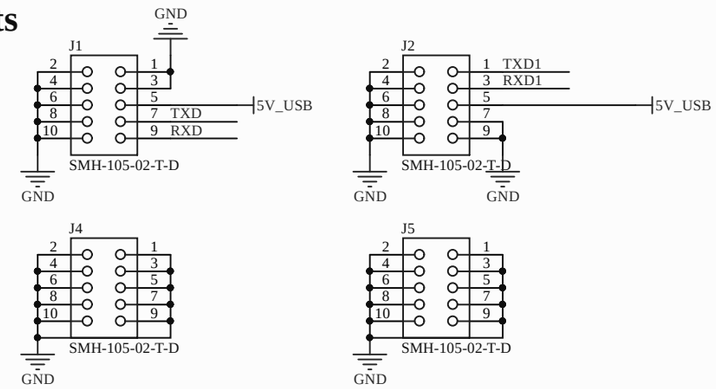
LED Array



LED Driver



Sync ports



Title: LeoBlinky 2018		
Project: LeoBlinky2018.PrjPCB		Revision: C
Date: 7/17/2018	Time: 11:48:08 PM	Sheet 1 of 1

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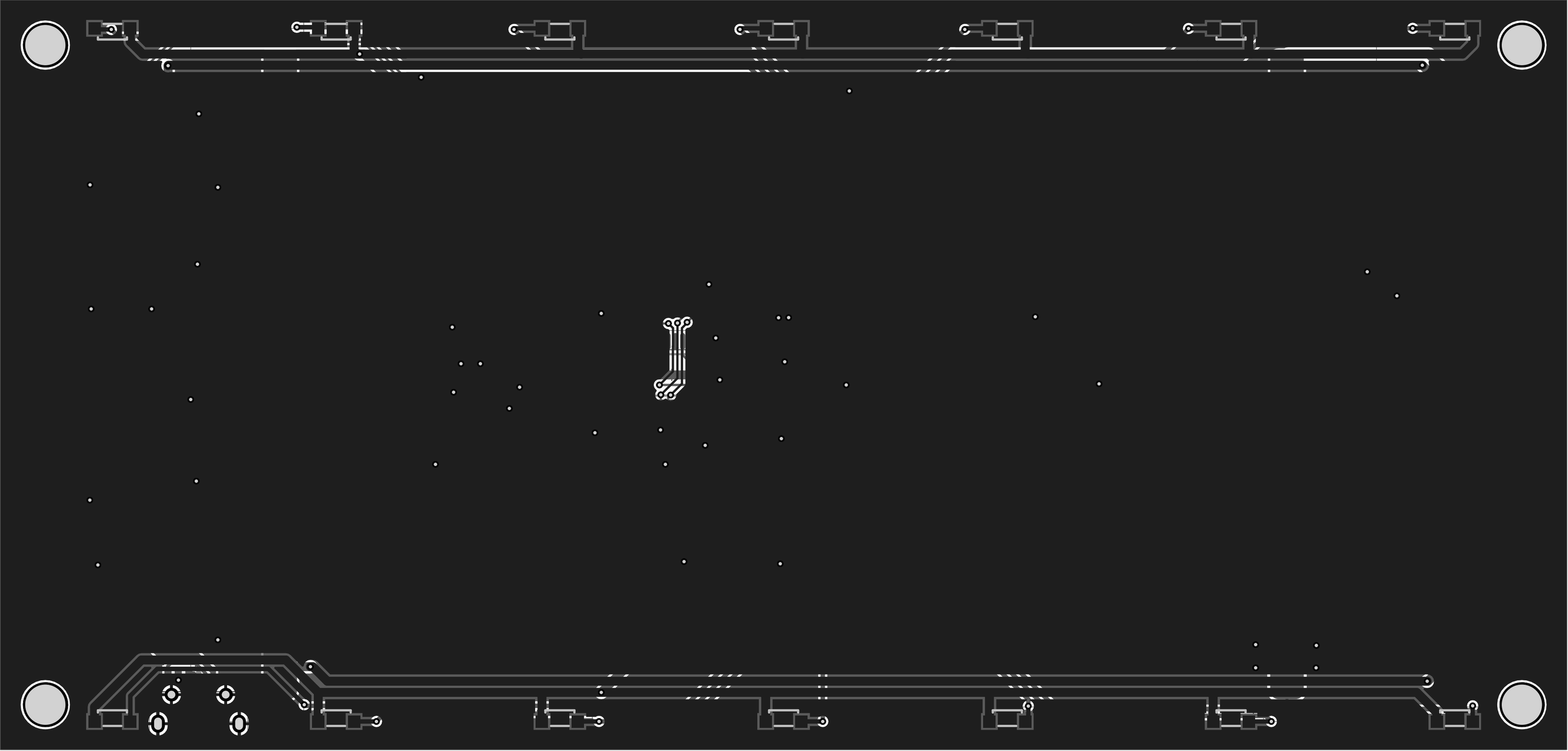

Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Blinkinlabs-Repos\LeoBlinky2018\pcb\LeoBlinky2018.PcbD

Warnings 0
Rule Violations 152

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	22
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=2mm) (Preferred=0.4mm) (All)	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.711mm) (PreferredHoleWidth=0.711mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.2mm) (Max=0.2mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=3.6mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	18
Minimum Solder Mask Sliver (Gap=0mm) (OnLayer('Top Solder') and isfree),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	97
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Room LeoBlinky2018 (Bounding Region = (187.45mm, 146.5mm, 333.45mm, 219.5mm)	0
Component Clearance Constraint (Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm)	15
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	152

Clearance Constraint (Gap=0.2mm) (All),(All)
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-1(72.565mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-10(78.28mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-10(78.28mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-11(78.915mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-13(79.55mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-14(78.915mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-15(78.28mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-16(77.645mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-17(77.01mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-18(76.375mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-19(75.74mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-2(73.2mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-20(75.105mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-21(74.47mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-22(73.835mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-23(73.2mm,30.775mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-3(73.835mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-4(74.47mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-5(75.105mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-6(75.74mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-7(76.375mm,36.225mm) on Bottom Layer And Pad
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-8(77.01mm,36.225mm) on Bottom Layer And Pad

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C1-1(69.55mm,30.425mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C3-1(50.895mm,28.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C4-1(57.9mm,28.45mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-D-(18.35mm,4.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-D-(18.35mm,4.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-D+(17.7mm,4.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad J3-GND(16.4mm,4.9mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm) Between Pad J3-GND(16.4mm,4.9mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm) Between Pad J3-S4(20.125mm,4.9mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-1(69.5mm,31.95mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R2-1(44.675mm,34.25mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R3-1(44.675mm,32.225mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-1(43.061mm,33.125mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U2-2(42.111mm,33.125mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(16.85mm,6.825mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(15.9mm,6.825mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-4(14.95mm,9.575mm) on Bottom Layer
And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-5(15.9mm,9.575mm) on Bottom Layer
And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Arc (43.911mm,33.125mm) on Bottom Overlay
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad B1-1(115mm,59.5mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad B1-2(115mm,7.5mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad B2-1(25mm,59.5mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad B2-2(25mm,7.5mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(41.995mm,37.925mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-1(41.995mm,37.925mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C2-2(43.795mm,37.925mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C2-2(43.795mm,37.925mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C5-1(38.5mm,27.7mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C5-1(38.5mm,27.7mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad C5-2(38.5mm,29.5mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.193mm < 0.254mm) Between Pad C5-2(38.5mm,29.5mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS10-1(91.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS10-1(91.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS10-2(88.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS10-2(88.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad DS1-1(8.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS1-1(8.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS11-1(71.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS11-1(71.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS11-2(68.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS11-2(68.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS1-2(11.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.192mm < 0.254mm) Between Pad DS1-2(11.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS12-1(51.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS12-1(51.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS12-2(48.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS12-2(48.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS13-1(31.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS13-1(31.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS13-2(28.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS13-2(28.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS14-1(11.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS14-1(11.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS14-2(8.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS14-2(8.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad DS2-1(28.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS2-1(28.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.192mm < 0.254mm) Between Pad DS2-2(31.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS2-2(31.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad DS3-1(48.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS3-1(48.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.192mm < 0.254mm) Between Pad DS3-2(51.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS3-2(51.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad DS4-1(68.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS4-1(68.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.192mm < 0.254mm) Between Pad DS4-2(71.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS4-2(71.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad DS5-1(88.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS5-1(88.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.192mm < 0.254mm) Between Pad DS5-2(91.6mm,64.5mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS5-2(91.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad DS6-1(108.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS6-1(108.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.192mm < 0.254mm) Between Pad DS6-2(111.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS6-2(111.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad DS7-1(128.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS7-1(128.4mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.192mm < 0.254mm) Between Pad DS7-2(131.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS7-2(131.6mm,64.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS8-1(131.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS8-1(131.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS8-2(128.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS8-2(128.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-1(111.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-1(111.6mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-2(108.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-2(108.4mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad L1-1(38.611mm,34.5mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.182mm < 0.254mm) Between Pad L1-1(38.611mm,34.5mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.254mm) Between Pad L1-2(38.611mm,35.9mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.185mm < 0.254mm) Between Pad L1-2(38.611mm,35.9mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW1-1(35.25mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW1-1(35.25mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW1-2(42.75mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW1-2(42.75mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW1-3(35.25mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW1-3(35.25mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW1-4(42.75mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW1-4(42.75mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW1-5(35.5mm,14mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW1-5(35.5mm,14mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW2-1(48.25mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW2-1(48.25mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW2-2(55.75mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW2-2(55.75mm,16.25mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW2-3(48.25mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW2-3(48.25mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad SW2-4(55.75mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad SW2-4(55.75mm,11.75mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW2-5(48.5mm,14mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW2-5(48.5mm,14mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW3-1(40.62mm,48mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW3-3(40.62mm,44mm) on Bottom Layer And
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad SW3-4(35.38mm,44mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW3-6(35.38mm,48mm) on Bottom Layer And

Component Clearance Constraint (Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm) (All),(All)
Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic DIS RevC
Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic DIS RevC
Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic DIS RevC
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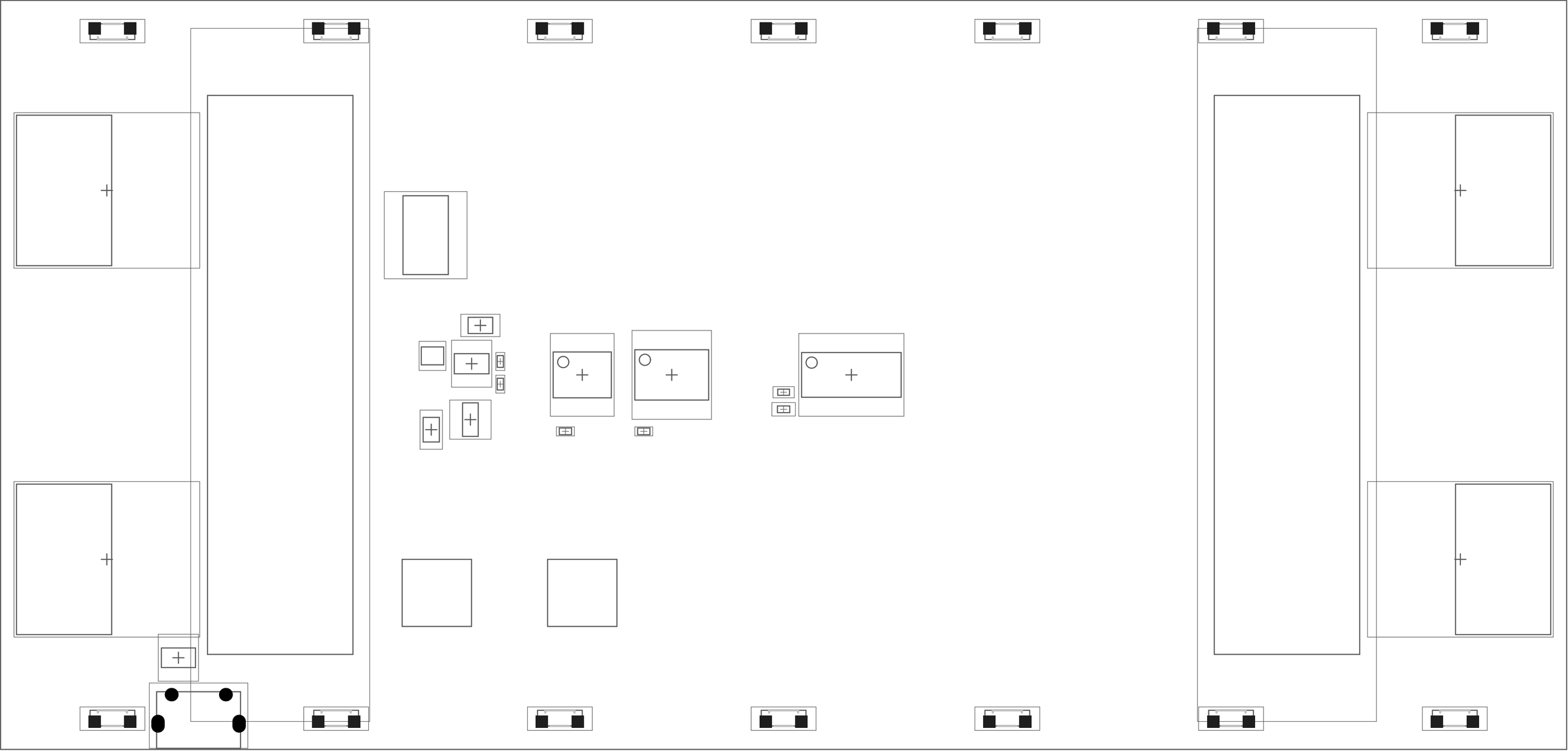
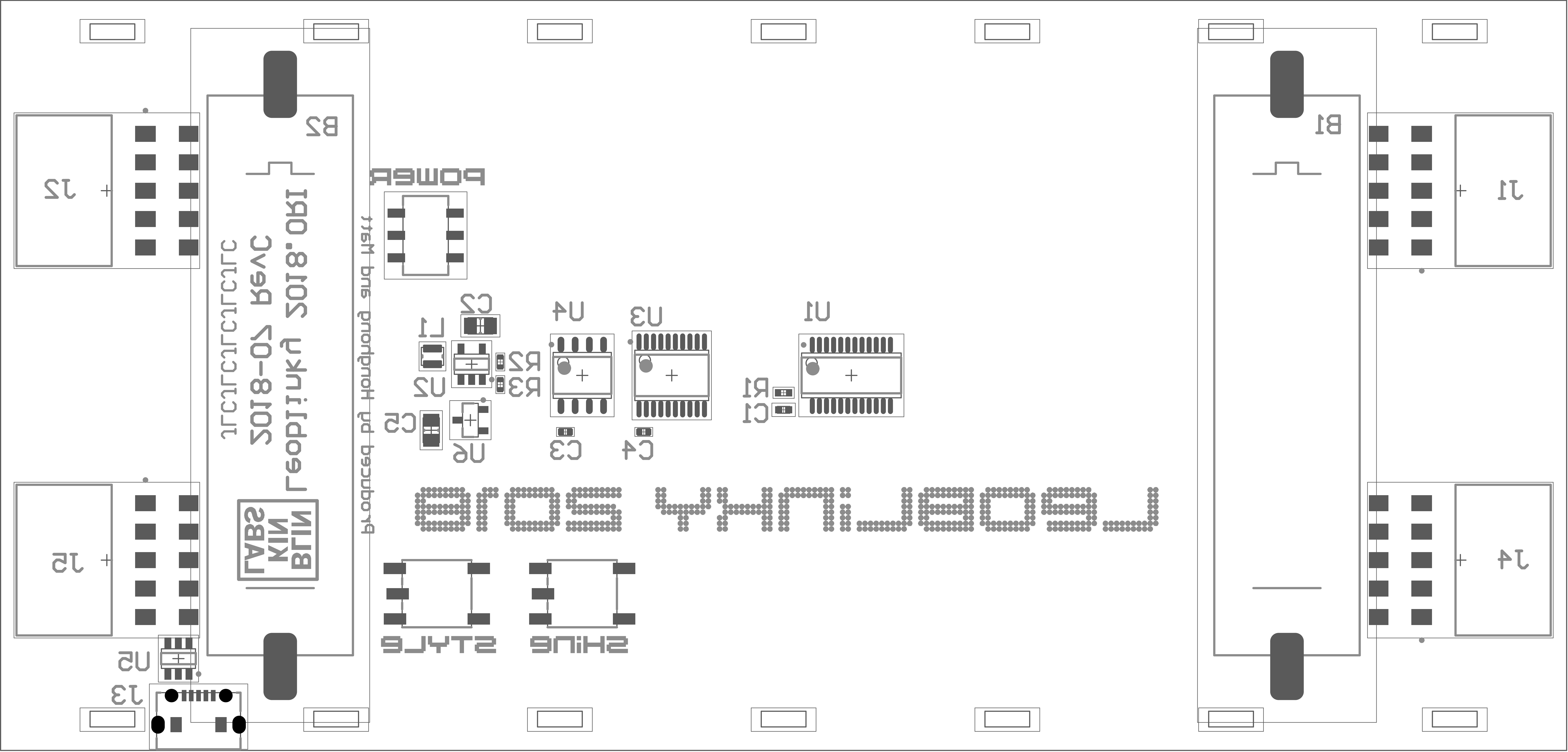
Component Clearance Constraint: (Collision < 0.254mm) Between 3D STEP 2018-07-17 LeoBlinky2018 Acrylic DIS RevC
Component Clearance Constraint: (Collision < 0.254mm) Between SMT Small Component B2-AAA_SMD (25mm,33.5mm)

on

Electrical Rules Check Report

Class	Document	Message
Warning	LeoBlinky2018.SchDoc	Net FLASH_CS has no driving source (Pin U3-2,Pin U4-1)
Warning	LeoBlinky2018.SchDoc	Net FLASH_SCK has no driving source (Pin U3-5,Pin U4-6)
Error	LeoBlinky2018.SchDoc	Net LED7 has only one pin (Pin U1-12)
Error	LeoBlinky2018.SchDoc	Net LED15 has only one pin (Pin U1-20)
Warning	LeoBlinky2018.SchDoc	Net LED_CLK has no driving source (Pin U1-3,Pin U3-16)
Warning	LeoBlinky2018.SchDoc	Net LED_GCLK has no driving source (Pin U1-21,Pin U3-7)
Warning	LeoBlinky2018.SchDoc	Net LED_LE has no driving source (Pin U1-4,Pin U3-17)
Warning	LeoBlinky2018.SchDoc	Net LED_MOSI has no driving source (Pin U1-2,Pin U3-8)
Error	LeoBlinky2018.SchDoc	Net RESET has only one pin (Pin U3-6)





LEOBLINKY 2018
POWER
STYLE
SHINE
B1
B2
J1
J2
J3
J4
J5
U1
U2
U3
U4
U5
U6
C1
C2
C3
C4
C5
R1
R2
R3
L1