







## Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Blinkinlabs-Repos\LeoBlinky\_2018\pcb\LeoBlinky2018.Pcb

Warnings 0  
Rule Violations 118

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	22
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=2mm) (Preferred=0.4mm) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	2
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	19
Silk To Solder Mask (Clearance=0.254mm) (Is Pad),(All)	75
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Room LeoBlinky2018 (Bounding Region = (187.45mm, 146.5mm, 333.45mm, 219.5mm))	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	118

Clearance Constraint (Gap=0.2mm) (All),(All)	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-1(72.565mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-10(78.28mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-10(78.28mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-11(78.915mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-13(79.55mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-14(78.915mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-15(78.28mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-16(77.645mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-17(77.01mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-18(76.375mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-19(75.74mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-2(73.2mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-20(75.105mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-21(74.47mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-22(73.835mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-23(73.2mm,30.775mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-3(73.835mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-4(74.47mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-5(75.105mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-6(75.74mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-7(76.375mm,36.225mm) on Bottom Layer And Pad	
Clearance Constraint: (0.185mm < 0.2mm) Between Pad U1-8(77.01mm,36.225mm) on Bottom Layer And Pad	

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (4mm > 2.54mm) Pad Free-1(136mm,63mm) on Multi-Layer Actual Hole Size = 4mm	
Hole Size Constraint: (4mm > 2.54mm) Pad Free-1(4mm,63mm) on Multi-Layer Actual Hole Size = 4mm	

<b>Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)</b>	
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm)	Between Pad C1-1(69.55mm,30.425mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm)	Between Pad C3-1(50.895mm,28.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm)	Between Pad C4-1(57.9mm,28.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-D-(4.9mm,5.95mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-D-(4.9mm,5.95mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-D+(4.9mm,6.6mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-GND(4.9mm,7.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm)	Between Pad J3-GND(4.9mm,7.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.073mm < 0.254mm)	Between Pad J3-S1(2.3mm,10.225mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm)	Between Pad J3-S4(4.9mm,4.175mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm)	Between Pad R1-1(69.5mm,31.95mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm)	Between Pad R2-1(44.675mm,34.25mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm)	Between Pad R3-1(44.675mm,32.225mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U2-1(43.061mm,33.125mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U2-2(42.111mm,33.125mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-1(9.025mm,7.644mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-2(9.025mm,8.594mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-4(11.775mm,9.544mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-5(11.775mm,8.594mm) on Bottom Layer

**Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)**

[illegible]

**Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)**

Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS6-1(108.15mm,64.5mm) on Top Layer
<del>Silk To Solder Mask Clearance Constraint: (0.192mm &lt; 0.254mm) Between Pad DS6-2(111.85mm,64.5mm) on Top Layer</del>
<del>Silk To Solder Mask Clearance Constraint: (0.15mm &lt; 0.254mm) Between Pad DS6-2(111.85mm,64.5mm) on Top Layer</del>
<del>Silk To Solder Mask Clearance Constraint: (0.248mm &lt; 0.254mm) Between Pad DS7-1(128.15mm,64.5mm) on Top Layer</del>
<del>Silk To Solder Mask Clearance Constraint: (0.15mm &lt; 0.254mm) Between Pad DS7-1(128.15mm,64.5mm) on Top Layer</del>
<del>Silk To Solder Mask Clearance Constraint: (0.192mm &lt; 0.254mm) Between Pad DS7-2(131.85mm,64.5mm) on Top Layer</del>
<del>Silk To Solder Mask Clearance Constraint: (0.15mm &lt; 0.254mm) Between Pad DS7-2(131.85mm,64.5mm) on Top Layer</del>
<del>Silk To Solder Mask Clearance Constraint: (0.15mm &lt; 0.254mm) Between Pad DS8-1(131.85mm,2.5mm) on Top Layer And</del>
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS8-1(131.85mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS8-2(128.15mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS8-2(128.15mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-1(111.85mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-1(111.85mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-2(108.15mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad DS9-2(108.15mm,2.5mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad L1-1(38.611mm,34.5mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.182mm < 0.254mm) Between Pad L1-1(38.611mm,34.5mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.254mm) Between Pad L1-2(38.611mm,35.9mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.185mm < 0.254mm) Between Pad L1-2(38.611mm,35.9mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW3-1(38.82mm,44.6mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad SW3-3(38.82mm,40.6mm) on Bottom Layer
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad SW3-4(33.58mm,40.6mm) on Bottom
<del>Silk To Solder Mask Clearance Constraint: (0.2mm &lt; 0.254mm) Between Pad SW3-6(33.58mm,44.6mm) on Bottom Layer</del>

## Electrical Rules Check Report

Class	Document	Message
Warning	LeoBlinky2018.SchDoc	Net FLASH_CS has no driving source (Pin U3-2,Pin U4-1)
Warning	LeoBlinky2018.SchDoc	Net FLASH_SCK has no driving source (Pin U3-5,Pin U4-6)
Error	LeoBlinky2018.SchDoc	Net LED7 has only one pin (Pin U1-12)
Error	LeoBlinky2018.SchDoc	Net LED15 has only one pin (Pin U1-20)
Warning	LeoBlinky2018.SchDoc	Net LED_CLK has no driving source (Pin U1-3,Pin U3-7)
Warning	LeoBlinky2018.SchDoc	Net LED_GCLK has no driving source (Pin U1-21,Pin U3-16)
Warning	LeoBlinky2018.SchDoc	Net LED_LE has no driving source (Pin U1-4,Pin U3-17)
Warning	LeoBlinky2018.SchDoc	Net LED_MOSI has no driving source (Pin U1-2,Pin U3-8)
Error	LeoBlinky2018.SchDoc	Net RESET has only one pin (Pin U3-6)
Warning	LeoBlinky2018.SchDoc	VCC contains IO Pin and Power Pin objects (Pin U4-3,Pin U4-7,Pin U4-8,Pin U3-19,Pin U3-20,Pin U1-24)





