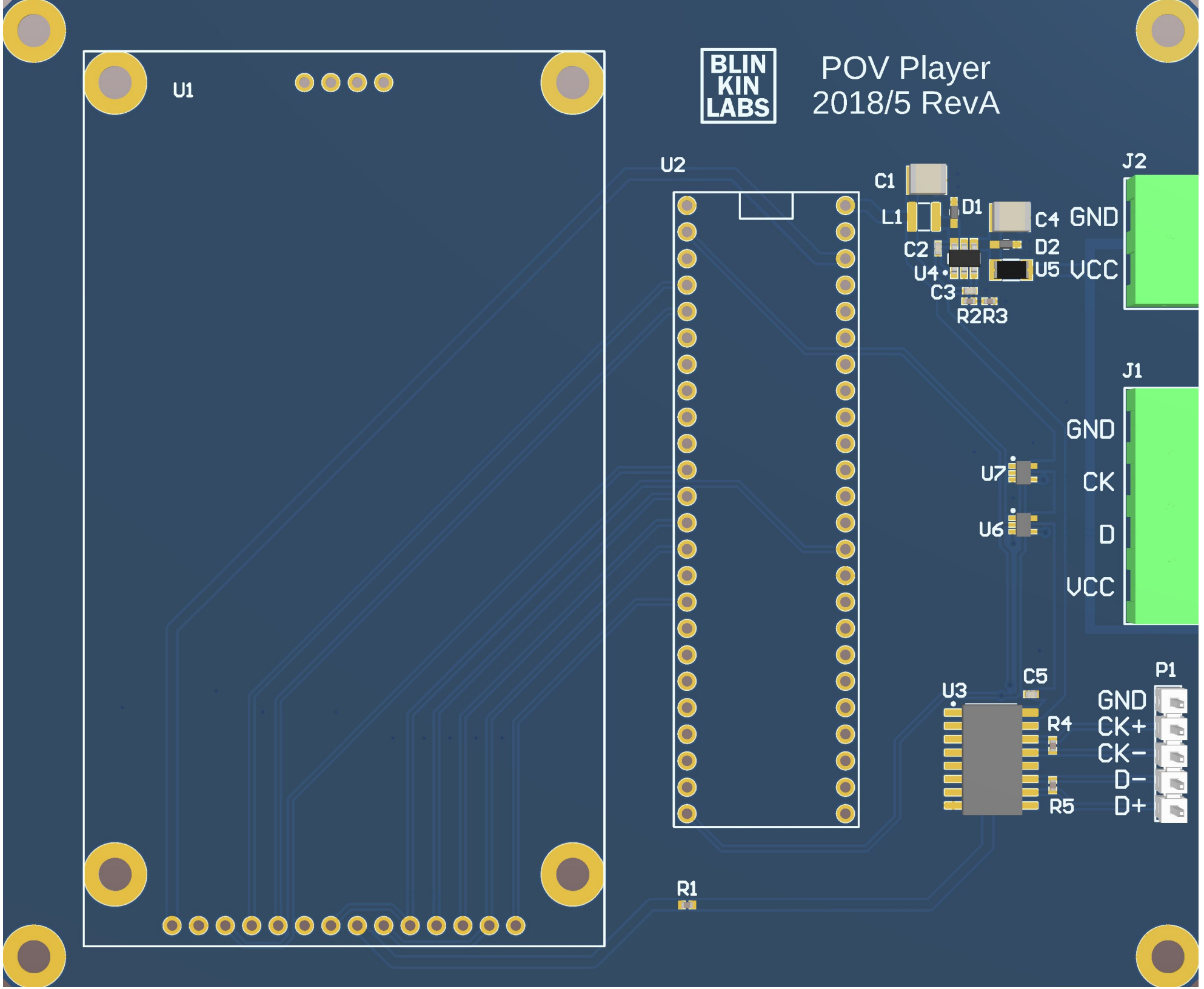
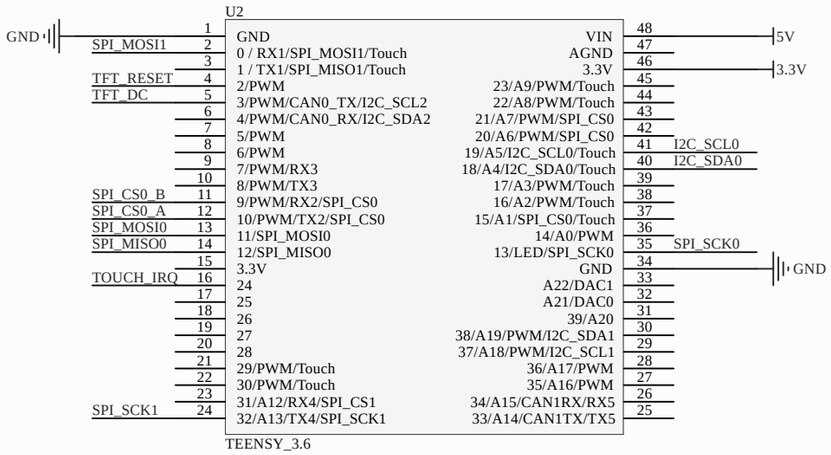
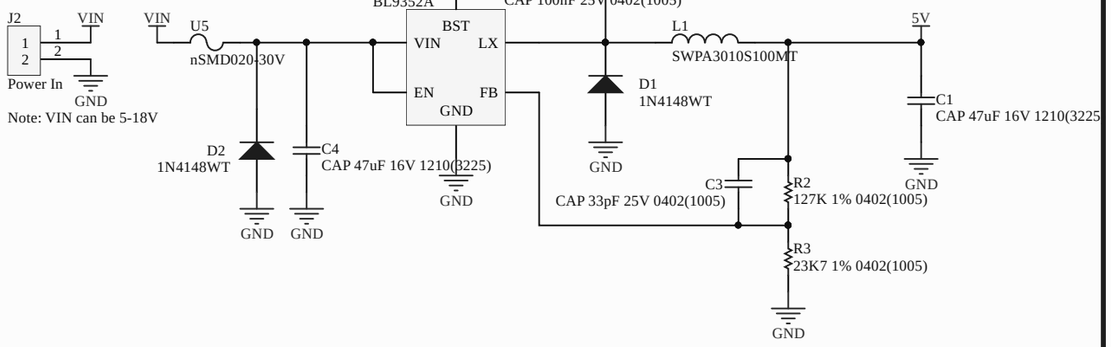

BLIN
KIN
LABS
POV Player
2018/5 RevA
U1
U2
C1
L1
D1
C4
GND
C2
D2
U4
U5
VCC
C3
R2
R3
J2
J1
GND
CK
D
VCC
U7
U6
U3
C5
R4
R5
P1
GND
CK+
CK−
D−
D+
R1

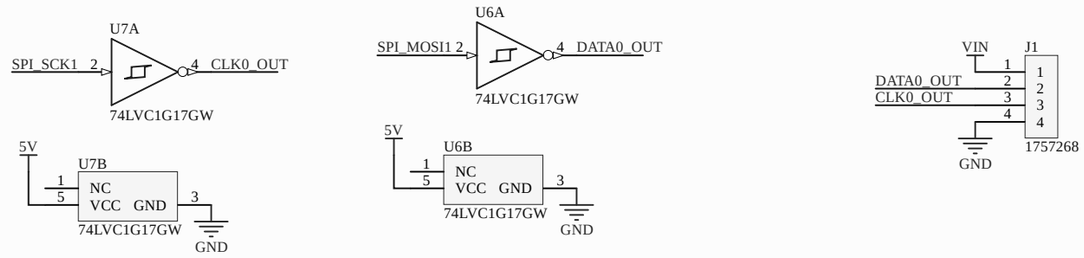
MCU



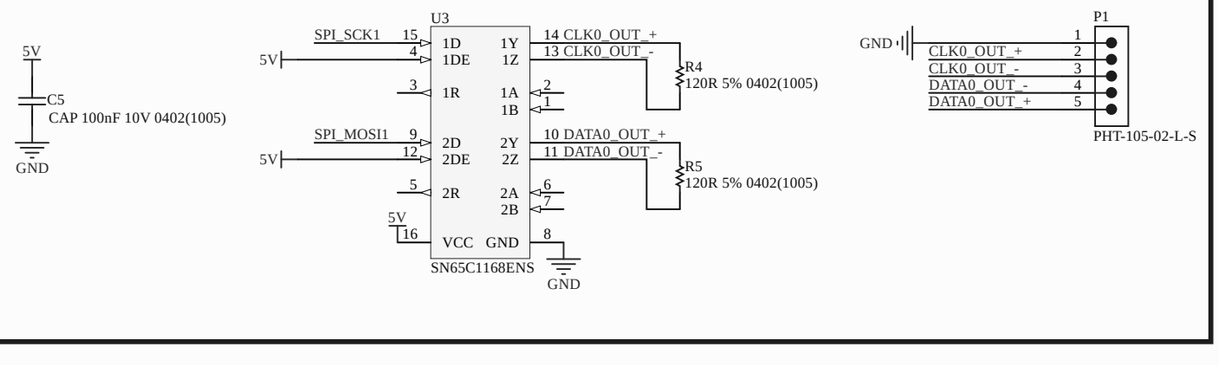
Power Supply



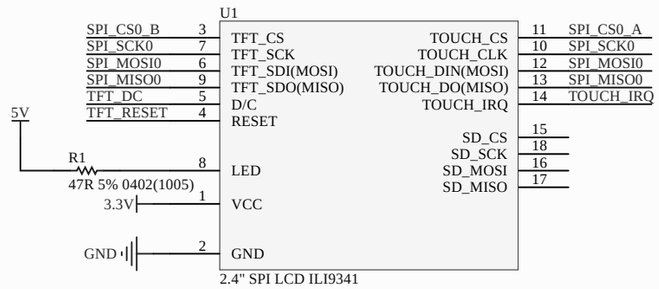
Buffered 5V output (APA102 strip)



Differential output (dot pixels)



LCD with touch screen



Title: *		
Project: POV_Player.PrjPCB	Revision: *	BLINKINLABS
Date: 5/29/2018 Time: 7:10:40 PM	Sheet * of *	

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POV Player
2018/5 RevA

U1
U2
C1
L1
D1
C4
GND
C2
D2
U4
U5
VCC
C3
R2R3
J2
J1
GND
U7
CK
D
U6
VCC
C5
P1
U3
GND
R4
CK+
CK-
D-
R5
D+
R1

Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Blinkinlabs-Repos\POV_Player\pcb\board.PcbDoc

Warnings 0
Rule Violations 39

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=3mm) (Preferred=0.8mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	8
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	16
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	14
Silk to Silk (Clearance=0.254mm) (All),(All)	1
Net Antennae (Tolerance=0mm) (All)	0
Room board (Bounding Region = (21.5mm, 4.5mm, 159.5mm, 142.5mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	39

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-M5(112mm,102mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-M6(112mm,13mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-M7(3mm,13mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-M8(3mm,102mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad U1-M1(10.81mm,20.92mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad U1-M2(10.81mm,97mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad U1-M3(54.81mm,97mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad U1-M4(54.81mm,20.92mm) on Multi-Layer Actual Hole Size = 3.2mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C2-1(89.899mm,80.65mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C3-1(93.349mm,77mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.077mm < 0.254mm) Between Pad C5-1(98.408mm,38.2mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-1(66.26mm,18mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R2-1(93.349mm,76mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R3-1(95.299mm,76mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R4-1(100.9mm,32.8mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R5-1(100.9mm,30mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-1(91.449mm,78.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-2(92.399mm,78.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-4(93.349mm,81.45mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-5(92.399mm,81.45mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U6-1(97.078mm,55.15mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U6-2(97.078mm,54.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U7-1(97.078mm,60.15mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad U7-2(97.078mm,59.5mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.194mm < 0.254mm) Between Pad L1-1(89.699mm,84.08mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.194mm < 0.254mm) Between Pad L1-1(89.699mm,84.08mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.254mm < 0.254mm) Between Pad L1-2(87.399mm,84.08mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad L1-2(87.399mm,84.08mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U1-M1(10.81mm,20.92mm) on Multi-Layer
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U1-M2(10.81mm,97mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U1-M2(10.81mm,97mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U1-M3(54.81mm,97mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U1-M3(54.81mm,97mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U1-M4(54.81mm,20.92mm) on Multi-Layer
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.254mm) Between Pad U5-1(98.399mm,79mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.254mm) Between Pad U5-1(98.399mm,79mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.254mm) Between Pad U5-2(95.399mm,79mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.254mm) Between Pad U5-2(95.399mm,79mm) on Top Layer And

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.247mm < 0.254mm) Between Text "R2" (91.899mm,74mm) on Top Overlay And Te›

Electrical Rules Check Report

Class	Document	Message
Error	board.SchDoc	Net I2C_SCL0 has only one pin (Pin U2-41)
Error	board.SchDoc	Net I2C_SDA0 has only one pin (Pin U2-40)
Error	board.SchDoc	Net NetU3_1 contains floating input pins (Pin U3-1)
Warning	board.SchDoc	Net NetU3_1 has no driving source (Pin U3-1)
Error	board.SchDoc	Net NetU3_2 contains floating input pins (Pin U3-2)
Warning	board.SchDoc	Net NetU3_2 has no driving source (Pin U3-2)
Error	board.SchDoc	Net NetU3_6 contains floating input pins (Pin U3-6)
Warning	board.SchDoc	Net NetU3_6 has no driving source (Pin U3-6)
Error	board.SchDoc	Net NetU3_7 contains floating input pins (Pin U3-7)
Warning	board.SchDoc	Net NetU3_7 has no driving source (Pin U3-7)
Warning	board.SchDoc	Net SPI_MOSI1 has no driving source (Pin U2-2,Pin U3-9,Pin U6-2)
Warning	board.SchDoc	Net SPI_SCK1 has no driving source (Pin U2-24,Pin U3-15,Pin U7-2)
Warning	board.SchDoc	Unconnected Pin U3-1 at 11100mil,6800mil
Warning	board.SchDoc	Unconnected Pin U3-2 at 11100mil,6900mil
Warning	board.SchDoc	Unconnected Pin U3-6 at 11100mil,6300mil
Warning	board.SchDoc	Unconnected Pin U3-7 at 11100mil,6200mil

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U1

U2

C1
L1
D1
C4
C2
D2
U4
U5
C3
R2
R3

J2
GND
VCC

J1
GND
CK
D
VCC

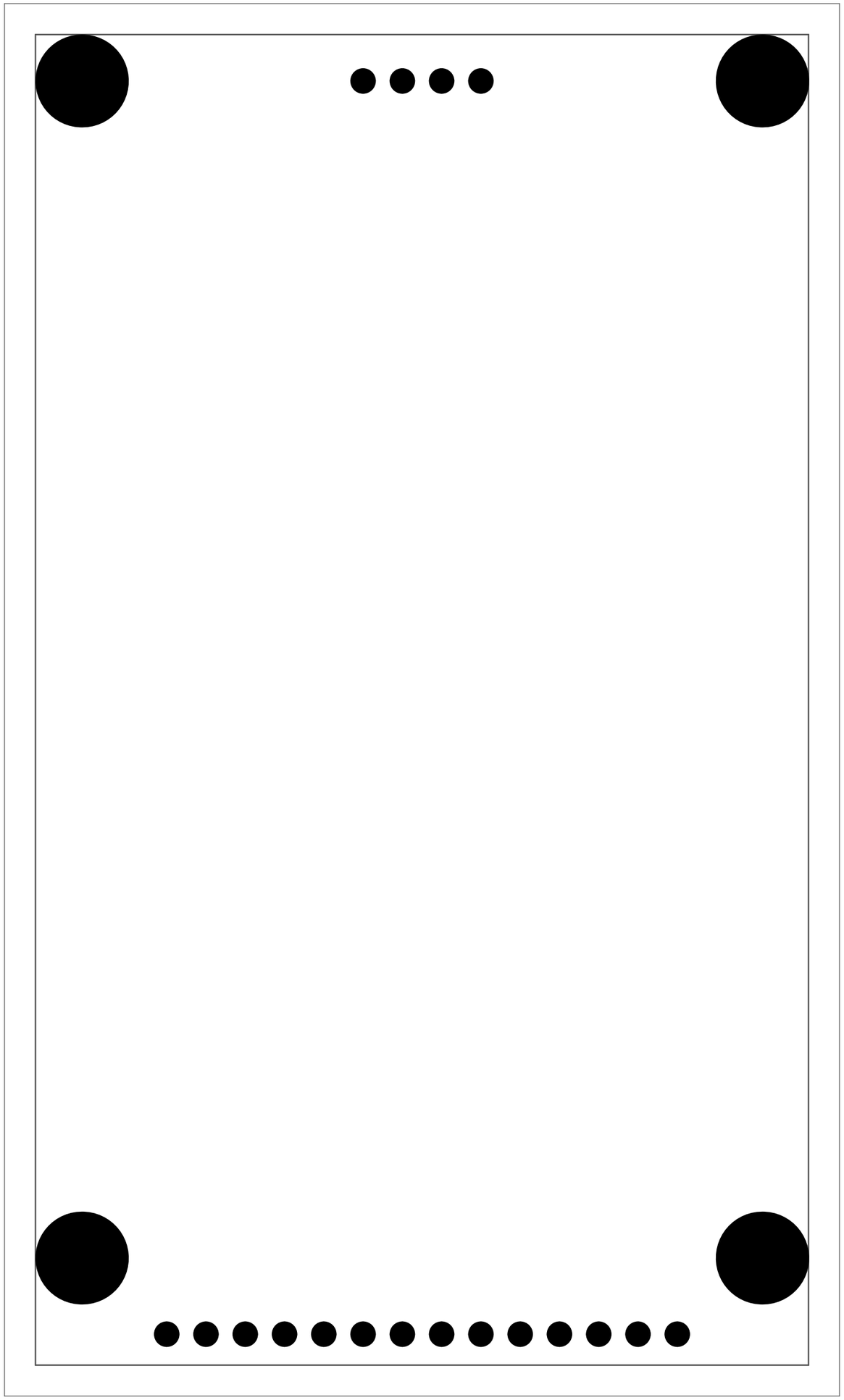
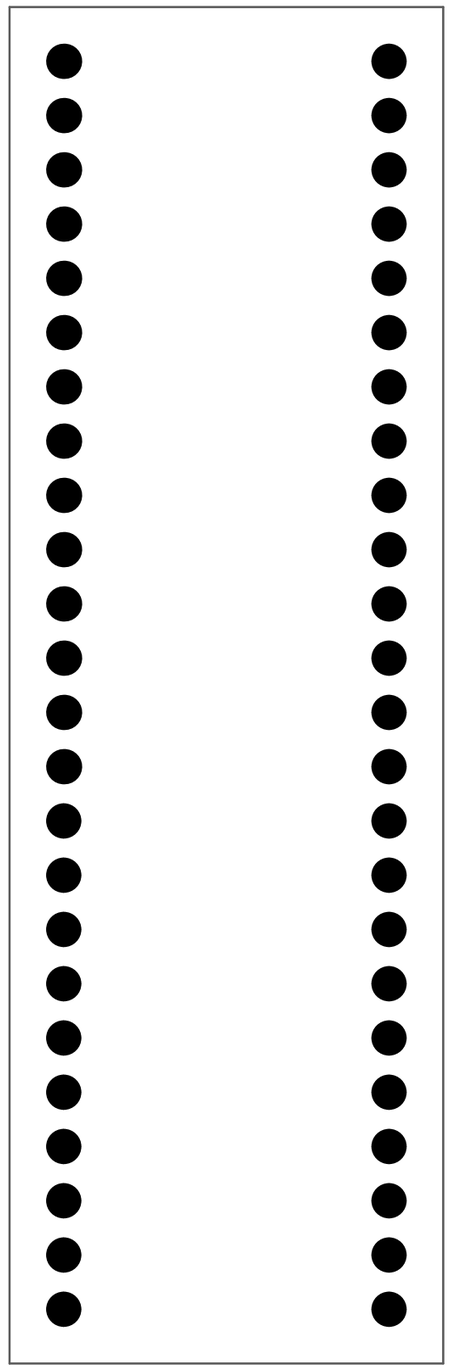
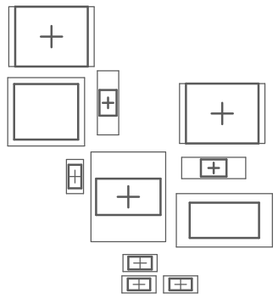
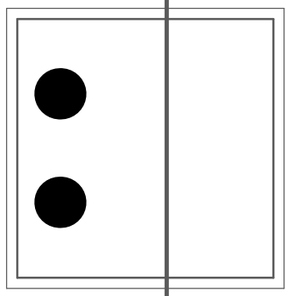
U7

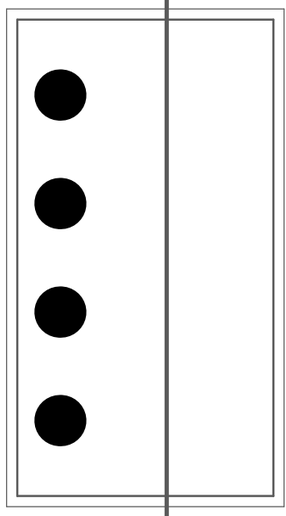
U6

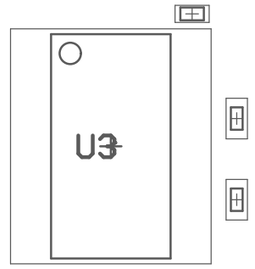
U3
C5
R4
R5

P1
GND
CK+
CK−
D−
D+

R1




U3