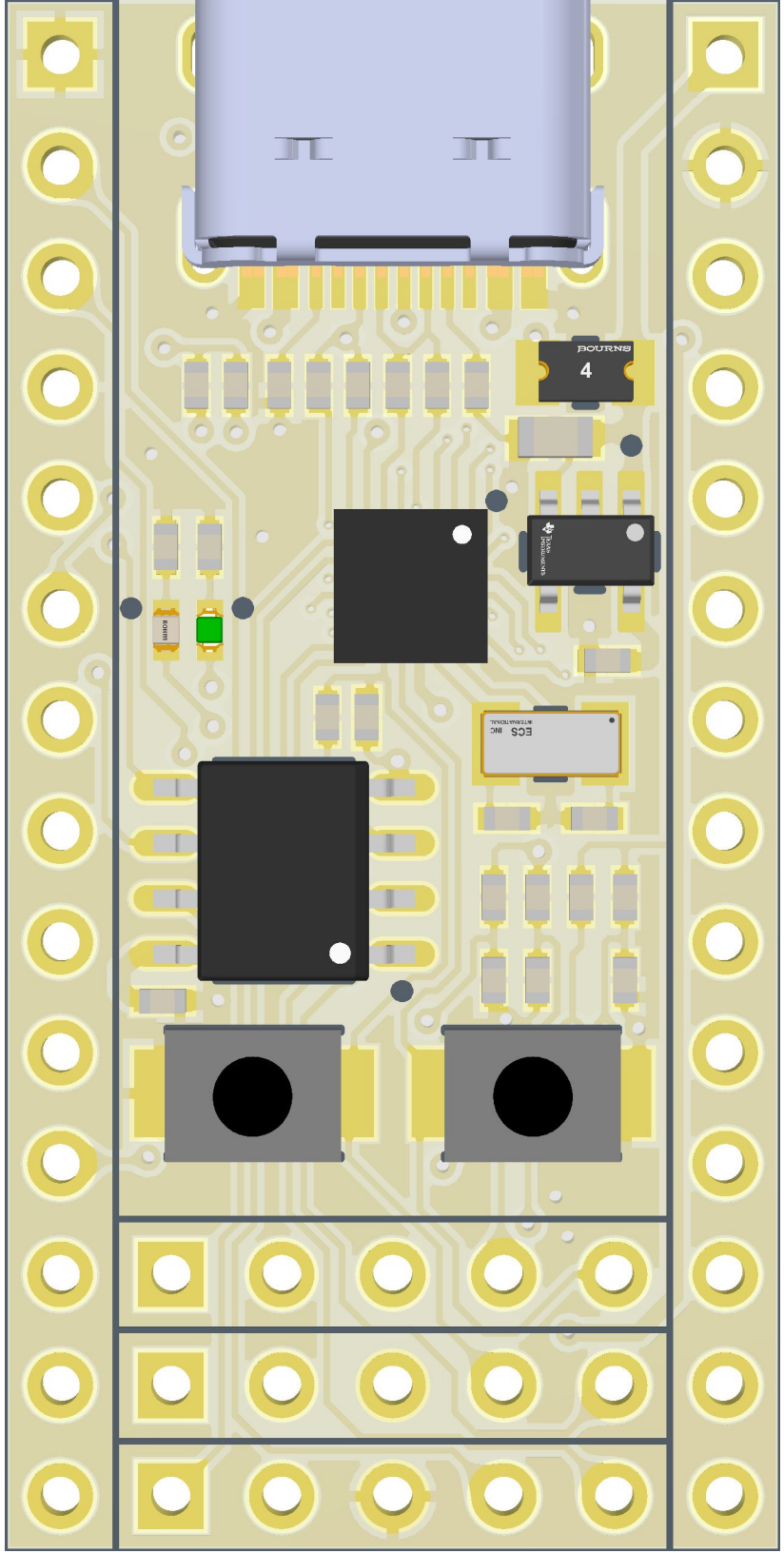

BOURNS
4

QL-EOS-S3 breakout

Variant: [No Variations]

10/9/2020

RevB1

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

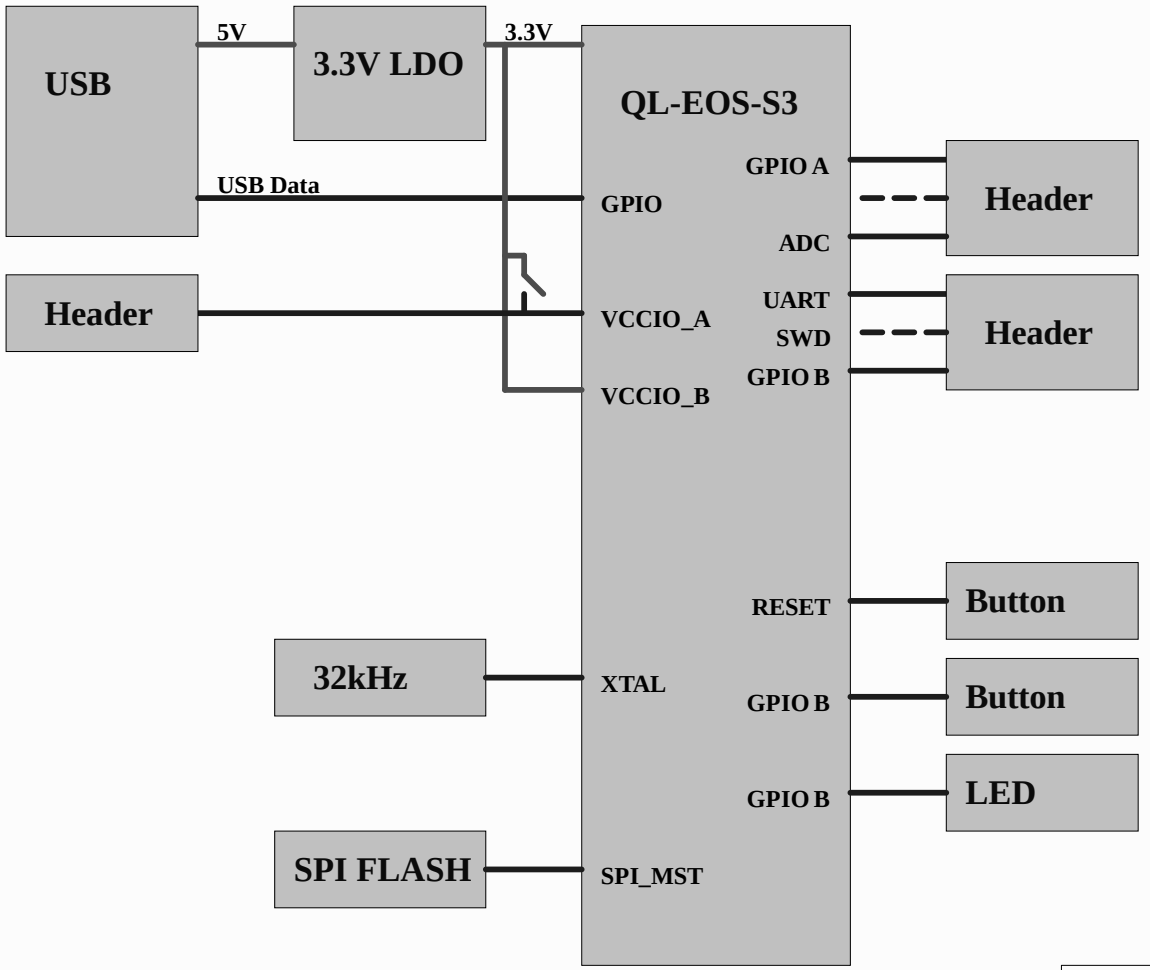
DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title: *		
Project: QL-EOS-S3-breakout.PrjPcb	Revision: RevB1	
Date: 10/9/2020 Time: 12:28:03 AM	Sheet 1 of 4	BLIN KIN LABS

QL-EOS-S3 breakout

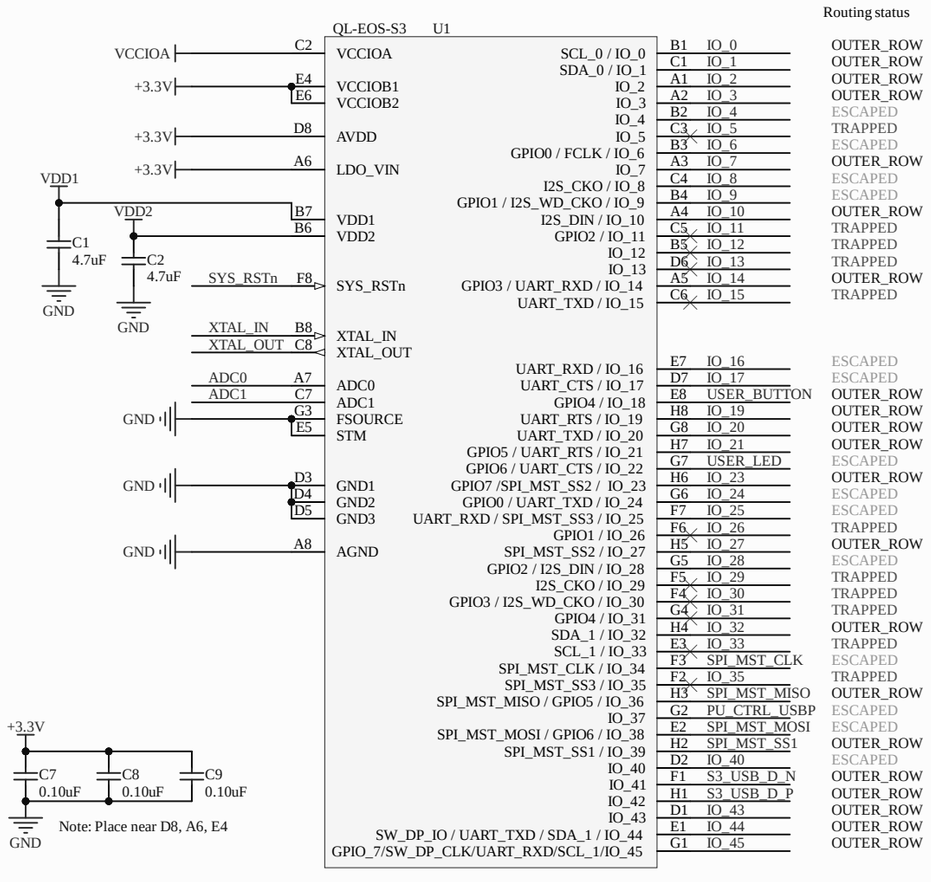


Title: Block Diagram		
Project: QL-EOS-S3-breakout.PrjPcb	Revision: RevB1	
Date: 10/9/2020 Time: 12:28:03 AM	Sheet 2 of 4	

BLIN KIN LABS

QL-EOS-S3 breakout

MCU/FPGA

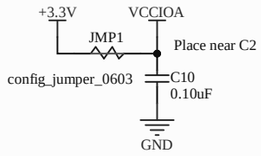


Design intent:
-Low-cost, minimum viable ARM+FPGA design that is breadboard compatable
-Footprint, power, UART pin compatibility with Teensy 3.2.
-All pins on Bank A placed in a group, so that they can have their IO voltage set with an external reference
-Bootstrap, SPI flash, and reset pins placed in non-breadboardable location to avoid inadvertant interference with application circuit
-Pins with multiple IO functions preferred over FPGA only pins
-Pins in ascending order by FPGA IO number when possible

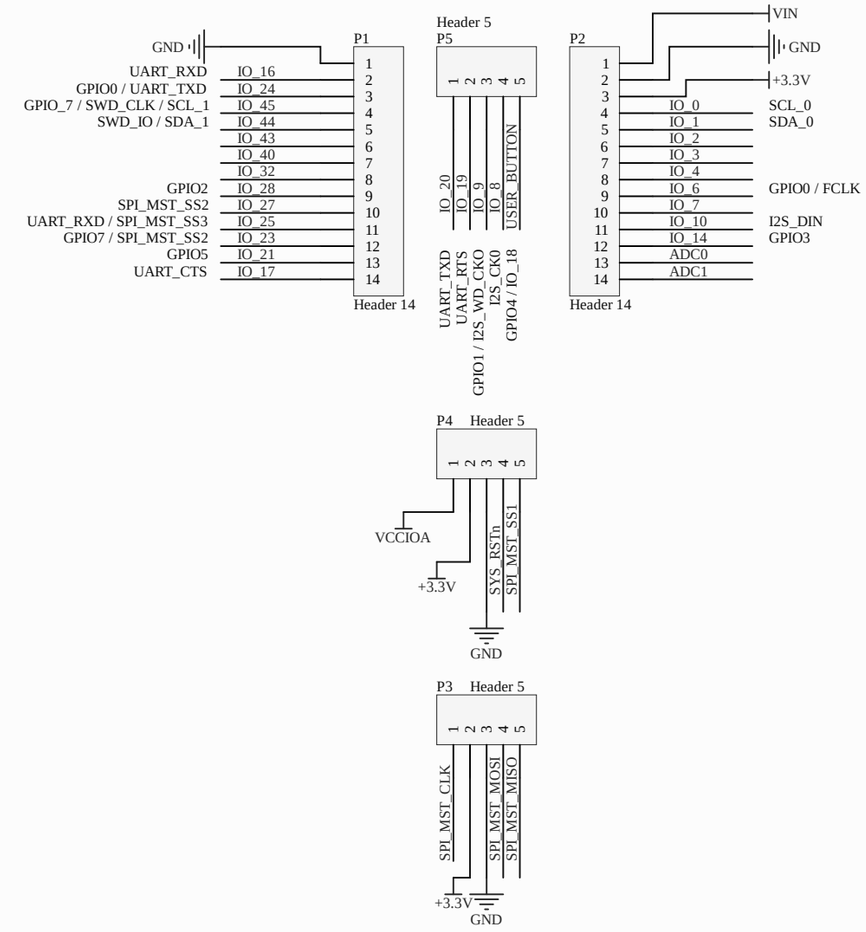
Useful connections:
-Bridge VCCIOA to 3.3V if the jumper was cut
-Bridge SYS_RSTn to GND to put processor in reset for external SPI Flash programming
-Bridge IO_19 to 3.3V to enable JTAG SWD on boot

I/O Bank A reference voltage

Cut jumper JMP1 and provide 1.2-3.3V (?) reference voltage on VCCIOA pin

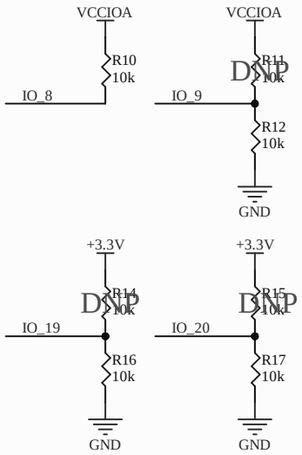


I/O Pins



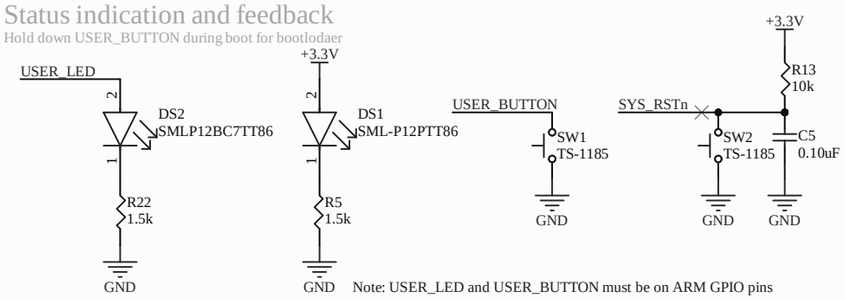
Bootstrap Configuration

IO_8: SWD pin assignment: pull down for 14/15 (default), up for 44/45
IO_8/IO_9: High speed oscillator selection; both pulled up for external oscillator, otherwise internal oscillator
IO_19: Enable SWD: pull down to disable, up to enable
IO_20: Boot mode: pull down for host (boot from SPI flash), pull up for companion (boot from external processor)



Status indication and feedback

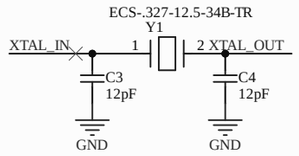
Hold down USER_BUTTON during boot for bootlodaer



Note: USER_LED and USER_BUTTON must be on ARM GPIO pins

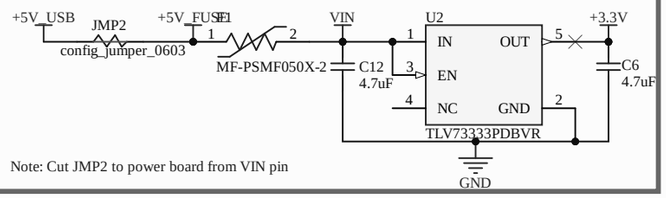
32.768k oscillator

Used for RTC and as a reference for the main clock



3.3V regulator

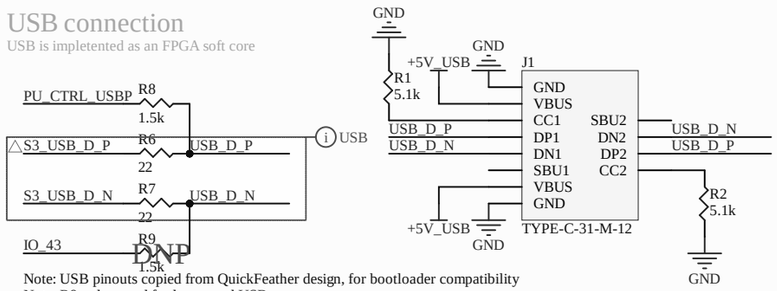
300mA max



Note: Cut JMP2 to power board from VIN pin

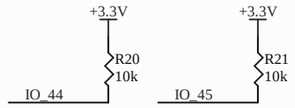
USB connection

USB is impletented as an FPGA soft core



Note: USB pinouts copied from QuickFeather design, for bootloader compatibility
Note: R9 only neeed for low-speed USB

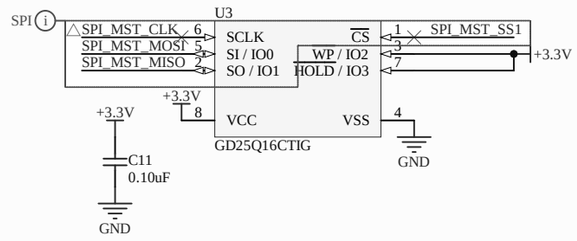
JTAG pull-ups



Note: Possible to omit these if JTAG isn't needed.

SPI Flash

Program memory loaded from SPI flash at boot

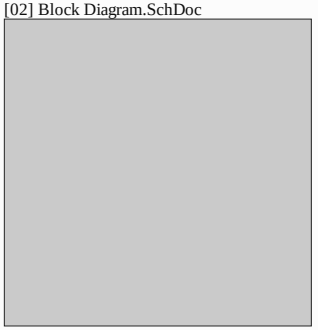


BLIN KIN LABS

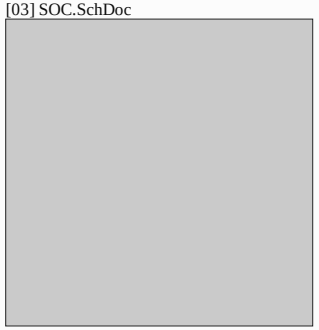
Title: SOC		
Project: QL-EOS-S3-breakout.PrjPcb		Revision: RevB1
Date: 10/9/2020	Time: 12:28:04 AM	Sheet 3 of 4

Designator
[01] cover page.SchDoc

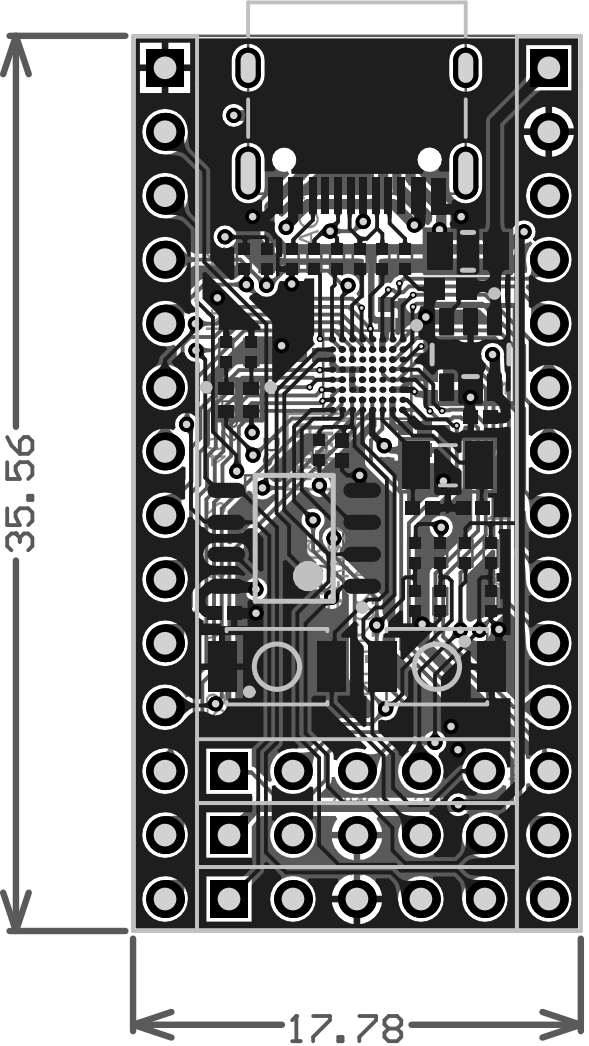
Designator
[02] Block Diagram.SchDoc



Designator
[03] SOC.SchDoc



Title: *			
Project: QL-EOS-S3-breakout.PrjPcb		Revision: RevB1	
Date: 10/9/2020	Time: 12:28:04 AM	Sheet 4 of 4	BLIN KIN LABS



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	SM-001	0.013mm	4
1	Top Layer	Copper	0.035mm	
	Dielectric 2	PP-022	0.200mm	4.6
2	Layer 1	Copper	0.018mm	
	Dielectric 3	Core-039	0.665mm	4.8
3	Layer 2	Copper	0.018mm	
	Dielectric 4	PP-022	0.200mm	4.6
4	Bottom Layer	Copper	0.035mm	
	Bottom Solder	SM-001	0.013mm	4
	Bottom Overlay			

Total board thickness: 1.195mm

Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Blinkinlabs-Repos\QL-EOS-S3-breakout\pcb\QL-EOS-S3-bre

Warnings 0
Rule Violations 60

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.148mm) (InComponent('U1') and ispad),(All)	0
Clearance Constraint (Gap=0.127mm) (istrack or ((ObjectKind = 'Via') And (AsMils(ViaDiameter)	0
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.152mm) (InComponent('JMP1') or	0
Short-Circuit Constraint (Allowed=Yes) (InComponent('JMP1') or	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=0.406mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.148mm) (All),(All)	9
Minimum Solder Mask Sliver (Gap=0mm) (HasFootprint('CAPC1005X06L') or	0
Minimum Solder Mask Sliver (Gap=0.05mm) (InComponent('U1') and IsPad) OR (InComponent('U1')	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	44
Silk to Silk (Clearance=0.254mm) (All),(All)	6
Net Antennae (Tolerance=0mm) (All)	1
Board Clearance Constraint (Gap=0mm) (IsPolygon)	0
Room [03] SOC (Bounding Region = (144.78mm, 45.72mm, 172.72mm, 86.36mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	60

Minimum Solder Mask Sliver (Gap=0.148mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A1/B12(12.115mm,29.19mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A12/B1(5.665mm,29.198mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A5(10.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A5(10.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A6(9.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A6(9.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A7(8.64mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A8(7.64mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.148mm) Between Pad J1-A8(7.64mm,29.198mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (13.165mm,11.5mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (2.9mm,21.6mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (4.615mm,9.5mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.211mm < 0.254mm) Between Arc (5.461mm,21.603mm) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-12(1.27mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-13(1.27mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-14(1.27mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad P2-12(16.51mm,6.35mm) on Multi-Layer
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Pad P2-13(16.51mm,3.81mm) on Multi-Layer
Silk To Solder Mask Clearance Constraint: (0.211mm < 0.254mm) Between Pad P2-14(16.51mm,1.27mm) on Multi-Layer
Silk To Solder Mask Clearance Constraint: (0.199mm < 0.254mm) Between Pad P3-1(3.81mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad P3-1(3.81mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-2(6.35mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-3(8.89mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad P3-4(11.43mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.235mm < 0.254mm) Between Pad P3-5(13.97mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad P3-5(13.97mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.199mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.219mm < 0.254mm) Between Pad P4-2(6.35mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P4-2(6.35mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad P4-3(8.89mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P4-3(8.89mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad P4-4(11.43mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad P4-4(11.43mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.204mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.203mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad P5-2(6.35mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.219mm < 0.254mm) Between Pad P5-2(6.35mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad P5-3(8.89mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad P5-3(8.89mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad P5-4(11.43mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.244mm < 0.254mm) Between Pad P5-4(11.43mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer And

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.202mm < 0.254mm) Between Text '".Project

ARM+FPGA

'.VersionRevision' 2020-10" (9.661mm,18.73mm) on Bottom Overlay And Track (6.12mm,17.55mm)(9.1

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.202mm < 0.254mm) Between Text '".Project

ARM+FPGA

'.VersionRevision' 2020-10" (9.661mm,18.73mm) on Bottom Overlay And Track (9.12mm,17.55mm)(9.1

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.178mm < 0.254mm) Between Text "BLIN

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,17.55mm)(6.12mm,20.55mm) on B(

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "BLIN

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,17.55mm)(9.12mm,17.55mm) on B(

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.108mm < 0.254mm) Between Text "BLIN

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,20.55mm)(9.12mm,20.55mm) on B(

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.192mm < 0.254mm) Between Text "BLIN

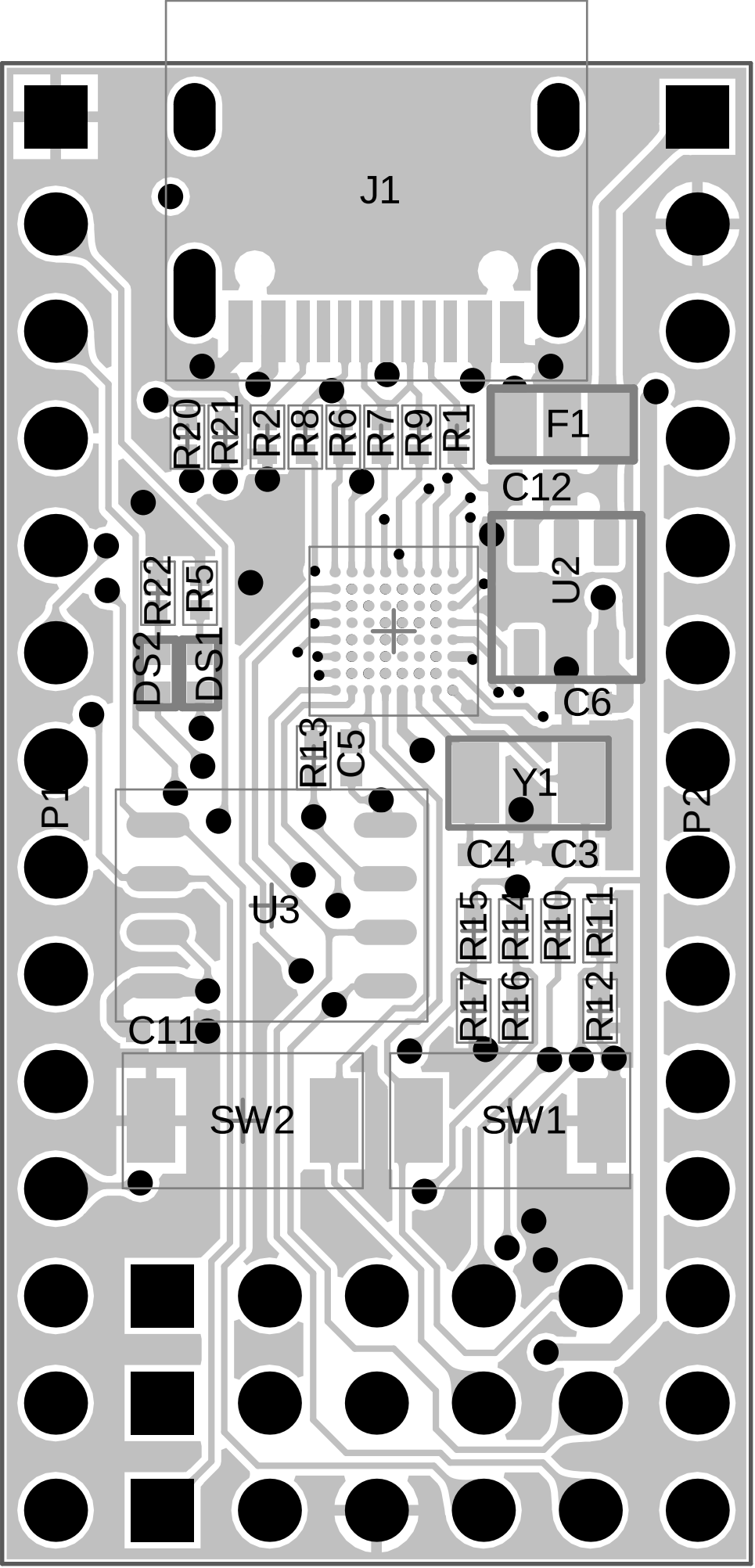
KIN

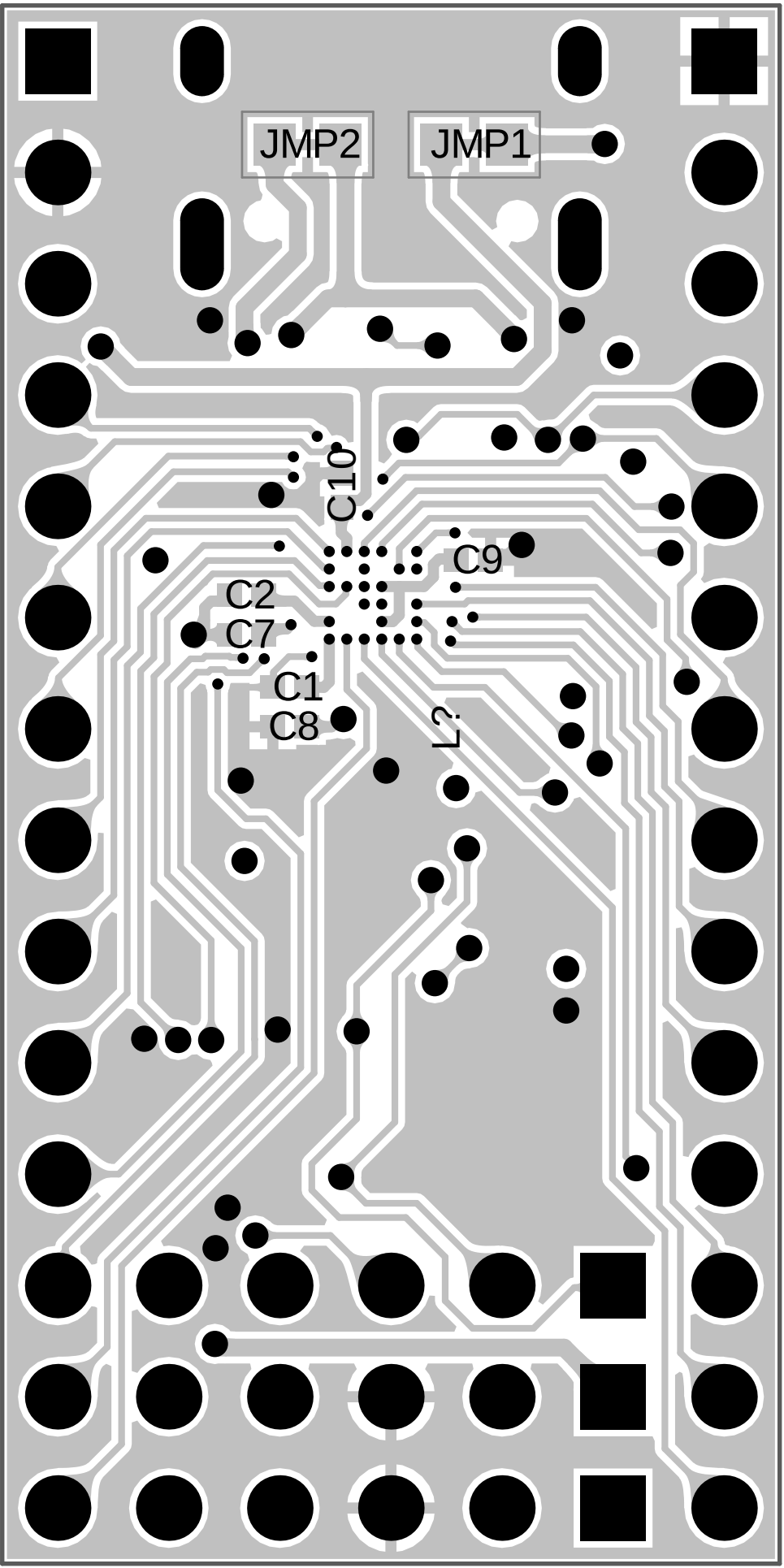
LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (9.12mm,17.55mm)(9.12mm,20.55mm) on B(

Net Antennae (Tolerance=0mm) (All)
Net Antennae: Track (6.235mm,32.385mm)(7.735mm,32.385mm) on Bottom Layer

Electrical Rules Check Report

Class	Document	Message
Warning	[03] SOC.SchDoc	Un-Designated Part L?


J1
R20
R21
R2
R8
R6
R7
R9
R1
F1
C12
U2
R22
R5
DS2
DS1
C6
R13
C5
Y1
P1
P2
C4
C3
U3
R15
R14
R10
R11
R17
R16
R12
C11
SW2
SW1


JMP2
JMP1
C10
C9
C2
C7
C1
C8
L2