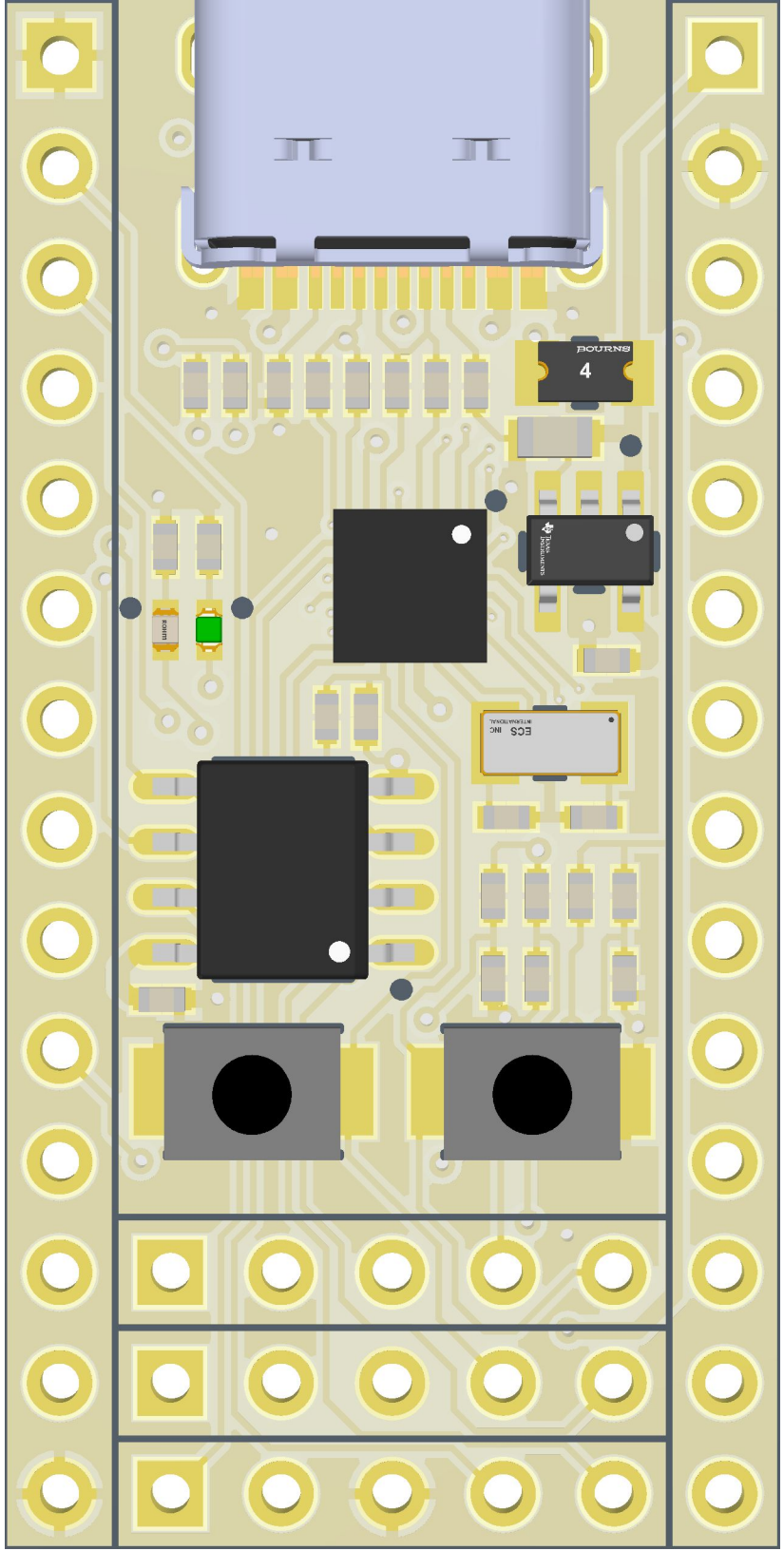

BOURNS
4

QL-EOS-S3 breakout

Variant: [No Variations]

8/13/2020

RevA

Release Candidate

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for critical design notes.

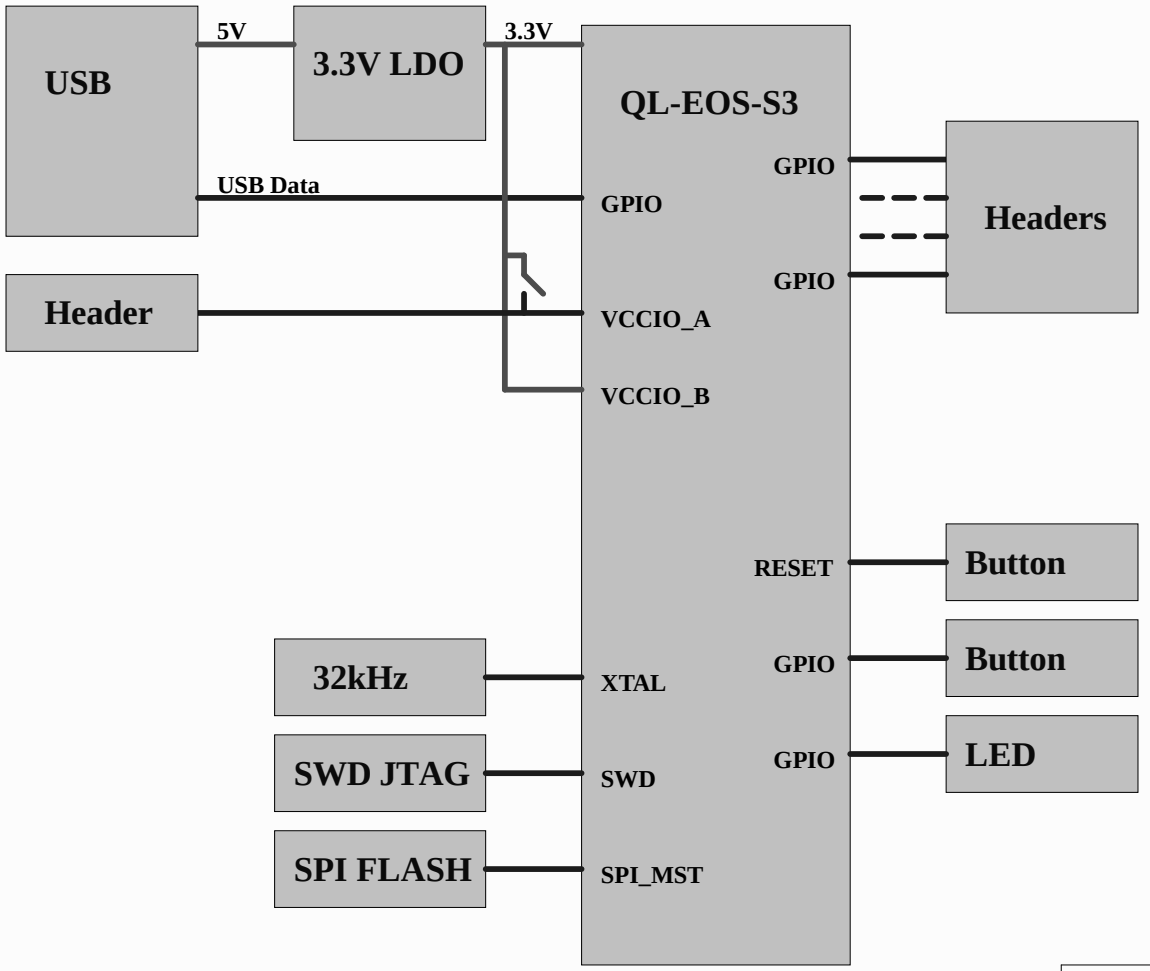
DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Title: *		
Project: QL-EOS-S3-breakout.PrjPcb	Revision: RevA	
Date: 8/13/2020 Time: 11:58:12 AM	Sheet 1 of 4	

BLIN KIN LABS

QL-EOS-S3 breakout

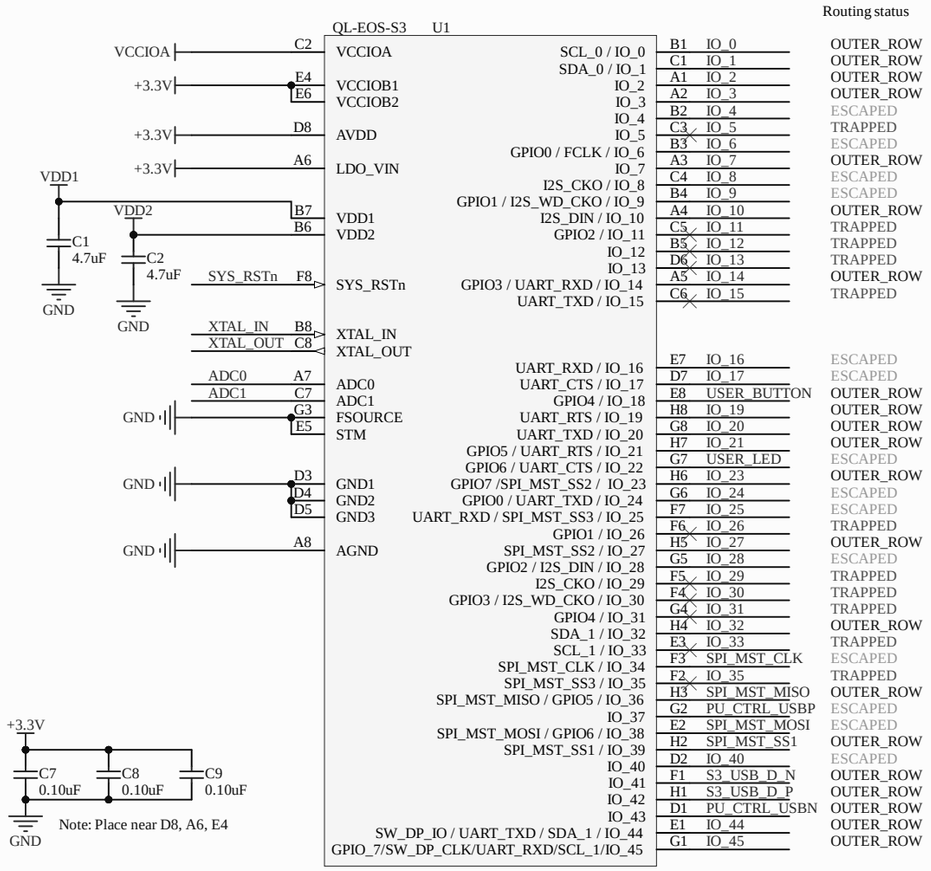


Title: Block Diagram		
Project: QL-EOS-S3-breakout.PrjPcb		Revision: RevA
Date: 8/13/2020	Time: 11:58:12 AM	Sheet 2 of 4

BLIN KIN LABS

QL-EOS-S3 breakout

MCU/FPGA

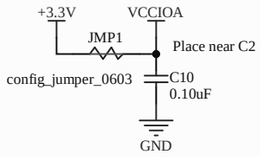


Design intent:
-Low-cost, minimum viable ARM+FPGA design that is breadboard compatable
-Footprint, power, UART pin compatibility with Teensy 3.2.
-All pins on Bank A placed in a group, because they can have their IO voltage set with a reference
-Bootstrap, SPI flash, and reset pins placed in non-breadboardable location to avoid inadvertant interference with application circuit
-Pins with multiple IO functions preferred over FPGA only pins
-Pins in ascending order by FPGA IO number when possible

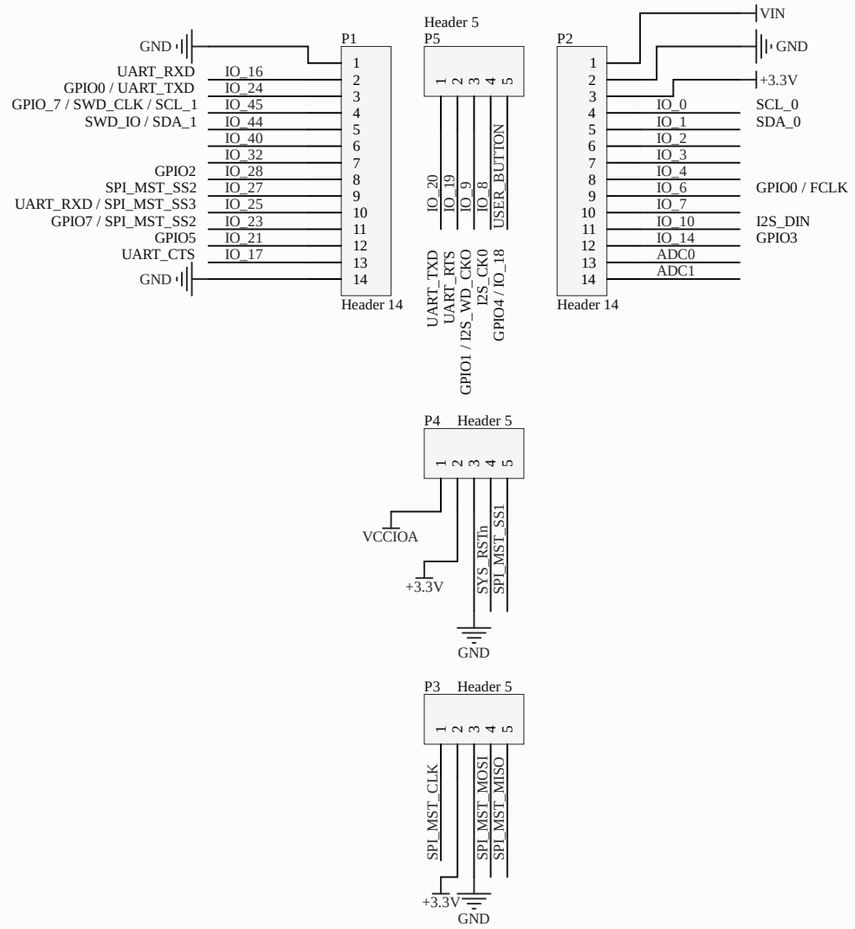
Useful connections:
-Jumper VCCIOA to 3.3V if the connection was cut
-Jumper SYS_RSTn to GND to put processor in reset for external SPI Flash programming
-Jumper IO_19 to 3.3V to enable JTAG SWD on boot

I/O Bank A reference voltage

Cut jumper JMP1 and provide 1.2-3.3V (?) reference voltage on VCCIOA pin

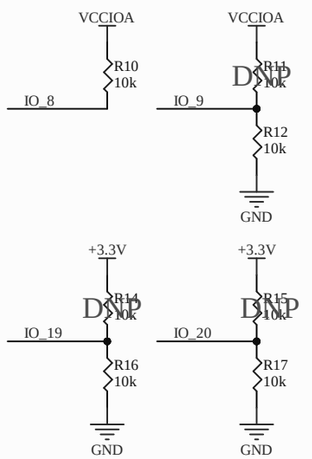


I/O Pins



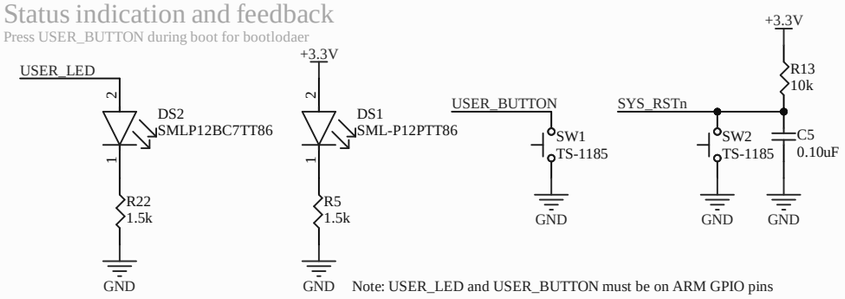
Bootstrap Configuration

IO_8: SWD pin assignment: pull down for 14/15 (default), up for 44/45
IO_8/IO_9: High speed oscillator selection; both pulled up for external oscillator, otherwise internal oscillator
IO_19: Enable SWD: pull down to disable, up to enable
IO_20: Boot mode: pull down for host (boot from SPI flash), pull up for companion (boot from ???)



Status indication and feedback

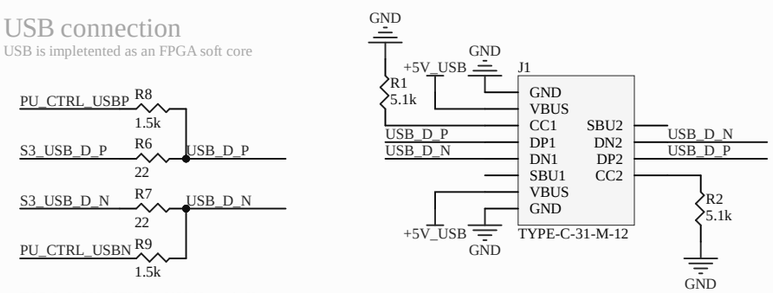
Press USER_BUTTON during boot for bootlodaer



Note: USER_LED and USER_BUTTON must be on ARM GPIO pins

USB connection

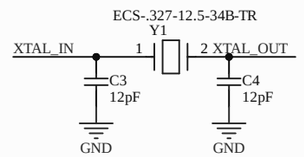
USB is impletented as an FPGA soft core



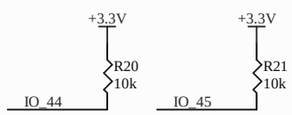
TODO: Is PU_CTRNL_USBN needed?

32.768k oscillator

Used for RTC and as a reference for the main clock

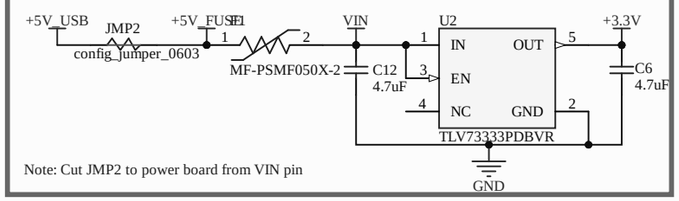


JTAG pull-ups



3.3V regulator

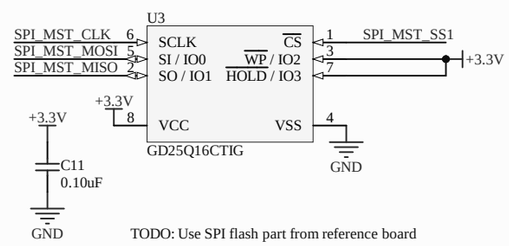
???mA max



Note: Cut JMP2 to power board from VIN pin

SPI Flash

Program memory loaded from SPI flash at boot



TODO: Use SPI flash part from reference board

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Title: SOC		
Project: QL-EOS-S3-breakout.PrjPcb		Revision: RevA
Date: 8/13/2020	Time: 11:58:12 AM	Sheet 3 of 4

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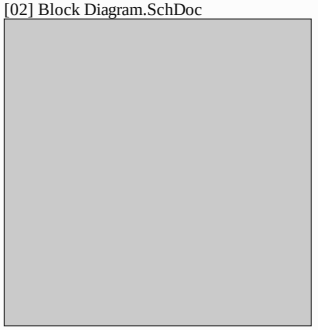
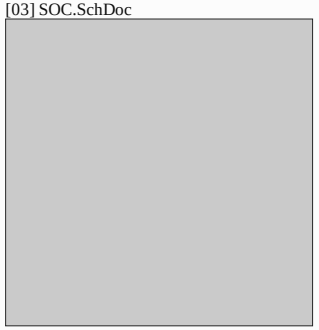
Designator
[01] cover page.SchDoc

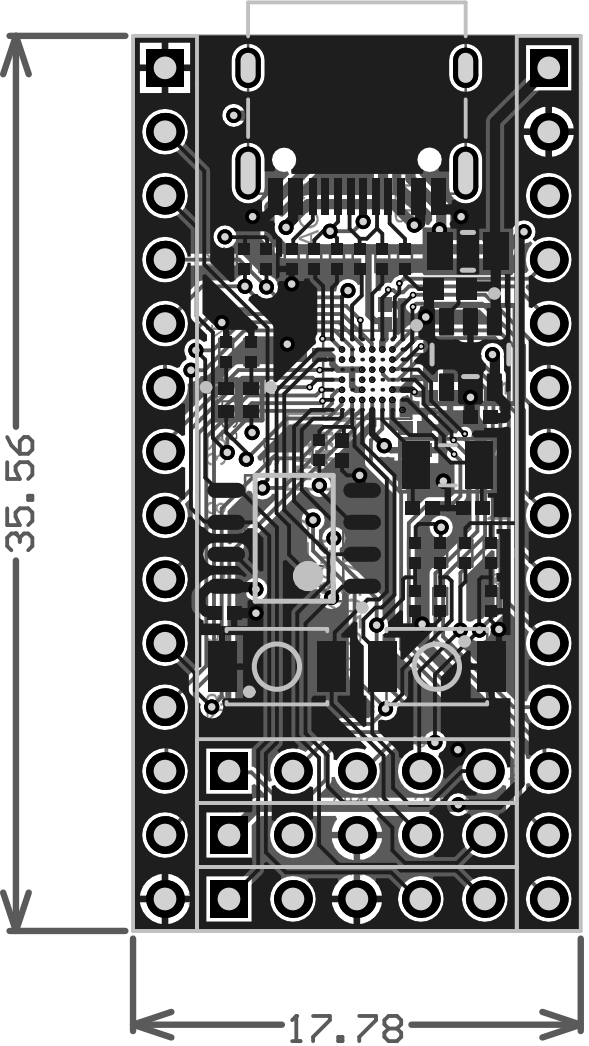
Designator
[02] Block Diagram.SchDoc



Designator
[03] SOC.SchDoc



Title: *		
Project: QL-EOS-S3-breakout.PrjPcb	Revision: RevA	BLIN KIN LABS
Date: 8/13/2020 Time: 11:58:13 AM	Sheet 4 of 4	



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	SM-001	0.013mm	4
1	Top Layer	Copper	0.035mm	
	Dielectric 2	PP-022	0.200mm	4.6
2	Layer 1	Copper	0.018mm	
	Dielectric 3	Core-039	0.665mm	4.8
3	Layer 2	Copper	0.018mm	
	Dielectric 4	PP-022	0.200mm	4.6
4	Bottom Layer	Copper	0.035mm	
	Bottom Solder	SM-001	0.013mm	4
	Bottom Overlay			

Total board thickness: 1.195mm

Design Rules Verification Report

Filename : C:\Users\matt\Blinkinlabs-Repos\QL-EOS-S3-breakout\pcb\QL-EOS-S3-breako

Warnings 0
Rule Violations 331

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.127mm) (istrack or ((ObjectKind = 'Via') And (AsMils(ViaDiameter)	0
Clearance Constraint (Gap=0.152mm) (InComponent('JMP1') or	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (InComponent('JMP1') o	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=0.406mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	281
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	44
Silk to Silk (Clearance=0.254mm) (All),(All)	5
Net Antennae (Tolerance=0mm) (All)	1
Room [03] SOC (Bounding Region = (144.78mm, 45.72mm, 172.72mm, 86.36mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	331

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C10-1(10mm,24.89mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(10.81mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C1-1(10.81mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C1-1(10.81mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C11-1(4.015mm,12.625mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C1-2(11.59mm,20mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C1-2(11.59mm,20mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.229mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.223mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.228mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.223mm < 0.254mm) Between Pad C12-2(11.95mm,25.5mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.223mm < 0.254mm) Between Pad C12-2(11.95mm,25.5mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C2-1(11.81mm,22.1mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C2-1(11.81mm,22.1mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C2-1(11.81mm,22.1mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C2-2(12.59mm,22.1mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C2-2(12.59mm,22.1mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C3-1(13.11mm,16.8mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(11.89mm,16.8mm) on Top Layer And Pac
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Minimum Solder Mask Sliver Constraint: (0.227mm < 0.254mm) Between Pad C5-2(8.3mm,19.49mm) on Top Layer And Pac
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Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C9-1(6.61mm,22.9mm) on Bottom Layer Anc
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A1/B12(12.115mm,29.19mm) on Top Laye
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad J1-A1/B12(12.115mm,29.19mm) on Top Laye
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A12/B1(5.665mm,29.198mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad J1-A12/B1(5.665mm,29.198mm) on Top Layer
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Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-A5(10.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-A5(10.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-A5(10.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-A5(10.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-A6(10.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-A6(10.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-A6(10.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-A6(10.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-A7(10.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-A7(10.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-A7(10.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-A7(10.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-A8(10.7mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-A8(10.7mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B1(10.3mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B1(10.3mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B1(10.3mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B2(10.3mm,23.1mm) on Top Layer And Pac

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B2(10.3mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B2(10.3mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B2(10.3mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B3(10.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B3(10.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B3(10.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B3(10.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B4(10.3mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B4(10.3mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B4(10.3mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B4(10.3mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B5(10.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B5(10.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B5(10.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B5(10.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B6(10.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B6(10.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B6(10.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B6(10.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B7(10.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B7(10.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B7(10.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B7(10.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-B8(10.3mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-B8(10.3mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C1(9.9mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C1(9.9mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C1(9.9mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C2(9.9mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C2(9.9mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C2(9.9mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C2(9.9mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C3(9.9mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C3(9.9mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C3(9.9mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C3(9.9mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C4(9.9mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C4(9.9mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C4(9.9mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C4(9.9mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C5(9.9mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C5(9.9mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C5(9.9mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C5(9.9mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C6(9.9mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C6(9.9mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C6(9.9mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C6(9.9mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C7(9.9mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C7(9.9mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C7(9.9mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C7(9.9mm,21.1mm) on Top Layer And Pac

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-C8(9.9mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-C8(9.9mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D1(9.5mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D1(9.5mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D1(9.5mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D2(9.5mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D2(9.5mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D2(9.5mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D2(9.5mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D3(9.5mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D3(9.5mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D3(9.5mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D3(9.5mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D4(9.5mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D4(9.5mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D4(9.5mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D4(9.5mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D5(9.5mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D5(9.5mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D5(9.5mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D5(9.5mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D6(9.5mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D6(9.5mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D6(9.5mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D6(9.5mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D7(9.5mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D7(9.5mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D7(9.5mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D7(9.5mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-D8(9.5mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-D8(9.5mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E1(9.1mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E1(9.1mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E1(9.1mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E2(9.1mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E2(9.1mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E2(9.1mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E2(9.1mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E3(9.1mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E3(9.1mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E3(9.1mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E3(9.1mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E4(9.1mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E4(9.1mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E4(9.1mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E4(9.1mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E5(9.1mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E5(9.1mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E5(9.1mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E5(9.1mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E6(9.1mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E6(9.1mm,21.5mm) on Top Layer And Pac

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E6(9.1mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E6(9.1mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E7(9.1mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E7(9.1mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E7(9.1mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E7(9.1mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-E8(9.1mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-E8(9.1mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F1(8.7mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F1(8.7mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F1(8.7mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F2(8.7mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F2(8.7mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F2(8.7mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F2(8.7mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F3(8.7mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F3(8.7mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F3(8.7mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F3(8.7mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F4(8.7mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F4(8.7mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F4(8.7mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F4(8.7mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F5(8.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F5(8.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F5(8.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F5(8.7mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F6(8.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F6(8.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F6(8.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F6(8.7mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F7(8.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F7(8.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F7(8.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F7(8.7mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-F8(8.7mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-F8(8.7mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G1(8.3mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G1(8.3mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G1(8.3mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G2(8.3mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G2(8.3mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G2(8.3mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G2(8.3mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G3(8.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G3(8.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G3(8.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G3(8.3mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G4(8.3mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G4(8.3mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G4(8.3mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G4(8.3mm,22.3mm) on Top Layer And Pac

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G8(8.3mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G8(8.3mm,20.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H1(7.9mm,23.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H2(7.9mm,23.1mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H3(7.9mm,22.7mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H4(7.9mm,22.3mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H5(7.9mm,21.9mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H6(7.9mm,21.5mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H7(7.9mm,21.1mm) on Top Layer And Pac

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (13.165mm,11.5mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (2.9mm,21.6mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (4.615mm,9.5mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (0.211mm < 0.254mm) Between Arc (5.461mm,21.603mm) on Top Overlay An
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer An
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-12(1.27mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-13(1.27mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad P1-14(1.27mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.219mm < 0.254mm) Between Pad P2-12(16.51mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.215mm < 0.254mm) Between Pad P2-13(16.51mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.211mm < 0.254mm) Between Pad P2-14(16.51mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad P3-1(3.81mm,1.27mm) on Multi-Layer And Tex
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P3-1(3.81mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-2(6.35mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad P3-3(8.89mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad P3-4(11.43mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-5(13.97mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad P3-5(13.97mm,1.27mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer And Tex
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.22mm < 0.254mm) Between Pad P4-2(6.35mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P4-2(6.35mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad P4-3(8.89mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad P4-3(8.89mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad P4-4(11.43mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad P4-4(11.43mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.237mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.205mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer And Tex
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad P5-2(6.35mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.22mm < 0.254mm) Between Pad P5-2(6.35mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad P5-3(8.89mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad P5-3(8.89mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad P5-4(11.43mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad P5-4(11.43mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer An
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer An

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.178mm < 0.254mm) Between Text "BLI

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,17.55mm)(6.12mm,20.55mm) on E

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.247mm < 0.254mm) Between Text "BLI

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,17.55mm)(9.12mm,17.55mm) on E

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.107mm < 0.254mm) Between Text "BLI

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,20.55mm)(9.12mm,20.55mm) on E

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.19mm < 0.254mm) Between Text "BLI

KIN

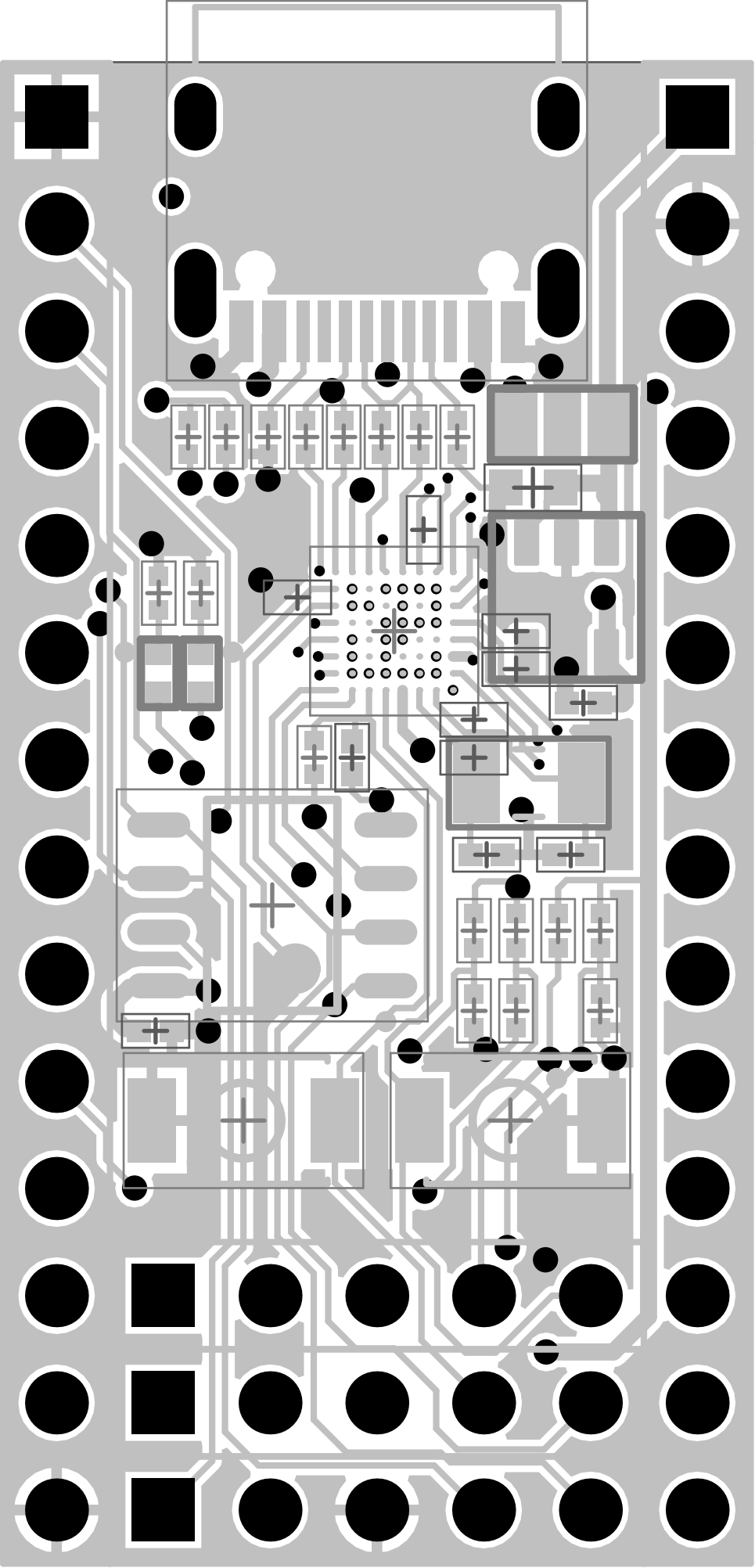
LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (9.12mm,17.55mm)(9.12mm,20.55mm) on E

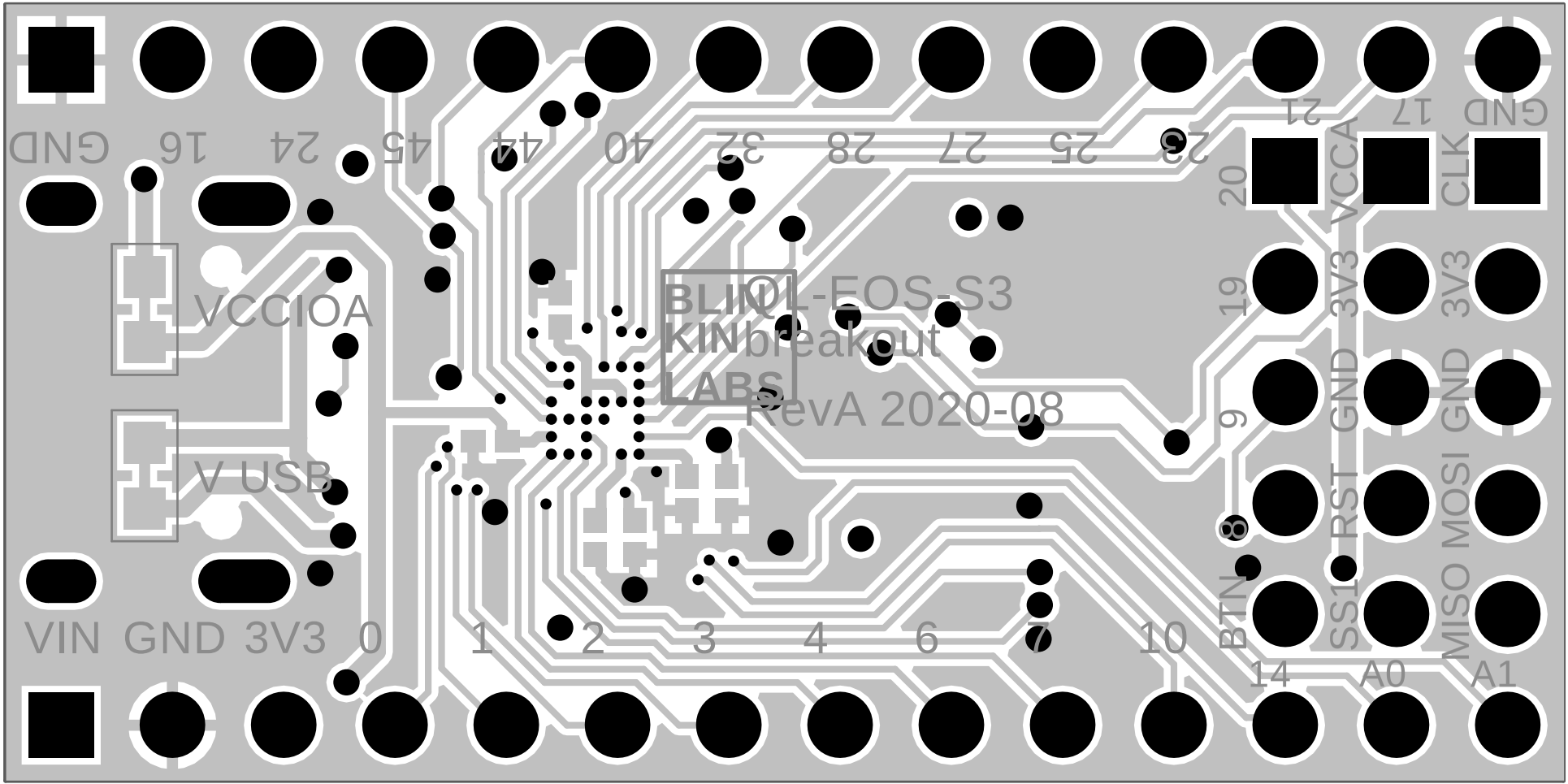
Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.251mm < 0.254mm) Between Text "CLK" (4.658mm,2.155mm) on Bottom Overlay An

Net Antennae (Tolerance=0mm) (All)
Net Antennae: Track (6.235mm,32.385mm)(7.735mm,32.385mm) on Bottom Layer

Electrical Rules Check Report

Class	Document	Message
Error	[03] SOC.SchDoc	+3.3V contains Output Pin and Power Pin objects (Pin U2-5, Pin U1-A6, Pin U1-D8, Pin U1-E4, Pin U1-E6, Pin U3-8).
Warning	[03] SOC.SchDoc	Component DS1 SML-P12PTT86 at 5300mil,4000mil: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component DS1 SML-P12PTT86: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component DS2 SMLP12BC7TT86 at 4100mil,4000mil: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component DS2 SMLP12BC7TT86: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component F1 MF-PSMF050X-2 at 12400mil,3900mil: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component F1 MF-PSMF050X-2: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component U2 TLV73333PDBVR at 13600mil,3900mil: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component U2 TLV73333PDBVR: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component Y1 ECS-.327-12.5-34B-TR at 9800mil,3600mil: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Component Y1 ECS-.327-12.5-34B-TR: Can't perform revision status validation: The server name could not be resolved..
Warning	[03] SOC.SchDoc	Net SPI_MST_CLK has no driving source (Pin P3-1, Pin U1-F3, Pin U3-6)
Warning	[03] SOC.SchDoc	Net SPI_MST_SS1 has no driving source (Pin P4-5, Pin U1-H2, Pin U3-1)
Warning	[03] SOC.SchDoc	Net SYS_RSTn has no driving source (Pin C5-2, Pin P4-4, Pin R13-2, Pin SW2-2, Pin U1-F8)
Warning	[03] SOC.SchDoc	Net XTAL_IN has no driving source (Pin C3-2, Pin U1-B8, Pin Y1-1)
Warning	[03] SOC.SchDoc	Un-Designated Part L?




GND 16 24 45 44 40 32 28 27 25 23 21 17 GND
20 VCCA CLK
19 3V3 3V3
9 GND GND
8 RST MISO
BTN SS1 MOSI
14 A0 A1
VCCIOA
V USB
BLINQ1-EOS-S3
KINbreakout
LABS
RevA 2020-08
VIN GND 3V3 0 1 2 3 4 6 7 10