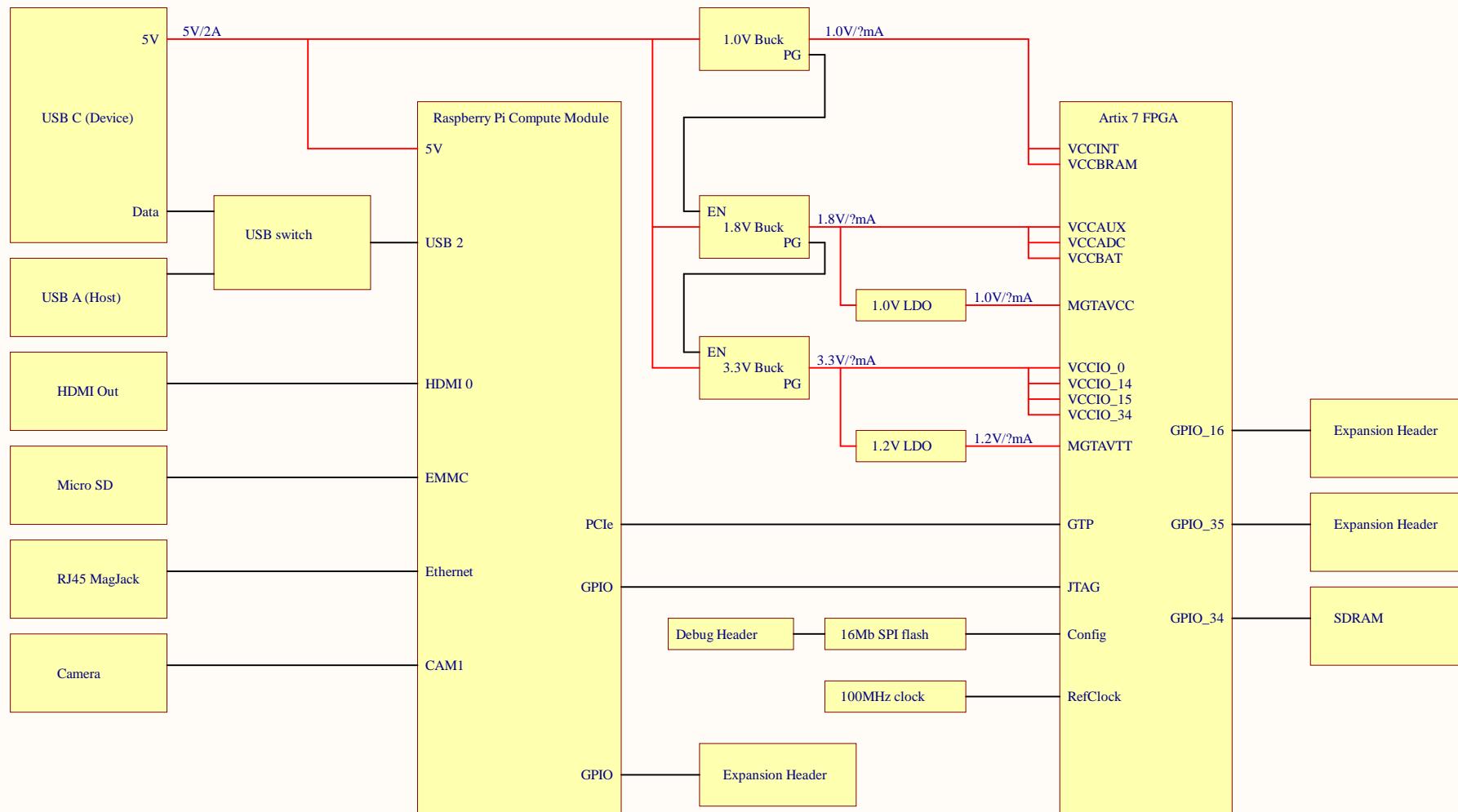


BLINKIN
LABS

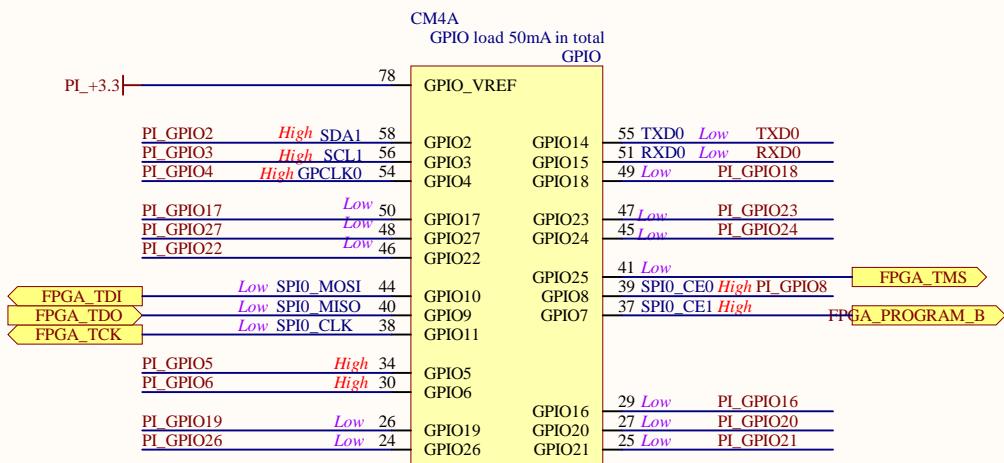
Raspberry Pincushion
RPi 4 Compute Module + Artix 7 FPGA

Raspberry Pincushion

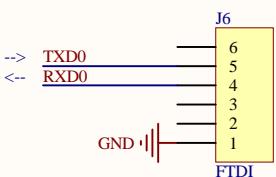


Title: Block diagram		
Project: Raspberry Pincushion	Revision: Rev0	
Date: 1/5/2021	Time: 10:43:18 PM	Sheet 1 of 14

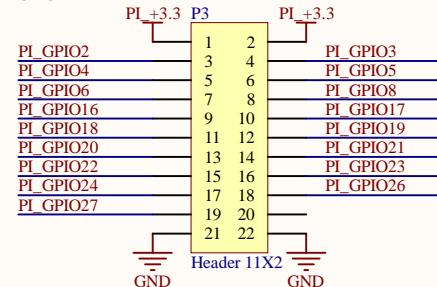
A



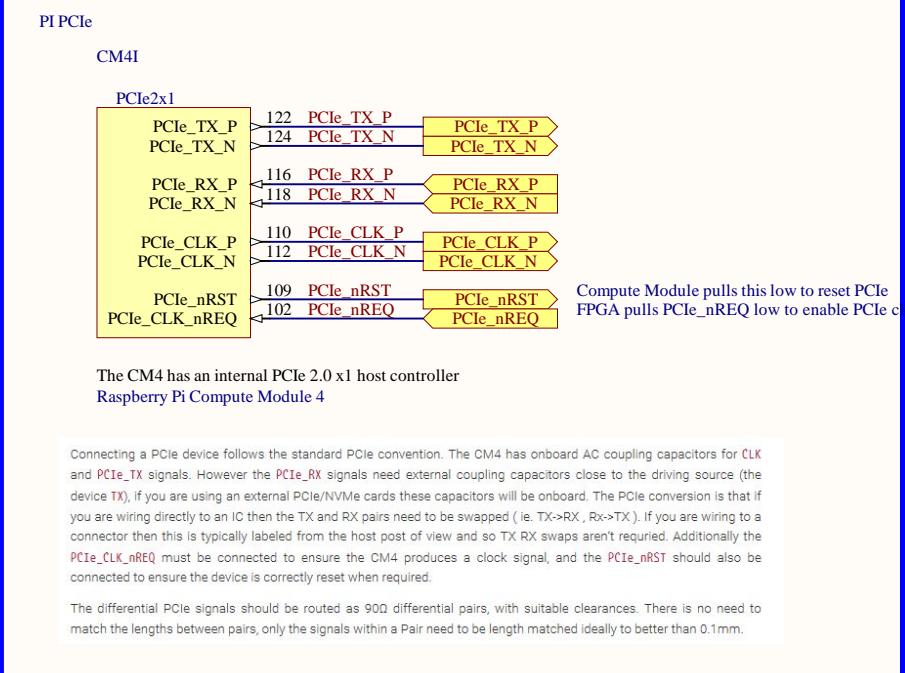
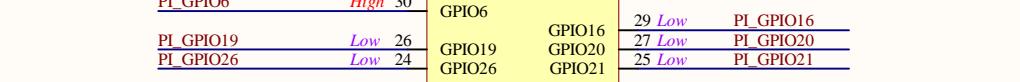
Serial console



Pi GPIO



B



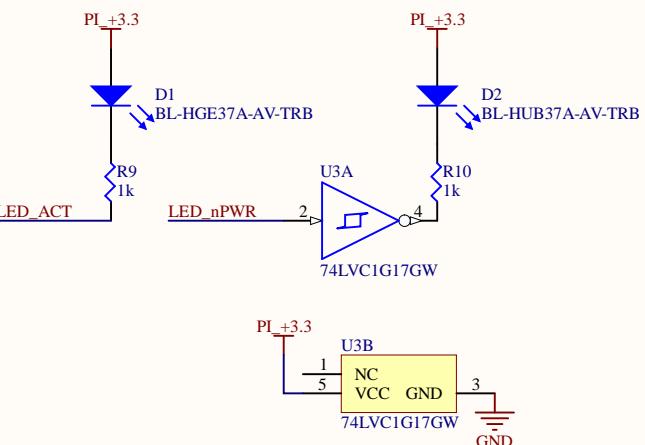
Status LEDs

CM4L
Pi_nLED_Activity
Low Active Pi Activity LED, 20mA Max 5V tolerant
(VOL<0.4V). (this is the signal that drives the Green LED on the Raspberry Pi 4, Model B)

LEDs

Pi_nLED_Activity
PI_LED_nPWR

PI_LED_nPWR
Low active Output to drive Power On LED. This signal needs to be buffered.



Title: Compute Module

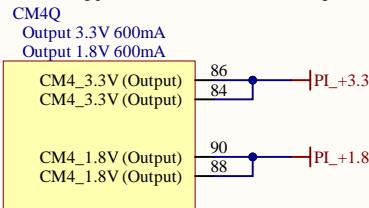
Project: Raspberry Pincushion

Revision: Rev0

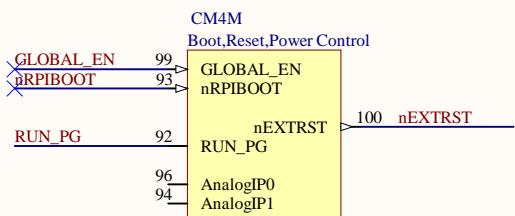
Date: 1/5/2021 Time: 10:43:18 PM Sheet 2 of 14

BLIN
KIN
LABS

3.3V +/-2.5% Power Output max 300mA per pin for a total of 600mA. This will be powered down during power off or GLOBAL_EN being set low



1.8V +/-2.5% Power Output max 300mA per pin for a total of 600mA. This will be powered down during power off or GLOBAL_EN being set low



GLOBAL_EN (Input)

Drive low to power off CM4. Internally pulled up with a 100K to +5V

nRPi_BOOT (Input)

During boot if this pin is low booting from eMMC will be stopped and booting will be transferred to rpi boot which is via

nEXTRST (Output)

Driven low during reset

Driven high (CM4_3.3V) once CM4 CPU has started to boot

RUN_PG

Bidirectional pin. Internally pulled up to +3.3V via 10K

>Input

Can be driven low (via a 220R resistor) to Reset the CM4 CPU.

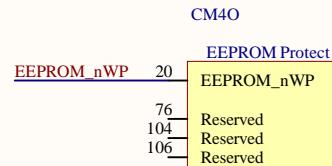
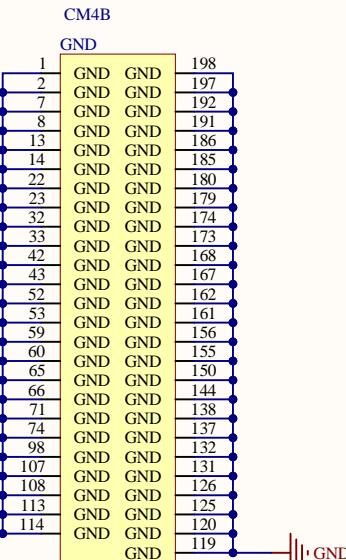
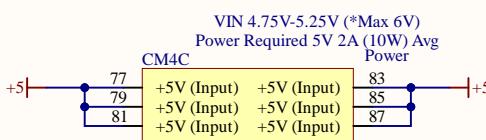
Output >

Output a high signals Power Good and CPU running.

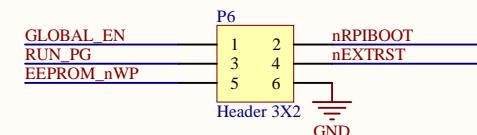
Raspberry Pi Compute Module 4

Analog IP0,IP1

Analog input of the MAX7704. Typically connected to CC pin of Type C power connector



Leaving floating NB internally pulled up to CM4_3.3V via 100K (VIL < 0.8V) but can be grounded to prevent writing to the on board EEPROM which stores the bootcode



Title: Compute Module power

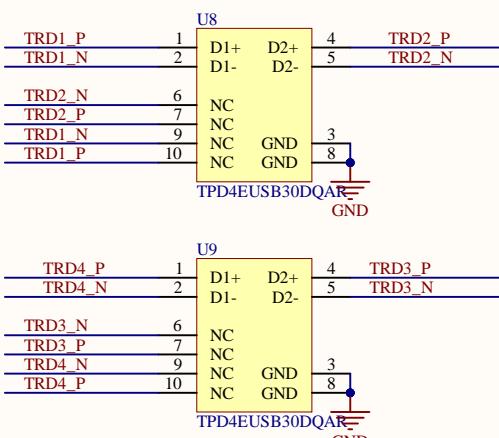
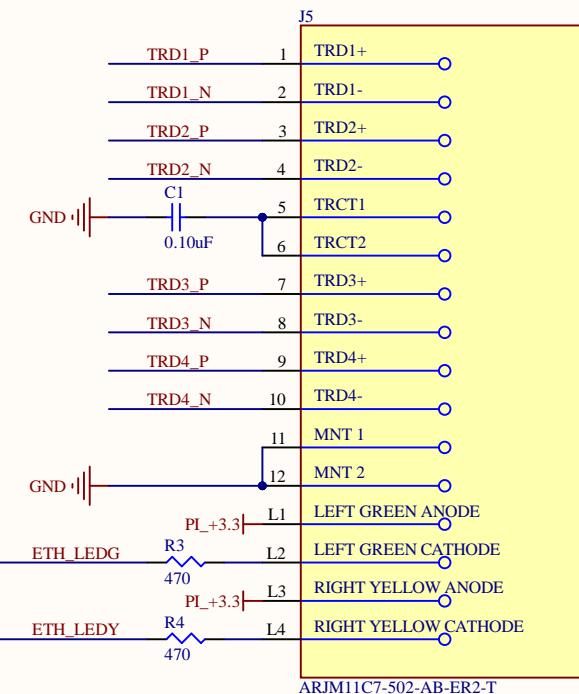
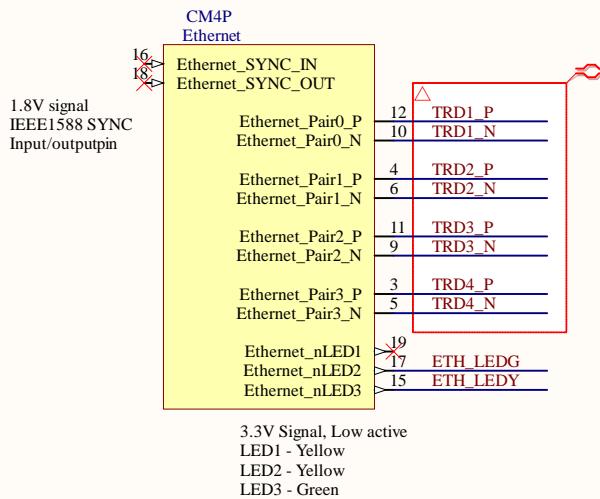
Project: Raspberry Pincushion

Revision: Rev0

Date: 1/5/2021 Time: 10:43:18 PM Sheet 3 of 14

BLIN
KIN
LABS

A



2.2. Ethernet

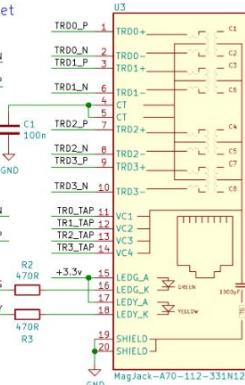
The CM4 has an onboard Gigabit Ethernet PHY — the Broadcom BCM54210PE — some of the major features of this PHY include;

- IEEE 1588-2008 compliant
- Detection and correction of swapped pairs
- MDI crossover, pair skew and pair polarity correction

A standard 1:1 RJ45 MagJack is all that is necessary to provide an Ethernet connection to the CM4. Typical wiring of a MagJack supporting POE, and with added ESD protection, can be seen in Figure 2.

Figure 2.

Ethernet schematic interface for the Raspberry Pi Compute Module 4 supporting POE and with added ESD protection



The differential Ethernet signals should be routed as 100Ω differential pairs, with suitable clearances. Length matching between pairs should be better than 50mm, so in the typical case no length matching is required. However the signals within a pair need to be length matched, ideally to better than 0.15mm.

The PHY also supports up to 3 LEDs to give user status feedback, these are low active. These LEDs can have a range of functions, and you should consult your OS driver to see which functions are supported by your driver.

The PHY also provides SYNC_IN and SYNC_OUT at 1.8v signalling to support IEEE 1588-2008.

Ethernet checklist:

- *100ohm differential pairs
- *Matching to .15mm length within pairs, pair sets do not need to be length matched

Title: Compute Module Ethernet

Project: Raspberry Pincushion

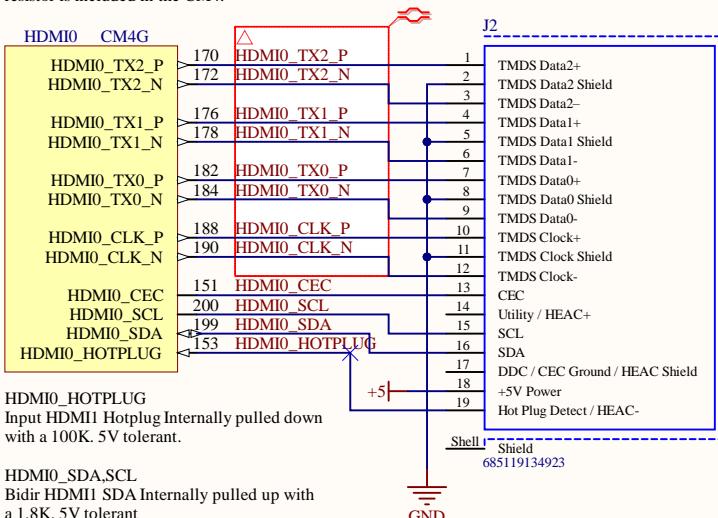
Revision: Rev0

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**BLIN
KIN
LABS**

A

CEC is also supported, an internal 27K pullup resistor is included in the CM4.



2.6. Dual HDMI 2.0

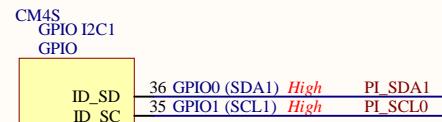
The CM4 supports two HDMI 2.0 interfaces each one capable of driving 4K images. If both HDMI outputs are used then each can be driven upto 4K@30, however if only HDMI0 interface is being used then images up to 4K@60 are possible.

HDMI signals should be routed as 100Ω differential pairs, each signal within a pair should ideally be matched to better than 0.15ppm . Pairs don't typically need any extra matching as they only have to be matched to 25mm .

CEC is also supported, an internal 27K pullup resistor is included in the CM4

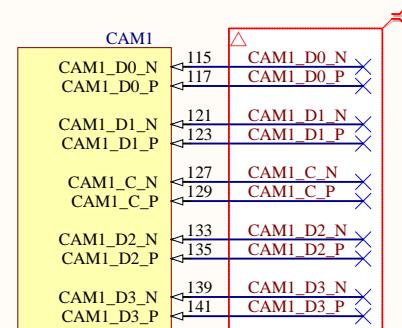
Basic onboard ESD protection is provided for the I₂C EDID signals and the CEC signals, internal pullup and down resistors are also provided. On the (rpi4) the HDMI signals don't have any extra ESD protection , depending on the application extra ESD protection maybe required.

Note: HDMI reference circuit has a 500mV limit on 5v line (RT9742SNGV)



*I2C1 - Use for CAM0,DSI0,GPIO,EEPROM HAT

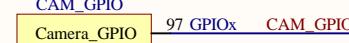
Sinal level refer to
GPIO Vref (3.3V or 1.8V)



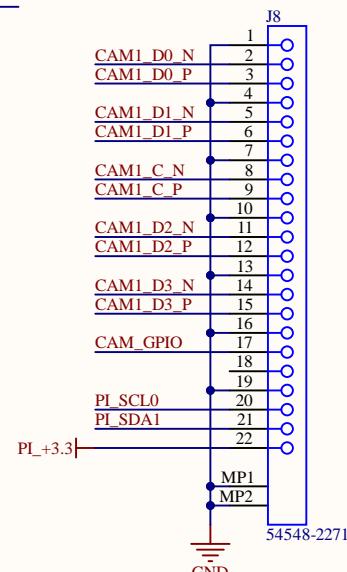
The CM4 supports two camera ports; CAM0 (2 lanes) and CAM1 (4 lanes).

Camera sensors supported by the official Raspberry Pi firmware are; the OmniVision OV5647, Sony IMX219 and Sony IMX477, no security device is required on Compute Module devices to use these camera sensors.

CMAE



CM4_3.3V
signalling, Typically
used to Shutdown the
camera to reduce power

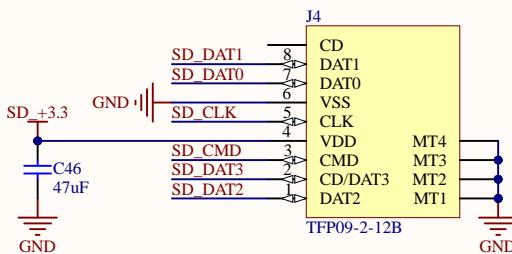
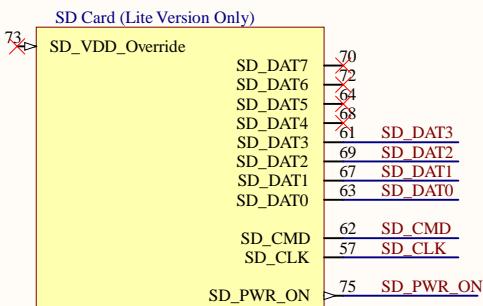


A

A

CM4J

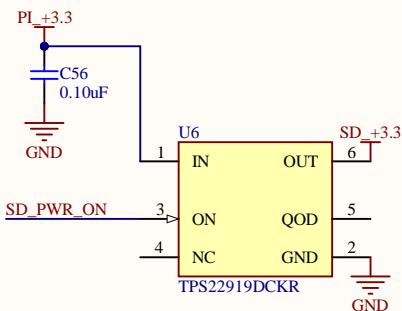
When SD_VDD_override is high, this signal is used to force 1.8v signalling on the SDIO interface. Typically this is used with eMMC memory



The SD_PWR_ON signal is used to enable an external power switch to turn on power to the SDCARD

B

B



C

C

D

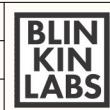
D

Title: Compute Module MicroSD

Project: Raspberry Pincushion

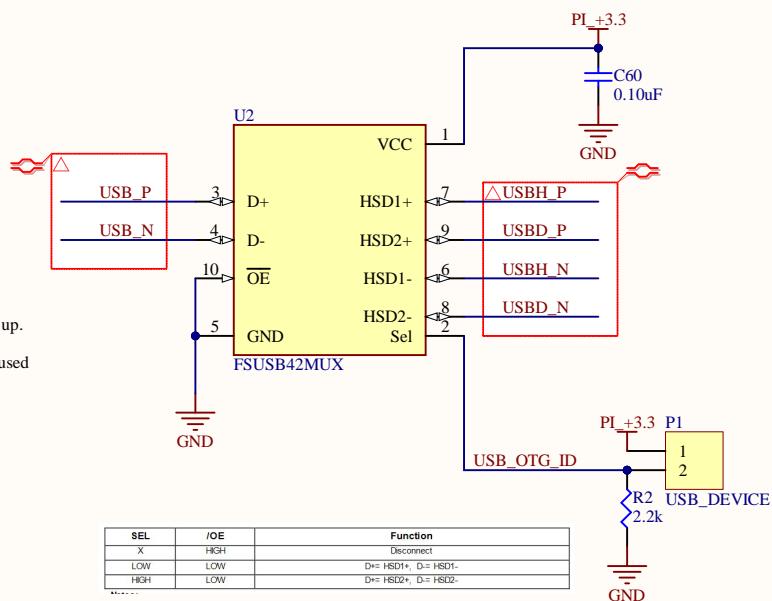
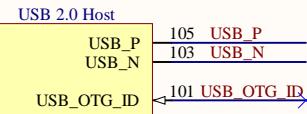
Revision: Rev0

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Compute module USB port, switchable between Host/Device

A



* Device power comes from J3 (USB device port)

* For host mode, configure the RPI as a host (should be default?), and disconnect header P1
* For device mode, configure the RPI as a device, and connect header P1

2.4. USB 2.0 (Hightspeed)

The USB 2.0 interface supports up to 480Mbps signalling. The differential pair should be routed as a 90Ω differential pair.
The P+N signals should ideally be matched to 0.15mm

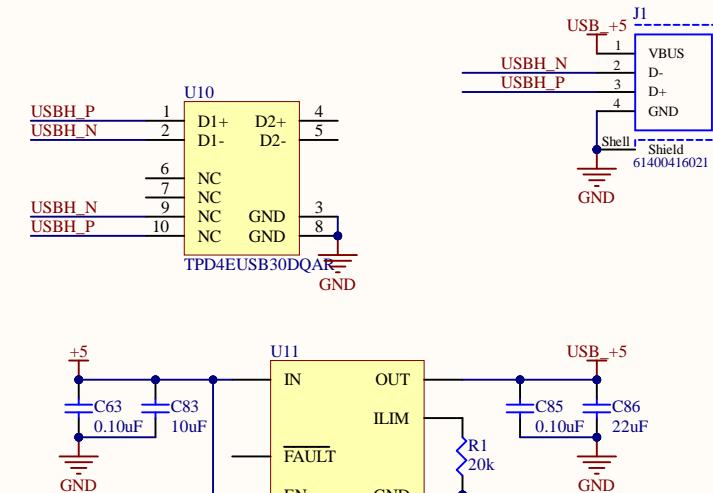
TIP

The USB interface is disabled to save power by default on the CM4 . To enable it you need to add
dtoverlay=dwc2,dr_mode=host to the config.txt file

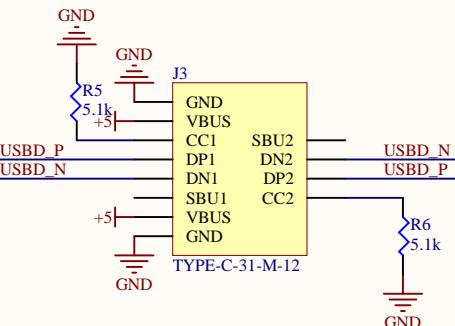
NOTE

The port is capable of being used as a true USB On-The-Go (OTG) port. While there is no official documentation, some users have had success making this work. The USB_0Tg pin is used to select between USB host and device that is typically wired to the ID pin of a Micro usb connector. To use this functionality it must be enabled in the OS that is used. If using either as a fixed slave or fixed master, please tie the USB_0Tg pin to ground

USB A port (host mode)



USB C port (device mode)



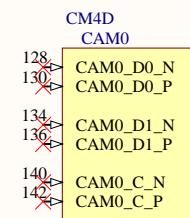
Title: Compute Module USB

Project: Raspberry Pincushion

Revision: Rev0

Date: 1/5/2021 Time: 10:43:19 PM Sheet 7 of 14

BLIN
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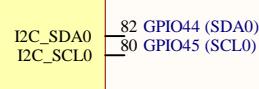


The CM4 supports two camera ports; CAM0 (2 lanes) and CAM1 (4 lanes).

Camera sensors supported by the official Raspberry Pi firmware are; the OmniVision OV5647, Sony IMX219 and Sony IMX477, no security device is required on Compute Module devices to use these camera sensors.

CM4R

GPIO I2C0
GPIO



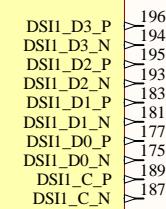
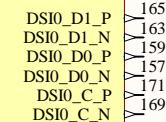
*I2C0 - Use for CAM1,DSI1,RTC

*Rpi4B using (2 lane CSI) CAM1,DSI1 and I2C0

Typically used for Camera and Displays
Internal 1.8K pull up to CM4_3.3V

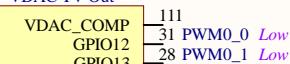
CM4F

DSI0,DSI1

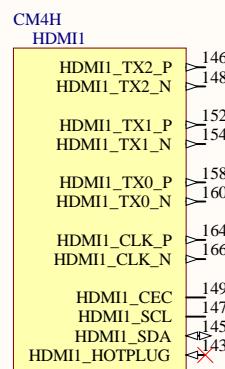


The CM4 supports two display ports; DISP0 (2 lanes) and DISP1 (4 lanes). Each lane supports a maximum of data rate per lane of 1Gbit/s.

VDAC TV Out



Video DAC output (TV OUT)
Can be use following pins for PWM signal
PWM0_0 = GPIO12
PWM0_1 = GPIO13



HDMI1_HOTPLUG
Input HDMI1 Hotplug Internally pulled down with a 100K. 5V tolerant.

HDMI1_SDA,SCL
Bidir HDMI1 SDA Internally pulled up with a 1.8K. 5V tolerant

Raspberry Pi Compute Module 4

CM4K

BT_nDisable

Can be left floating if driven low the Bluetooth interface will be disabled. Internal pulled up via 1.8K to CM4_3.3V

BT,WiFi Control

BT_nDisable

WL_nDisable

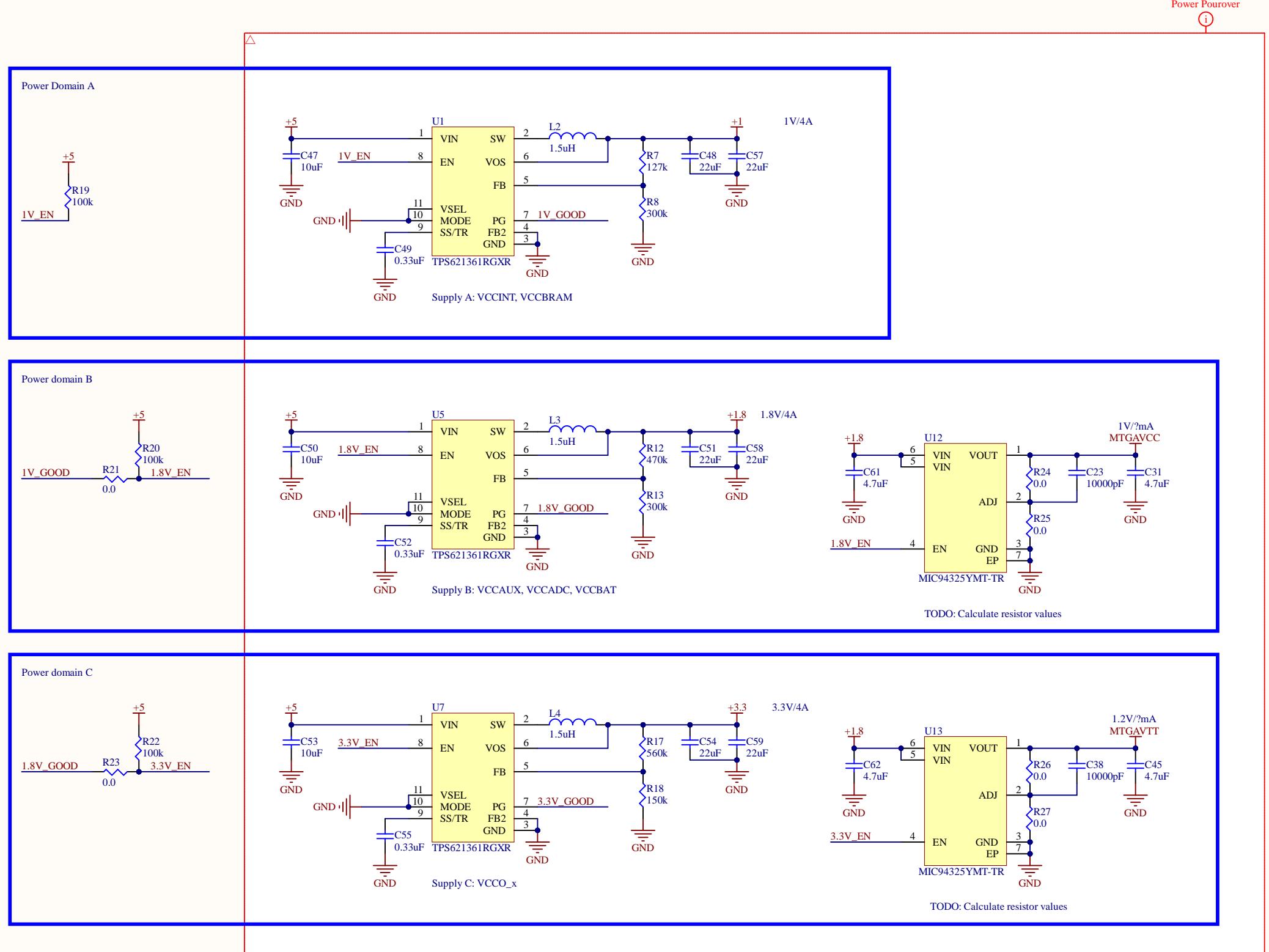
WL_nDisable

Can be left floating if driven low the wireless interface will be disabled. Internal pulled up via 1.8K to CM4_3.3V

Title: Compute Module Unused

Project: Raspberry Pincushion Revision: Rev0

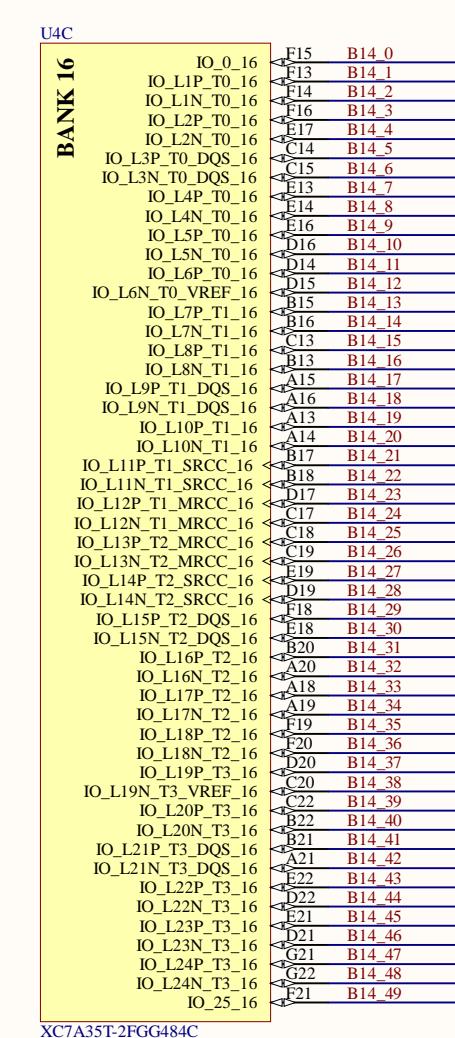
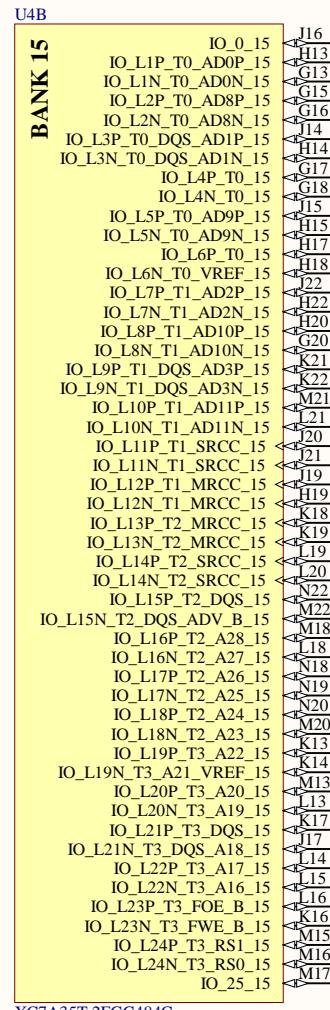
Date: 1/5/2021 Time: 10:43:19 PM Sheet 8 of 14



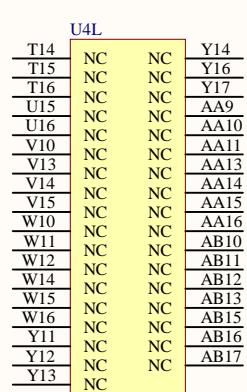
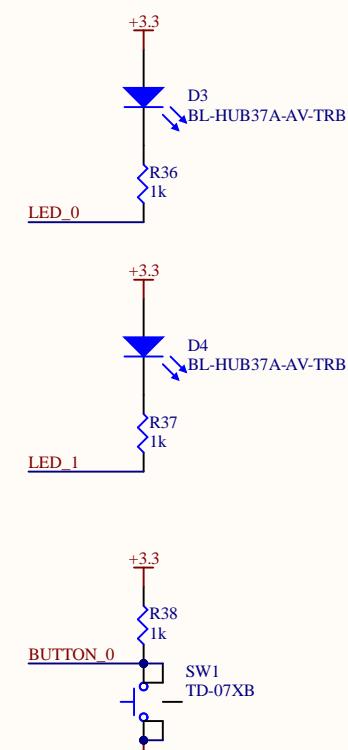
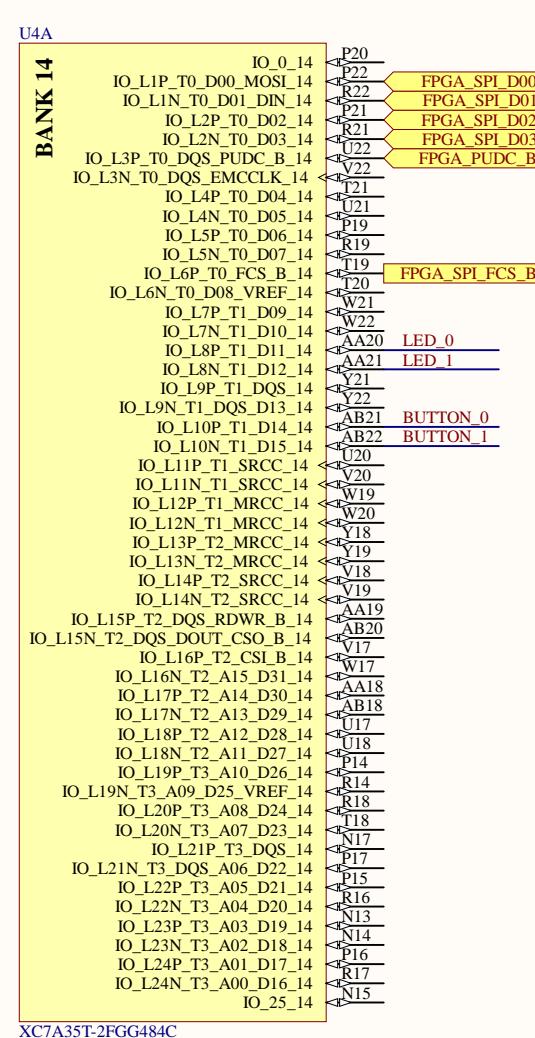
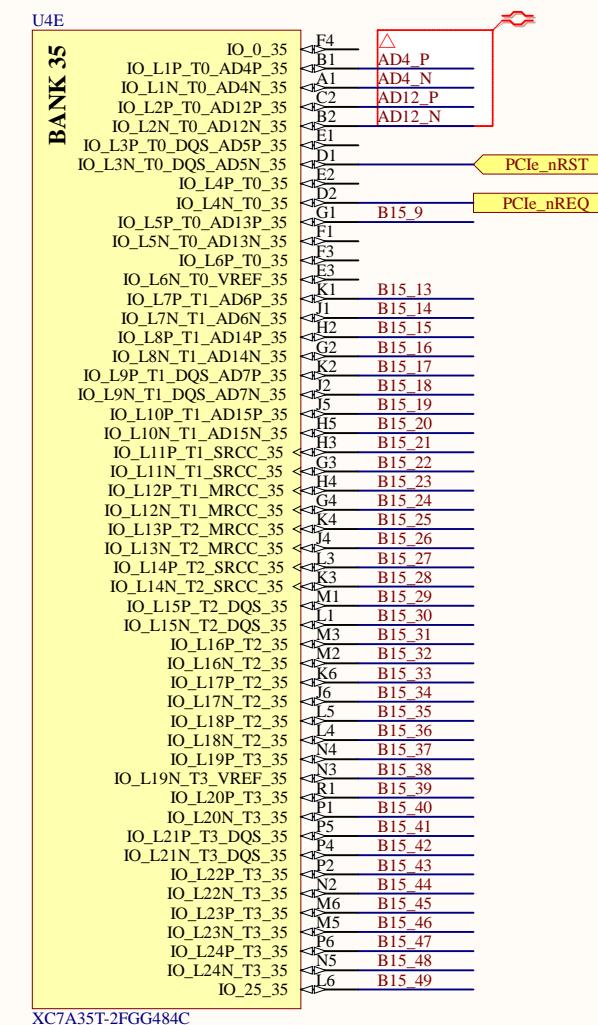
Supply	Rails	Type	Voltage	Starts after?
A	VCCINT, VCCBRAM,	DC-DC	1V	First
B	VCCAUX, VCCADC, VCCBAT	DC-DC	1.8V	A
C	MGTAVCC	Linear	1V	A
D	VCCO_x	DC-DC	3.3V	B
E	MGTAVTT	Linear	1.2V	B

For the FPGA to work correctly, the power supplies must be turned on in the specified order

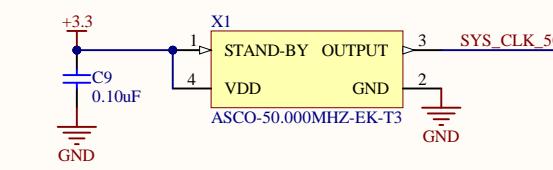
Title: FPGA Power Supply		
Project: Raspberry Pincushion	Revision: Rev0	
Date: 1/5/2021	Time: 10:43:19 PM	Sheet 9 of 14



Pins close to the PCIe clock should be pulled to GND



XC7A35T-2FGG484C



Title: FPGA GPIO		
Project: Raspberry Pincushion	Revision: Rev0	
Date: 1/5/2021	Time: 10:43:19 PM	Sheet 10 of 14



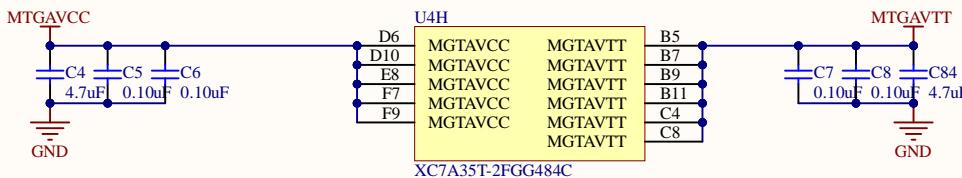
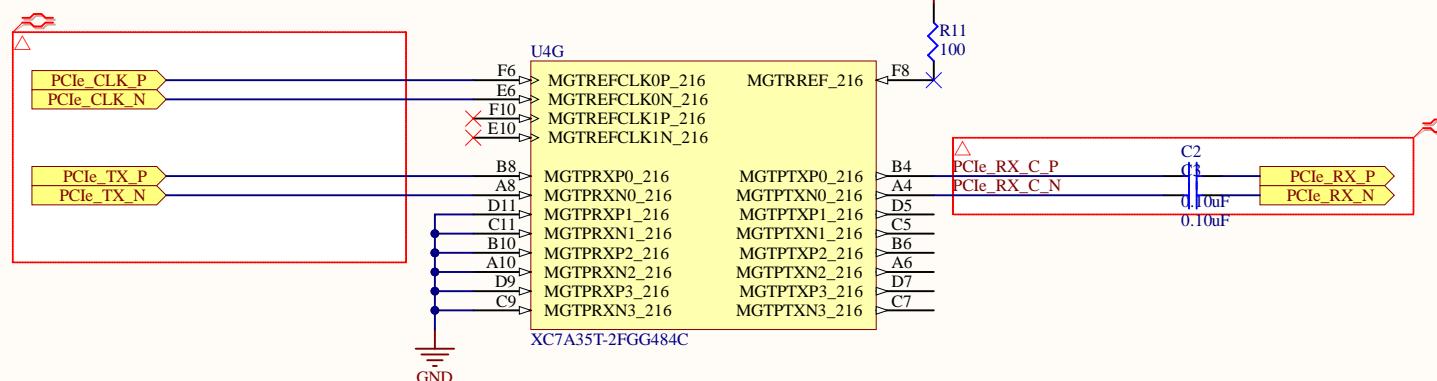


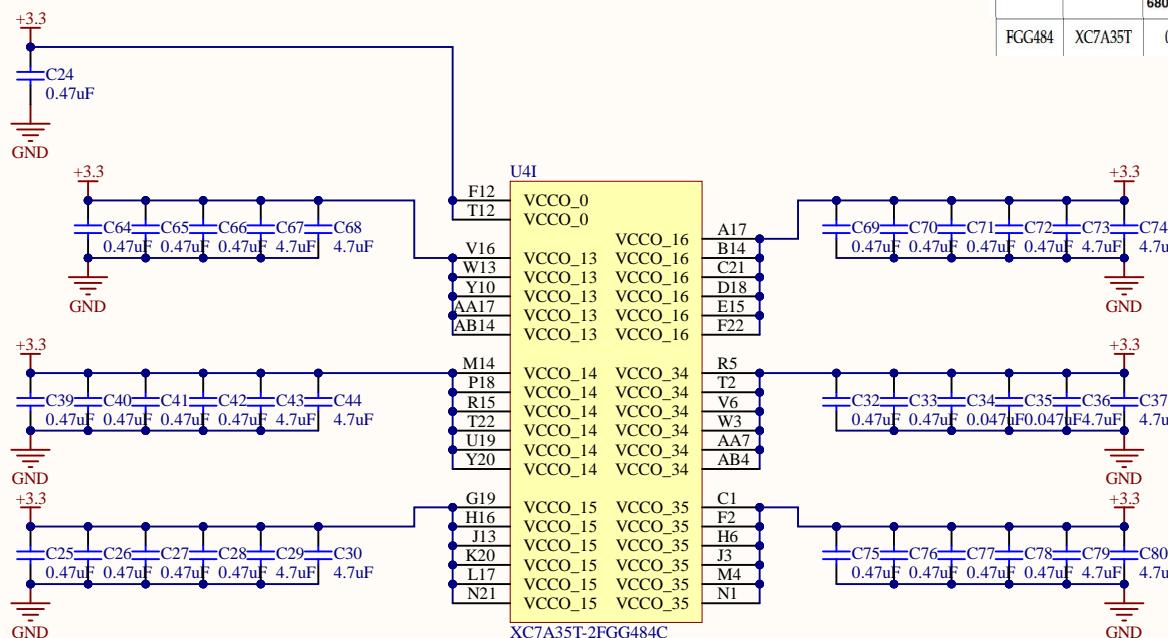
Table 5-11: FGG484/FBG484/SBG484 Package – 0.1 μ F Capacitor Placement

Capacitor	Package Pins			Value
	MGTAVCC	MGTAVTT	GND	
Cap1	D6	-	C6	0.1 μ F
Cap2	D10	-	C10	
Cap3	-	C4	C3	
Cap4	-	B11	B12	

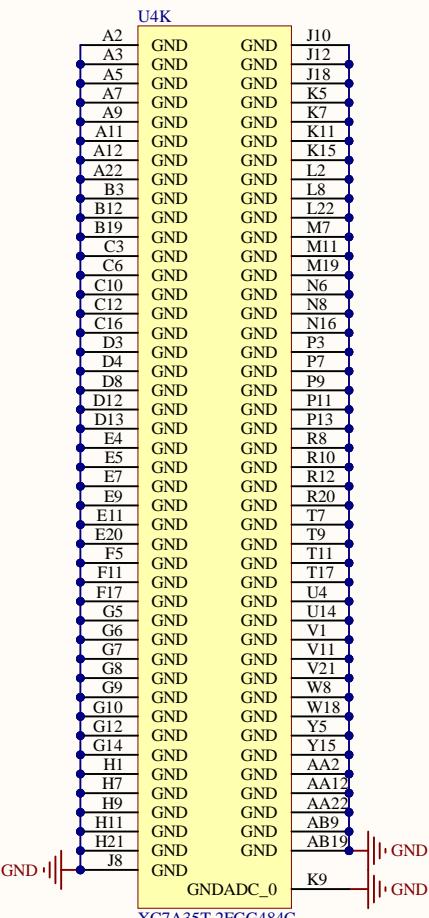
Title: FPGA PCIe			
Project: Raspberry Pincushion	Revision: Rev0		
Date: 1/5/2021	Time: 10:43:19 PM	Sheet 11	of 14



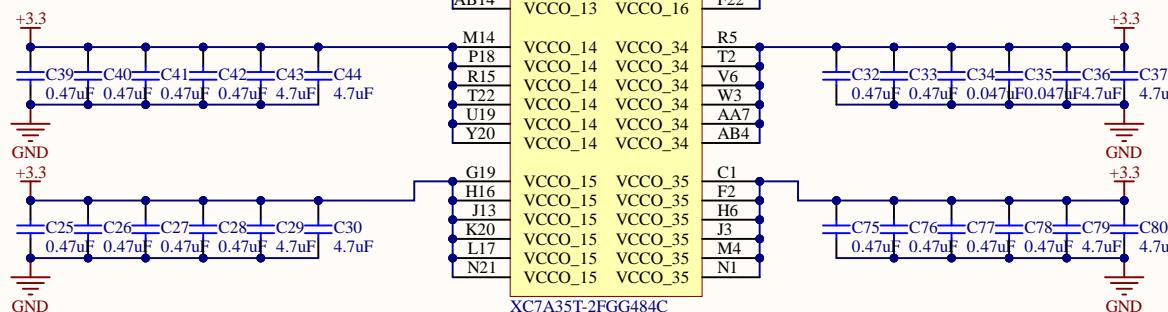
A



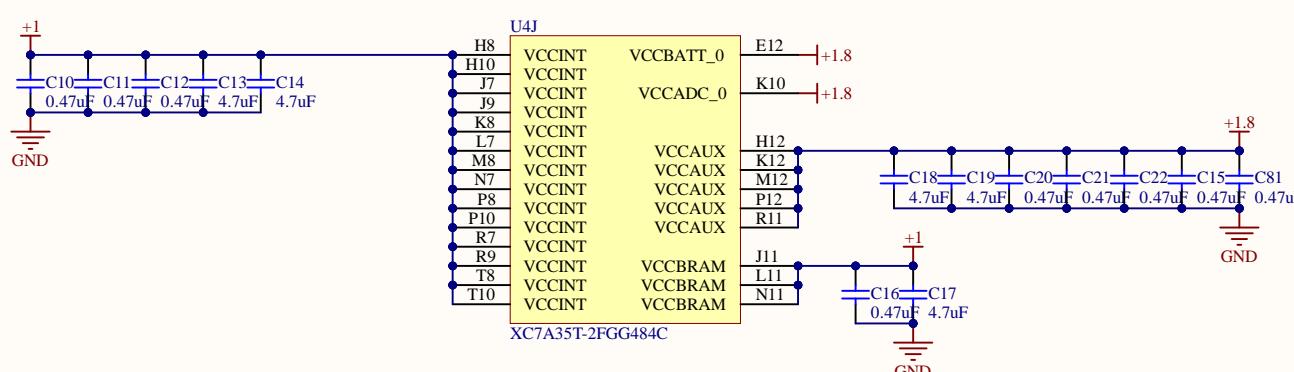
Package	Device	V _{CCINT}						V _{CCBRAM}				V _{CCAUX}			V _{CC} Bank 0	V _{CC} all other Banks (per Bank)		
		680 μ F	330 μ F	100 μ F	47 μ F	4.7 μ F	0.47 μ F	100 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F or 100 μ F ⁽³⁾	4.7 μ F	0.47 μ F	
FGG484	XC7A35T	0	0	1	0	2	3	0	1	0	1	1	2	5	1	1	2	4



B

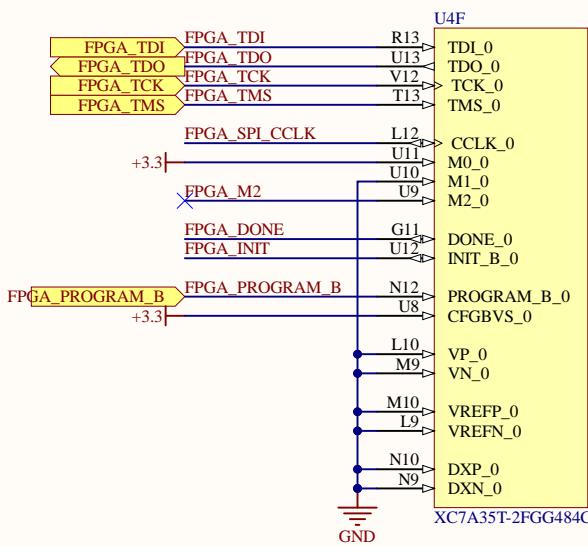


C



D

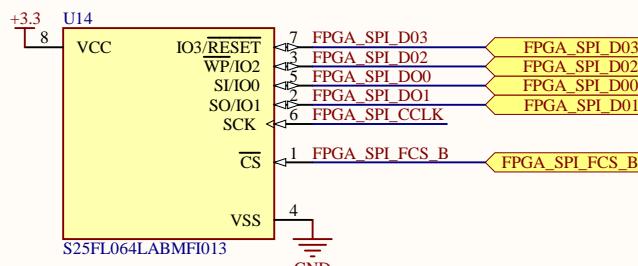
Title: FPGA power		
Project: Raspberry Pincushion	Revision: Rev0	
Date: 1/5/2021	Time: 10:43:20 PM	Sheet 12 of 14



JTAG: Use OpenOCD on RPi
Master SPI: TBD (bitbang from RPi?)

For JTAG: M2:1 M1:0 M0:1
For Master SPI: M2:0 M1:0 M0:1

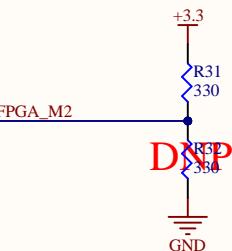
Pull CFGBVS_0 to 3.3V, when bank 0 is 3.3V



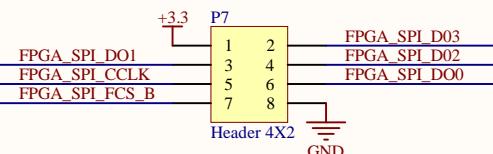
Pull low to reset Pull low to prevent boot Config guide says not needed



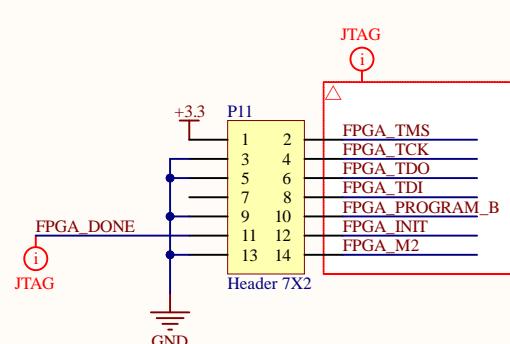
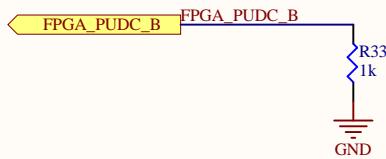
Place R31 for JTAG, R32 for SPI



TODO: Connect these to CM GPIO



Enable selectIO pullups



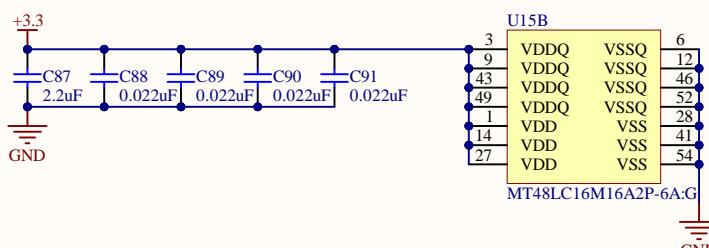
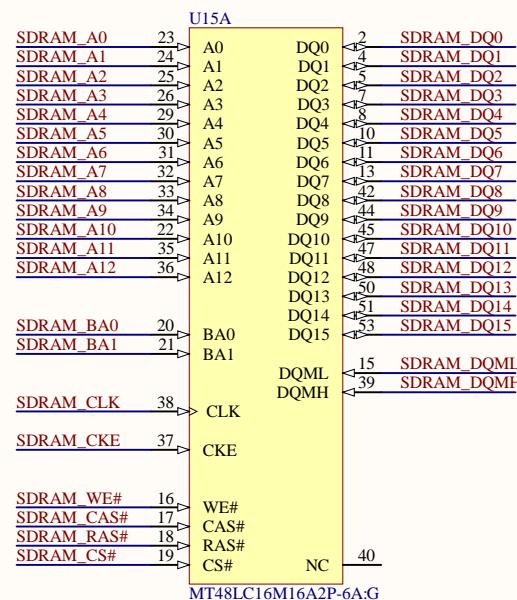
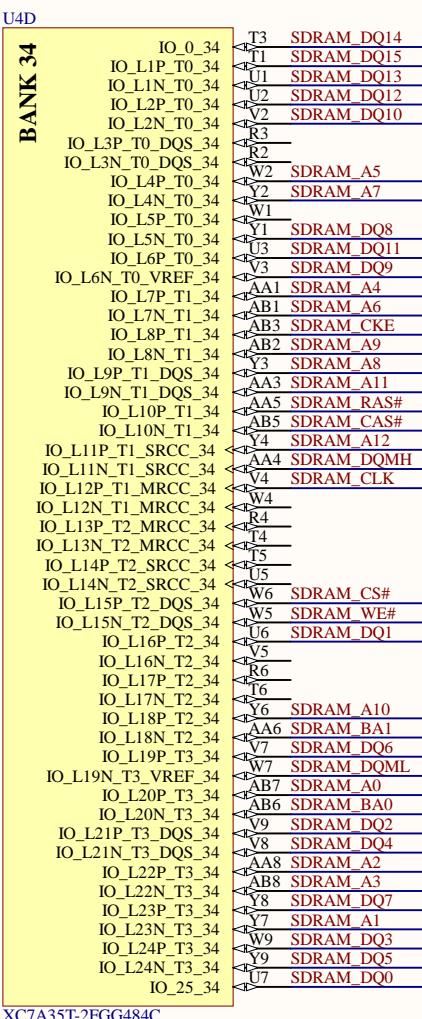
Title: **FPGA Configuration**

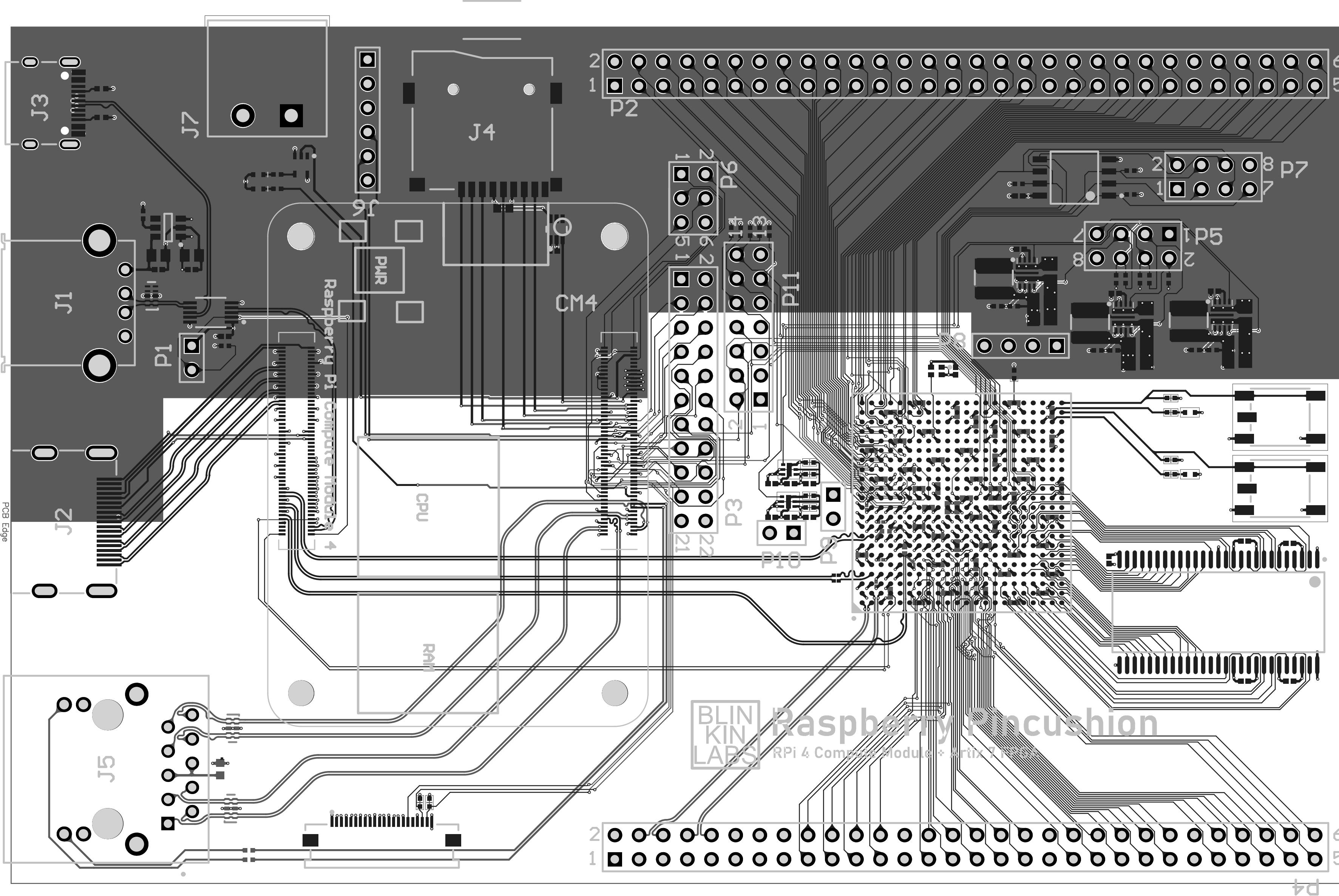
Project: **Raspberry Pincushion**

Revision: **Rev0**

Date: **1/5/2021** Time: **10:43:20 PM** Sheet **13** of **14**

A





Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Desktop\compute_fpga\pcb\PCB1.PcbDoc

Warnings 0
Rule Violations 4

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.099mm) (All),(All)	4
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.1mm) (Max=0.254mm) (Preferred=0.1mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor	0
Width 0.254mm constraint (Min=0.025mm) (Max=4mm) (All)	0
Hole To Hole Clearance (Gap=0.2mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Matched Lengths(Tolerance=0.15mm) (InNetClass('HDMI'))	0
Matched Lengths(Tolerance=0.15mm) (InNetClass('CAM'))	0
Matched Lengths(Tolerance=0.15mm) (InNetClass('USB_480MBps'))	0
Matched Lengths(Tolerance=0.15mm) (InNetClass('GBE_1Gbps'))	0
Matched Lengths(Tolerance=0.1mm) (InNetClass('PCIE'))	0
Room PCIE_escape (Bounding Region = (122mm, 68.663mm, 125mm, 75.25mm) (False)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	4

Clearance Constraint (Gap=0.099mm) (All),(All)

Clearance Constraint: (0.098mm < 0.099mm) Between Arc (93.828mm,34.445mm) on Top Layer And Arc (94.2mm,34.4mm)

Clearance Constraint: (0.094mm < 0.099mm) Between Arc (94.2mm,34.4mm) on Top Layer And Track

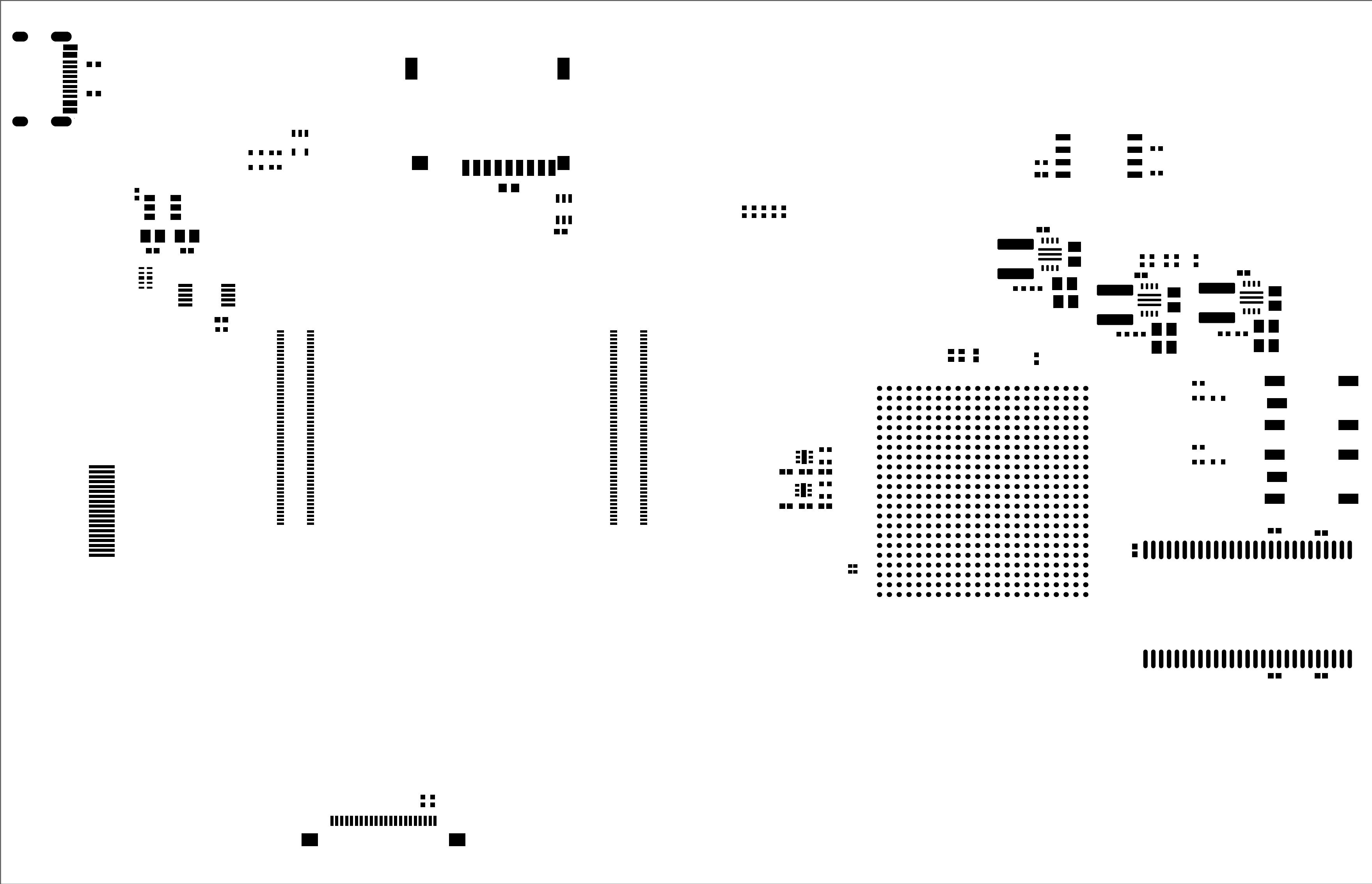
Clearance Constraint: (0.094mm < 0.099mm) Between Track (93.901mm,32.504mm)(93.906mm,33.13mm) on Top Layer

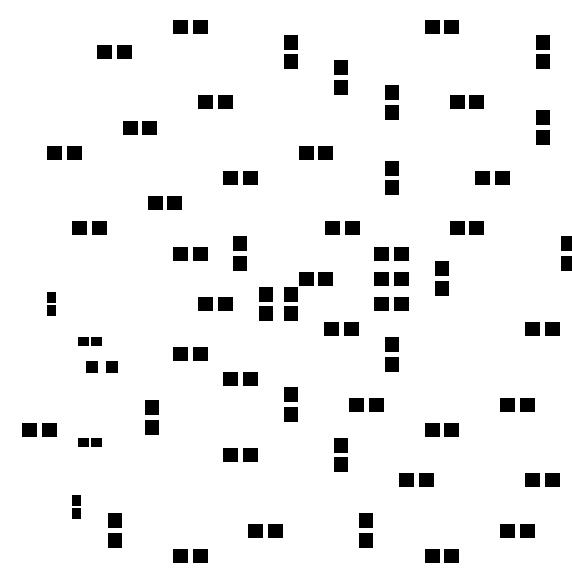
Clearance Constraint: (0.094mm < 0.099mm) Between Track (93.906mm,33.13mm)(93.906mm,34.445mm) on Top Layer

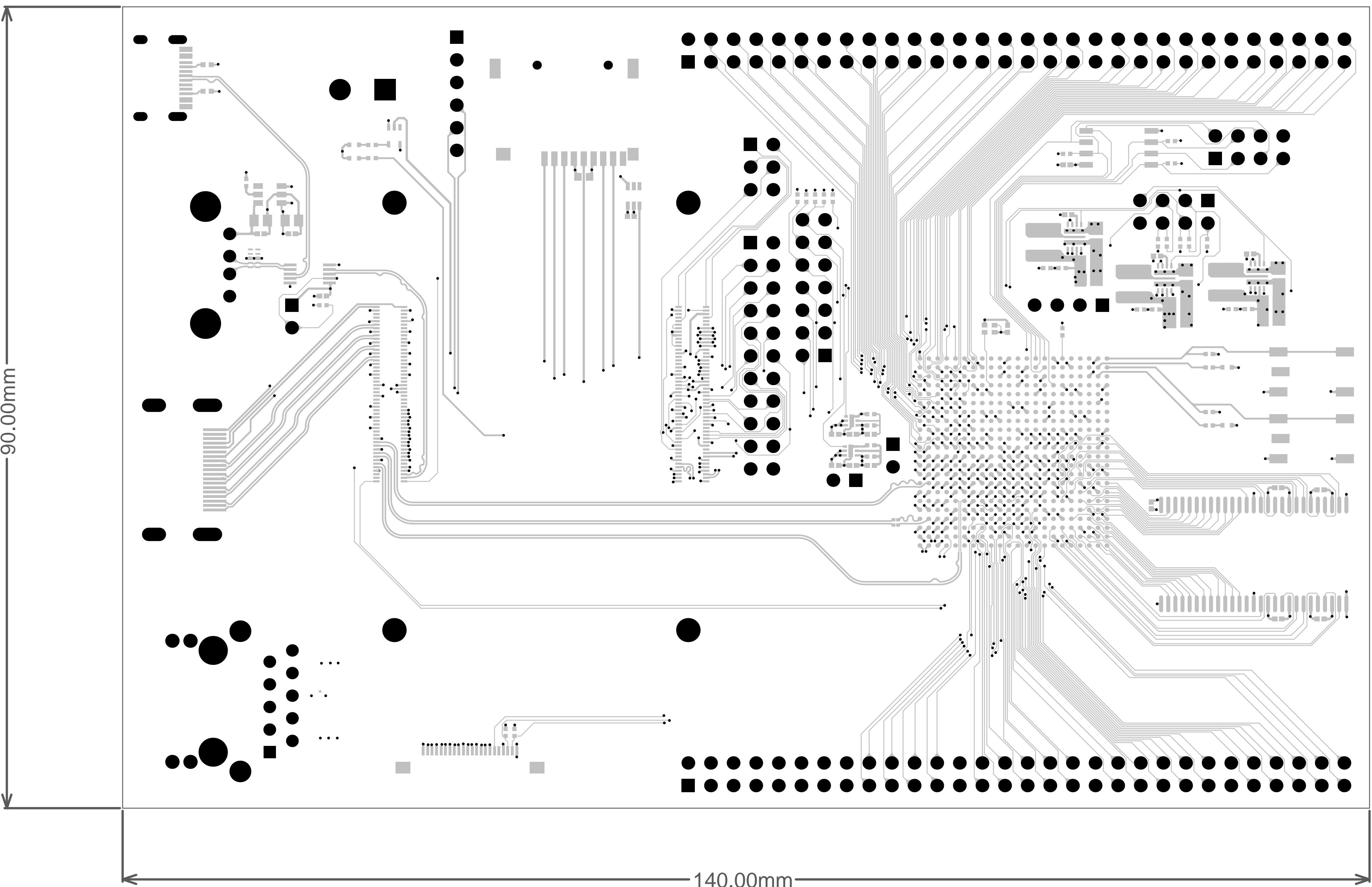
And

Electrical Rules Check Report

Class	Document	Message
Warning	compute module.SchDoc	Component U3 74LVC1G17GW at 4300mil,1900mil: Component revision is
Warning	FPGA GPIO.SchDoc	NetU4_D1 contains IO Pin and Input Port objects (Pin U4-D1, Port PCle_nRST).
Warning	FPGA GPIO.SchDoc	NetU4_D2 contains IO Pin and Output Port objects (Pin U4-D2, Port PCle_nREQ).
Warning	FPGA GPIO.SchDoc	NetU4_T19 contains IO Pin and Output Port objects (Pin U4-T19, Port FPGA_SPI_FCS_B).
Warning	FPGA GPIO.SchDoc	NetU4_U22 contains IO Pin and Input Port objects (Pin U4-U22, Port FPGA_PUDC_B).
Warning	FPGA GPIO.SchDoc	PCle_nRST contains IO Pin and Output Pin objects (Pin U4-D1, Pin CM4-109).
Warning	FPGA GPIO.SchDoc	SYS_CLK_50 contains IO Pin and Output Pin objects (Pin U4-J19, Pin X1-3).







Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	Solder Resist	0.59mil	3.9
1	Top Layer	Copper	1.81mil	
	Dielectric 2	PP-006	4.37mil	3.23
2	GND	Copper	0.59mil	
	Dielectric 4	Core-009	4.02mil	3.66
3	Power	Copper	0.59mil	
	Dielectric 6	PP-006	7.72mil	3.61

