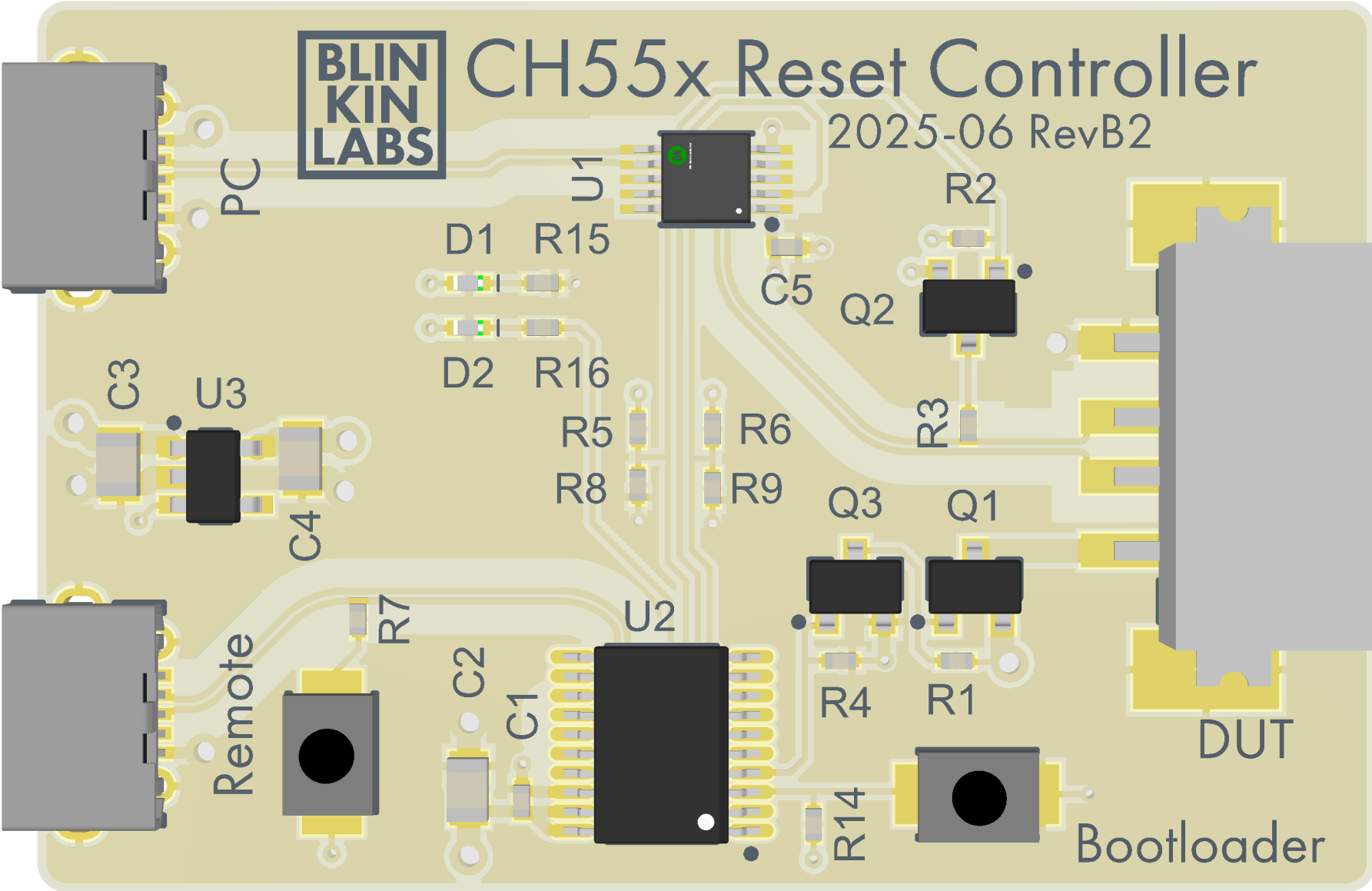




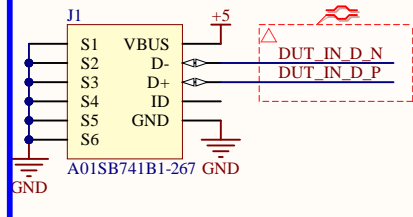
# CH55x Reset Controller

2025-06 RevB2

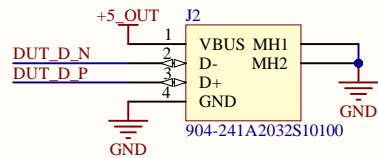


# CH55x Reset Controller

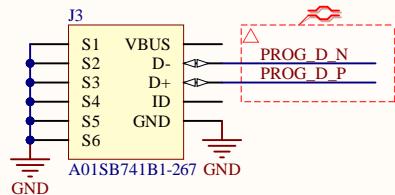
DUT micro USB input



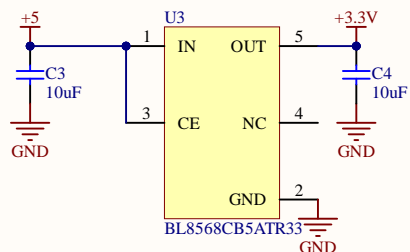
DUT USB A output



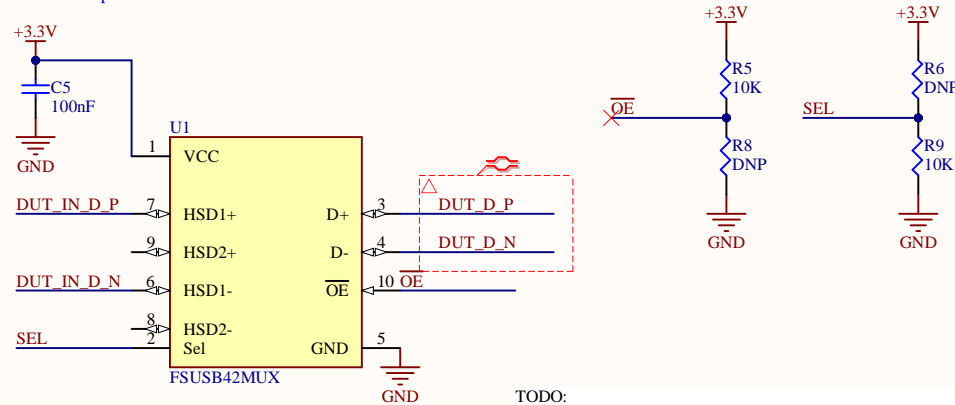
Switch control Micro USB input



3.3V regulator

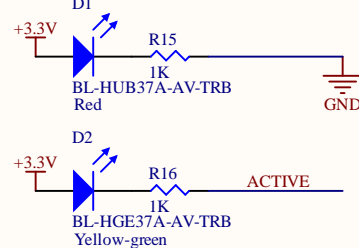


USB mux chip

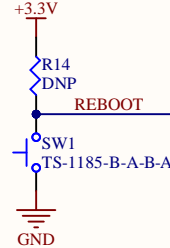


TODO:  
\* Add (optional) diode path from Switch control USB input, so that U2 can be put into programming mode more easily

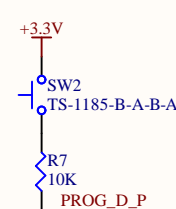
Feedback LEDs



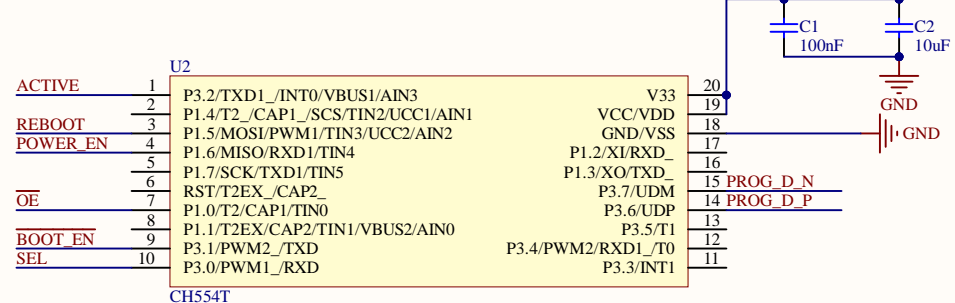
Put DUT in program mode



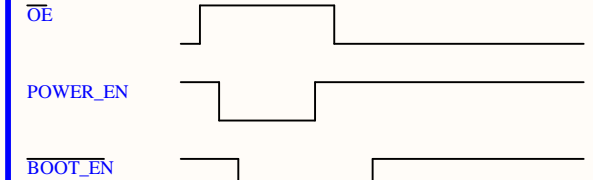
Put U2 in program mode



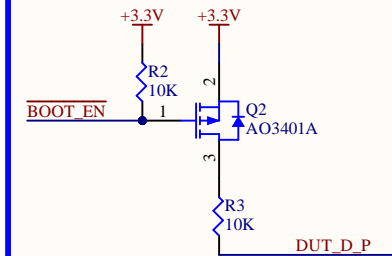
CH554 for reset sequencing



Reboot sequence

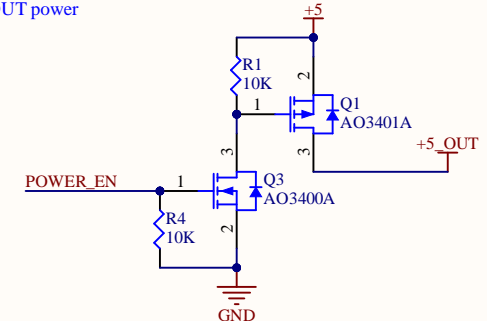


D+ pullup



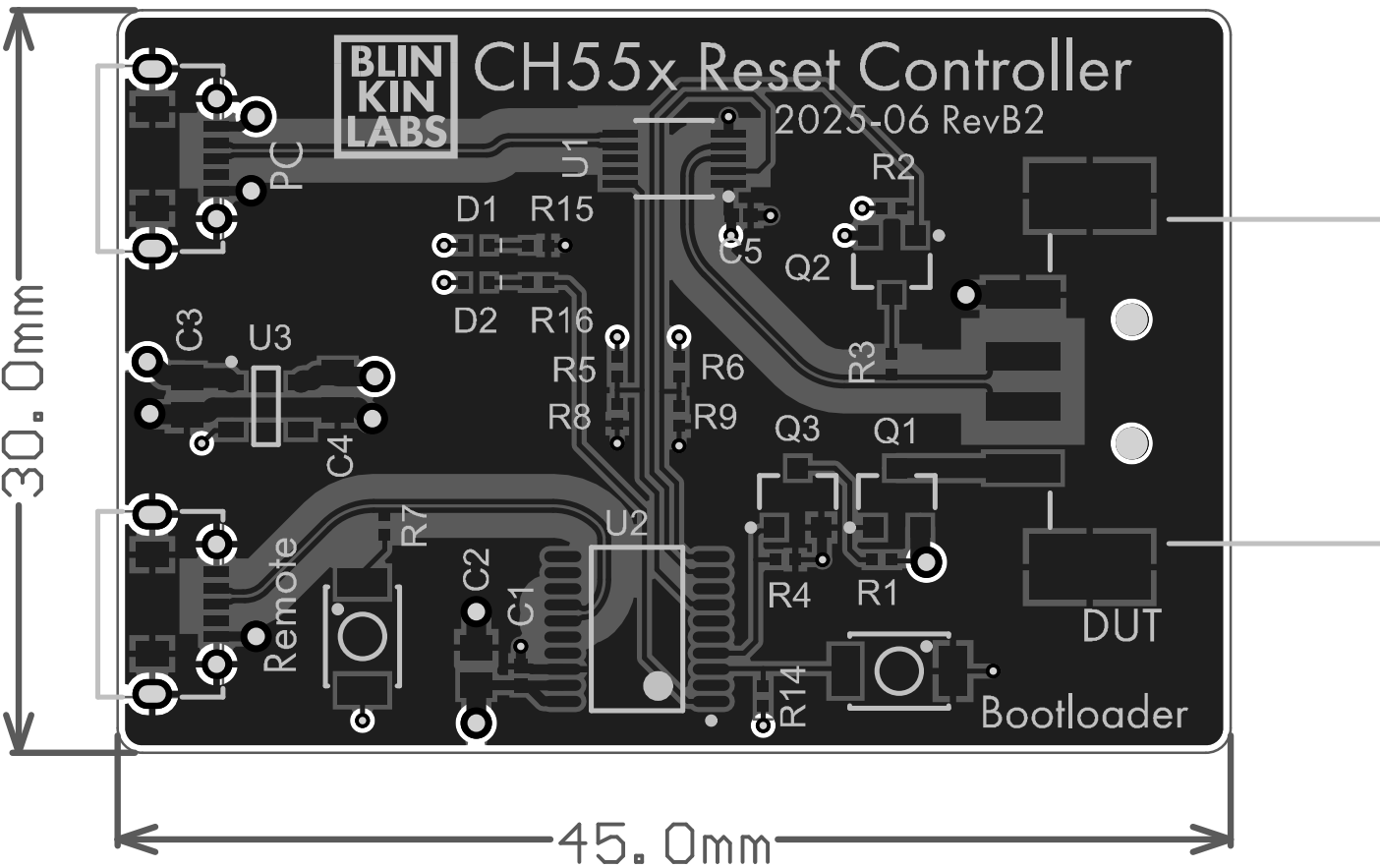
When BOOT\_EN is high, Q2 is off and R3 is left floating  
When BOOT\_EN is low, Q2 is on and R3 is connected to 3.3V

DUT power



When POWER\_EN is high, Q3 is on, Q1 is on, so +5V out is +5V  
When POWER\_EN is low, Q3 is off, Q1 is off, so +5V\_OUT is floating

# CH55x Reset Controller



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	SM-001	0.013mm	4
1	Top Layer	CF-004	0.035mm	
	Dielectric 2	PP-022	0.200mm	4.6
2	Layer 1	CF-004	0.015mm	
	Dielectric 3	Core-039	0.700mm	4.8
3	Layer 2	CF-004	0.015mm	
	Dielectric 4	PP-022	0.200mm	4.6
4	Bottom Layer	CF-004	0.035mm	
	Bottom Solder	SM-001	0.013mm	4
	Bottom Overlay			

Total board thickness:

1.226mm

Silkscreen: white / don't care

Soldermask: green / don't care

Surface finish: ENIG

Copper weight: 1oz outer, 0.5oz inner

## Design Rules Verification Report

Filename : C:\Users\matt\reference\ch55x\_programmer\pcb\PCB1.PcbDoc

Warnings 0  
Rule Violations 55

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.127mm)	0
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Clearance Constraint (Gap=1mm) (InDifferentialPairClass('D90')),(InPolygon)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=0.8mm) (Preferred=0.4mm) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor	0
Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	39
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	7
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	9
Room Sheet1 (Bounding Region = (120.775mm, 77.5mm, 184mm, 122.5mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	55

<b>Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)</b>	
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C1-1(16.3mm,2.71mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad C4-1(8.9mm,15.35mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad C4-2(8.9mm,13.85mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm)	Between Pad C4-2(8.9mm,13.85mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C5-1(24.81mm,21.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J1-D-(4mm,24.65mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J1-D-(4mm,24.65mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J1-D+(4mm,24mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J1-GND(4mm,22.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm)	Between Pad J1-GND(4mm,22.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm)	Between Pad J1-S4(4mm,26.425mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-D-(4mm,6.65mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-D-(4mm,6.65mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-D+(4mm,6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad J3-GND(4mm,4.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm)	Between Pad J3-GND(4mm,4.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm)	Between Pad J3-S4(4mm,8.425mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R1-1(30.5mm,7.8mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R14-1(26.1mm,2.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R15-1(16.6mm,20.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R16-1(16.6mm,19mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R2-1(31.7mm,22mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R3-1(31.3mm,15.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R4-1(27.4mm,7.8mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R5-1(20.2mm,15.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R6-1(22.7mm,15.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R7-1(10.8mm,9.6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R8-1(20.2mm,13.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R9-1(22.7mm,13.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-1(24.7mm,23mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-10(20.3mm,23mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-2(24.7mm,23.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-3(24.7mm,24mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-4(24.7mm,24.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-6(20.3mm,25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-7(20.3mm,24.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm)	Between Pad U1-8(20.3mm,24mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U3-1(4.6mm,14.95mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U3-2(4.6mm,14mm) on Top Layer And Pad

<b>Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)</b>	
Silk To Solder Mask Clearance Constraint: (0.124mm < 0.254mm)	Between Arc (24.7mm,22.476mm) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm)	Between Arc (32.7mm,4.3mm) on Top Overlay And Pac
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm)	Between Arc (8.9mm,5.8mm) on Top Overlay And Pac
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm)	Between Pad D1-2(15.025mm,20.5mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm)	Between Pad D2-2(15.025mm,19mm) on Top Layer Anc
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm)	Between Pad J2-5(39.3mm,22.5mm) on Top Layer Anc
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm)	Between Pad J2-6(39.3mm,7.5mm) on Top Layer Anc

**Board Clearance Constraint (Gap=0mm) (All)**

Board Outline Clearance(Outline Edge): (Collision < 0.1mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (Collision < 0.1mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (Collision < 0.1mm) Between Board Edge And Track
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Board Outline Clearance(Outline Edge): (Collision < 0.1mm) Between Board Edge And Track

## Electrical Rules Check Report

Class	Document	Message
		Successful Compile for ch55x_programmer.PrjPcb

