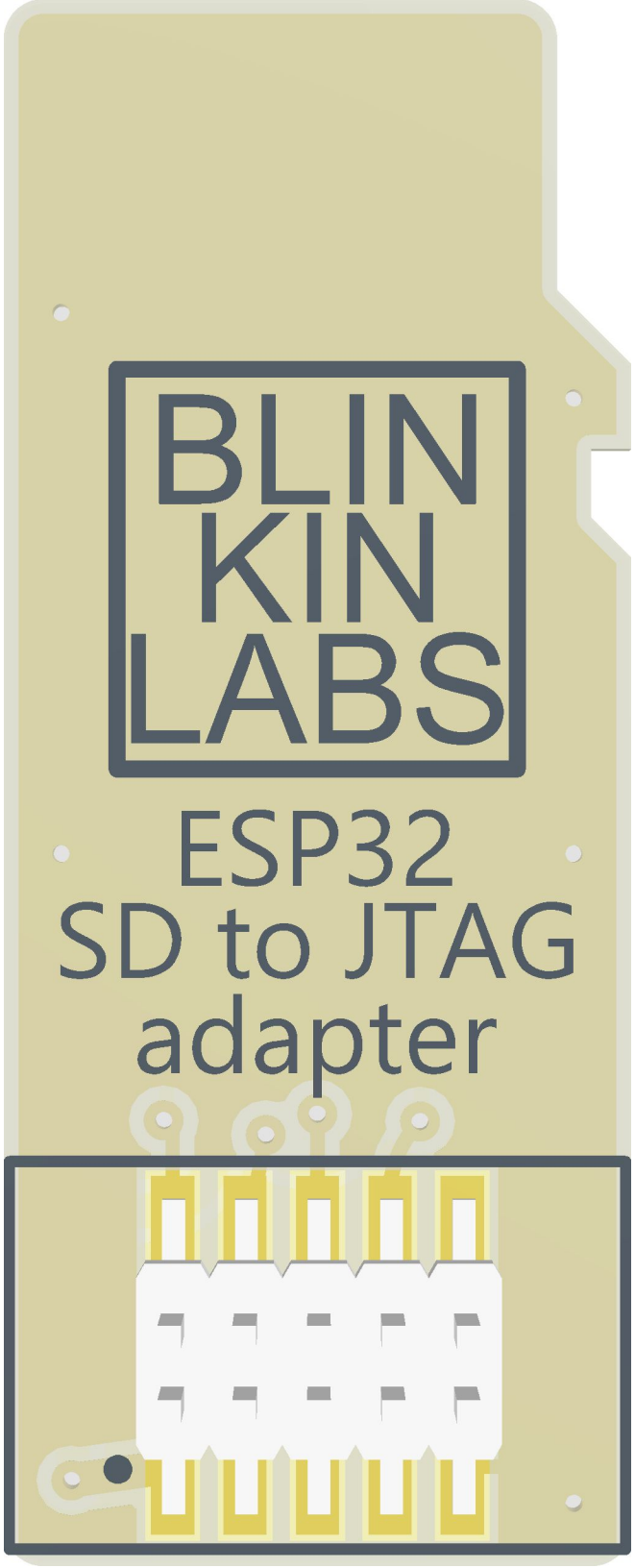
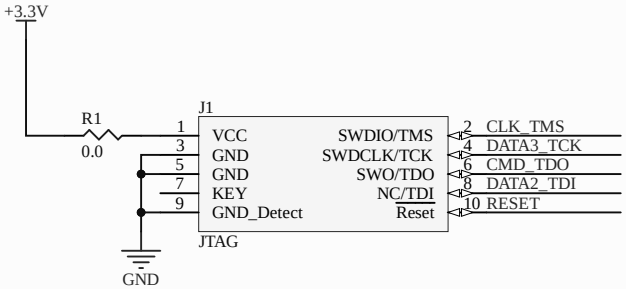
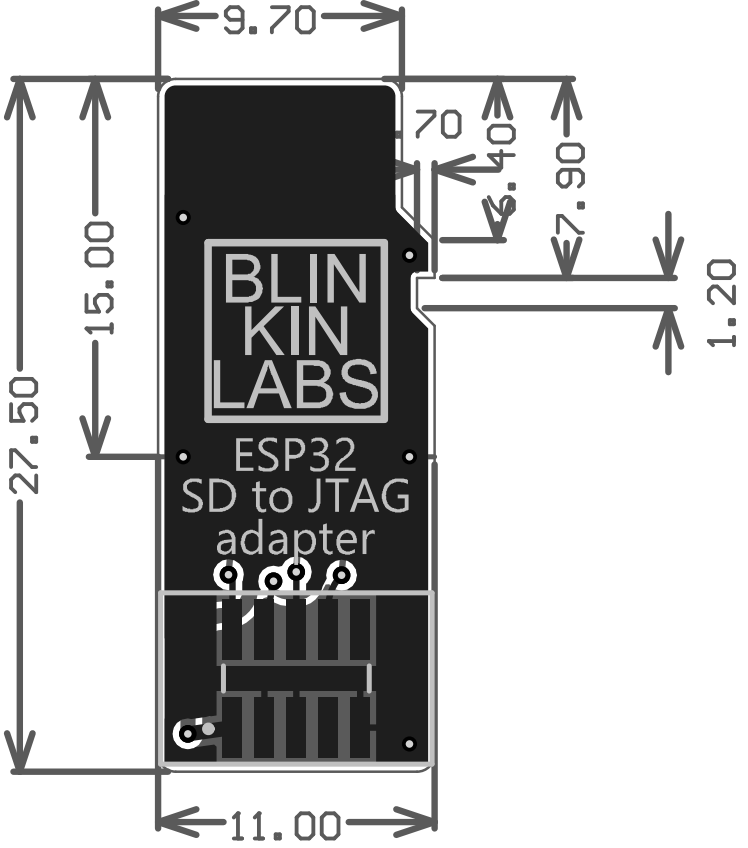

BLIN
KIN
LABS
ESP32
SD to JTAG
adapter



BLIN
KIN
LABS

Title: *		BLIN KIN LABS
Project: esp_sd_debug_adapter.PrjPcb	Revision: *	
Date: 6/17/2020 Time: 1:50:50 PM	Sheet * of *	



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	Solder Resist	0.013mm	3.8
1	Top Layer	Copper	0.036mm	
	Dielectric 1	FR-4	0.702mm	4.8
2	Bottom Layer	Copper	0.036mm	
	Bottom Solder	Solder Resist	0.013mm	3.8
	Bottom Overlay			
Total board thickness:			0.799mm	

Design Rules Verification Report

Filename : C:\Users\matt\Desktop\esp_sd_debug_adapter\esp_sd_debug_adapter.PcbDoc

Warnings 0
Rule Violations 33

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.6mm) (Preferred=0.254mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	7
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	14
Silk to Silk (Clearance=0.254mm) (All),(All)	4
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	8
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	33

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad Free-P1(8.7mm,12.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad Free-P2(7.6mm,12.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad Free-P3(6.5mm,12.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad Free-P4(5.4mm,12.6mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad Free-P5(4.3mm,12.45mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad Free-P6(3.2mm,12.6mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad Free-P7(2.1mm,12.45mm) on Bottom Layer

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(2.96mm,-10.75mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-1(2.96mm,-10.75mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-10(8.04mm,-6.85mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J1-10(8.04mm,-6.85mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(2.96mm,-6.85mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-2(2.96mm,-6.85mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-3(4.23mm,-10.75mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-4(4.23mm,-6.85mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-5(5.5mm,-10.75mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-6(5.5mm,-6.85mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-7(6.77mm,-10.75mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-8(6.77mm,-6.85mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(8.04mm,-10.75mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J1-9(8.04mm,-10.75mm) on Top Layer And

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.158mm < 0.254mm) Between Text "BLIN" (2mm,6.1mm) on Top Overlay And Text "KIN
Silk To Silk Clearance Constraint: (0.209mm < 0.254mm) Between Text "KIN" (2mm,4mm) on Top Overlay And Text "LABS
Silk To Silk Clearance Constraint: (0.096mm < 0.254mm) Between Text "LABS" (2mm,1.9mm) on Top Overlay And Trac
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "LABS" (2mm,1.9mm) on Top Overlay And Trac

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.076mm < 0.254mm) Between Board Edge And Polygon Region (0 hole(s)) Bottom
Board Outline Clearance(Outline Edge): (0.076mm < 0.254mm) Between Board Edge And Polygon Region (2 hole(s)) Top
Board Outline Clearance(Outline Edge): (0mm < 0.254mm) Between Board Edge And Text "DATA

DATA3

GND

CLK / TMS

3.3V

CMD / TDO

DATA3 / TCK

DATA2 / TDI" (9.7mm,10.4mm) on Bottom Overlay

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Text "ESP32

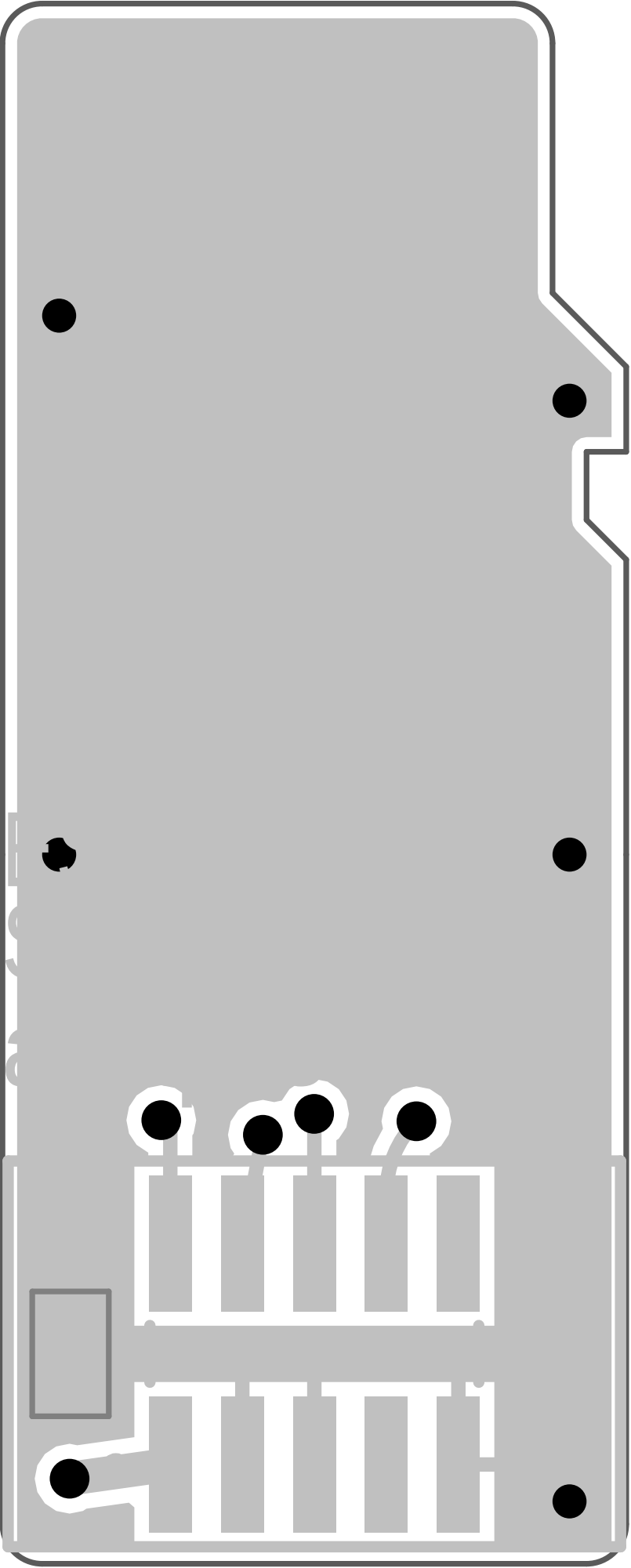
SD to JTAG

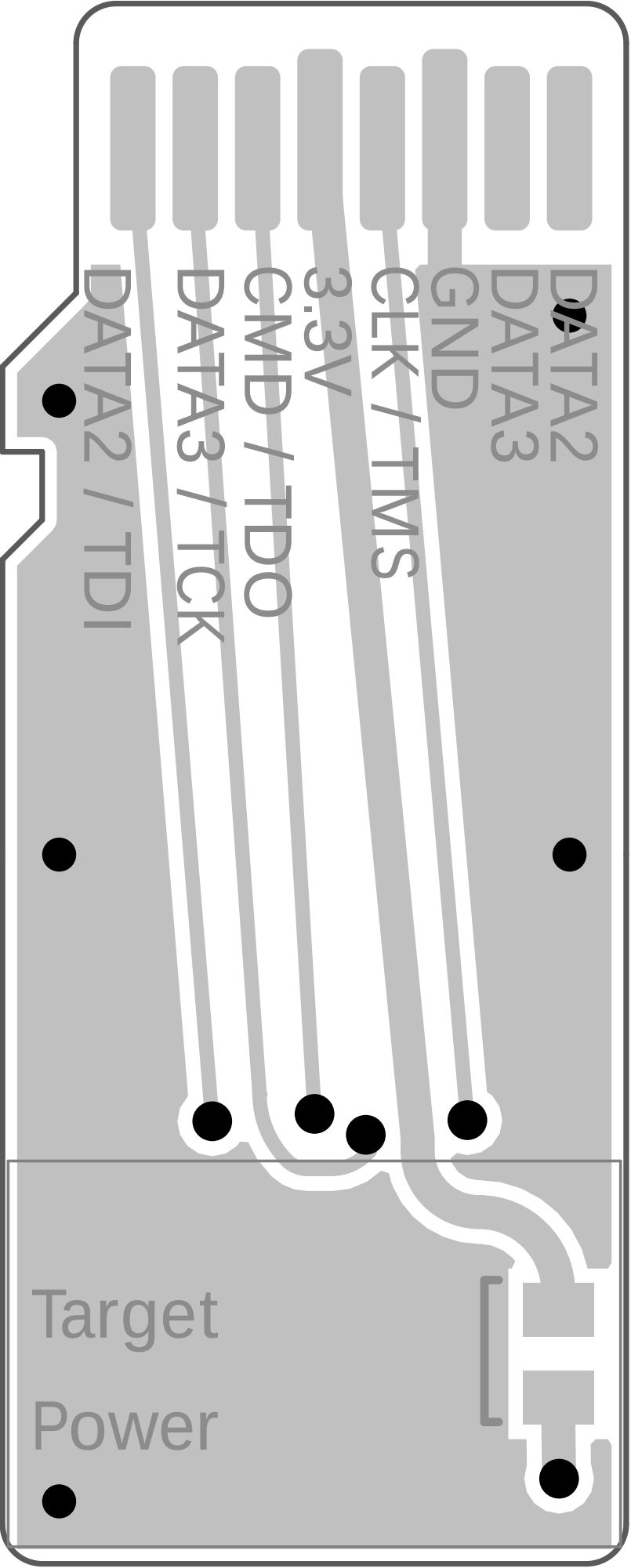
adapter" (-0.018mm,-4.5mm) on Top Overlay

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (Collision < 0.254mm) Between Board Edge And Track

Electrical Rules Check Report

Class	Document	Message
Error	esp_sd_debug_adapter.SchDoc	Net +3.3V has only one pin (Pin R1-1)
Error	esp_sd_debug_adapter.SchDoc	Net CLK_TMS has only one pin (Pin J1-2)
Error	esp_sd_debug_adapter.SchDoc	Net CMD_TDO has only one pin (Pin J1-6)
Error	esp_sd_debug_adapter.SchDoc	Net DATA2_TDI has only one pin (Pin J1-8)
Error	esp_sd_debug_adapter.SchDoc	Net DATA3_TCK has only one pin (Pin J1-4)
Error	esp_sd_debug_adapter.SchDoc	Net RESET has only one pin (Pin J1-10)
Warning	esp_sd_debug_adapter.SchDoc	Off grid L? at 1111.955mil,3352.254mi
Warning	esp_sd_debug_adapter.SchDoc	Un-Designated Part L?




DATA2
DATA3
GND
CLK / TMS
3.3V
CMD / TDO
DATA3 / TCK
DATA2 / TDI
Target
Power