





Design Rules Verification ReportFilename: C:\Users\matt\Desktop\upduino_tinymatrix\upduino_tinymatrix.PcbDoc

Warnings 0 Rule Violations 42

Warnings Total

Rule Violations		
Clearance Constraint (Gap=10mil) (All),(All)	0	
Short-Circuit Constraint (Allowed=No) (All),(All)	0	
Un-Routed Net Constraint ((All))	0	
Modified Polygon (Allow modified: No), (Allow shelved: No)		
Width Constraint (Min=10mil) (Max=60mil) (Preferred=10mil) (All)	0	
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0	
Hole To Hole Clearance (Gap=10mil) (All),(All)	0	
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0	
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	42	
Silk to Silk (Clearance=10mil) (All),(All)		
Net Antennae (Tolerance=0mil) (All)		
Room upduino_tinymatrix (Bounding Region = (4675mil, 2325mil, 6975mil, 4800mil)		
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)		
Total		

Silk To Solder Mask (Clearance=10mil) (IsPad),(All) Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-1(6400mil,3700mil) on Top Layer And Trac Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-1(6400mil,3700mil) on Top Layer And Traci Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-10(6553.543mil,3500mil) on Top Layer And Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-10(6553.543mil,3500mil) on Top Layer And Silk To Solder Mask Clearance Constraint: (5.937mil < 10mil) Between Pad OUT1-2(6553.543mil,3700mil) on Top Layer And Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-2(6553.543mil,3700mil) on Top Layer And Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-3(6400mil,3650mil) on Top Layer And Traci Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-4(6553.543mil,3650mil) on Top Layer And Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-5(6400mil,3600mil) on Top Layer And Traci Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-6(6553.543mil,3600mil) on Top Layer And Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-7(6400mil,3550mil) on Top Layer And Trac Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-8(6553.543mil,3550mil) on Top Layer And Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-9(6400mil,3500mil) on Top Layer And Traci Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT1-9(6400mil, 3500mil) on Top Layer And Trac Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT2-1(6400mil,2850mil) on Top Layer And Traci Silk To Solder Mask Clearance Constraint: (5.906mil < 10mil) Between Pad OUT2-1(6400mil,2850mil) on Top Layer And Traci Silk To Solder Mask Clearance Constraint: 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10mil) Between Pad OUT3-9(5146.457mil,2650mil) on Top Layer And

Electrical Rules Check Report

Class	Document	Message
Error	upduino_tinymatrix.SchDoc	Net +3.3V has only one pin (Pin P1-1)
Error	upduino_tinymatrix.SchDoc	Net J8_OSC_OUT has only one pin (Pin P2-2)
Warning	upduino_tinymatrix.SchDoc	Off grid L? at 8007.223mil,3995.733mil
Warning	upduino_tinymatrix.SchDoc	Un-Designated Part L?



