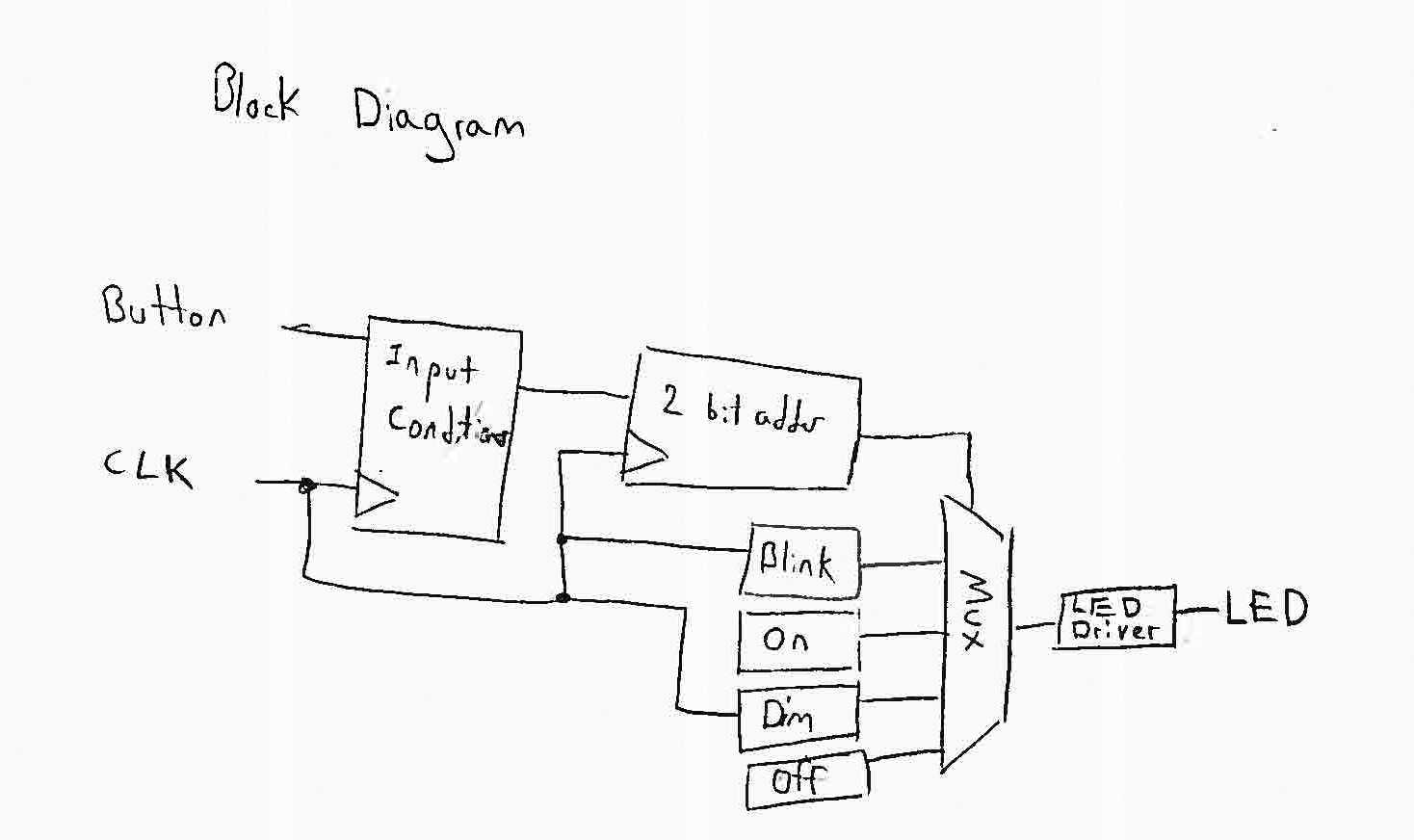
# Computer Architecture Midterm – Schematic and Block Diagram

Marie-Caroline Finke

## Block Diagram:



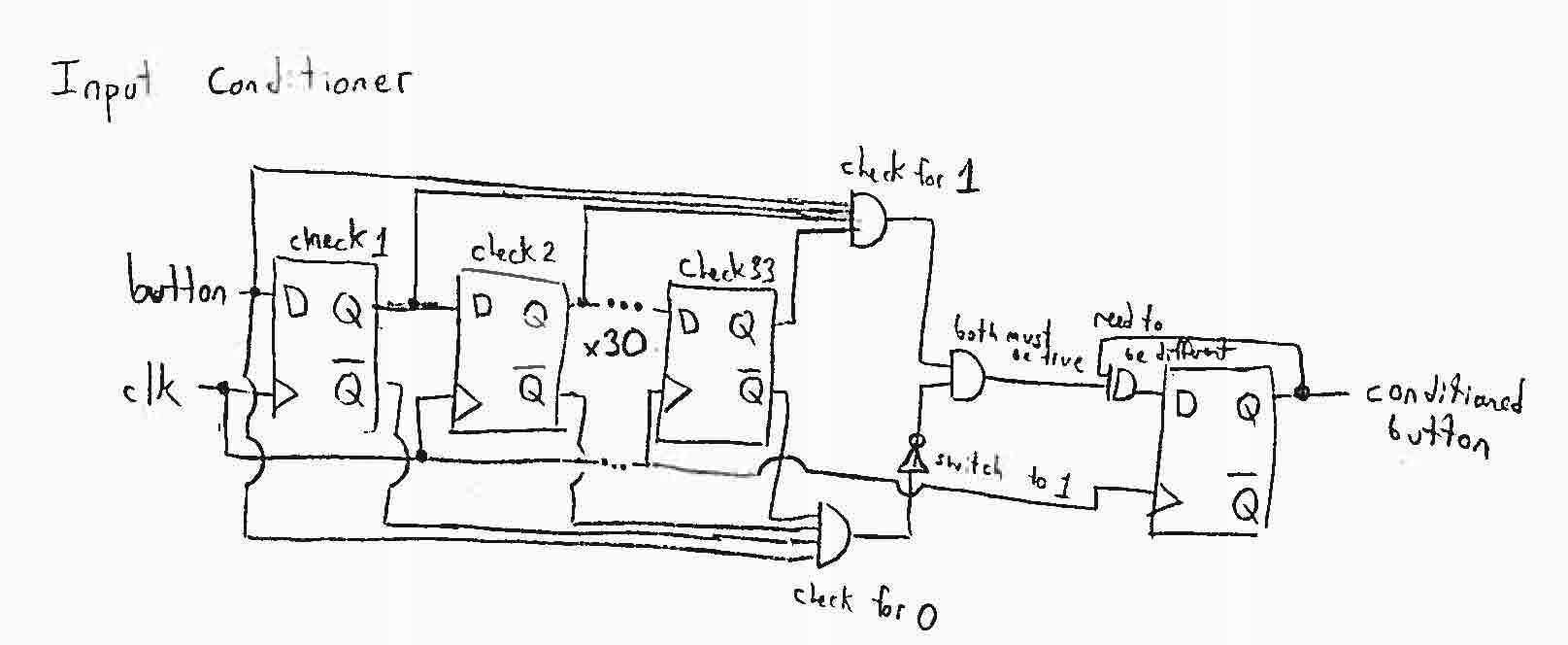
## Schematic:

### Input Conditioner:

Specification: Makes sure the button press is actually a button press and not just noise and only sends the signal once whenever the signal changes. To make sure the signal isn’t noise a series of 33 D Flip-flops are used and all the outputs are compared to make sure they are all the same and the signal has stabilized. This number was found by dividing the length of the suspected signal noise decay: .001 seconds by the amount of seconds in a clock cycle: .0000305 seconds.

Inputs: Button, CLK

Outputs: Conditioned Button

Schematic: 

Size:

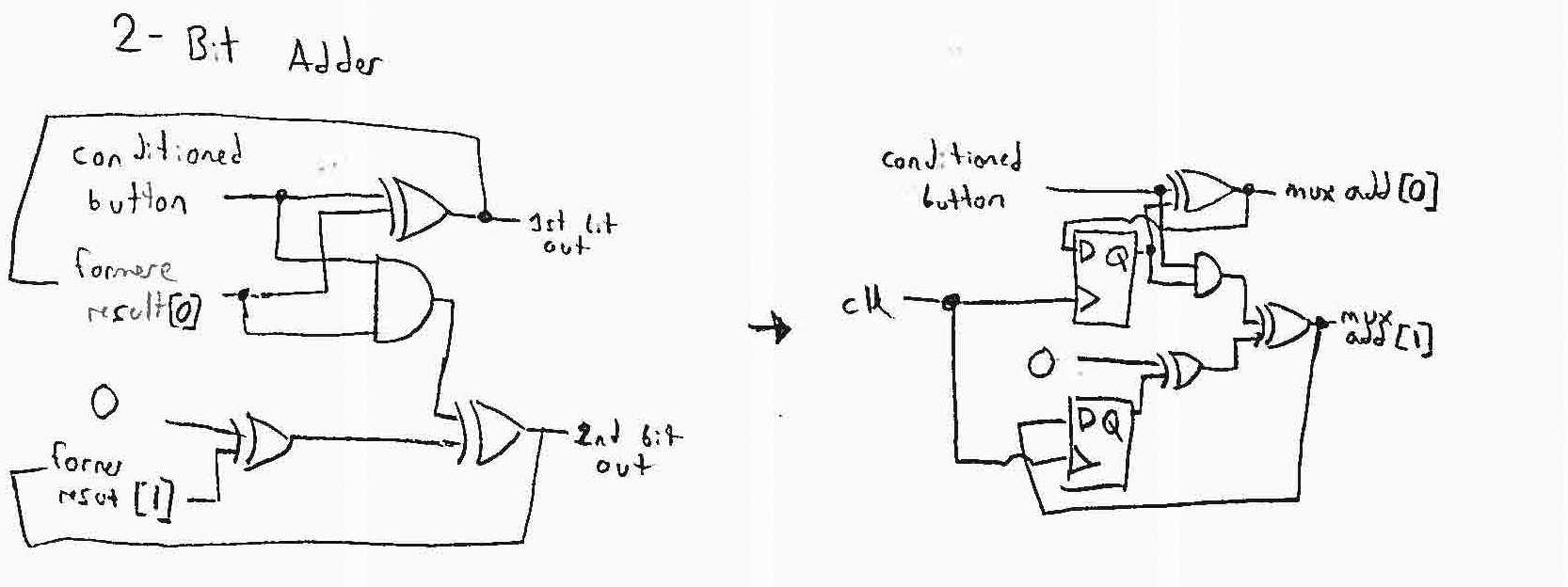
|  |  |  |  |
| --- | --- | --- | --- |
| Type | Number | Cost | Total |
| 4 Input AND | 2 | 5 | 10 |
| 2 Input AND | 1 | 3 | 3 |
| 2 Input NAND | 1 | 2 | 2 |
| Inverter | 1 | 1 | 1 |
| Edge Triggered DFF | 34 | 13 | 442 |
| TOTAL |  |  | 458 |

### 2-bit Adder

Specification: Creates the output used to address the MUX by having each press of the button add 1 to the current total. It does not deal with overflow for the second but and thus cycles through 0-3 continuously.

Inputs: Conditioned Button, CLK

Outputs: 2-bit Bus address for MUX

Schematic: 

Size:

|  |  |  |  |
| --- | --- | --- | --- |
| Type | Number | Cost | Total |
| 2 Input AND | 1 | 3 | 3 |
| 2 Input NOR | 3 | 2 | 6 |
| Edge Triggered DFF | 2 | 13 | 26 |
| TOTAL |  |  | 35 |

### Modes:

**On:**

Input: 1, Output: On Out for MUX

**Off:**

Input: 0, Output: Off Out for MUX

**Dim:**

Input: CLK, Output: Dim Out for MUX

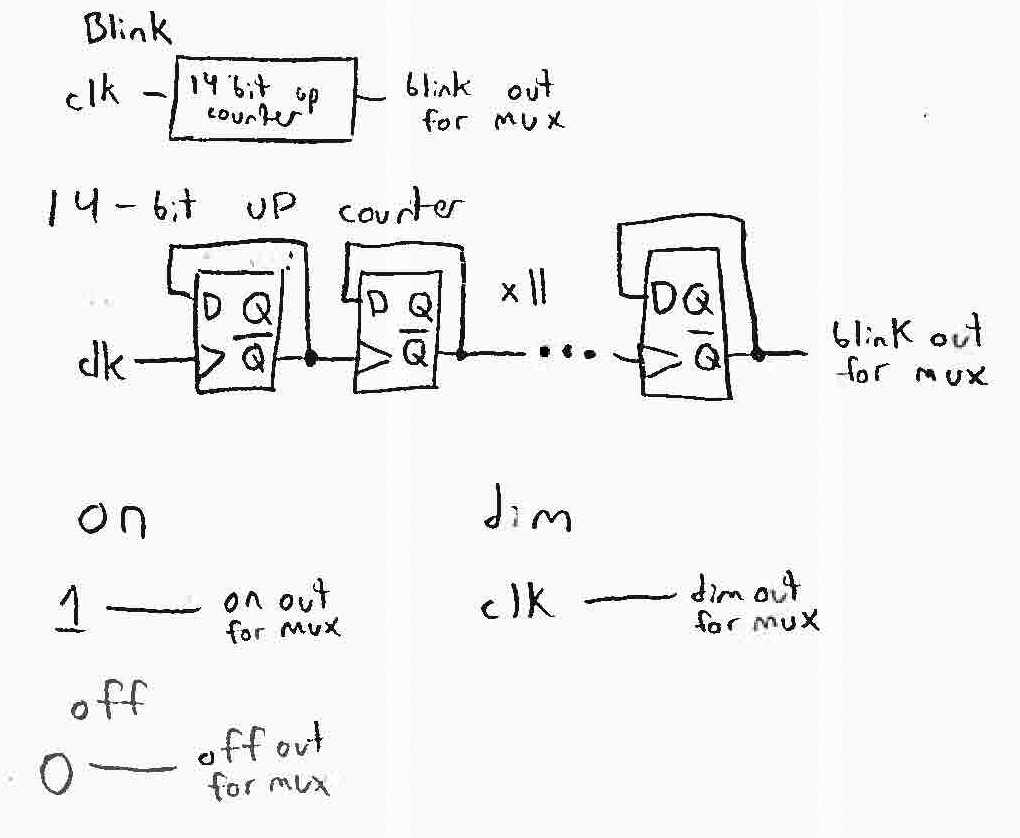
**Blink:**

Specification: Causes the LED to blink at a rate visible to the eye. In this example a blink rate of .5 seconds or 2Hz was chosen and so the original Hz of the clock: 32,768 was reduced to 2 Hz by dividing it in half 14 times using a 14-bit up counter out of 14 Ede-triggered D- Flip-flops.

Input: CLK, Output: Blink Out for MUX

Cost:

|  |  |  |  |
| --- | --- | --- | --- |
| Type | Number | Cost | Total |
| Edge Triggered DFF | 14 | 13 | 182 |

Schematic: 

## Cost Estimation:

|  |  |
| --- | --- |
| Component | Cost |
| Input Conditioner | 458 |
| 2-bit Adder | 35 |
| MUX | 23 |
| Blink | 182 |
| LED Driver | 211 |
| System Clock | 2 |
| TOTAL | 911 |

## Other resources used:

<http://www.circuitsgallery.com/2013/01/Binary-Up-Counter.html>

<http://www.edwardbosworth.com/CPSC2105/Lectures/Slides_05/Chapter_03/DecodersAndMux_files/image015.jpg>

<http://i.stack.imgur.com/TpBpr.gif>

<http://www.allaboutcircuits.com/textbook/digital/chpt-11/synchronous-counters/>

I also used work I did with my teammates during Lab 2 as I didn’t consider this assistance from others for this particular assignment

I did a lot of internet searching however the pages I ended up putting information into my work from are listed above.