Q5) Consider a memory organization in which cache & main memories are of size 1KB and 4GB respectively. Identify the tag, index & offset bits of the main memory address for the following

a) Fully associative cache organization

→ Cache block size = 64 bytes (Given in question)

For fully associative, the amount of cache lines are = $\frac{\text{Cache size}}{\text{Cache block size}}$

$= \frac{1\text{kB}}{64\text{ B}} = \frac{1024}{64} = 16$ cache lines

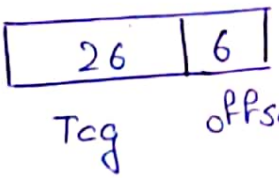
As there is only 1 set, no bits will be part of index but will go to offset, tag.

∴ 32 bit address with 6 bit offset:

offset : 6 bits

Tag : ~~22~~ 26 bits

Index : 0 bit



b) Directly mapped with cache line size of 64 bytes

→ Cache lines = $\frac{\text{Cache size}}{\text{Cache line size}}$ = 16 lines

For directly mapped, no of sets is equal to amount of cache lines.

∴ Amount of index bits required = $\log_2$ (amount of sets)

= $\log_2$ 16 bits

= 4 bits

offset = 6 bits

⇒ Tag bits = 32 - (offset + index)

= 22 bits

22	4	6
Tag	Idex	offset

c) 4-way set associative organization with cache line size 64 bytes

→ Cache is 4-way set associative

⇒ 4 sets

∴ Index = $\log_2 4 = 2$

∴ Tag = -(Offset + Index) + 32

= 24

24	2	6
Tag	Index	offset