CSO End Sem 2018113003

Q1)

→ SEQ+ is the reorganised sequential processor, to which adding pipeline registers making it PIPE. processor.

SEQ+	PIPE-
i) Only PC predicted & other is sequential & flows directly	ii) F, D, E, M, W registers are present as pipeline registers which contain last computed values
ii) There is single value for signals like valC, valE, at any point in time	ii) Each pipeline register has its own pipeline status signals.
iii) dstE & dstM are destination registers for valE & valM can be directly written to the register file	iii) The values & addresses need to be carried to write back stage before it is written & to ensure their addresses.
iv) Data block in SEQ+ takes data from valA or valP & feeds it to data memory	iv) A special block is present to compute E_valA from valP or choosing value from register file
v) SEQ+ does not have dependency hazards	v) PIPE- needs handles for dependency hazards