CSO End Sem 20R113003

Q43 Describe PC selection & Fetch logic in Y.86 PIPE processor architecture design

→ Fetch is the first process that starts the understanding of an instruction, and hence must select current value of program counter (to find the instruction) & also predict the next program counter.

There are hardware units that can read the instructions from memory & extract different instructional fields. They are the same as that for SEQ.

In Fetch instage reads the bytes from an instruction from memory, using PC. From the instruction it extracts the two 4-bit portions of instruction specified byte (icode) & (ifun). [icode → instruction code, ifun → instruction function] It also possibly fetches register specified byte (rA & rB) and also possibly 8 bit constant (val c). valP can also be computed which is the value of PC plus length of fetched instruction.

PC selection logic chooses between three program counter values. If a misplaced branch enters memory stage, the value of valP from this stage is read from pipeline register. If a ret instruction enters write back stage, the return address is read from pipeline register W. All other cases use predicted value stored in pipeline register F.