

DM74LS00 Quad 2-Input NAND Gate

General Description

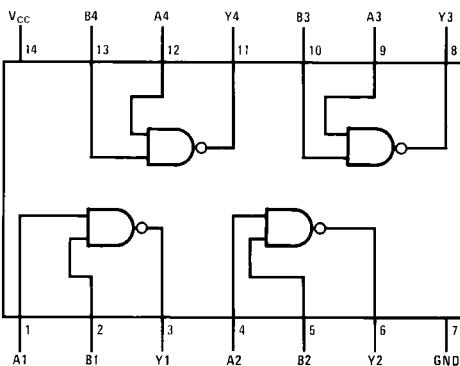
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

$$Y = \overline{AB}$$

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max		0.8	1.6	mA
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max		2.4	4.4	mA

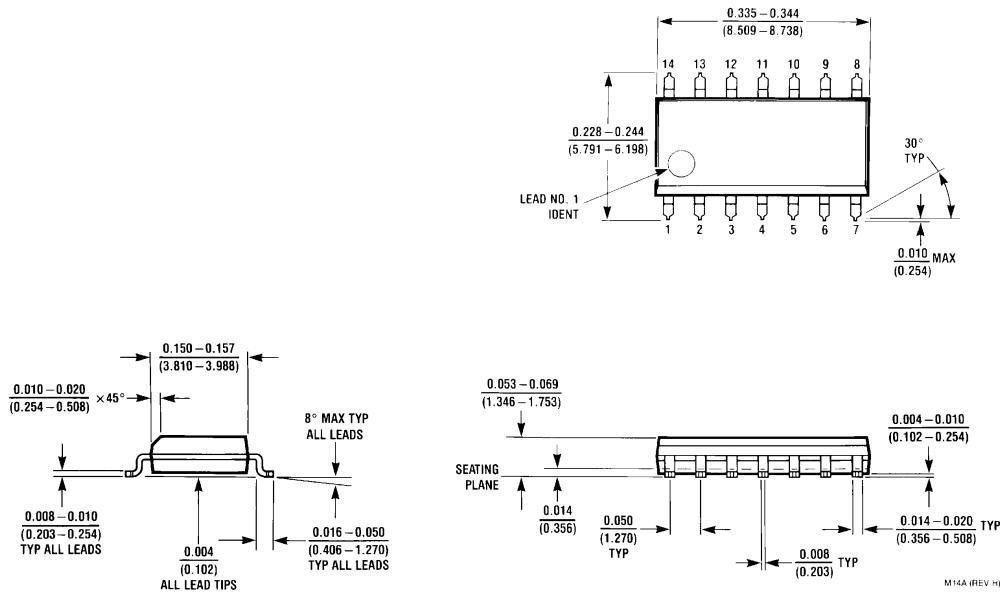
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

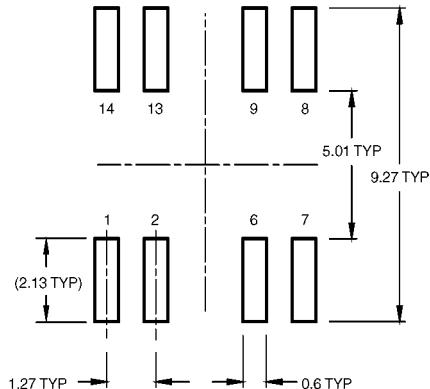
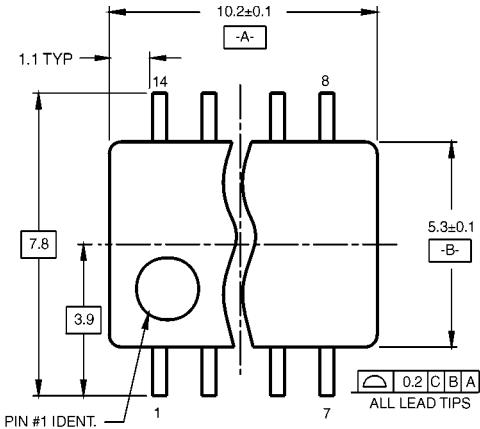
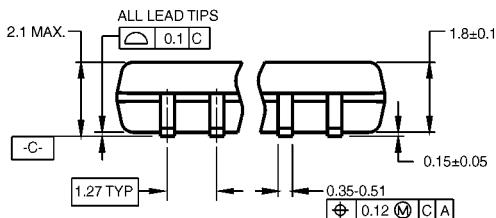
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R _L = 2 kΩ				Units	
		C _L = 15 pF		C _L = 50 pF			
		Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns	

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

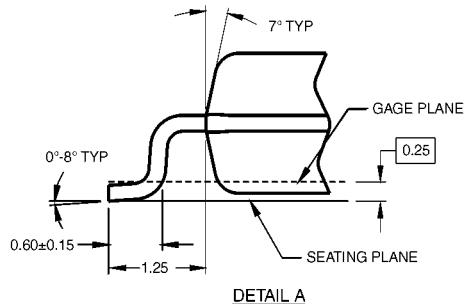
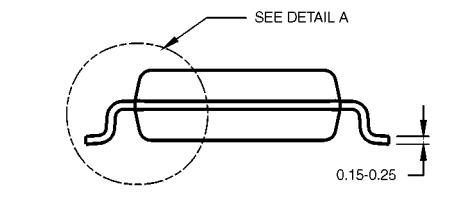
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

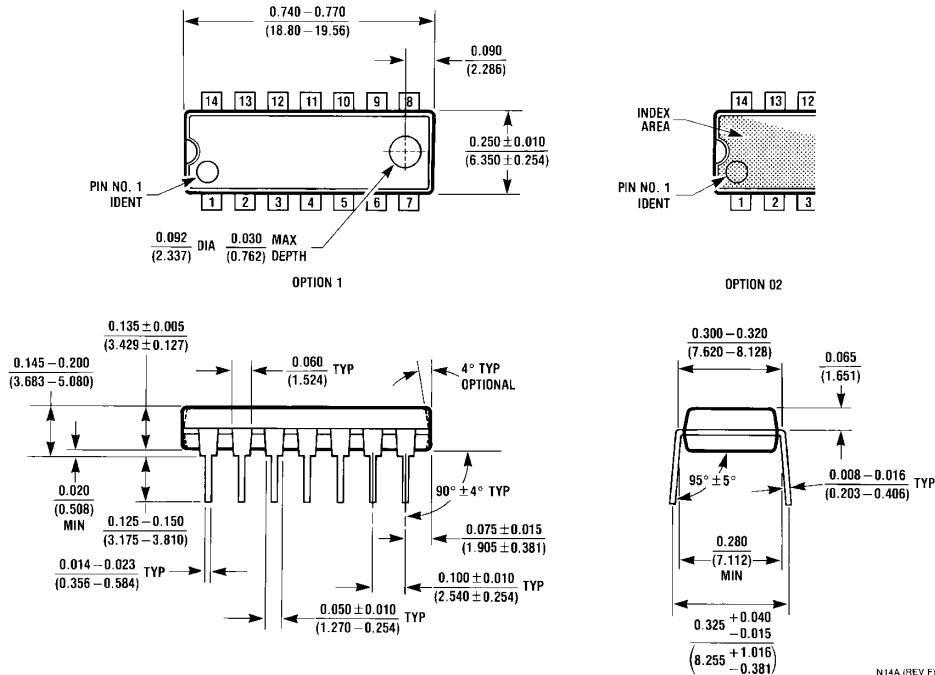
M14DRevB1



DETAIL A

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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DM74LS04 Hex Inverting Gates

General Description

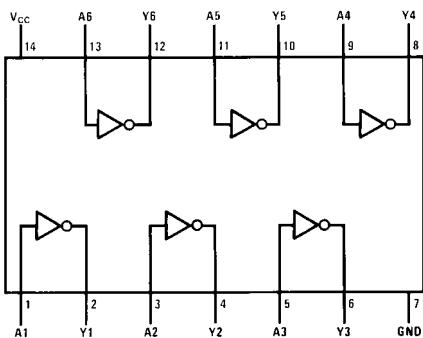
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \bar{A}$	
Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	µA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max		1.2	2.4	mA
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max		3.6	6.6	mA

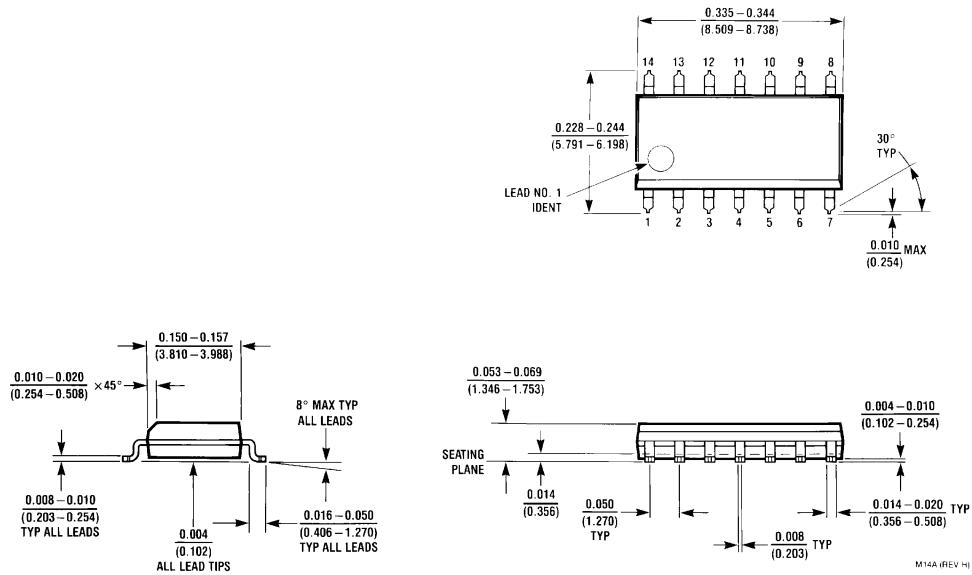
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

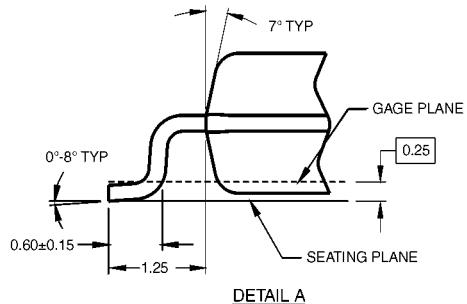
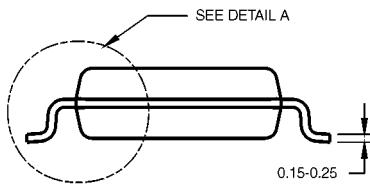
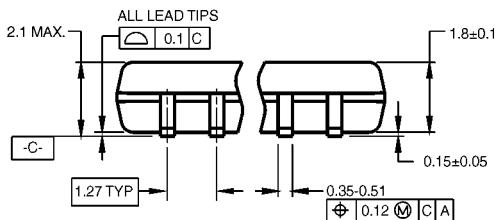
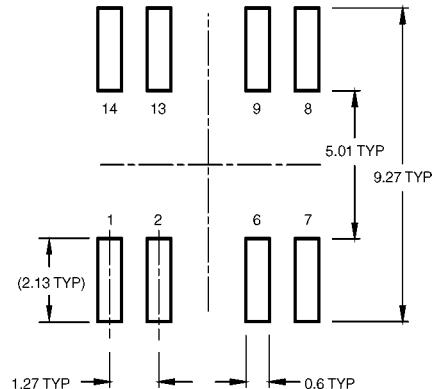
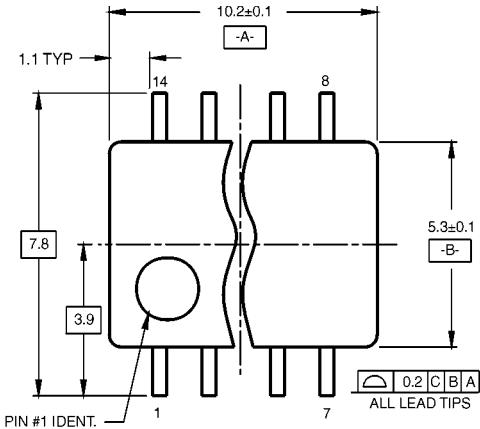
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R _L = 2 kΩ				Units	
		C _L = 15 pF		C _L = 50 pF			
		Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns	

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

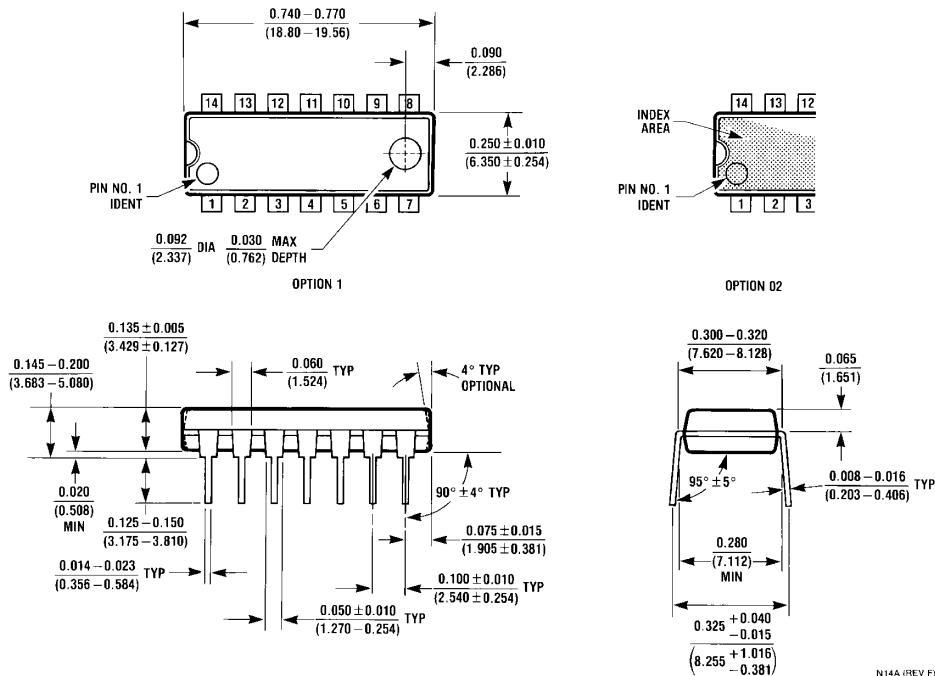
NOTES:

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- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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DM74LS08

Quad 2-Input AND Gates

General Description

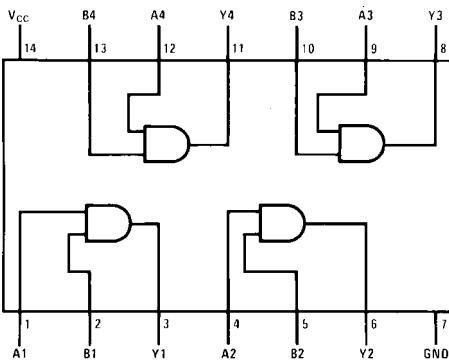
This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Y = AB		
Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IL} = Max		0.35	0.5	
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max		2.4	4.8	mA
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max		4.4	8.8	mA

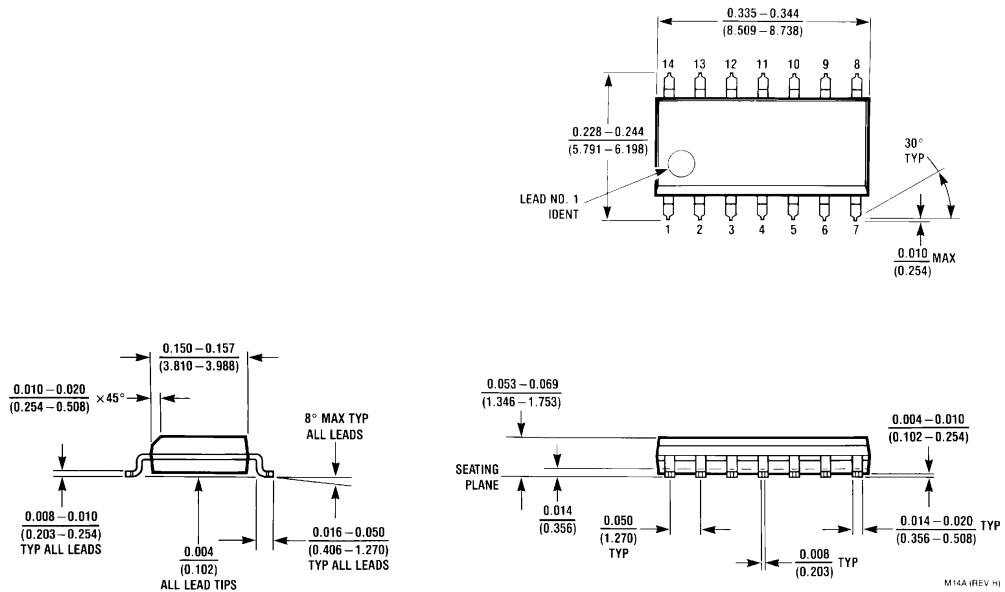
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

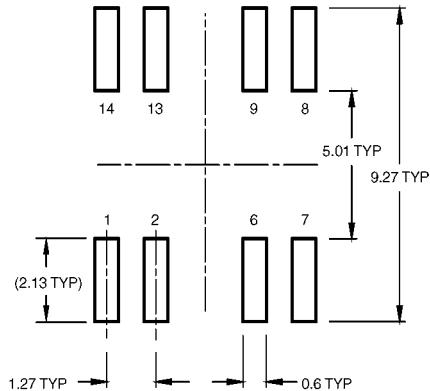
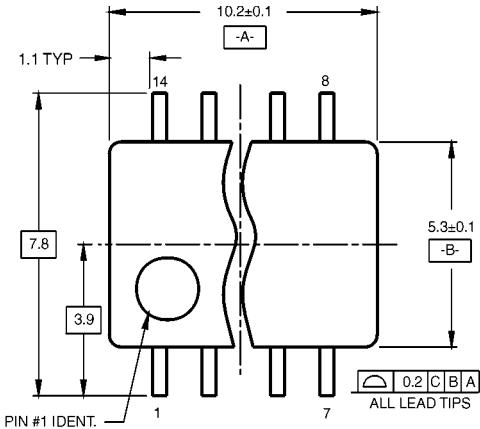
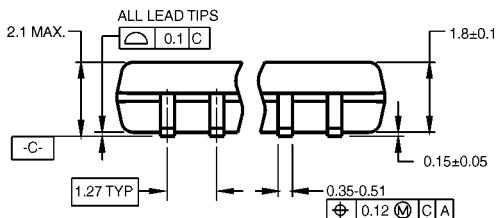
Symbol	Parameter	R _L = 2 kΩ				Units	
		C _L = 15 pF		C _L = 50 pF			
		Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

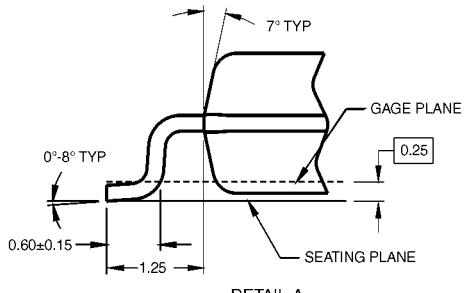
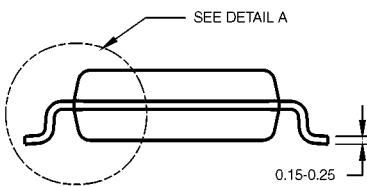
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS

DETAIL A

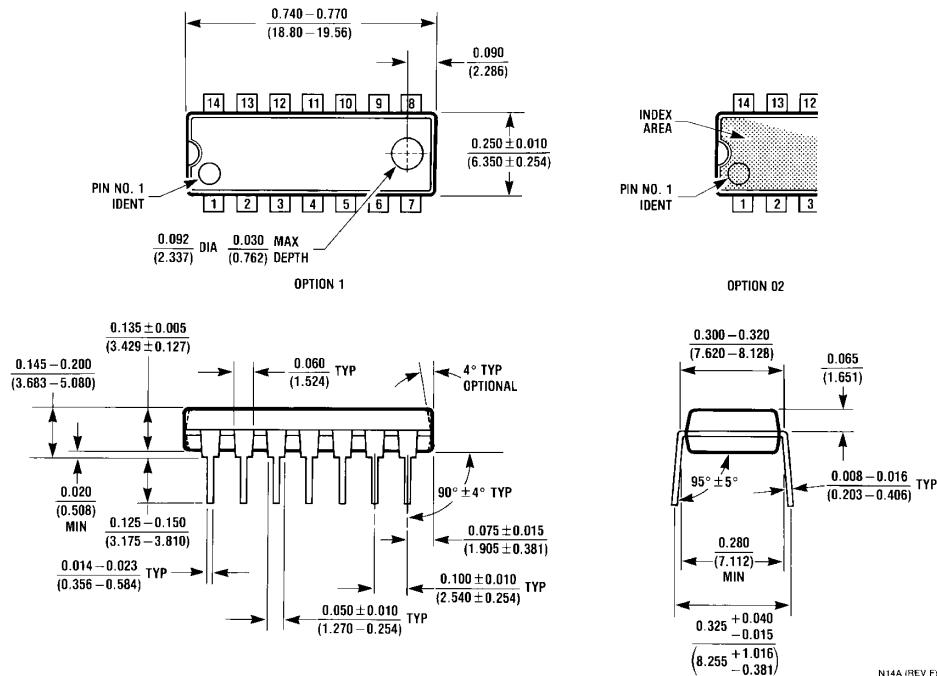
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M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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June 1986
Revised March 2000

DM74LS32

Quad 2-Input OR Gate

General Description

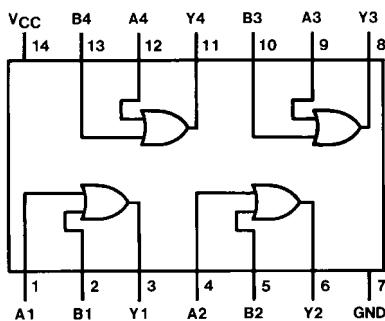
This device contains four independent gates each of which performs the logic OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS32N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = A + B$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IL} = Max		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max		3.1	6.2	mA
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max		4.9	9.8	mA

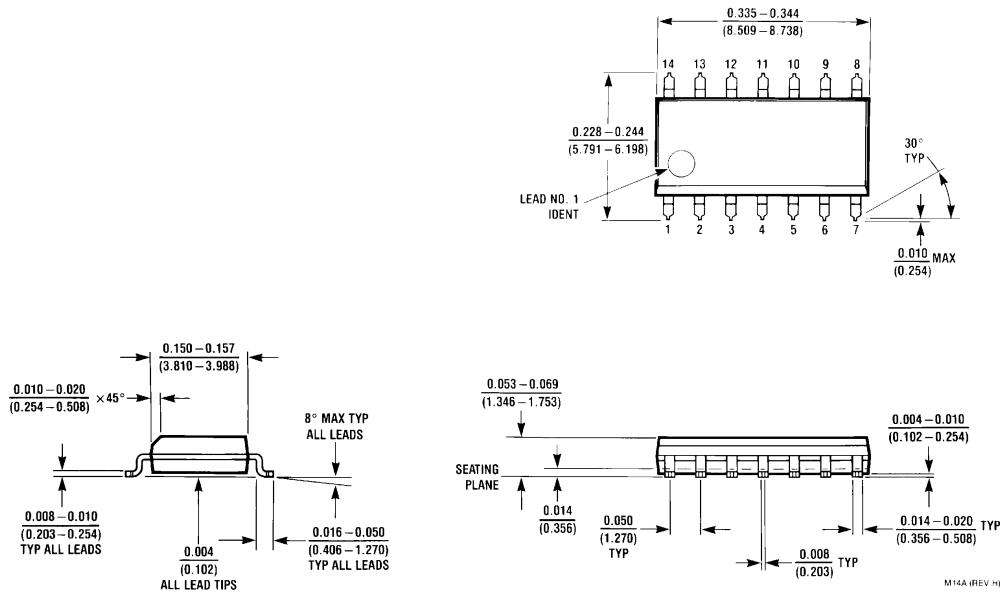
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

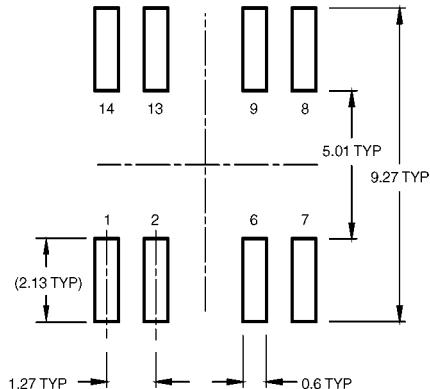
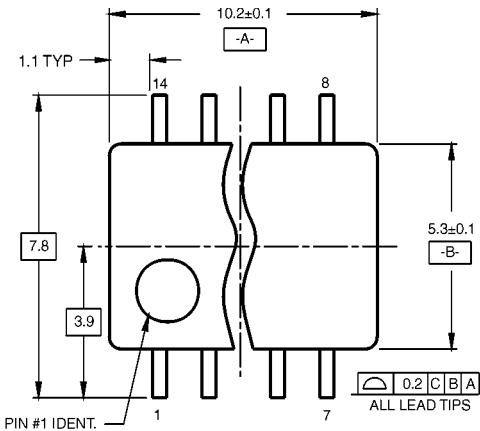
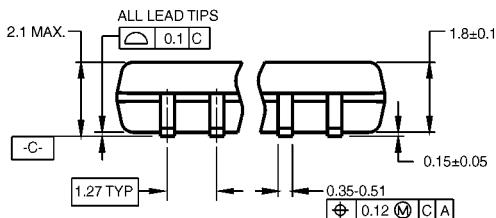
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

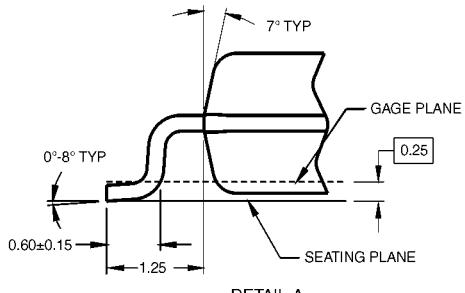
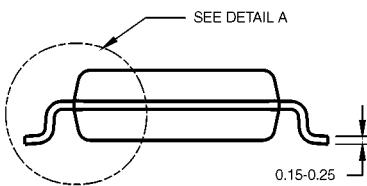
Symbol	Parameter	R _L = 2 kΩ				Units	
		C _L = 15 pF		C _L = 50 pF			
		Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns	

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS

DETAIL A

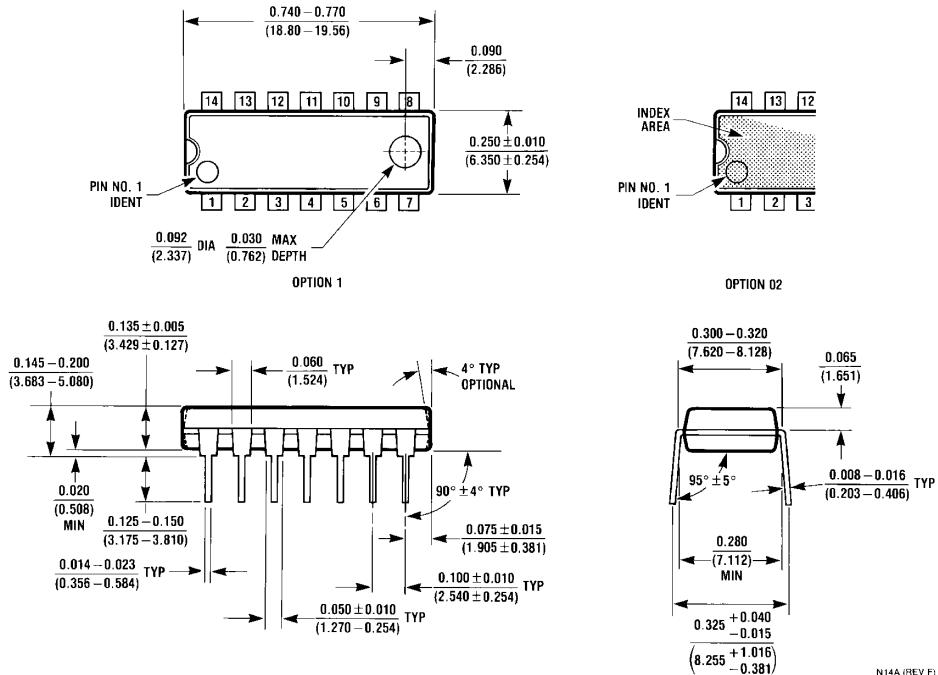
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

N14A (REV F)

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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SN74LS76A

Dual JK Flip-Flop with Set and Clear

The SN74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.



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LOW
POWER
SCHOTTKY

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{C}_D	J	K	Q	\bar{Q}
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	\bar{q}	q
Load "0" (Reset)	H	H	I	h	L	H
Load "1" (Set)	H	H	h	I	H	L
Hold	H	H	I	I	q	\bar{q}

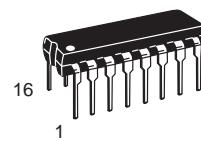
* Both outputs will be HIGH while both \bar{S}_D and \bar{C}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{C}_D go HIGH simultaneously.

H, h = HIGH Voltage Level

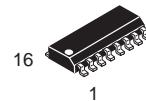
L, I = LOW Voltage Level

X = Immaterial

I, h (q) = Lower case letters indicate the state of the referenced input
(or output) one setup time prior to the HIGH-to-LOW clock transition



16
1
PLASTIC
N SUFFIX
CASE 648



16
1
SOIC
D SUFFIX
CASE 751B

GUARANTEED OPERATING RANGES

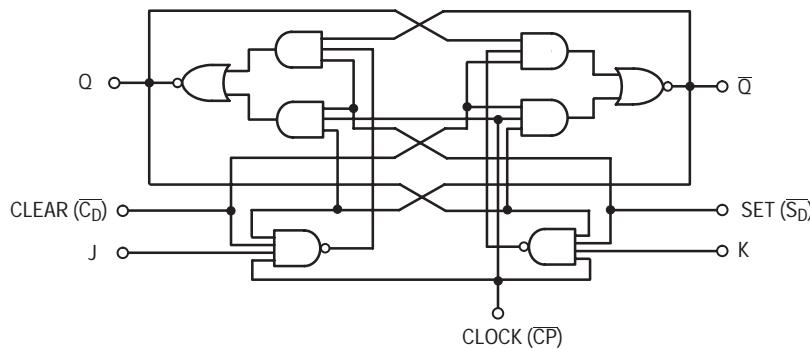
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			-0.4	mA
I_{OL}	Output Current – Low			8.0	mA

ORDERING INFORMATION

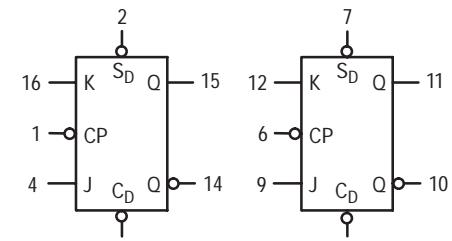
Device	Package	Shipping
SN74LS76AN	16 Pin DIP	2000 Units/Box
SN74LS76AD	16 Pin	2500/Tape & Reel

SN74LS76A

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = PIN 5
GND = PIN 13

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current	J, K Clear Clock		20 60 80	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
		J, K Clear Clock		0.1 0.3 0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current	J, K Clear, Clock		-0.4 -0.8	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)		-20		mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			6.0	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	30	45		MHz	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		15	20	ns	
			15	20	ns	

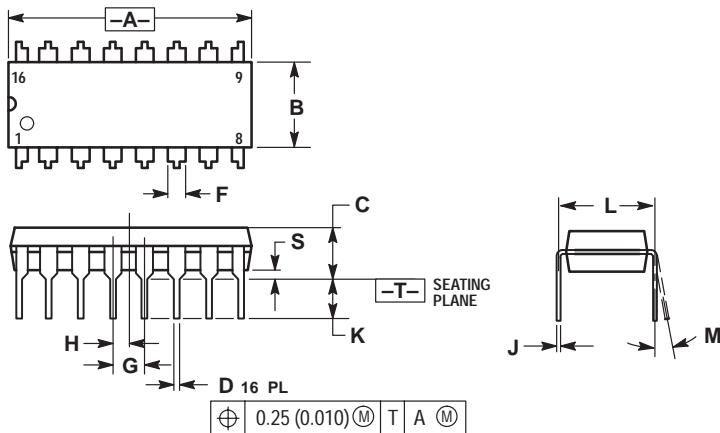
AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width High	20			ns	$V_{CC} = 5.0 \text{ V}$
t_W	Clear Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

SN74LS76A

PACKAGE DIMENSIONS

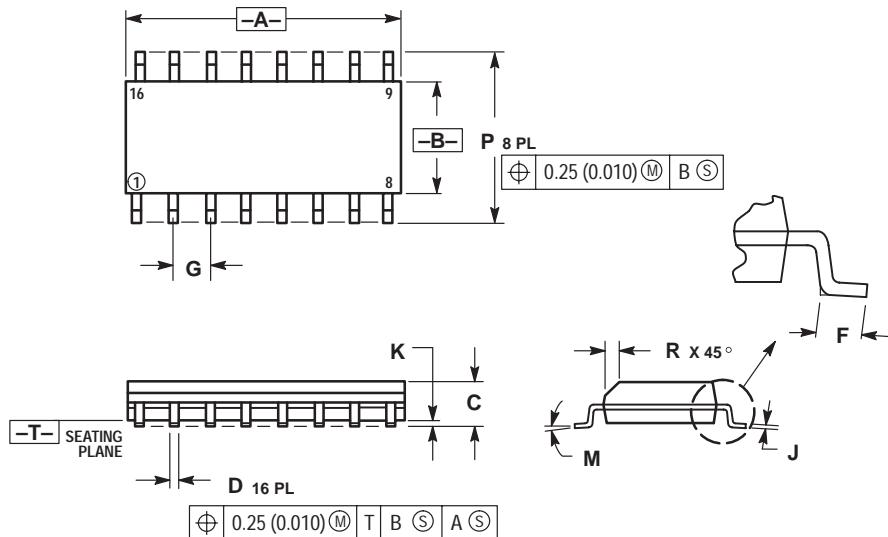
N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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DM74LS85 4-Bit Magnitude Comparator

General Description

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

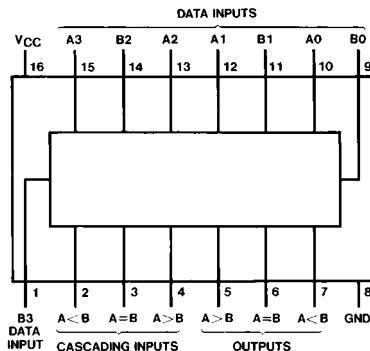
- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns

Ordering Code:

Order Number	Package Number	Package Description
DM74LS85M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS85N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

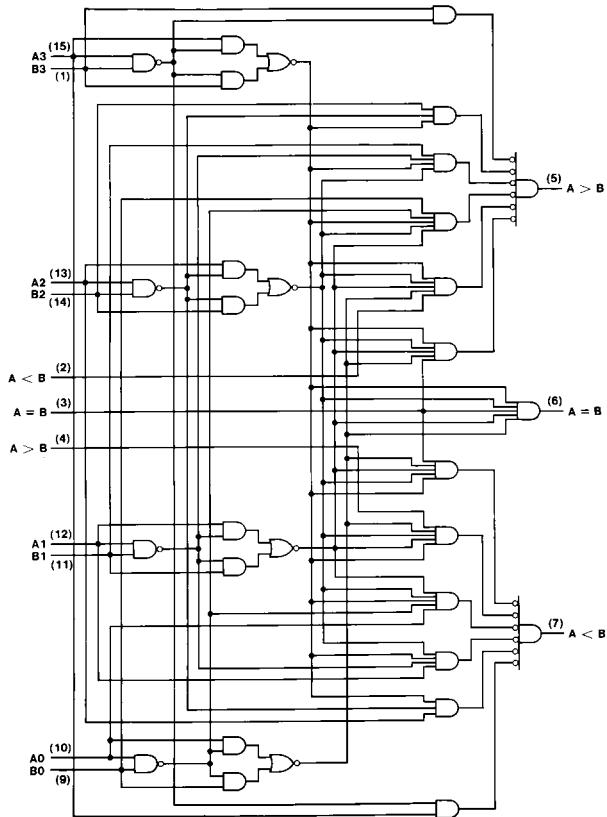
Connection Diagram



Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = HIGH Level, L = LOW Level, X = Don't Care

Logic Diagram

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ $I_{OL} = 4 \text{ mA}$, $V_{CC} = \text{Min}$		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7V$	A < B A > B Others	0.1 0.1 0.3		mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7V$	A < B A > B Others	20 20 60		μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4V$	A < B A > B Others	-0.4 -0.4 -1.2		mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	-20		-100	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 4)		10	20	mA

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$.

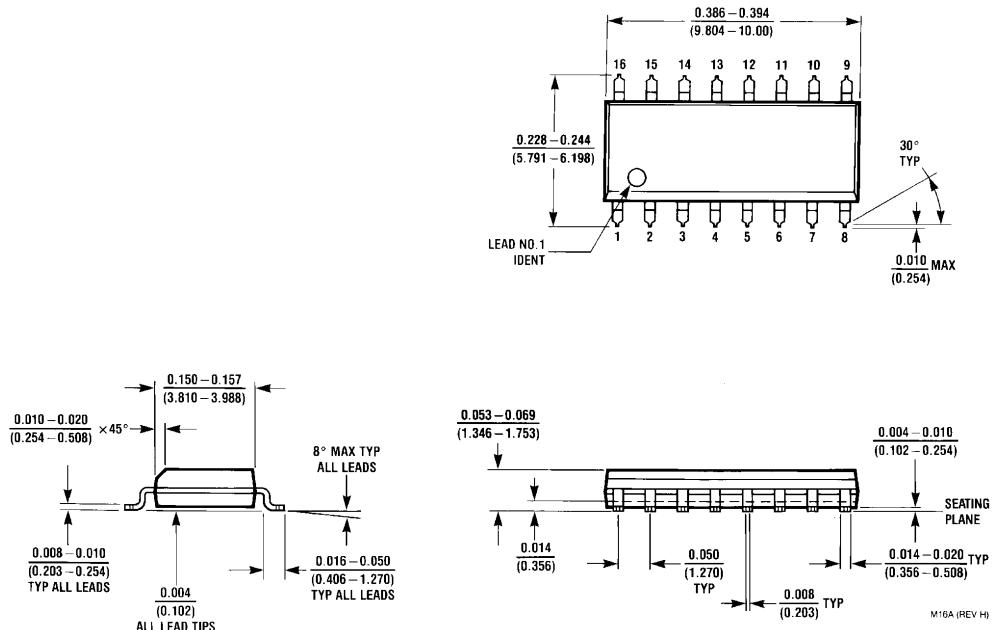
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs OPEN, A = B grounded and all other inputs at 4.5V.

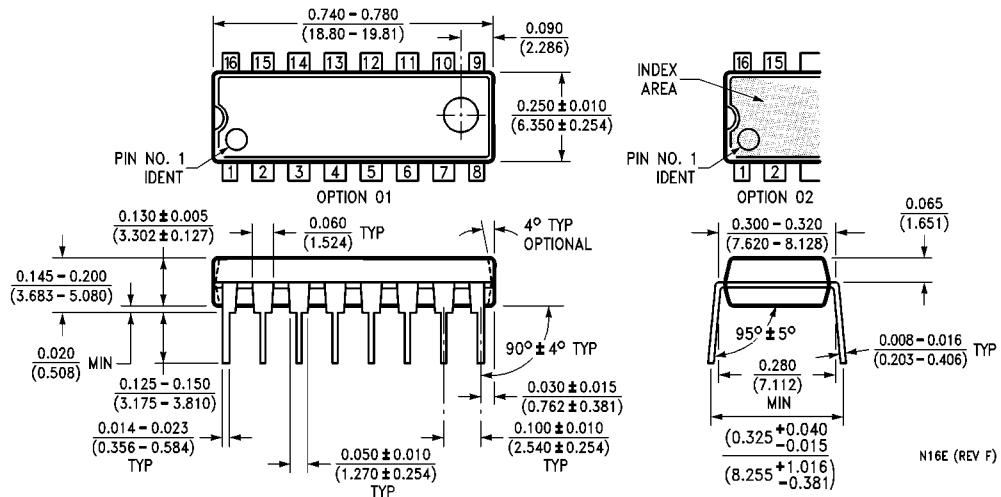
Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

Symbol	Parameter	From Input	To Output	Number of Gate Levels	$R_L = 2 \text{ k}\Omega$				Units	
					$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$			
					Min	Max	Min	Max		
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Any A or B Data Input	A < B, A > B	3		36		42	ns	
			A = B	4		40		40		
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Any A or B Data Input	A < B, A > B	3		30		40	ns	
			A = B	4		30		40		
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	A < B or A = B	A > B	1		22		26	ns	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	A < B or A = B	A > B	1		17		26	ns	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	A = B	A = B	2		20		25	ns	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	A = B	A = B	2		17		26	ns	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	A > B or A = B	A < B	1		22		26	ns	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	A > B or A = B	A < B	1		17		26	ns	

Physical Dimensions inches (millimeters) unless otherwise noted

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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DM74LS86

Quad 2-Input Exclusive-OR Gate

General Description

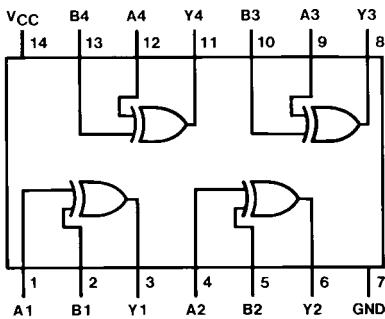
This device contains four independent gates each of which performs the logic exclusive-OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS86SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS86N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IL} = Max, V _{IH} = Min		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.2	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			40	µA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.6	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max (Note 4)		6.1	10	mA
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max (Note 5)		9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

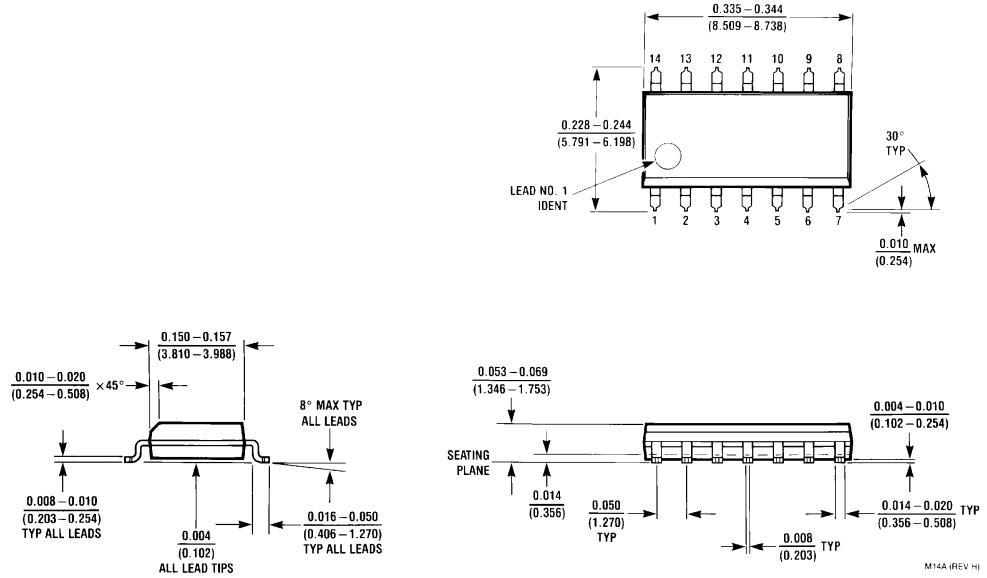
Note 4: I_{CCH} is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

Note 5: I_{CCL} is measured with all outputs OPEN and all inputs grounded.

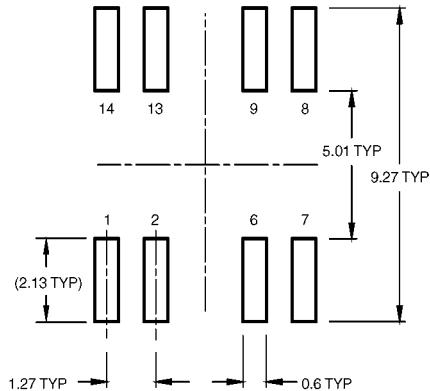
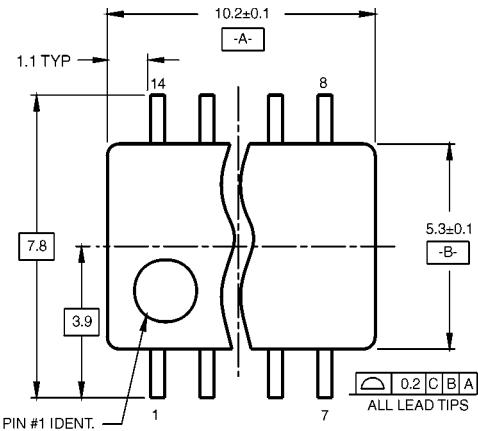
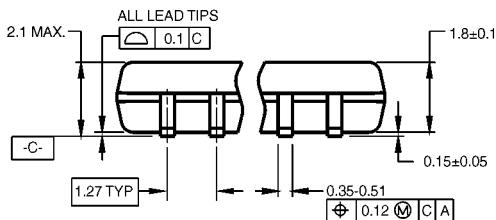
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

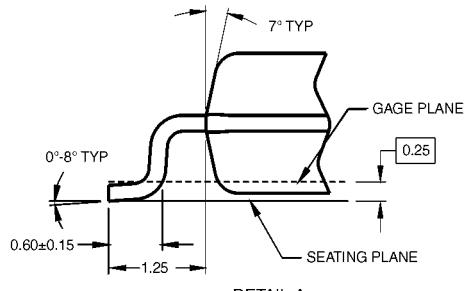
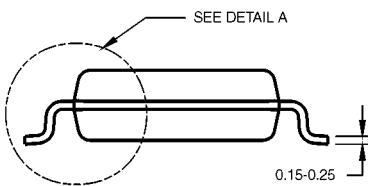
Symbol	Parameter	Conditions	R _L = 2 kΩ				Units	
			C _L = 15 pF		C _L = 50 pF			
			Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input Low		18		23	ns	
	Propagation Delay Time HIGH-to-LOW Level Output			17		21	ns	
t _{PHL}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input High		10		15	ns	
	Propagation Delay Time HIGH-to-LOW Level Output			12		15	ns	

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS

DETAIL A

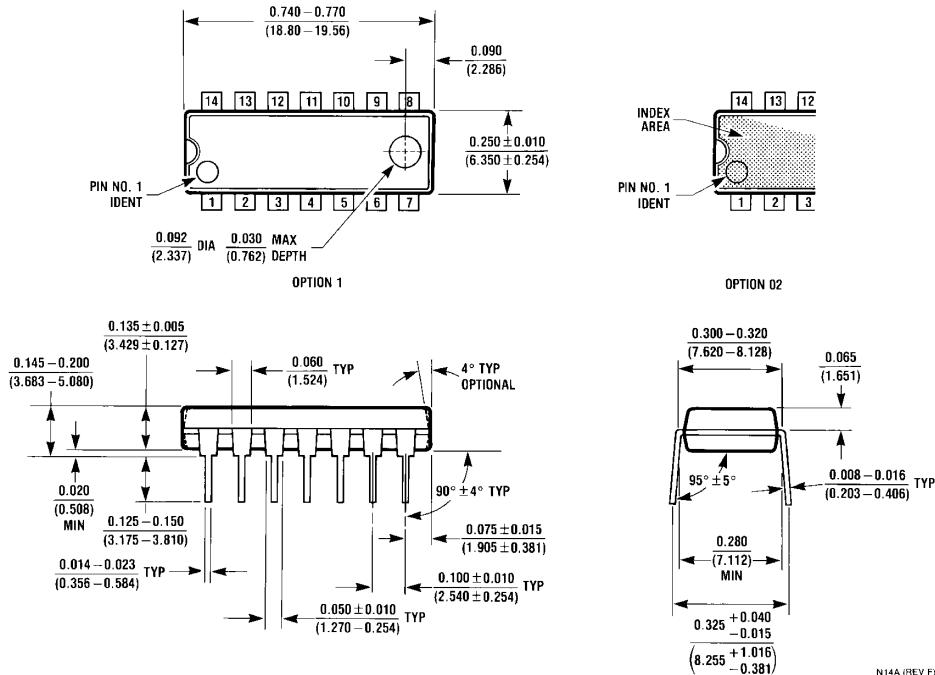
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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DM74LS126A

Quad 3-STATE Buffer

General Description

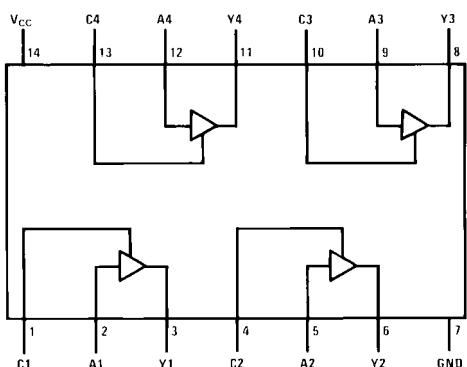
This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned OFF presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS126AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS126AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs		Output
A	C	Y
L	H	L
H	H	H
X	L	Hi-Z

H = HIGH Logic Level
 L = LOW Logic Level
 X = Either LOW or HIGH Logic Level
 Hi-Z = 3-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage				V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-2.6	mA
I _{OL}	LOW Level Output Current			24	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IH} = Min	2.4			V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min I _{OL} = 12 mA, V _{CC} = Min		0.35 0.25	0.5 0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OZH}	Off-State Output Current with HIGH Level Output Voltage Applied	V _{CC} = Max, V _O = 2.4V V _{IH} = Min, V _{IL} = Max			20	μA
I _{OZL}	Off-State Output Current with LOW Level Output Voltage Applied	V _{CC} = Max, V _O = 0.4V V _{IH} = Min, V _{IL} = Max			-20	μA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max		12	22	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

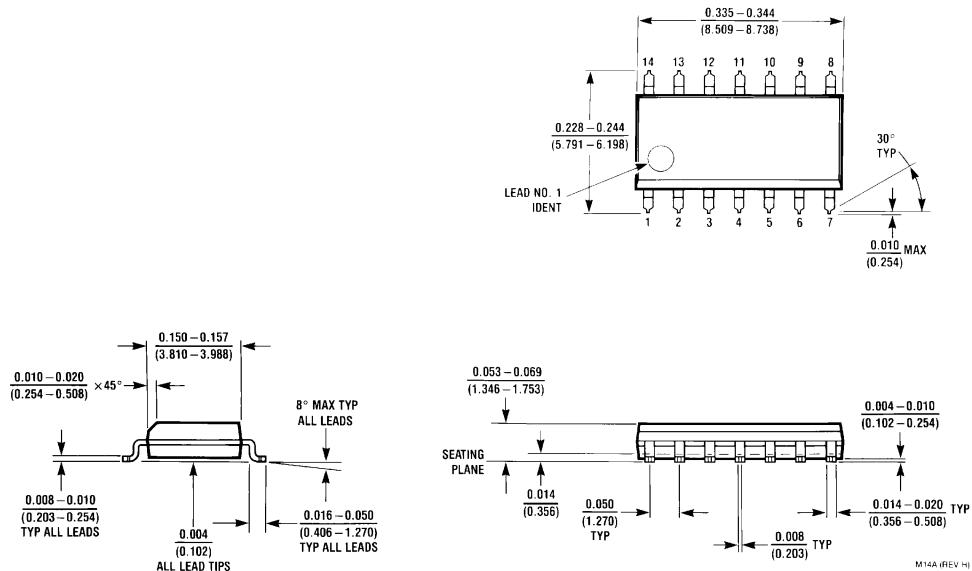
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

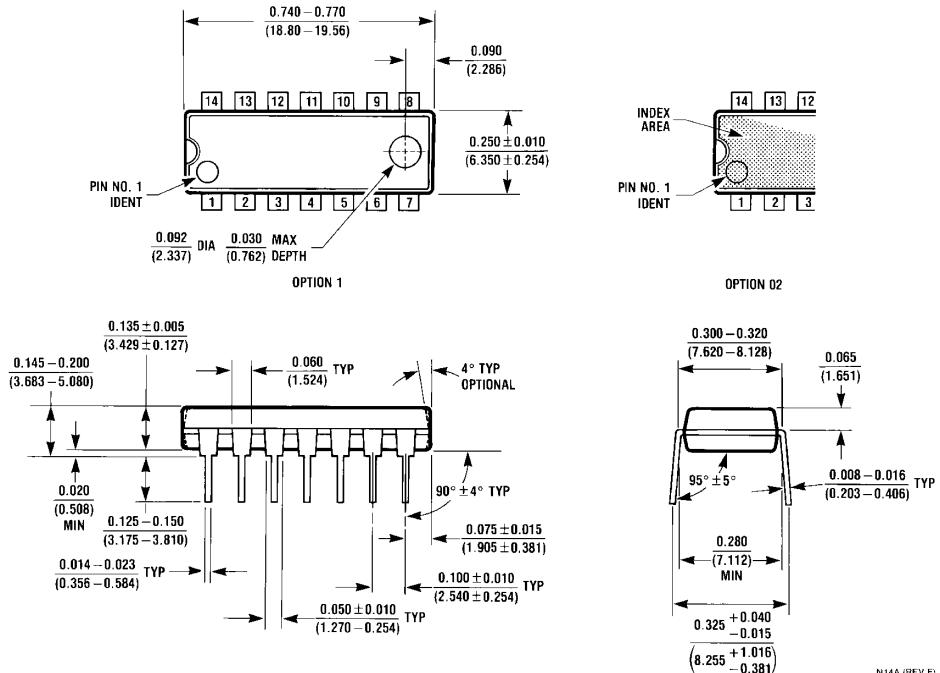
V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	R _L = 667Ω				Units	
		C _L = 50 pF		C _L = 150 pF			
		Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		15		21	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		18		22	ns	
t _{PZH}	Output Enable Time to HIGH Level Output		30		36	ns	
t _{PZL}	Output Enable Time to LOW Level Output		30		42	ns	
t _{PHZ}	Output Disable Time from HIGH Level Output (Note 4)		25			ns	
t _{PLZ}	Output Disable Time from LOW Level Output (Note 4)		25			ns	

Note 4: C_L = 5pF.

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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August 1986
Revised March 2000

DM74LS138 • DM74LS139 Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
 - Memory decoders
 - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
 - DM74LS138 21 ns
 - DM74LS139 21 ns
- Typical power dissipation
 - DM74LS138 32 mW
 - DM74LS139 34 mW

Ordering Code:

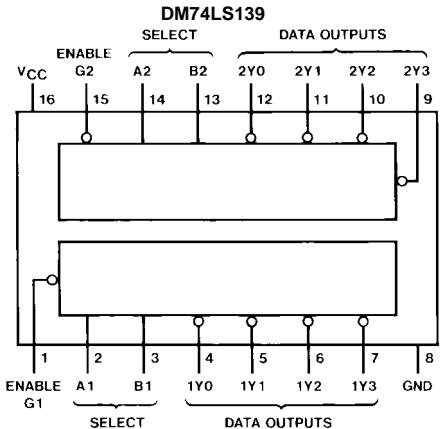
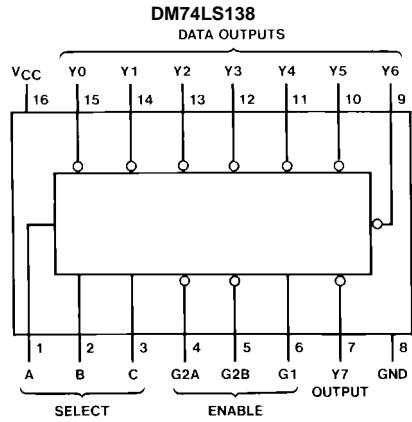
Order Number	Package Number	Package Description
DM74LS138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS139M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS139SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS139N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

DM74LS138 • DM74LS139 Decoder/Demultiplexer

DM74LS138 • DM74LS139

Connection Diagrams



Function Tables

DM74LS138

Inputs		Outputs											
Enable	Select	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	
X	H	X	X	X	H	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	L

DM74LS139

Inputs		Outputs						
Enable	Select	G	B	A	Y ₀	Y ₁	Y ₂	Y ₃
H	X	X	X	X	H	H	H	H
L	L	L	L	L	L	H	H	H
L	L	H	H	H	L	H	H	H
L	H	L	H	H	H	L	H	H
L	H	H	H	H	H	H	L	H

H = HIGH Level

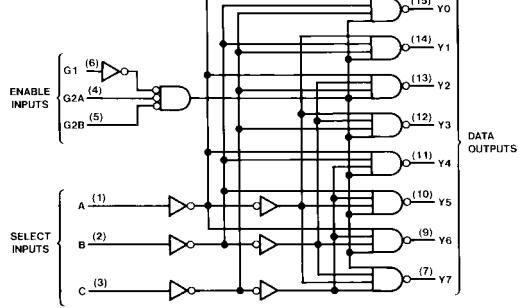
L = LOW Level

X = Don't Care

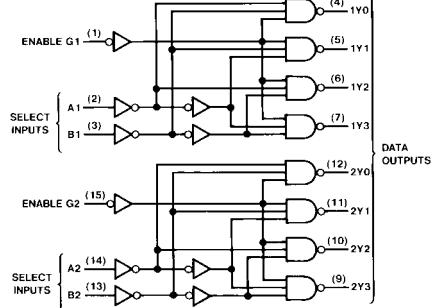
Note 1: G₂ = G_{2A} + G_{2B}

Logic Diagrams

DM74LS138



DM74LS139



Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS138 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

DM74LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IL} = Max, V _{IH} = Min		0.35	0.5	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 4)	-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 5)		6.3	10	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R _L = 2 kΩ		Units	
				C _L = 15 pF			
				Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	2		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	2		27		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	3		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	3		27		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	2		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	2		24		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	3		18		
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	3		28		

DM74LS139 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

DM74LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	µA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 7)	-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 8)		6.8	11	mA

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

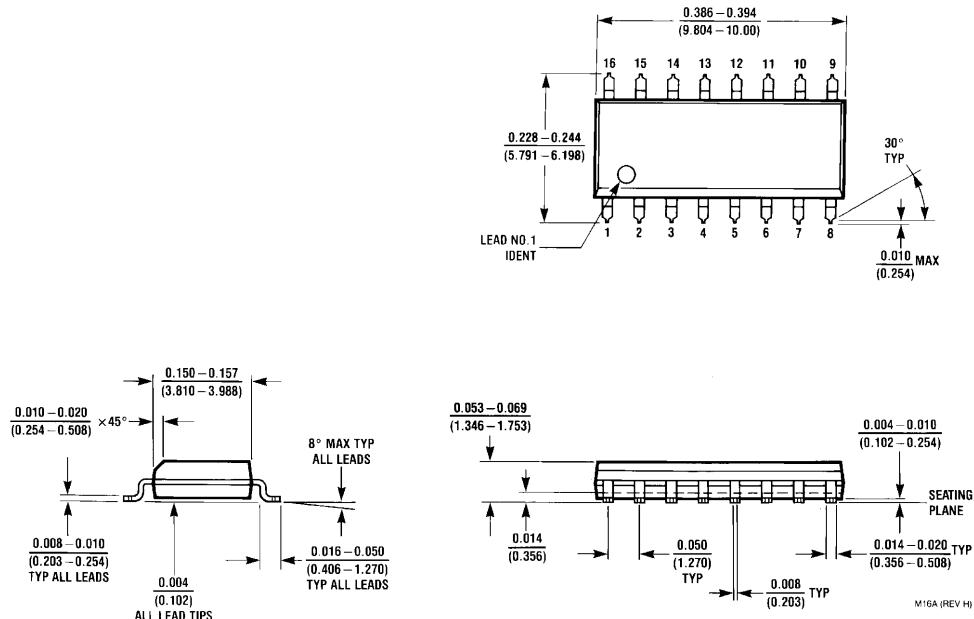
Note 8: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R _L = 2 kΩ				Units	
			C _L = 15 pF		C _L = 50 pF			
			Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output		18		27	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output		27		40	ns	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output		18		27	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output		24		40	ns	

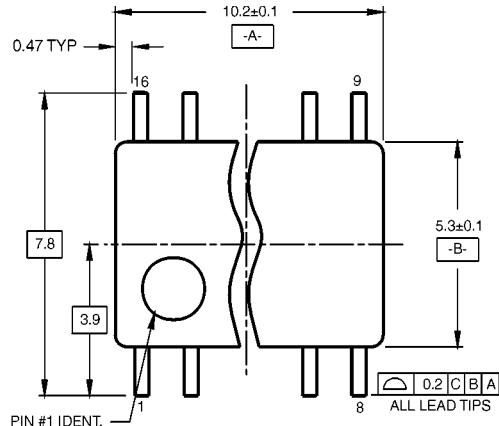
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

DM74LS138 • DM74LS139

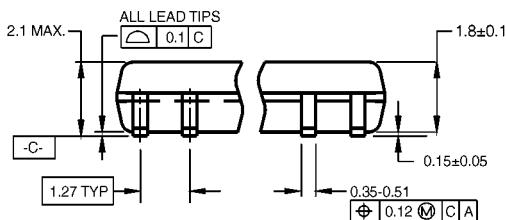
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



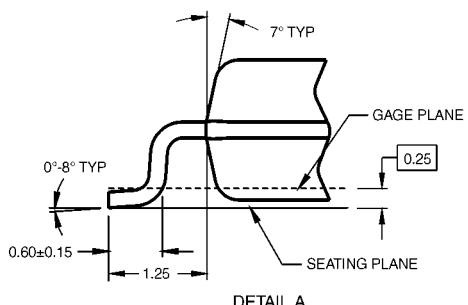
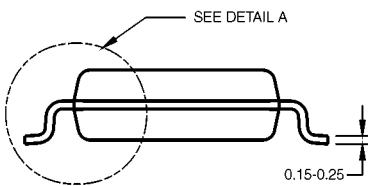
The diagram illustrates the layout of 16 components on a board. The center of the board is marked with a dashed horizontal line. Components are positioned on both sides of this center line. The components and their distances from the center are:

- Component 16 is located 1.27 TYP on the left side.
- Component 15 is located 2.13 TYP on the left side.
- Components 10 and 9 are located 5.01 TYP on the right side.
- Components 7 and 8 are located 9.27 TYP on the right side.
- Components 1 and 2 are located 1.27 TYP on the left side.
- Components 3 and 4 are located 2.13 TYP on the left side.
- Components 5 and 6 are located 5.01 TYP on the right side.
- Components 11 and 12 are located 9.27 TYP on the right side.
- Components 13 and 14 are located 1.27 TYP on the right side.

LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



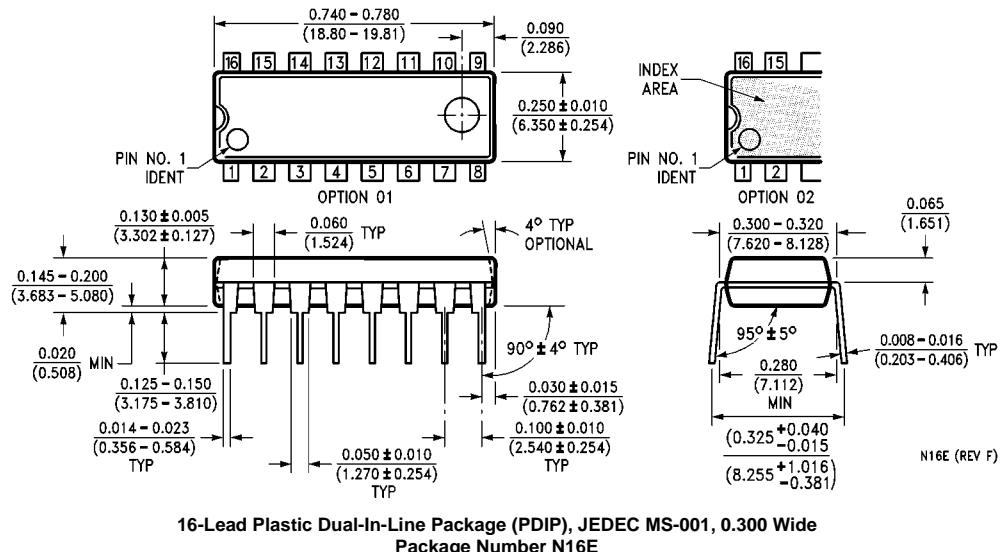
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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DM74LS153

Dual 1-of-4 Line Data Selectors/Multiplexers

General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

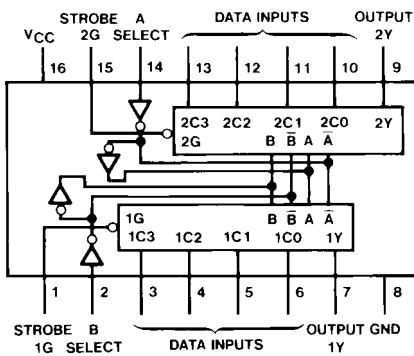
- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
 - From data 14 ns
 - From strobe 19 ns
 - From select 22 ns
- Typical power dissipation 31 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS153M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS153N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

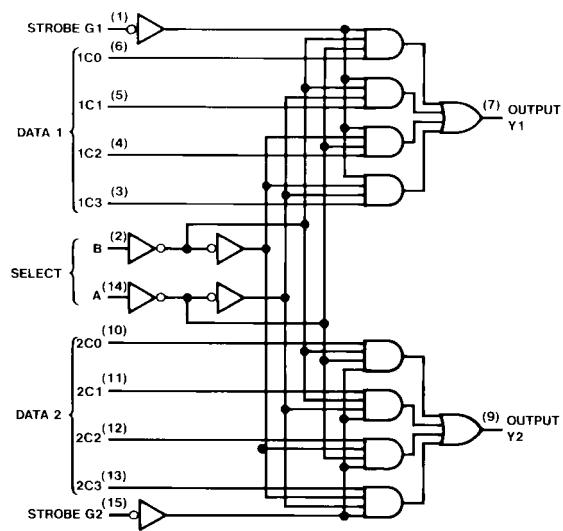
Select inputs A and B are common to both sections.

H = HIGH Level

L = LOW Level

X = Don't Care

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IL} = Max, V _{IH} = Min I _{OL} = 4 mA, V _{CC} = Min		0.35	0.5	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 4)		6.2	10	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs OPEN and all other inputs GROUNDED.

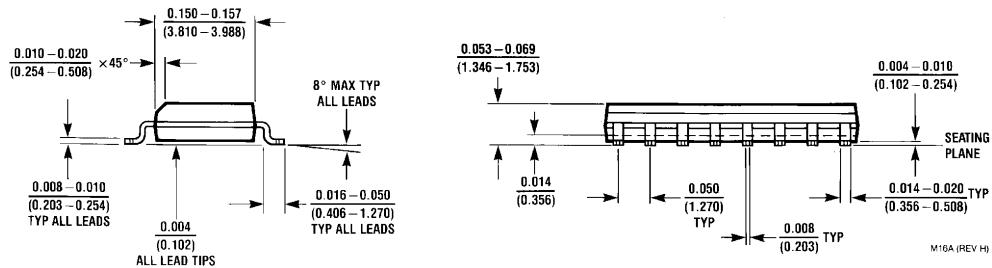
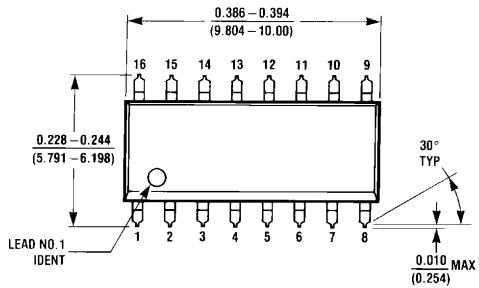
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) to (Output)	R _L = 2 kΩ				Units	
			C _L = 15 pF		C _L = 50 pF			
			Min	Max	Min	Max		
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Data to Y		15		20	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Data to Y		26		35	ns	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Y		29		35	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Y		38		45	ns	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Strobe to Y		24		30	ns	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Strobe to Y		32		40	ns	

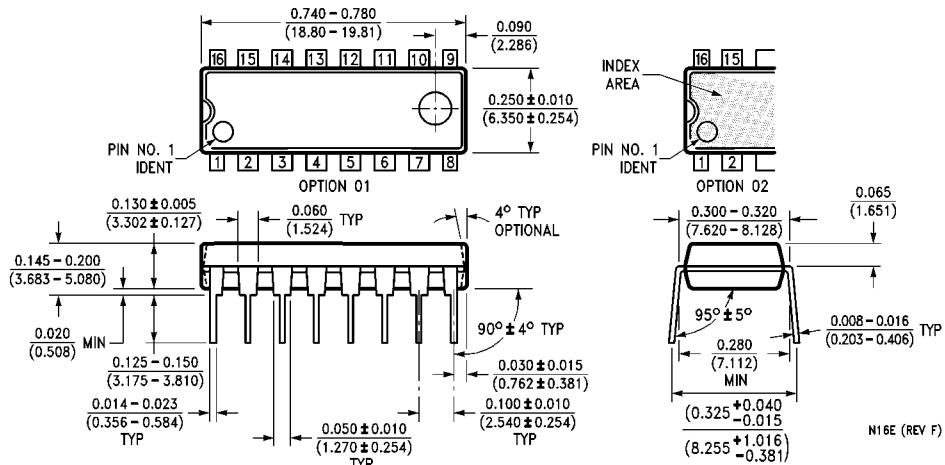
DM74LS153

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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SDLS058

**SN54157, SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158**
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

MARCH 1974 — REVISED MARCH 1988

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION	SN54157, SN54LS157, SN54S157, SN54LS158, SN54S158 . . . J OR W PACKAGE SN74157 . . . N PACKAGE SN74LS157, SN74S157, SN74LS158, SN74S158 . . . D OR N PACKAGE
	(TOP VIEW)		
'157	9 ns	150 mW	A/B 1 16 VCC
'LS157	9 ns	49 mW	1A 2 15 G
'S157	5 ns	250 mW	1B 3 14 4A
'LS158	7 ns	24 mW	1Y 4 13 4B
'S158	4 ns	195 mW	2A 5 12 4Y
			2B 6 11 3A
			2Y 7 10 3B
			GND 8 9 3Y

applications

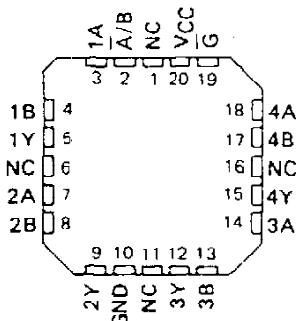
- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables
(One Variable Is Common)
- Source Programmable Counters

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

SN54LS157, SN54S157, SN54LS158,
SN54S158 . . . FK PACKAGE

(TOP VIEW)



NC = No internal connection

FUNCTION TABLE

INPUTS			OUTPUT Y		
STROBE G	SELECT A/B	A	B	'157, 'LS157, 'S157	'LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (See Note 1)	7 V
Input voltage: '157, 'S158	5.5 V
'LS157, 'LS158	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

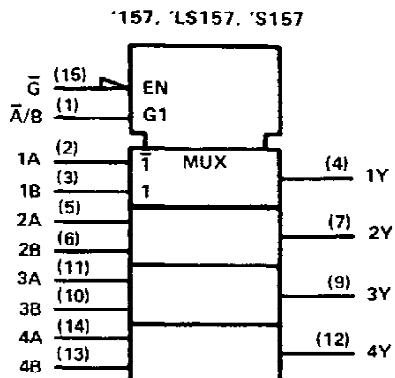
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

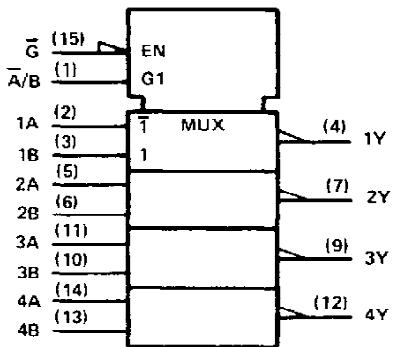
POST OFFICE BOX 5012 - DALLAS, TEXAS 75222

**SN54157, SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158**
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

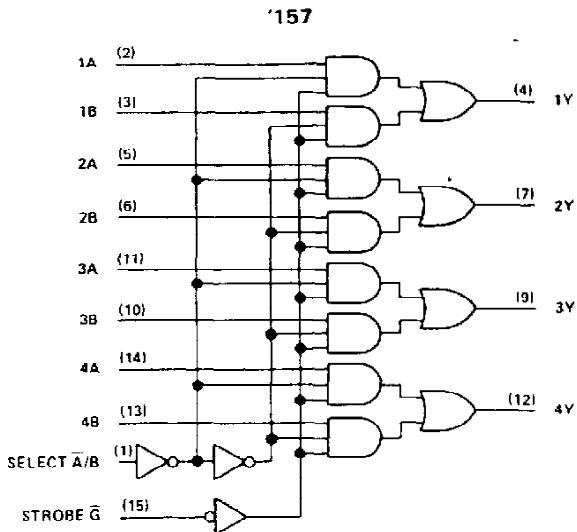
logic symbols[†]



'158, 'LS158, 'S158



logic diagram (positive logic)

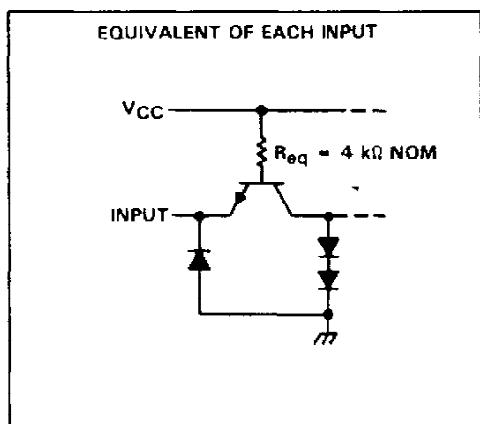


[†] These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

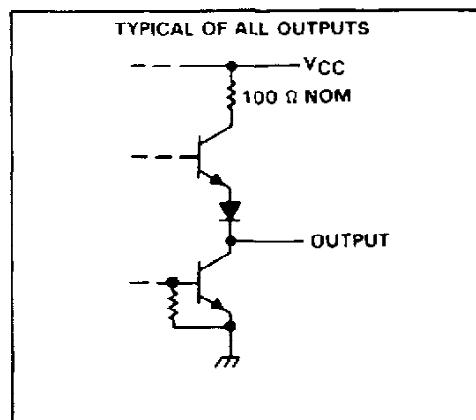
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

'157



'157

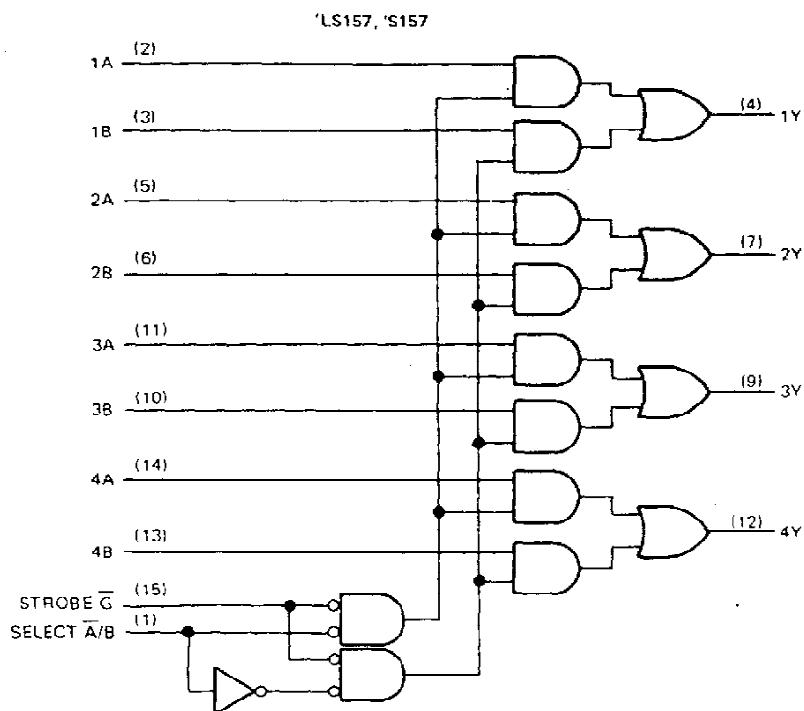


TEXAS
INSTRUMENTS

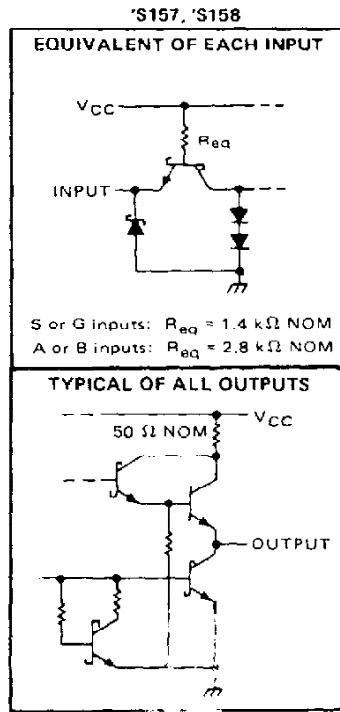
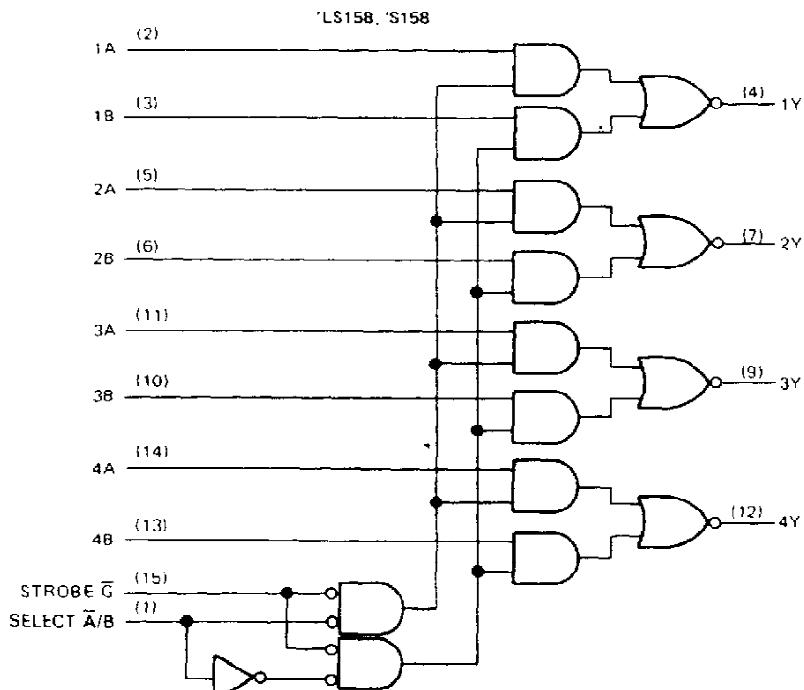
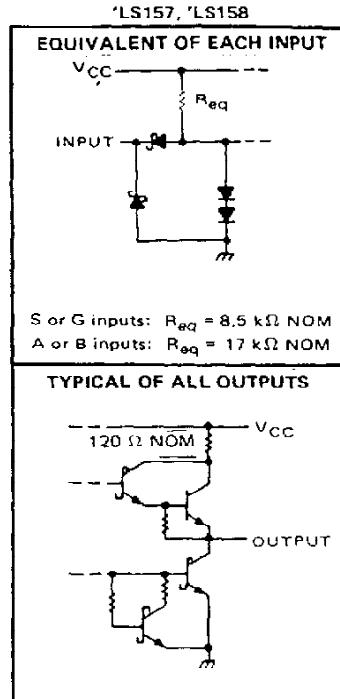
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**SN54LS157, SN54LS158, SN54S157, SN54S158,
SN74LS157, SN74LS158, SN74S157, SN74S158**
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

logic diagrams (positive logic)



schematics of inputs and outputs



Pin numbers shown are for D, J, N, and W packages.

SN54157, SN74157
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

recommended operating conditions

	SN54157			SN74157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55	125	0	0	70	70	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54157			SN74157			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2		2				V
V_{IL} Low-level input voltage			0.8				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$		-1.5				-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu A$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-55	-18	-55	-18	-55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2	30	48	30	48	30	48	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§]Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER [¶]	FROM (INPUT)	TEST CONDITIONS	MIN TYP MAX UNIT		
			MIN	TYP	MAX UNIT
t_{PLH}	Data		9	14	ns
t_{PHL}			9	14	ns
t_{PLH}	Strobe \bar{G}	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 3	13	20	ns
t_{PHL}			14	21	ns
t_{PLH}	Select \bar{A}/B		15	23	ns
t_{PHL}			18	27	ns

[¶] t_{PLH} = propagation delay time, low-to-high-level output

[¶] t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

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SN54LS157, SN54LS158, SN74LS157, SN74LS158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-400			-400	μA
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54LS'			SN74LS'			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -400 μA	2.5	3.4		2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA V _{IL} = MAX, I _{OL} = 8 mA	0.25	0.4		0.25	0.4		V
I _I	Input current at maximum input voltage	A/B or G			0.2			0.2	mA
		A or B	V _{CC} = MAX, V _I = 7 V		0.1			0.1	
I _{IH}	High-level input current	A/B or G			40			40	μA
		A or B	V _{CC} = MAX, V _I = 2.7 V		20			20	
I _{IL}	Low-level input current	A/B or G			-0.8			-0.8	mA
		A or B	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4	
I _{OS}	Short-circuit output current [§]		V _{CC} = MAX		-20	-100	-20	-100	mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 2	'LS157	9.7	16	9.7	16	mA
				'LS158	4.8	8	4.8	8	
			V _{CC} = MAX, All A inputs at 4.5 V, All other inputs at 0 V	'LS158	6.5	11	6.5	11	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[¶]	FROM (INPUT)	TEST CONDITIONS	'LS157			'LS158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PtLH}	Data		9	14		7	12		ns
t _{PHL}			9	14		10	15		
t _{PtLH}	Strobe G	C _L = 15 pF, R _L = 2 kΩ, See Note 3	13	20		11	17		ns
t _{PHL}			14	21		18	24		
t _{PtLH}	Select A/B		15	23		13	20		ns
t _{PHL}			18	27		16	24		

[¶]t_{PtLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage diagrams are shown in Section 1.

SN54S157, SN54S158, SN74S157, SN74S158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MUXES

recommended operating conditions

	SN54S157 SN54S158			SN74S157 SN74S158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}			-1			-1	mA
Low-level output current, I _{OL}			20			20	mA
Operating free-air temperature, T _A	55	125	0	70		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH} High-level input voltage		2		2			2	V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2			-1.2	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	Series 54S	2.5	3.4	2.5	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	Series 74S	2.7	3.4	2.7	3.4		V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			0.5			0.5	V
I _{IH} High-level input current	A/B or G A or B	V _{CC} = MAX, V _I = 2.7 V		100			100	μA
I _{IL} Low-level input current	A/B or G A or B	V _{CC} = MAX, V _I = 0.5 V		50			50	mA
I _{OS} Short-circuit output current [§]	V _{CC} = MAX		-4		-4			
I _{CC} Supply current	V _{CC} = MAX, All inputs at 4.5 V, See Note 2		-2		-2			
	V _{CC} = MAX, A inputs at 4.5 V, B,G,S, inputs at 0 V, See Note 2		40	-100	40	-100		mA
			50	78	39	61		
							81	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Note 2: I_{CC} is measured with all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER [¶]	FROM (INPUT)	TEST CONDITIONS	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Data			5	7.5	4	6		
t _{PHL}			4.5	6.5		4	6		ns
t _{PLH}	Strobe G		8.5	12.5		6.5	11.5		
t _{PHL}			7.5	12		7	12		ns
t _{PLH}	Select A/B		9.5	15		8	12		
t _{PHL}			9.5	15		8	12		ns

[¶]t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

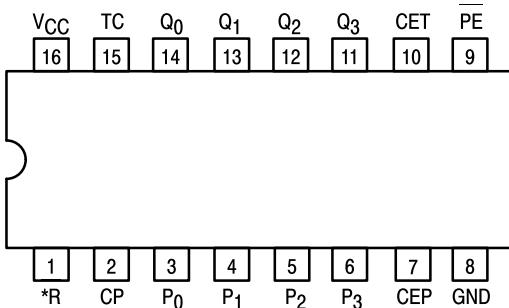
The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary).

The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram)
as the Dual In-Line Package.

*MR for LS160A and LS161A
*SR for LS162A and LS163A

PIN NAMES

LOADING (Note a)		
	HIGH	LOW
PE	Parallel Enable (Active LOW) Input	1.0 U.L.
P ₀ -P ₃	Parallel Inputs	0.5 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.
CET	Count Enable Trickle Input	1.0 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.
SR	Synchronous Reset (Active LOW) Input	1.0 U.L.
Q ₀ -Q ₃	Parallel Outputs (Note b)	10 U.L.
TC	Terminal Count Output (Note b)	10 U.L.

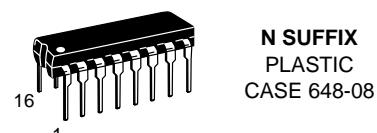
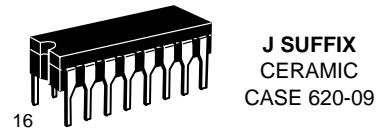
NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74)
Temperature Ranges.

**SN54/74LS160A
SN54/74LS161A
SN54/74LS162A
SN54/74LS163A**

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

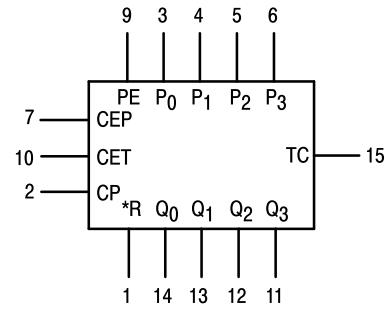
LOW POWER SCHOTTKY



ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

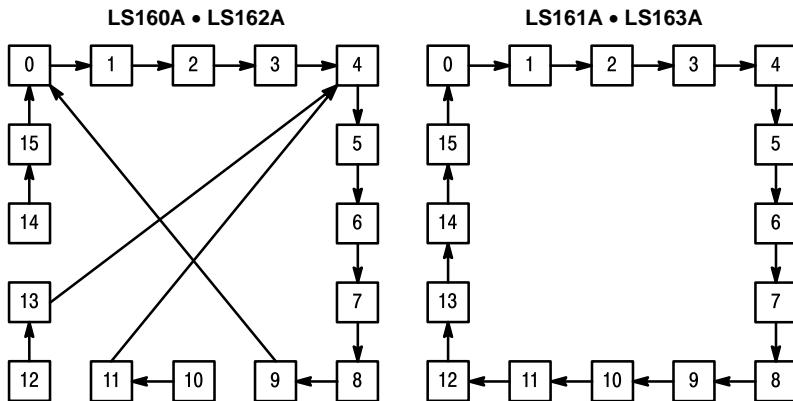
LOGIC SYMBOL



*MR for LS160A and LS161A
*SR for LS162A and LS163A

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = $CEP \bullet CET \bullet PE$
 TC for LS160A & LS162A = $CET \bullet Q_0 \bullet \bar{Q}_1 \bullet \bar{Q}_2 \bullet Q_3$
 TC for LS161A & LS163A = $CET \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$
 Preset = $\overline{PE} \bullet CP + (\text{rising clock edge})$
 Reset = \overline{MR} (LS160A & LS161A)
 Reset = $SR \bullet CP + (\text{rising clock edge})$
 (LS162A & LS163A)

NOTE:

The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FUNCTIONAL DESCRIPTION

The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and PE inputs are HIGH. When the PE is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET•CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for

the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset (MR) of the LS160A and LS161A is asynchronous. When the MR is LOW, it overrides all other input conditions and sets the outputs LOW. The MR pin should never be left open. If not used, the MR pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset (SR) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and PE, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge (↑)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \quad Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162A and LS163A only.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage		54 74	4.5 4.75	5.0 5.0	V
T _A	Operating Ambient Temperature Range		54 74	-55 0	25 25	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

LS160A and LS161A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5	V	
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA
		74	0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current MR, Data, CEP, Clock PE, CET			20 40	µA	V _{CC} = MAX, V _{IN} = 2.7 V
	MR, Data, CEP, Clock PE, CET			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current MR, Data, CEP, Clock PE, CET			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

LS162A and LS163A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
VIH	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
VIL	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
VOH	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = VIH or VIL per Truth Table
		74	2.7	3.5		
VOL	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA
		74	0.35	0.5		I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current <u>Data, CEP, Clock</u> PE, CET, SR			20 40	µA	V _{CC} = MAX, V _{IN} = 2.7 V
	<u>Data, CEP, Clock</u> PE, CET, SR			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current <u>Data, CEP, Clock, PE, SR</u> CET			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	32		MHz	
t _{PLH} t _{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t _{PLH} t _{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t _{PHL}	MR or SR to Q		20	28	ns	

V_{CC} = 5.0 V
C_L = 15 pF

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{WCP}	Clock Pulse Width Low	25			ns	$V_{CC} = 5.0 \text{ V}$
t_W	MR or SR Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time PE or SR	25			ns	
t_h	Hold Time, data	3			ns	
t_h	Hold Time, other	0			ns	
t_{rec}	Recovery Time MR to CP	15			ns	

*CEP, CET or DATA

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.

A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

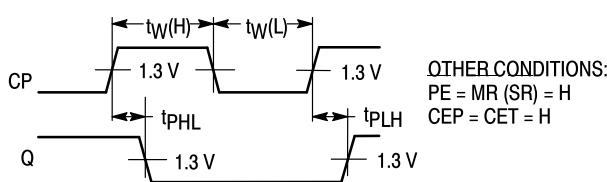


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

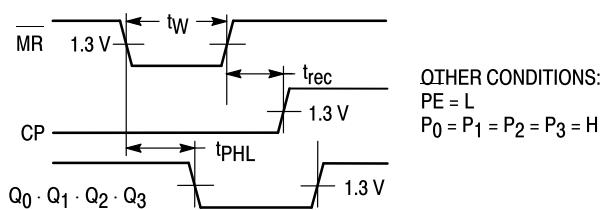


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

AC WAVEFORMS (continued)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the LS160 and LS162 and the $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the LS161 and LS163.

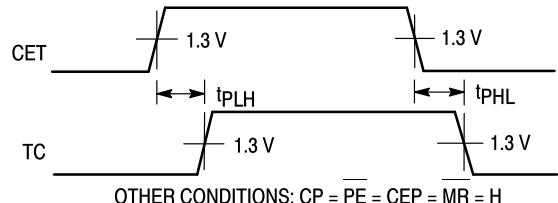


Figure 3

CLOCK TO TERMINAL COUNT DELAYS

The positive TC pulse is coincident with the output state $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ for the LS161 and LS163 and $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ for the LS161 and LS163.

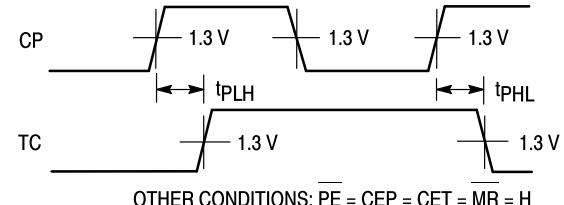


Figure 4

SETUP TIME (t_S) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

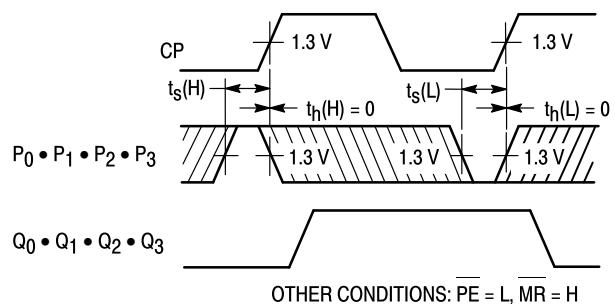


Figure 5

SETUP TIME (t_S) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE (PE) INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

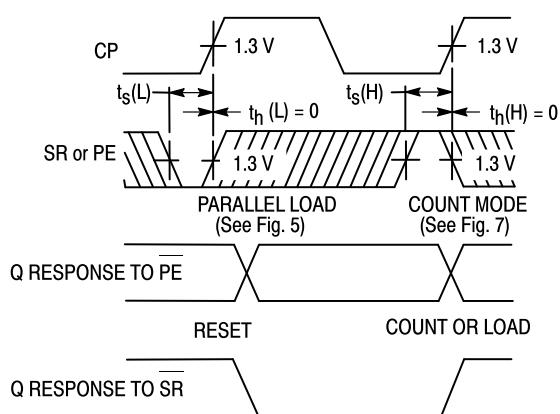


Figure 6

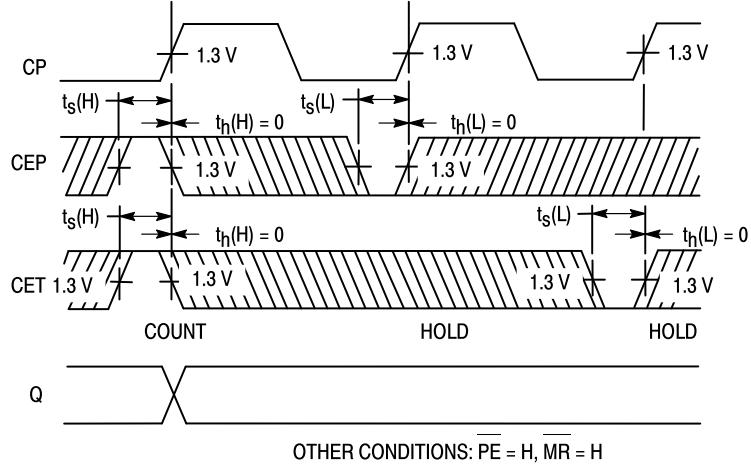


Figure 7

SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

- **3-State Outputs Interface Directly With System Bus**
- **Gated Output-Control Lines for Enabling or Disabling the Outputs**
- **Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:**
 - Parallel Load
 - Do Nothing (Hold)
- **For Application as Bus Buffer Registers**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

TYPE	TYPICAL PROPAGATION DELAY TIME	MAXIMUM CLOCK FREQUENCY
'173	23 ns	35 MHz
'LS173A	18 ns	50 MHz

description

The '173 and 'LS173A 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs can be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable (\overline{G}_1 , \overline{G}_2) inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output-control (M, N) inputs also are provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54173 and SN54LS173A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74173 and SN74LS173A are characterized for operation from 0°C to 70°C .



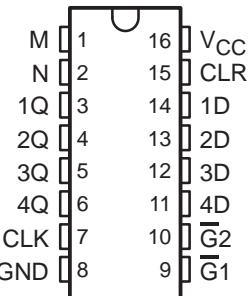
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

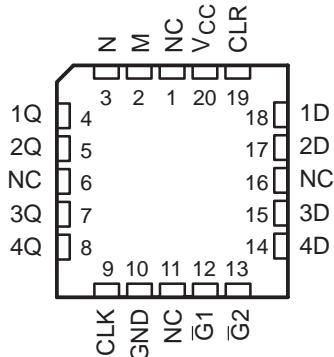


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**SN54173, SN54LS173A . . . J OR W PACKAGE
SN74173 . . . N PACKAGE
SN74LS173A . . . D OR N PACKAGE
(TOP VIEW)**



**SN54LS173A . . . FK PACKAGE
(TOP VIEW)**



NC – No internal connection

SN54173, SN54LS173A, SN74173, SN74LS173A

4-BIT D-TYPE REGISTERS

WITH 3-STATE OUTPUTS

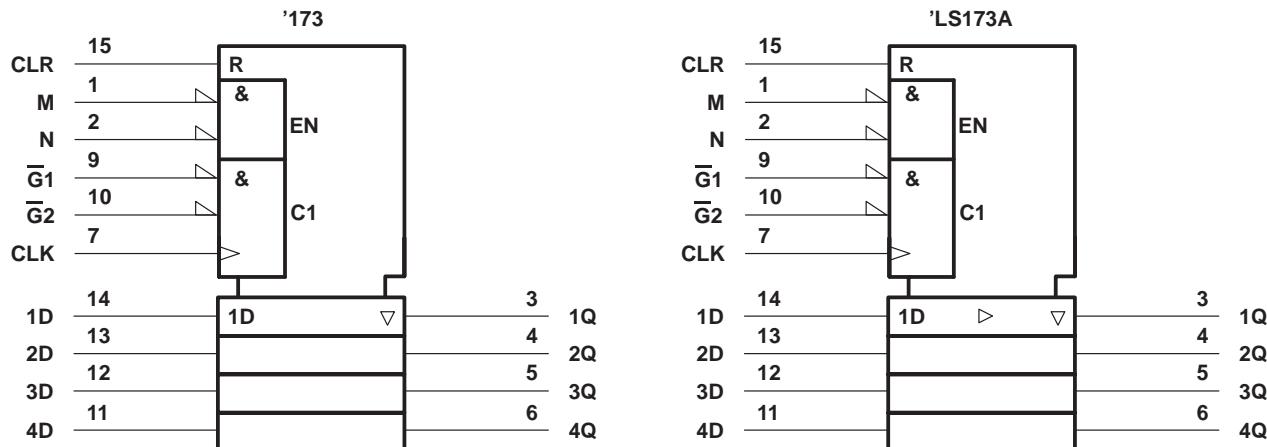
SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

FUNCTION TABLE

		INPUTS			OUTPUT Q
CLR	CLK	DATA ENABLE		DATA D	
		\bar{G}_1	\bar{G}_2		
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

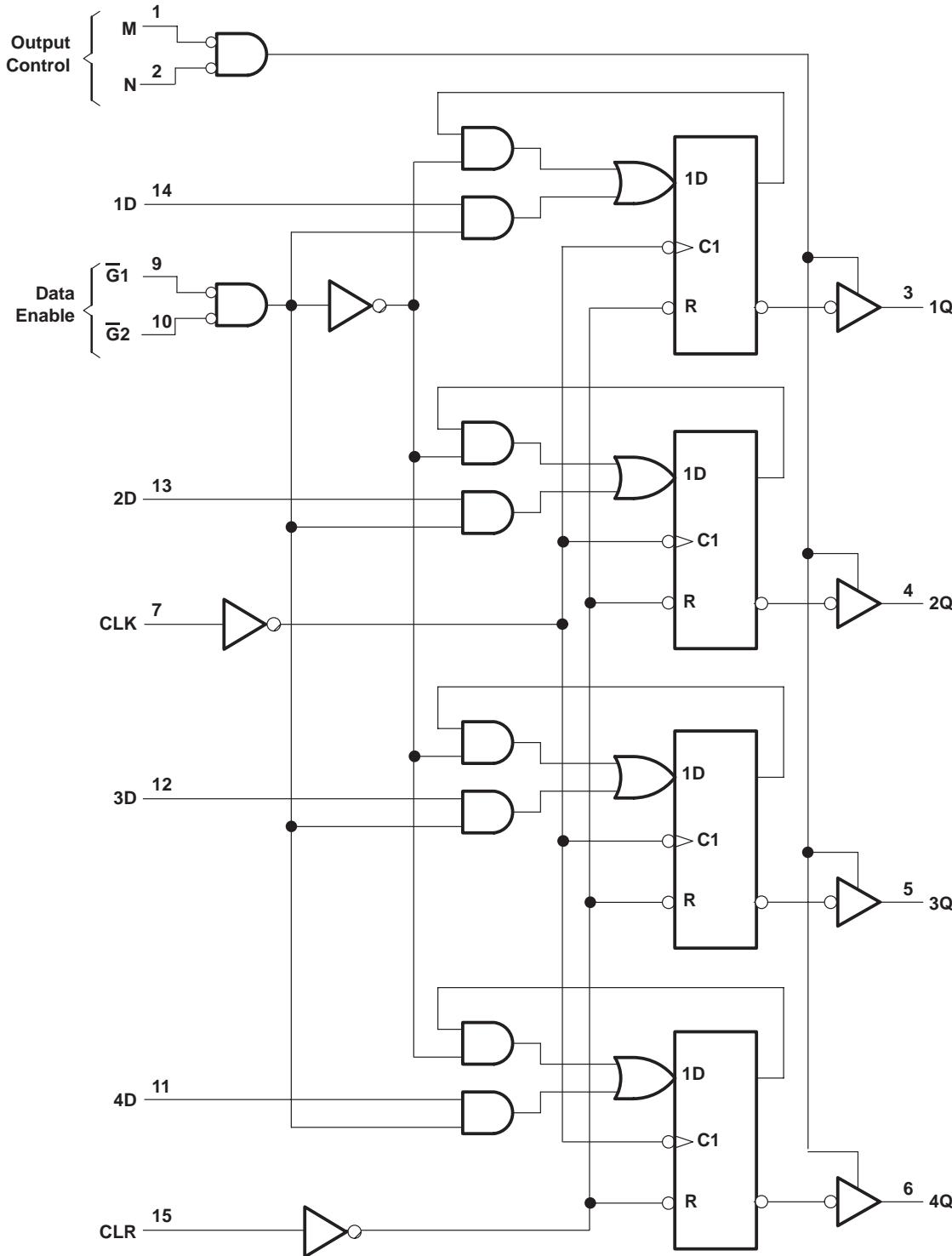
When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

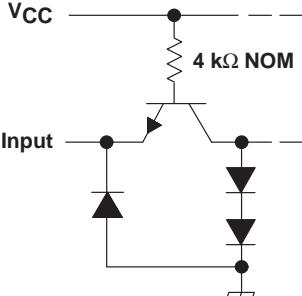
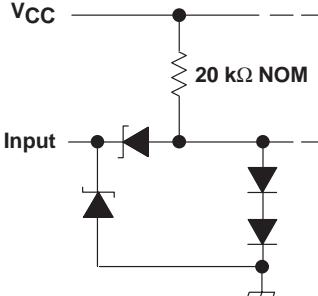
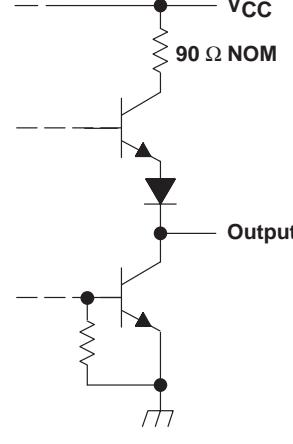
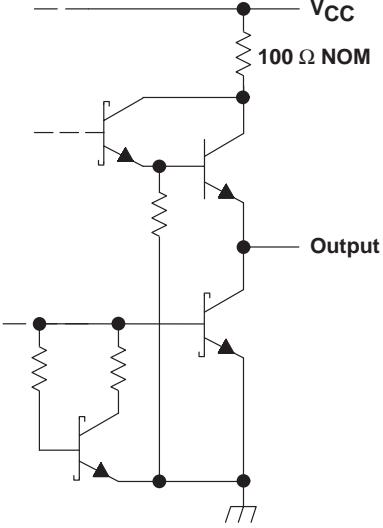
SN54173, SN54LS173A, SN74173, SN74LS173A

4-BIT D-TYPE REGISTERS

WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

schematics of inputs and outputs

'173	'LS173A
Equivalent of Each Input 	Equivalent of Each Input 
Typical of All Outputs 	Typical of All Outputs 

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	-0.5 V to 7 V
Input voltage: '173	-0.5 V to 5.5 V
'LS173A	-0.5 V to 7 V
Off-state output voltage	-0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
N package	78°C/W
Storage temperature range, T_{STG}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SN54173, SN54LS173A, SN74173, SN74LS173A
4-BIT D-TYPE REGISTERS
WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

recommended operating conditions (see Note 3)

		SN54173			SN74173			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-2			-5.2	mA
I _{OL}	Low-level output current			16			16	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54173			SN74173			UNIT	
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX		
V _{IH}	High-level input voltage			2			2	V	
V _{IL}	Low-level input voltage			0.8			0.8	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5		-1.5	V	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = MAX		2.4			2.4	V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 16 mA			0.4		0.4	V	
I _{O(off)}	Off-state (high-impedance state) output current	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.4 V	150			40	μA	
			V _O = 0.4 V	-150			-40		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1		1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.4 V			40		40	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1.6		-1.6	mA	
I _{OS}	Short-circuit output current [§]	V _{CC} = MAX		-30	-70	-30	-70	mA	
I _{CC}	Supply current	V _{CC} = MAX, See Note 4		50	72		50	72	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, \bar{G}_1 , \bar{G}_2 , and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

		SN54173		SN74173		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Input clock frequency			25	25	MHz
t _w	Pulse duration	CLK or CLR		20	20	ns
t _{su}	Setup time	Data enable (\bar{G}_1 , \bar{G}_2)		17	17	ns
		Data		10	10	
		CLR (inactive state)		10	10	
t _h	Hold time	Data enable (\bar{G}_1 , \bar{G}_2)		2	2	ns
		Data		10	10	



SN54173, SN54LS173A, SN74173, SN74LS173A**4-BIT D-TYPE REGISTERS****WITH 3-STATE OUTPUTS**

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, $R_L = 400 \Omega$ (see Figure 1)

PARAMETER	TEST CONDITIONS	SN54173			SN74173			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	$C_L = 50 \text{ pF}$	25	35		25	35		MHz
t_{PHL}		18	27		18	27		ns
t_{PLH}		28	43		28	43		ns
t_{PHL}		19	31		19	31		
t_{PZH}		7	16	30	7	16	30	ns
t_{PZL}		7	21	30	7	21	30	
t_{PHZ}	$C_L = 5 \text{ pF}$	3	5	14	3	5	14	ns
t_{PLZ}		3	11	20	3	11	20	

SN54173, SN54LS173A, SN74173, SN74LS173A
4-BIT D-TYPE REGISTERS
WITH 3-STATE OUTPUTS

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

recommended operating conditions

		SN54LS173A			SN74LS173A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-1			-2.6	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS173A			SN74LS173A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage			2			2	V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.4	2.4	3.1		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, I _{OL} = 12 mA V _{IL} = 0.8 V, I _{OL} = 24 mA	0.25	0.4	0.25	0.4		V
I _{O(off)}	Off-state (high-impedance state) output current	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.7 V		20		20	V
			V _O = 0.4 V		-20		-20	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20		20	µA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA
I _{OS}	Short-circuit output current [§]	V _{CC} = MAX	-30	-130	-30	-130		mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 4		19	30	19	24	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, G₁, G₂, and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

		SN54LS173A		SN74LS173A		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Input clock frequency			30	25	MHz
t _w	Pulse duration	CLK or CLR		25	25	ns
t _{su}	Setup time	Data enable (G ₁ , G ₂)		35	35	ns
		Data		17	17	
		CLR (inactive state)		10	10	
t _h	Hold time	Data enable (G ₁ , G ₂)		0	0	ns
		Data		3	3	

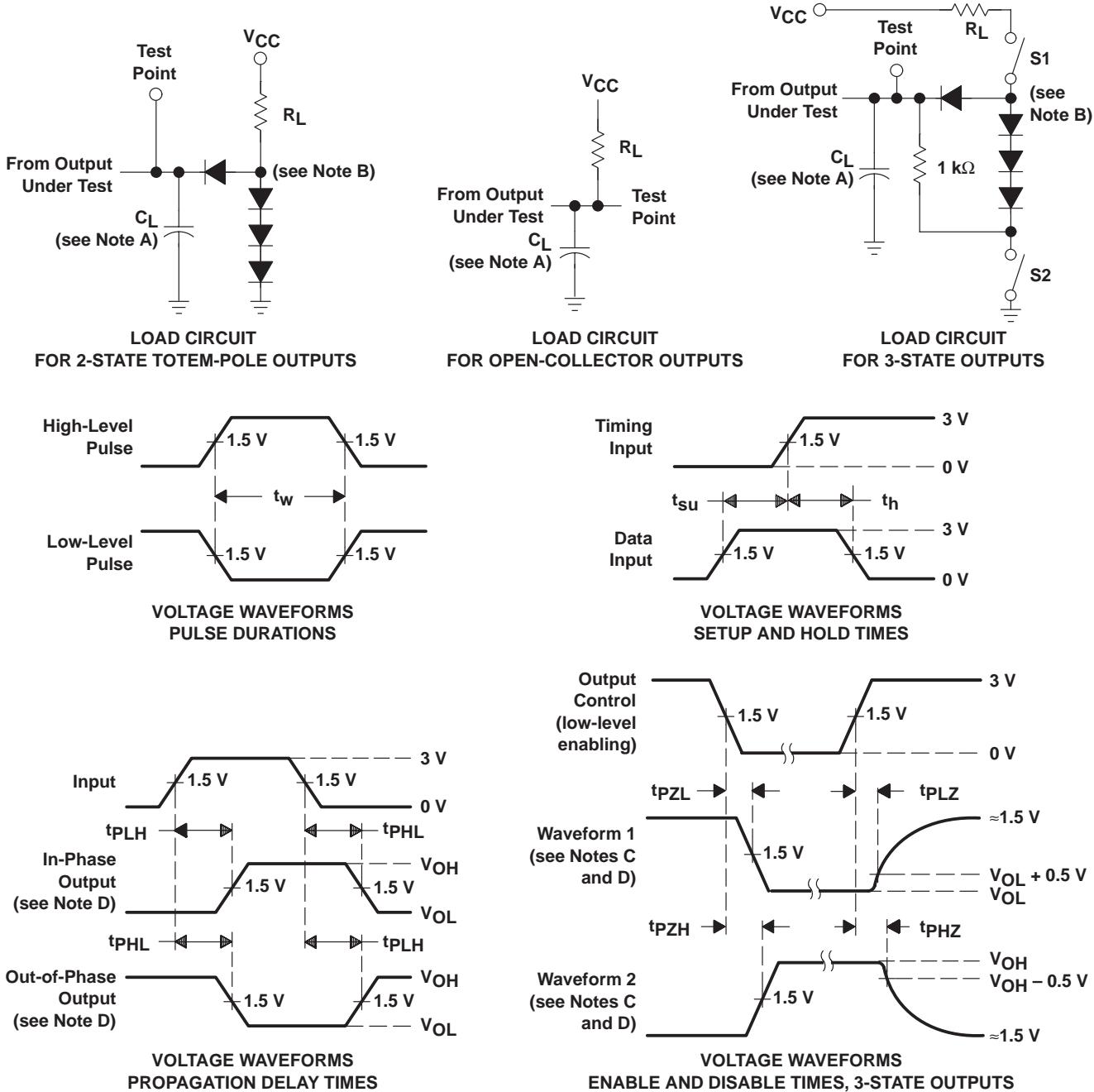
SN54173, SN54LS173A, SN74173, SN74LS173A**4-BIT D-TYPE REGISTERS****WITH 3-STATE OUTPUTS**

SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, $R_L = 667 \Omega$ (see Figure 2)

PARAMETER	TEST CONDITIONS	SN54LS173A			SN74LS173A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	$C_L = 45 \text{ pF}$	30	50		30	50		MHz
t_{PHL}		26	35		26	35		ns
t_{PLH}		17	25		17	25		ns
t_{PHL}		22	30		22	30		
t_{PZH}		15	23		15	23		ns
t_{PZL}		18	27		18	27		
t_{PHZ}	$C_L = 5 \text{ pF}$	11	20		11	20		ns
t_{PLZ}		11	17		11	17		

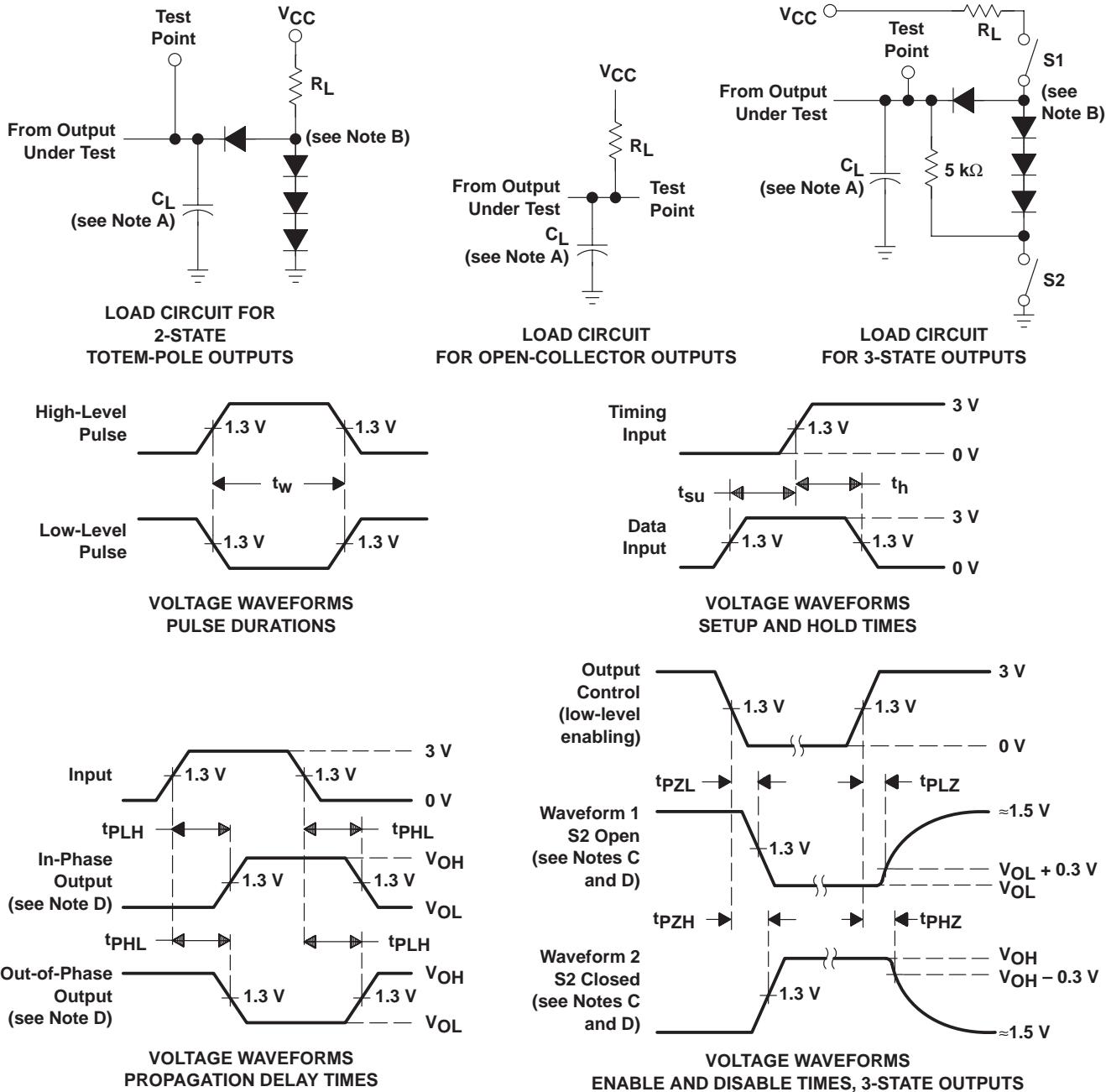
PARAMETER MEASUREMENT INFORMATION
 SERIES 54/74 AND 54S/74S DEVICES



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PZH} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 - E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50 \Omega$, t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 - F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PZL} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 - F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O \approx 50 \Omega$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
 - G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/36101B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/36101BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/36101BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/36101SEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/36101SFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54173J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS173AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74173N	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74LS173AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS173ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS173ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS173ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54173J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54173W	OBsolete	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS173AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS173AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS173AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

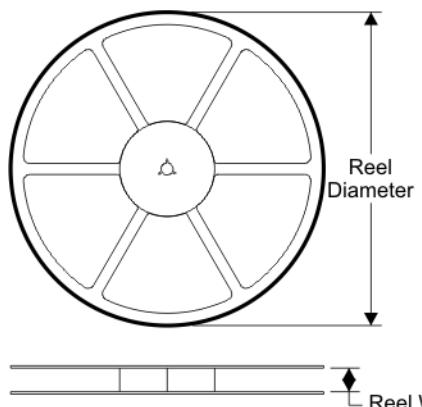
(³) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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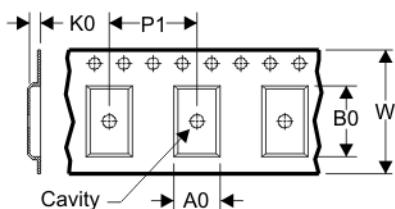
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TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

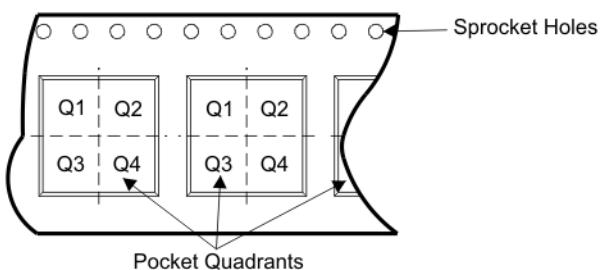


TAPE DIMENSIONS



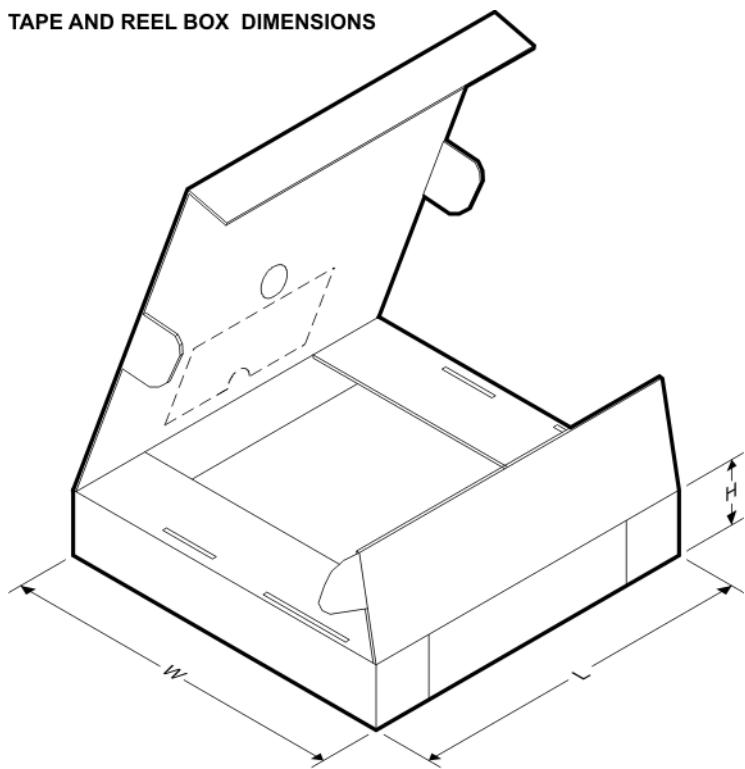
A_0	Dimension designed to accommodate the component width
B_0	Dimension designed to accommodate the component length
K_0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A_0 (mm)	B_0 (mm)	K_0 (mm)	P_1 (mm)	W (mm)	Pin1 Quadrant
SN74LS173ADR	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1
SN74LS173ANSR	NS	16	SITE 41	330	16	8.2	10.5	2.5	12	16	Q1

TAPE AND REEL BOX DIMENSIONS

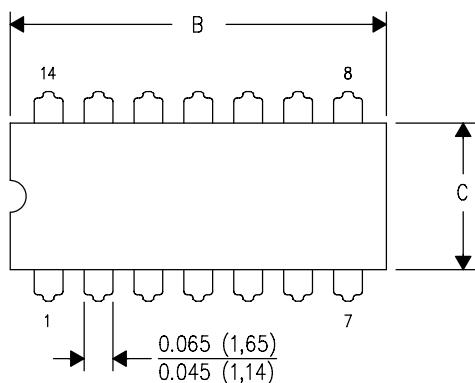


Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LS173ADR	D	16	SITE 27	342.9	336.6	28.58
SN74LS173ANSR	NS	16	SITE 41	346.0	346.0	33.0

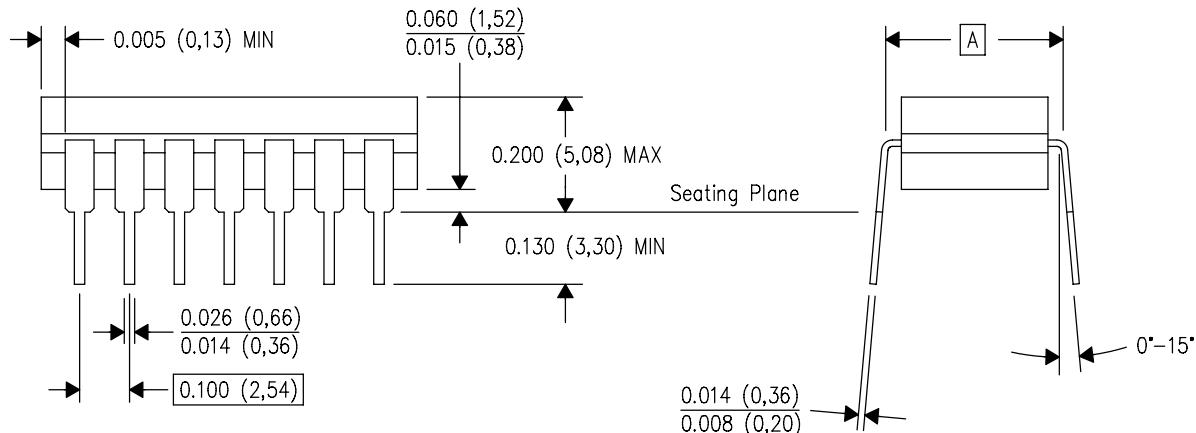
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

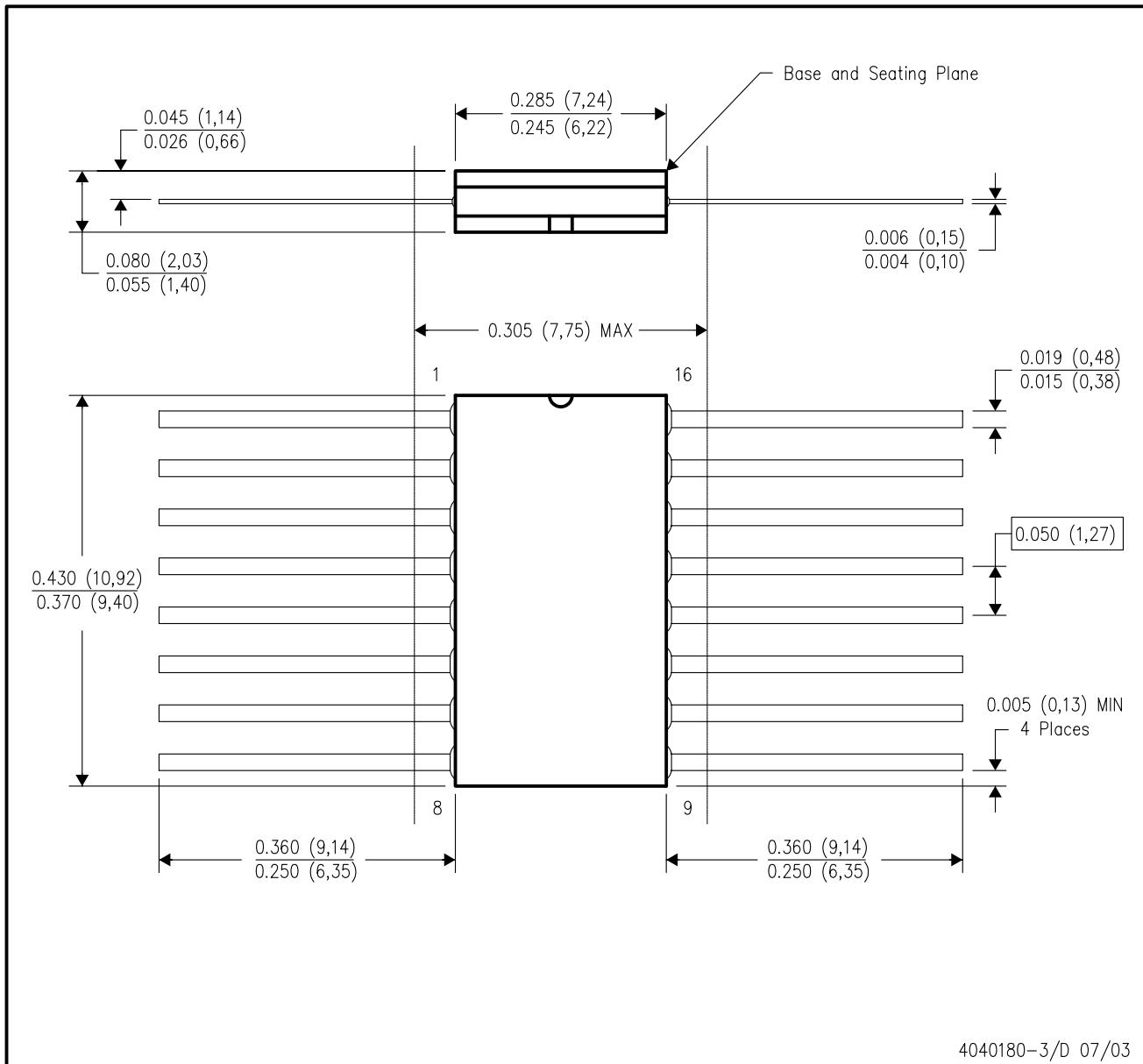


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

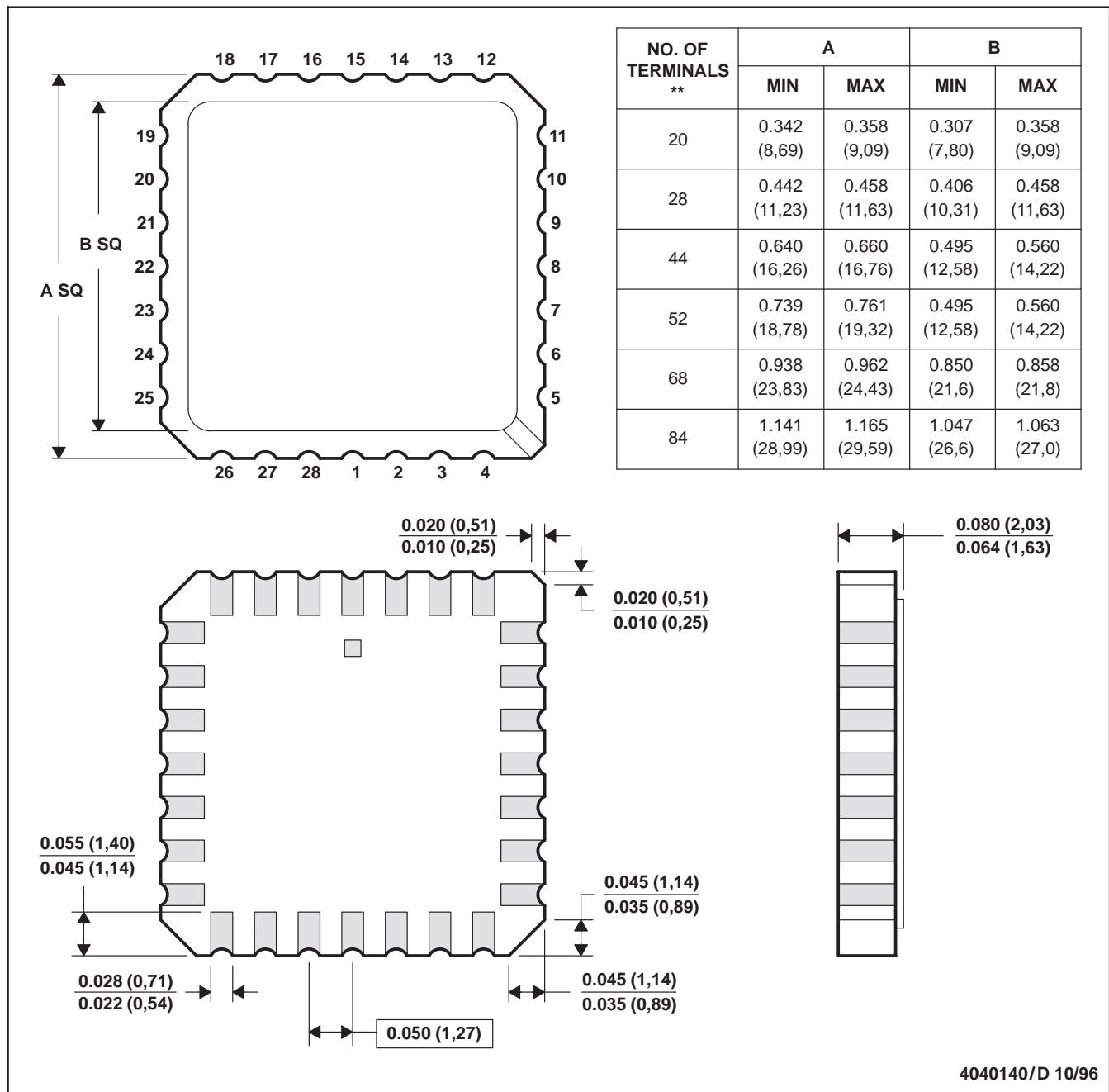


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL-STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals are gold plated.

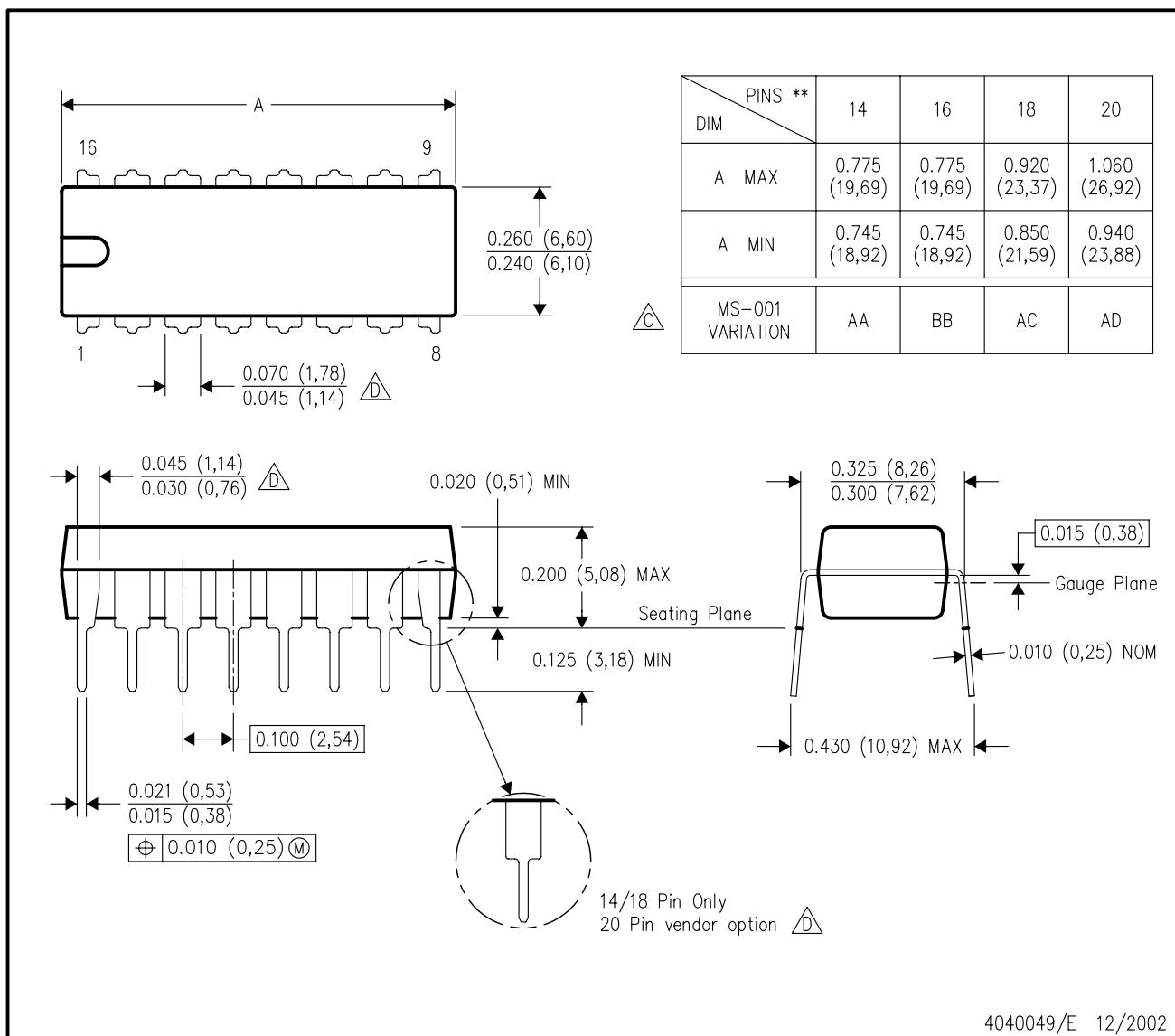
E. Falls within JEDEC MS-004

4040140/D 10/96

N (R-PDIP-T**)

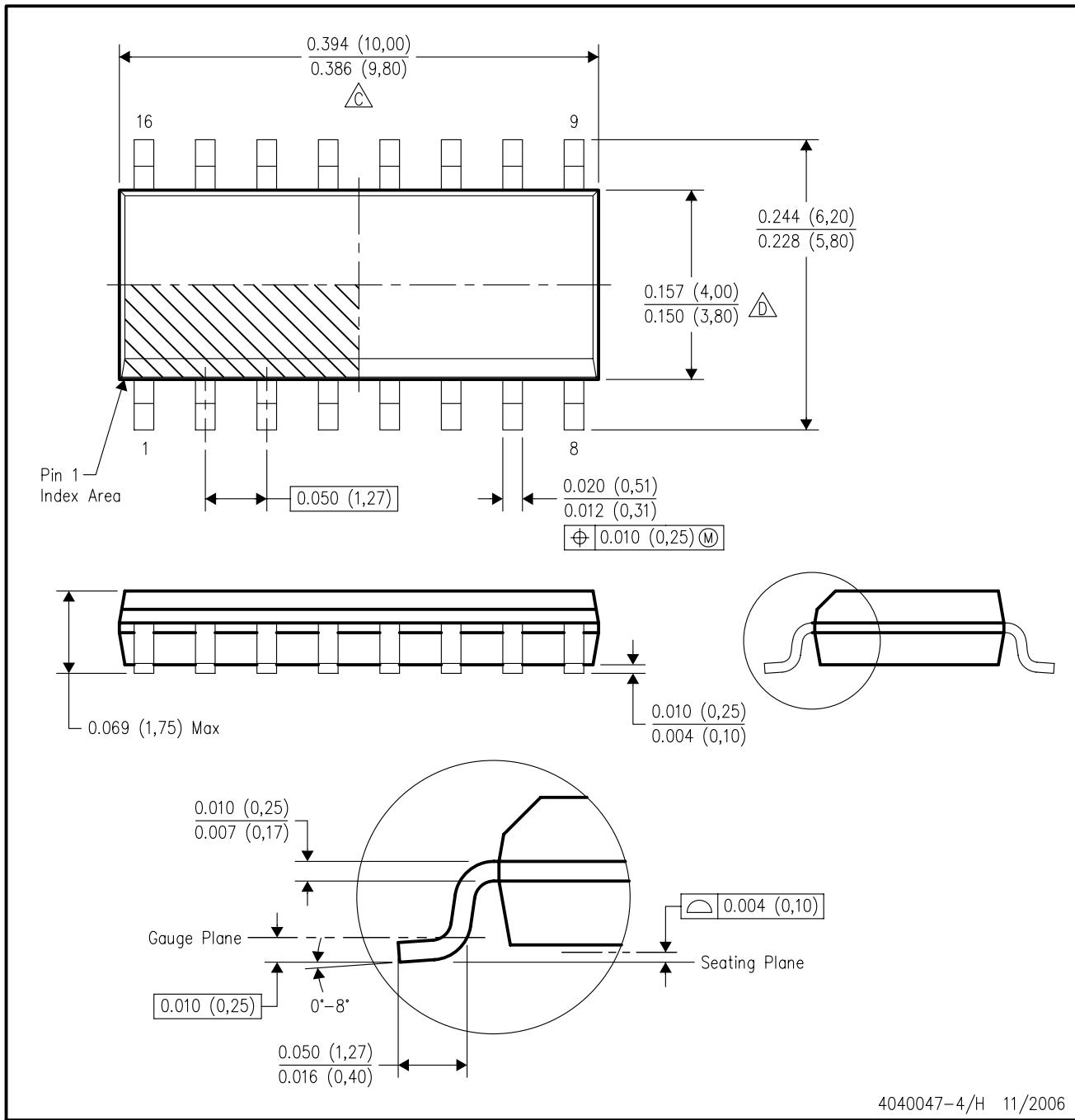
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

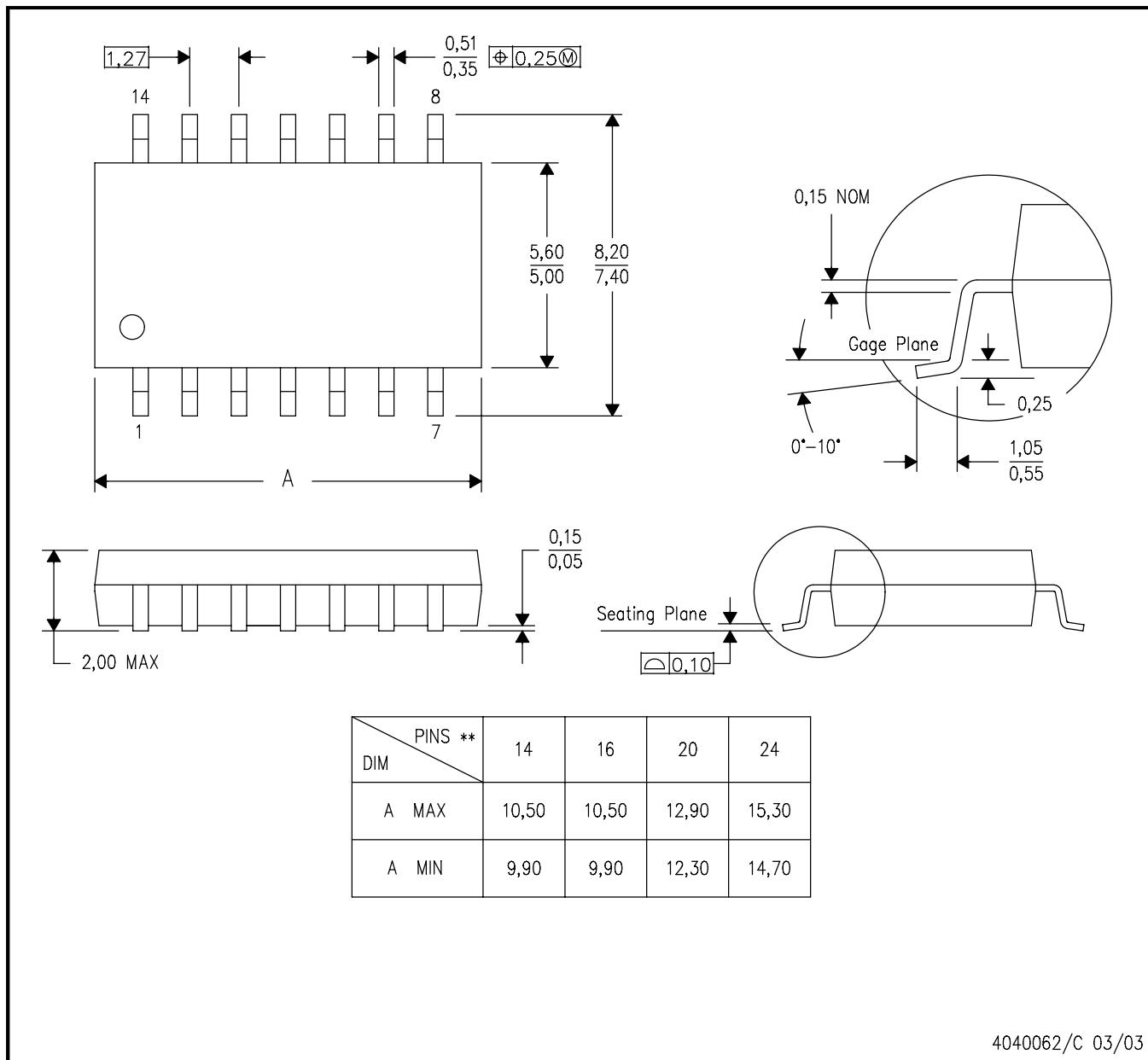
△D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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		Wireless	www.ti.com/wireless

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DM74LS245

3-STATE Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A Bus to the B Bus or from the B Bus to the A Bus depending upon the logic level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

Features

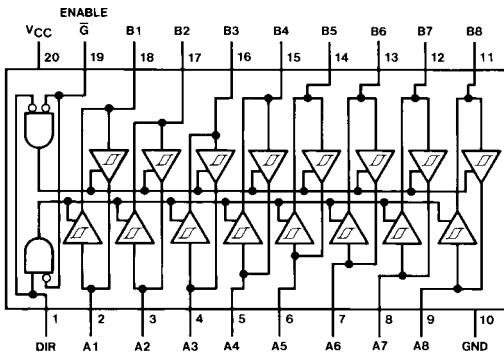
- Bi-Directional bus transceiver in a high-density 20-pin package
- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
24 mA
- I_{OH} (source current)
-15 mA

Ordering Code:

Order Number	Package Number	Package Description
DM74LS245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS245N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Enable \bar{G}	Direction Control DIR	Operation
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

Absolute Maximum Ratings^(Note 1)

Supply Voltage	7V
Input Voltage DIR or \bar{G}	7V
A or B	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18 \text{ mA}$			-1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{Min}$	0.2	0.4		V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}$, $V_{IH} = \text{Min}$				V
		$V_{IL} = \text{Max}$, $I_{OH} = -1 \text{ mA}$	2.7			
		$V_{CC} = \text{Min}$, $V_{IL} = \text{Min}$	2.4	3.4		
		$V_{IL} = \text{Max}$, $I_{OH} = -3 \text{ mA}$				
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}$, $V_{IH} = \text{Min}$				V
		$V_{IL} = 0.5V$, $I_{OH} = \text{Max}$	2			
		$V_{CC} = \text{Min}$, $I_{OL} = 12 \text{ mA}$			0.4	
I_{OZH}	Off-State Output Current, HIGH Level Voltage Applied	$V_{CC} = \text{Max}$ $V_{IL} = \text{Max}$ $V_{IH} = \text{Min}$	$V_O = 2.7V$		20	μA
					-200	
I_{OZL}	Off-State Output Current, LOW Level Voltage Applied	$V_{IH} = \text{Min}$	$V_O = 0.4V$			μA
I_I	Input Current at Maximum Input Voltage	$V_{CC} = \text{Max}$	$A \text{ or } B$	$V_I = 5.5V$	0.1	mA
			$\text{DIR or } \bar{G}$	$V_I = 7V$	0.1	
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}$, $V_I = 2.7V$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}$, $V_I = 0.4V$			-0.2	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	-40		-225	mA
I_{CC}	Supply Current	Outputs HIGH			48	mA
		Outputs LOW	$V_{CC} = \text{Max}$		62	
					64	

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$.

Note 3: Not more than one output should be shorted at a time, not to exceed one second duration

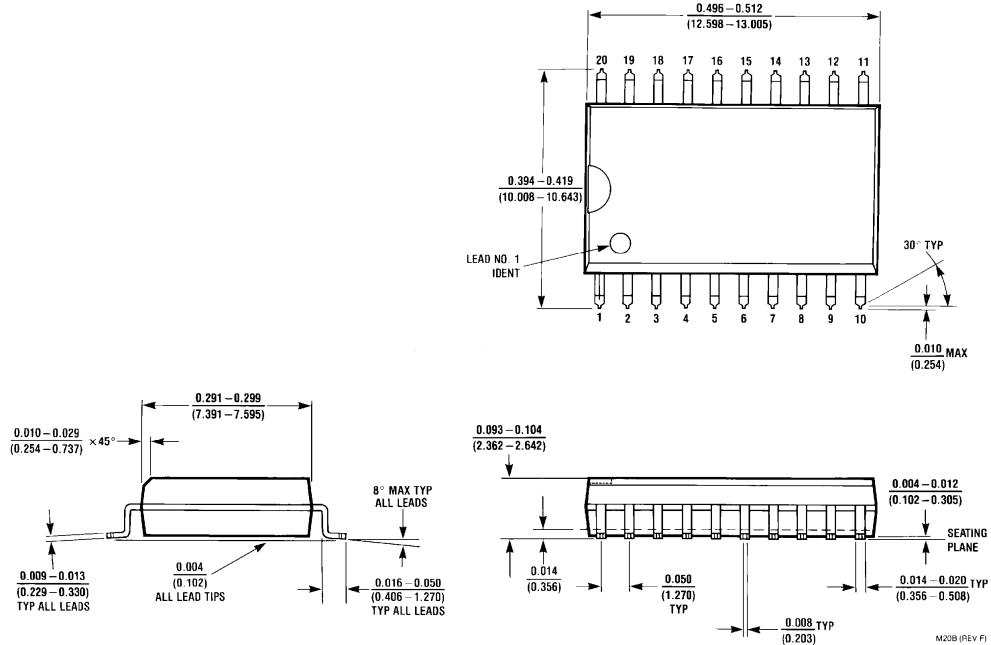
Switching Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$		12	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output			12	ns
t_{PZL}	Output Enable Time to LOW Level			40	ns
t_{PZH}	Output Enable Time to HIGH Level			40	ns
t_{PLZ}	Output Disable Time from LOW Level	$C_L = 5 \text{ pF}$ $R_L = 667\Omega$		25	ns
t_{PHZ}	Output Disable Time from HIGH Level			25	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$		16	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output			17	ns
t_{PZL}	Output Enable Time to LOW Level			45	ns
t_{PZH}	Output Enable Time to HIGH Level			45	ns

DM74LS245

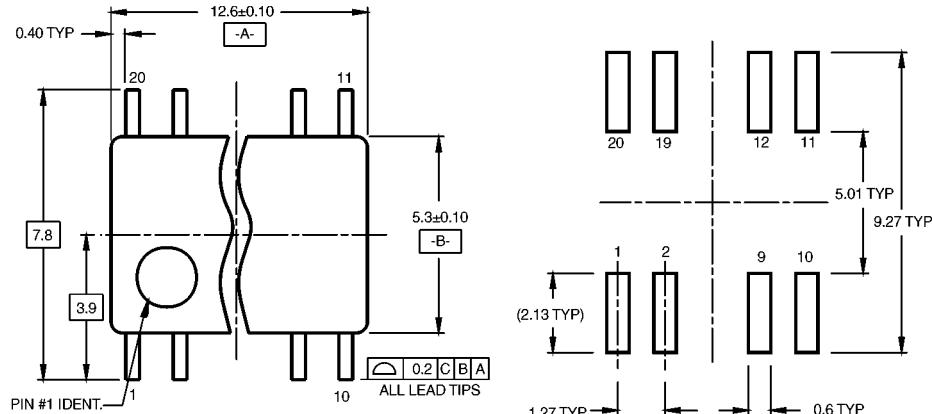
Physical Dimensions inches (millimeters) unless otherwise noted



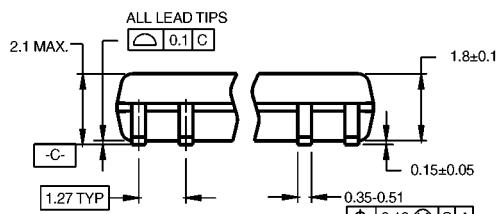
**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

M20B (REV F)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

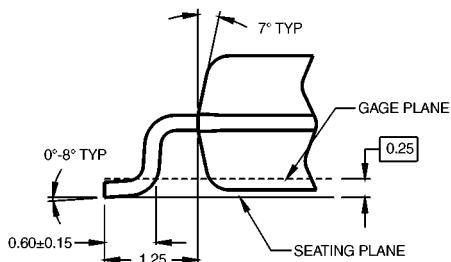
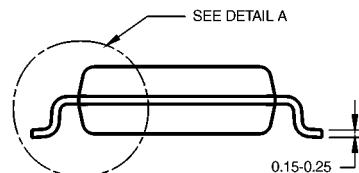


DIMENSIONS ARE IN MILLIMETERS

NOTES:

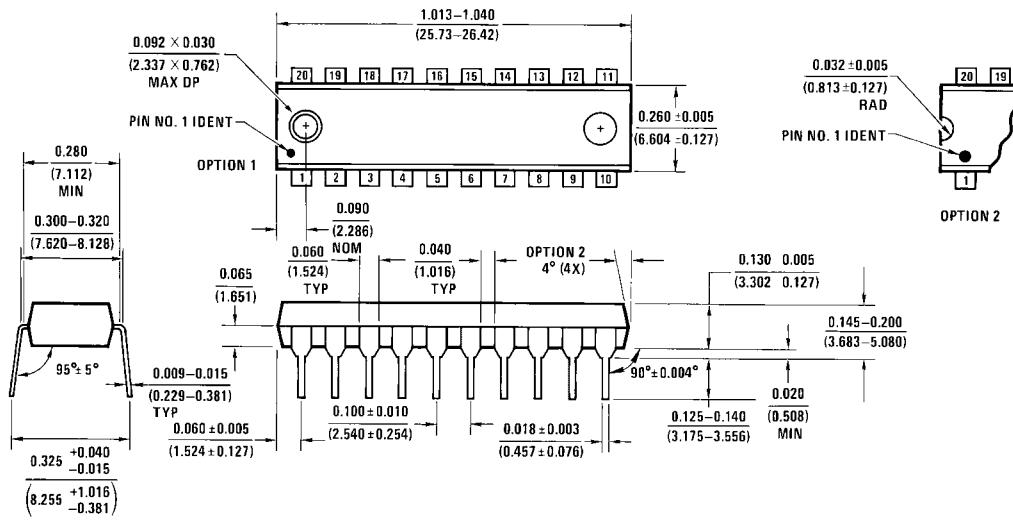
- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1



DETAIL A

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

54LS283/DM54LS283/DM74LS283 4-Bit Binary Adders with Fast Carry

General Description

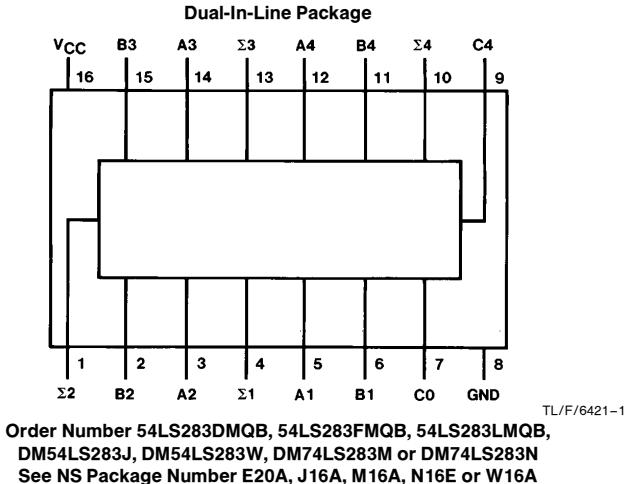
These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
 - Two 8-bit words 25 ns
 - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS283) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS283			DM74LS283			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			−0.4			−0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max	DM54	2.5	3.4	V
		V _{IL} = Max, V _{IH} = Min	DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max	DM54	0.25	0.4	V
		V _{IL} = Max, V _{IH} = Min	DM74	0.35	0.5	
	I _{OL} = 4 mA, V _{CC} = Min	DM74		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max	A, B		0.2	mA
		V _I = 7V	C0		0.1	
I _{IH}	High Level Input Current	V _{CC} = Max	A, B		40	μA
		V _I = 2.7V	C0		20	
I _{IL}	Low Level Input Current	V _{CC} = Max	A, B		−0.8	mA
		V _I = 0.4V	C0		−0.4	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	−20	−100	mA
			DM74	−20	−100	
I _{CC1}	Supply Current	V _{CC} = Max (Note 3)		19	34	mA
I _{CC2}	Supply Current	V _{CC} = Max (Note 4)		22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2 k\Omega$				Units	
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$			
			Min	Max	Min	Max		
t_{PLH}	Propagation Delay Time Low to High Level Output	C_0 to Σ_1, Σ_2		24		28	ns	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_0 to Σ_1, Σ_2		24		30	ns	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_0 to Σ_3		24		28	ns	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_0 to Σ_3		24		30	ns	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_0 to Σ_4		24		28	ns	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_0 to Σ_4		24		30	ns	
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to Σ_i		24		28	ns	
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to Σ_i		24		30	ns	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_0 to C_4		17		24	ns	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_0 to C_4		17		25	ns	
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to C_4		17		24	ns	
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to C_4		17		26	ns	

Function Table

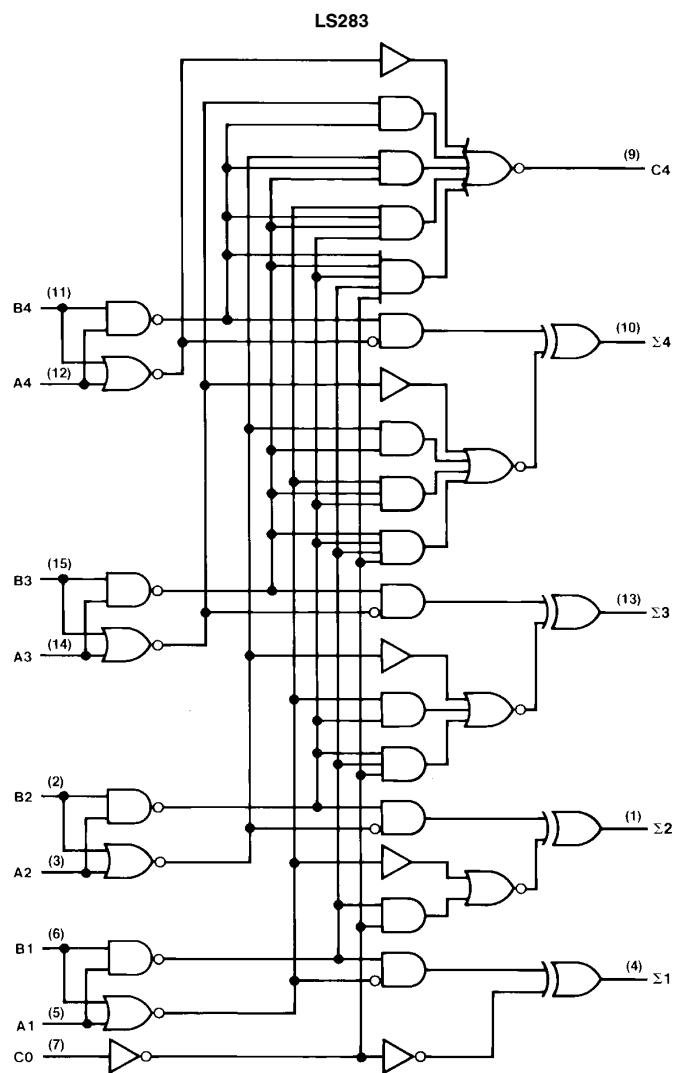
Input					Outputs												
					When $C_0 = L$				When $C_0 = H$								
A1		B1		A2		B2		Σ_1	Σ_2	C2	Σ_3	Σ_4	C2	Σ_1	Σ_2	Σ_4	C4
A1 A3	B1 B3	A2 A4	B2 B4		Σ_3	Σ_4				C4							
L	L	L	L		L	L	L	L	H	L	L	L	L	L	L	L	L
H	L	L	L		H	L	L	L	L	H	L	H	L	H	L	H	L
L	H	L	L		H	L	L	L	L	H	L	H	L	H	L	H	L
H	H	L	L		L	H	L	L	L	H	H	H	H	H	H	H	L
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L	L	L	H		L	H	H	L	H	L	H	H	H	H	H	H	L
H	L	H	H		H	H	L	L	H	L	H	H	H	H	H	H	H
L	H	H	H		H	H	L	L	H	H	H	H	H	H	H	H	H
H	H	H	H		L	H	L	H	H	L	H	H	H	H	H	H	H

H = High Level, L = Low Level

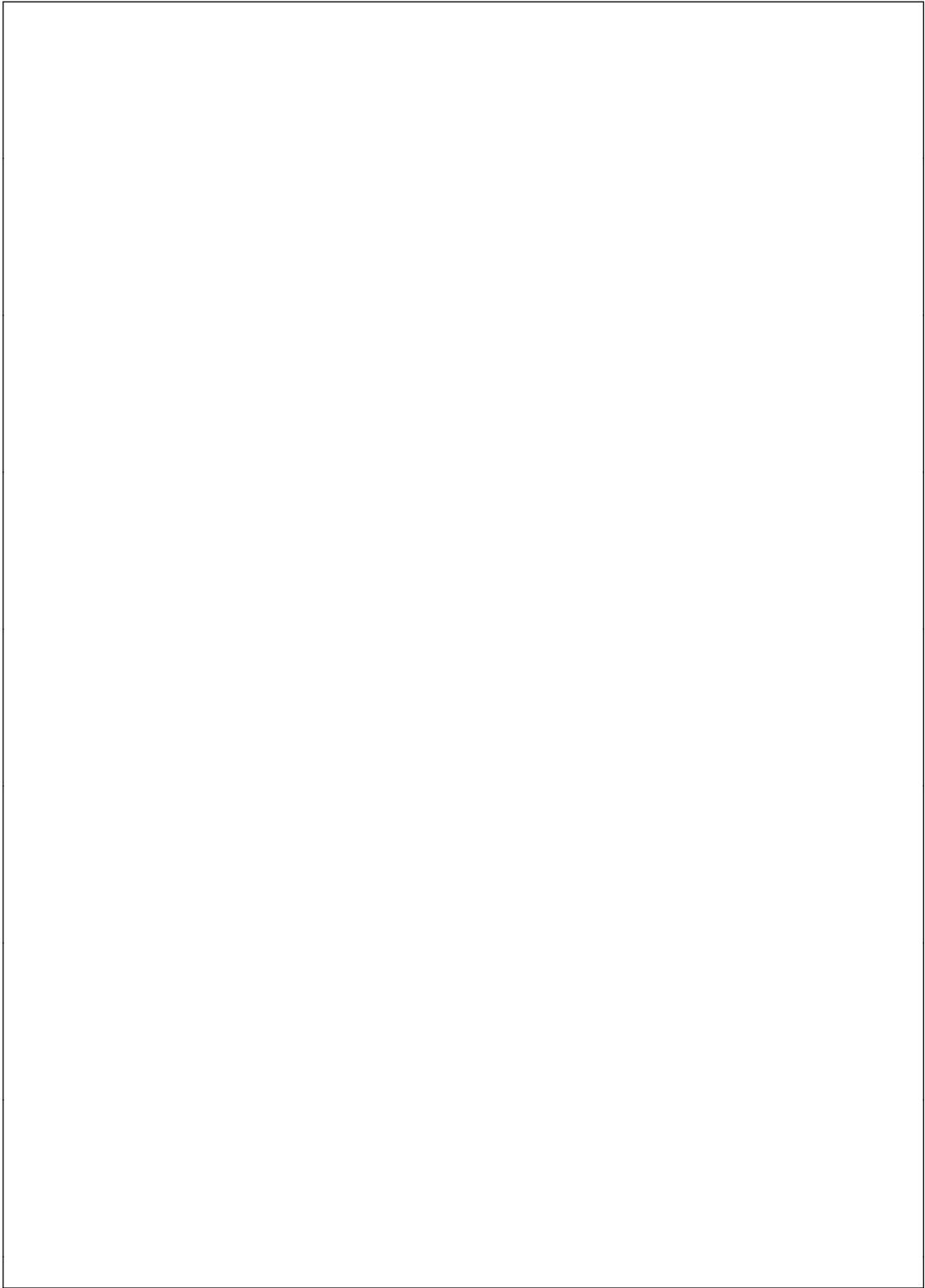
Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ_3 , Σ_4 , and C4.

TL/F/6421-3

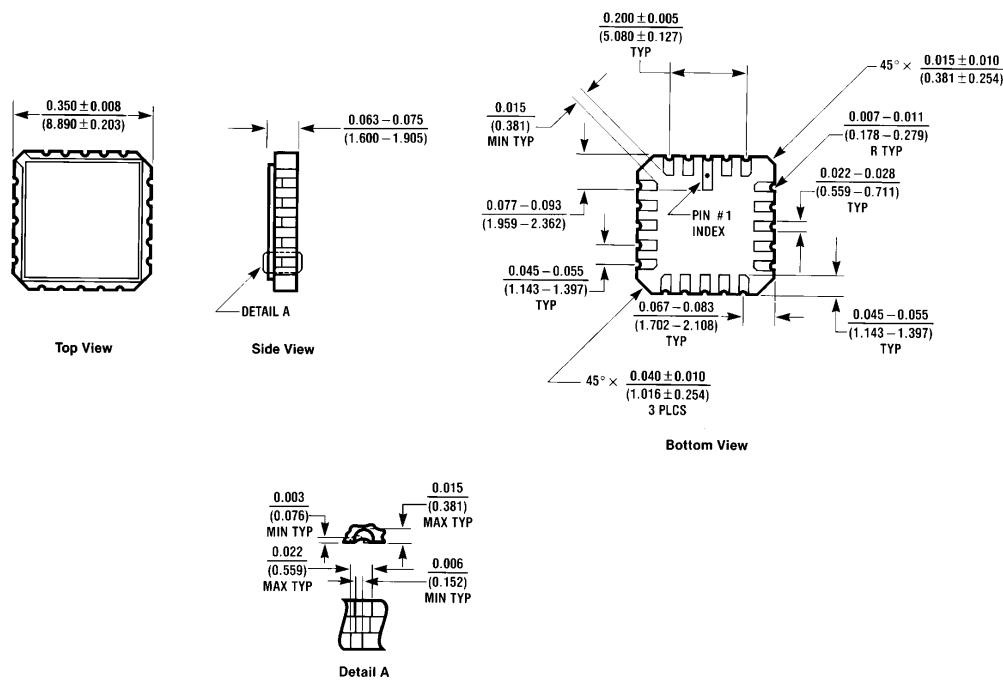
Logic Diagram



TL/F/6421-2

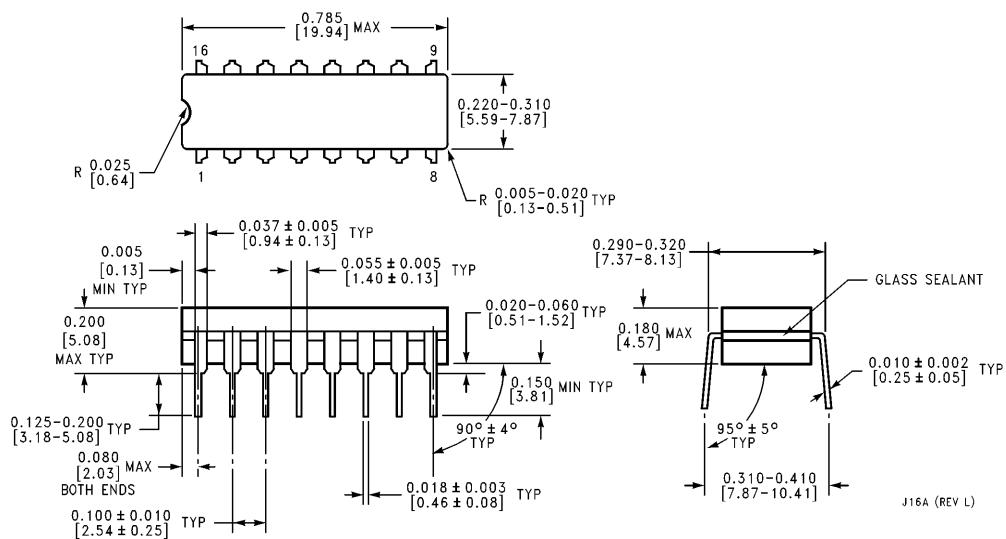


Physical Dimensions inches (millimeters)



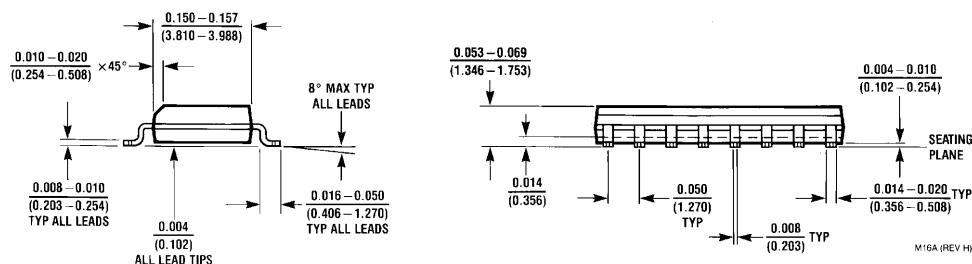
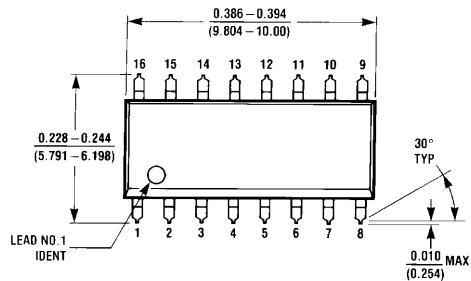
Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS283LMQB
NS Package Number E20A

E20A (REV D)

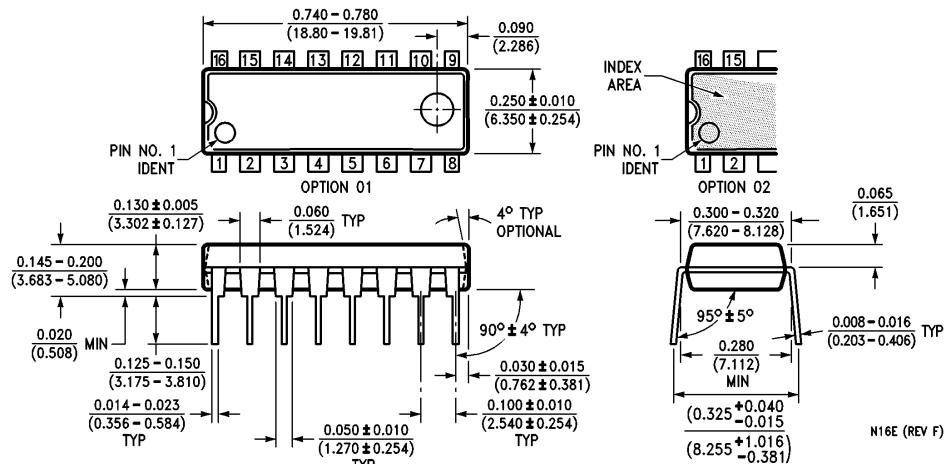


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS283DMQB or DM54LS283J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

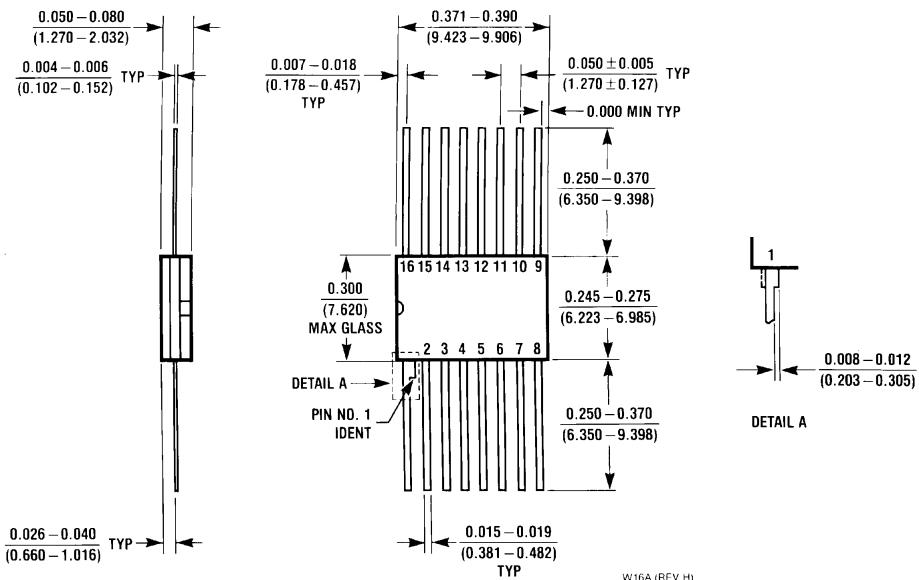


16-Lead Small Outline Molded Package (M)
Order Number DM74LS283M
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS283N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS283FMQB or DM54LS283W
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT299

8-bit universal shift register; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

8-bit universal shift register; 3-state**74HC/HCT299****FEATURES**

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes:
 - shift left
 - shift right
 - hold (store)
 - load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability: bus driver (parallel I/Os), standard (serial outputs)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

$GND = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_0, Q_7	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	20	19	ns
	CP to I/O_n		20	19	ns
	\overline{MR} to Q_0, Q_7 or I/O_n		20	23	ns
f_{max}	maximum clock frequency		50	46	MHz
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	120	125	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

The 74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S_0 and S_1), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O_0 to I/O_7) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q_0 and Q_7) are used for expansion in serial shifting of longer words.

A LOW signal on the asynchronous master reset input (MR) overrides the S_n and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP , are observed.

A HIGH signal on the 3-state output enable inputs (\overline{OE}_1 or \overline{OE}_2) disables the 3-state buffers and the I/O_n outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 , when in preparation for a parallel load operation.

ORDERING INFORMATION

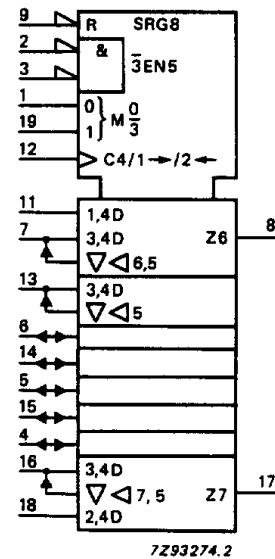
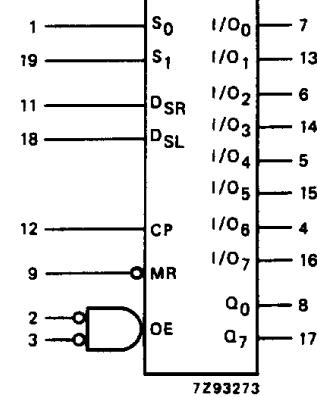
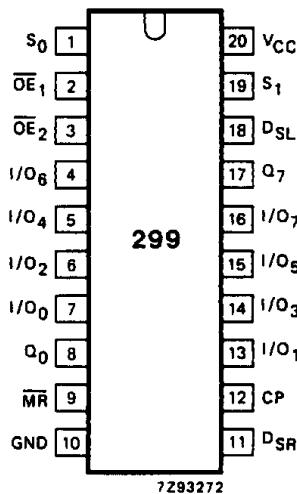
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-bit universal shift register; 3-state

74HC/HCT299

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	S ₀ , S ₁	mode select inputs
2, 3	OE ₁ , OE ₂	3-state output enable inputs (active LOW)
7, 13, 6, 14, 5, 15, 4, 16	I/O ₀ to I/O ₇	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17	Q ₀ , Q ₇	serial outputs (standard output)
9	MR	asynchronous master reset input (active LOW)
10	GND	ground (0 V)
11	D _{SR}	serial data shift-right input
12	CP	clock input (LOW-to-HIGH, edge-triggered)
18	D _{SL}	serial data shift-left input
20	V _{CC}	positive supply voltage



8-bit universal shift register; 3-state

74HC/HCT299

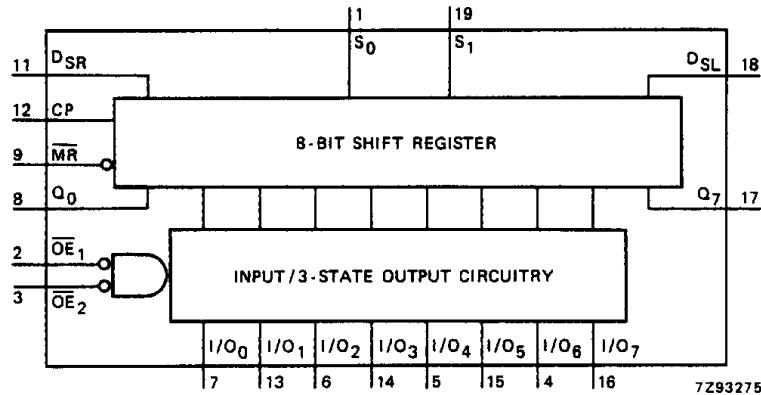


Fig.4 Functional diagram.

MODE SELECT TABLE

INPUTS				RESPONSE
MR	S ₁	S ₀	CP	
L	X	X	X	asynchronous reset; Q ₀ -Q ₇ = LOW
H	H	H	↑	parallel load; I/O _n → Q _n
H	L	H	↑	shift right; D _{SR} → Q ₀ , Q ₀ → Q ₁ etc.
H	H	L	↑	shift left; D _{SL} → Q ₇ , Q ₇ → Q ₆ etc.
H	L	L	X	hold

Notes

1. H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition

8-bit universal shift register; 3-state

74HC/HCT299

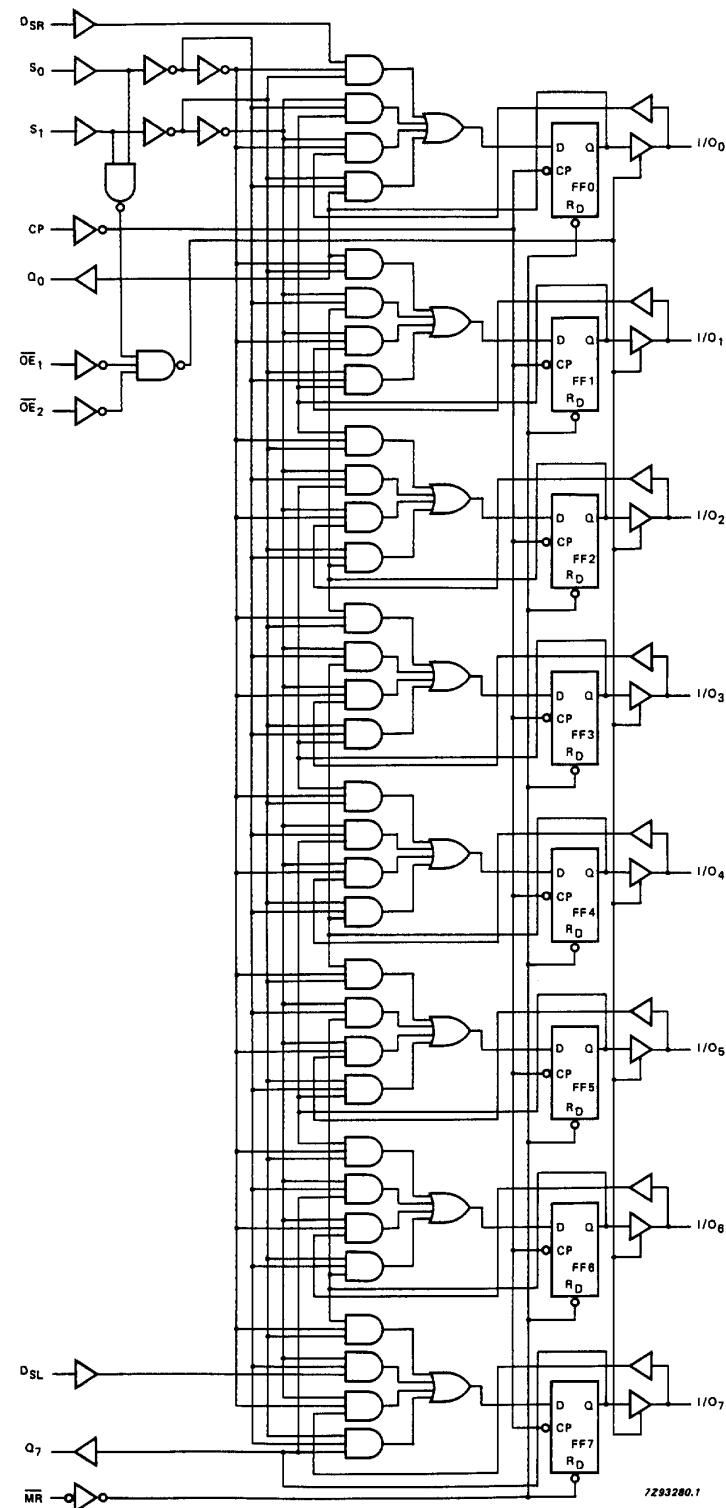


Fig.5 Logic diagram.

8-bit universal shift register; 3-state

74HC/HCT299

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".Output capability: bus driver (parallel I/Os)
standard (serial outputs) I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay CP to Q ₀ , Q ₇	66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6		
t _{PHL} / t _{PLH}	propagation delay CP to I/O _n	66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6		
t _{PHL} /	propagation delay MR to Q ₀ , Q ₇ or I/O _n	66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.7		
t _{PZH}	3-state output enable time OE _n to I/O _n	50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9		
t _{PZL}	3-state output enable time OE _n to I/O _n	41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig.9		
t _{PHZ}	3-state output disable time OE _n to I/O _n	66 24 19	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.9		
t _{PLZ}	3-state output disable time OE _n to I/O _n	55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9		
t _{THL} / t _{TLH}	output transition time bus driver (I/O _n)	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6		
t _{THL} / t _{TLH}	output transition time standard (Q ₀ , Q ₇)	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6		
t _W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.6		
t _W	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.7		

8-bit universal shift register; 3-state

74HC/HCT299

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{rem}	removal time MR to CP	5 5 5	−14 −5 −4		5 5 5		5 5 5		ns	2.0 4.5 6.0		
t _{su}	set-up time D _{SR} , D _{SL} to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0		
t _{su}	set-up time S ₀ , S ₁ to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0		
t _{su}	set-up time I/O _n to CP	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0		
t _h	hold time I/O _n , D _{SR} , D _{SL} to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0		
t _h	hold time S ₀ , S ₁ to CP	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0		
f _{max}	maximum clock pulse frequency	5.0 25 29	15 45 54		4.0 20 24		3.4 17 20		MHz	2.0 4.5 6.0		

8-bit universal shift register; 3-state74HC/HCT299

DC CHARACTERISTICS FOR 74HCTFor the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".Output capability: bus driver (parallel I/Os)
standard (serial outputs)I_{CC} category: MSI**Note to HCT types**The value of additional quiescent supply current (ΔI_{CC}) for unit load of 1 is given in the family specifications.To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I/O _n	0.25
D _{SR} , D _{SL}	0.25
CP, S ₀	0.60
MR, S ₁	0.25
OE _n	0.30

8-bit universal shift register; 3-state

74HC/HCT299

AC CHARACTERISTICS FOR 74HCT

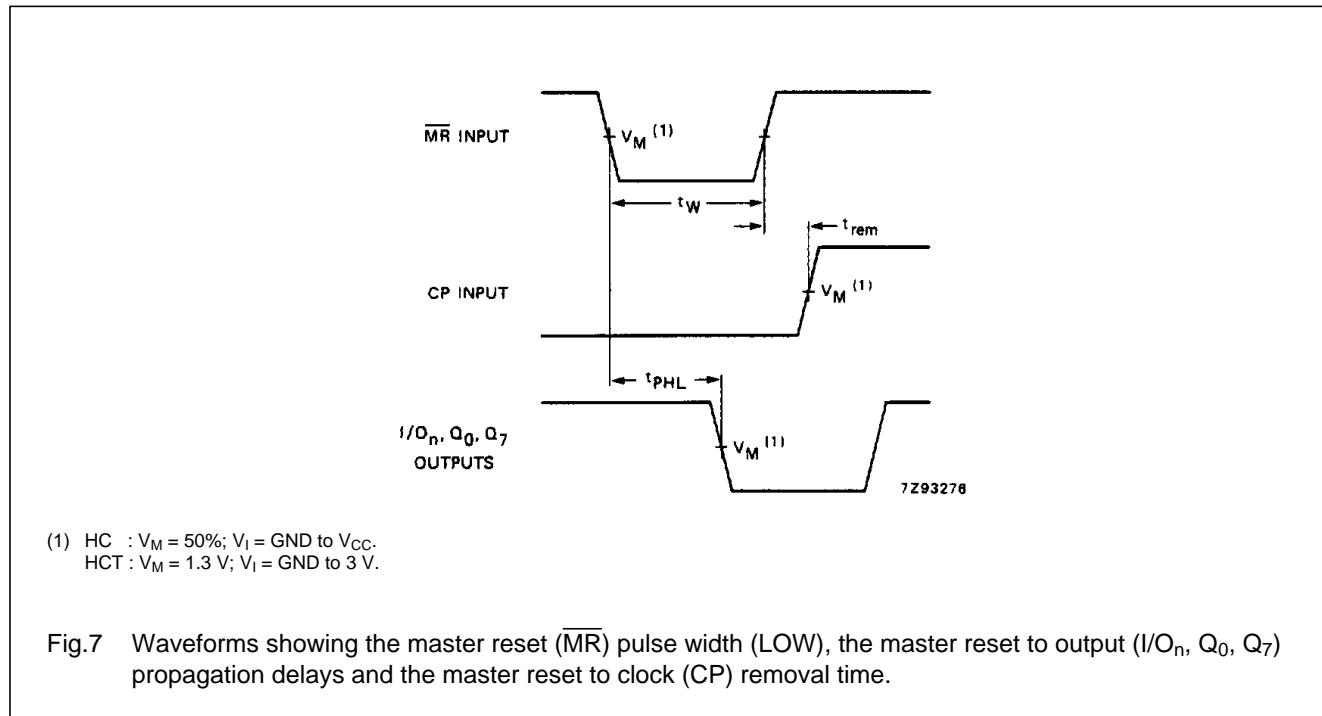
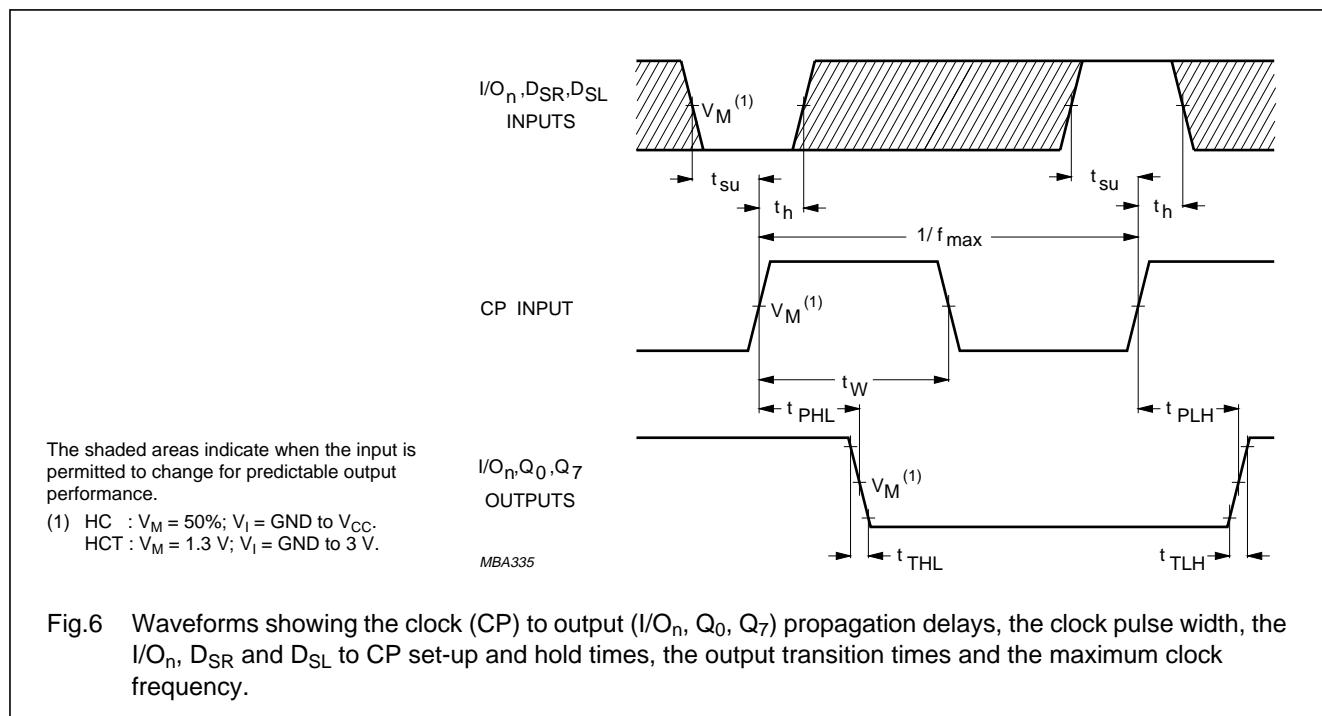
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay CP to Q_0, Q_7	22	37		46		56	ns	4.5	Fig.6		
t_{PHL}/t_{PLH}	propagation delay CP to I/O_n	22	37		46		56	ns	4.5	Fig.6		
t_{PHL}	propagation delay \overline{MR} to Q_0, Q_7 or I/O_n	27	46		58		69	ns	4.5	Fig.7		
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE}_n to I/O_n	19	30		38		45	ns	4.5	Fig.9		
t_{PHZ}	3-state output disable time \overline{OE}_n to I/O_n	24	37		46		56	ns	4.5	Fig.9		
t_{PLZ}	3-state output disable time \overline{OE}_n to I/O_n	20	32		40		48	ns	4.5	Fig.9		
t_{THL}/t_{TLH}	output transition time bus driver (I/O_n)	5	12		15		18	ns	4.5	Fig.6		
t_{THL}/t_{TLH}	output transition time standard (Q_0, Q_7)	7	15		19		22	ns	4.5	Fig.6		
t_W	clock pulse width HIGH or LOW	20	10		25		30	ns	4.5	Fig.6		
t_W	master reset pulse width LOW	20	11		25		30	ns	4.5	Fig.7		
t_{rem}	removal time \overline{MR} to CP	10	2		9		11	ns	4.5	Fig.7		
t_{su}	set-up time $I/O_n, D_{SR}, D_{SL}$ to CP	25	14		31		38	ns	4.5	Fig.6		
t_{su}	set-up time S_0, S_1 to CP	32	18		40		48	ns	4.5	Fig.8		
t_h	hold time $I/O_n, D_{SR}, D_{SL}$ to CP	0	−11		0		0	ns	4.5	Fig.6		
t_h	hold time S_0, S_1 to CP	0	−17		0		0	ns	4.5	Fig.8		
f_{max}	maximum clock pulse frequency	25	42		20		17	MHz	4.5	Fig.6		

8-bit universal shift register; 3-state

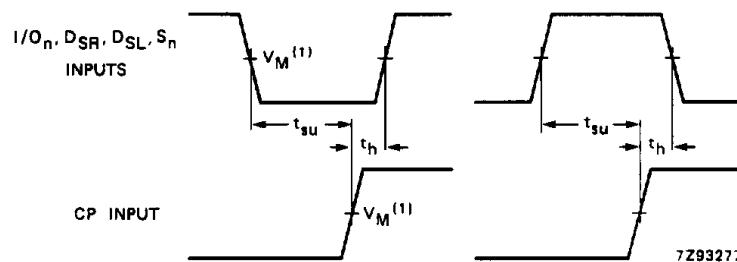
74HC/HCT299

AC WAVEFORMS

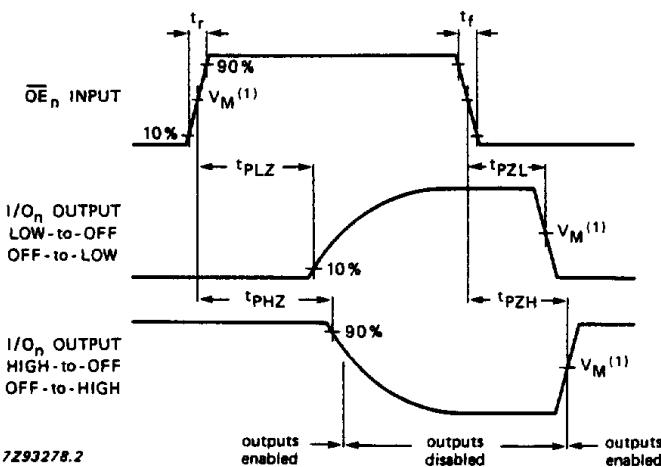


8-bit universal shift register; 3-state

74HC/HCT299



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.8 Waveforms showing the set-up and hold times from the mode control inputs (S_0, S_1) to the clock (CP).

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.9 Waveforms showing the 3-state enable and disable times for \overline{OE}_n inputs.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

MM74HC595

8-Bit Shift Registers with Output Latches

General Description

The MM74HC595 high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

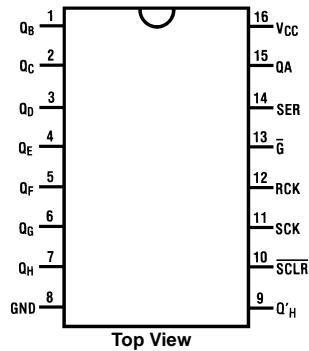
- Low quiescent current: 80 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

Ordering Code:

Order Number	Package Number	Package Description
MM74HC595M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC595SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC595MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC595N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



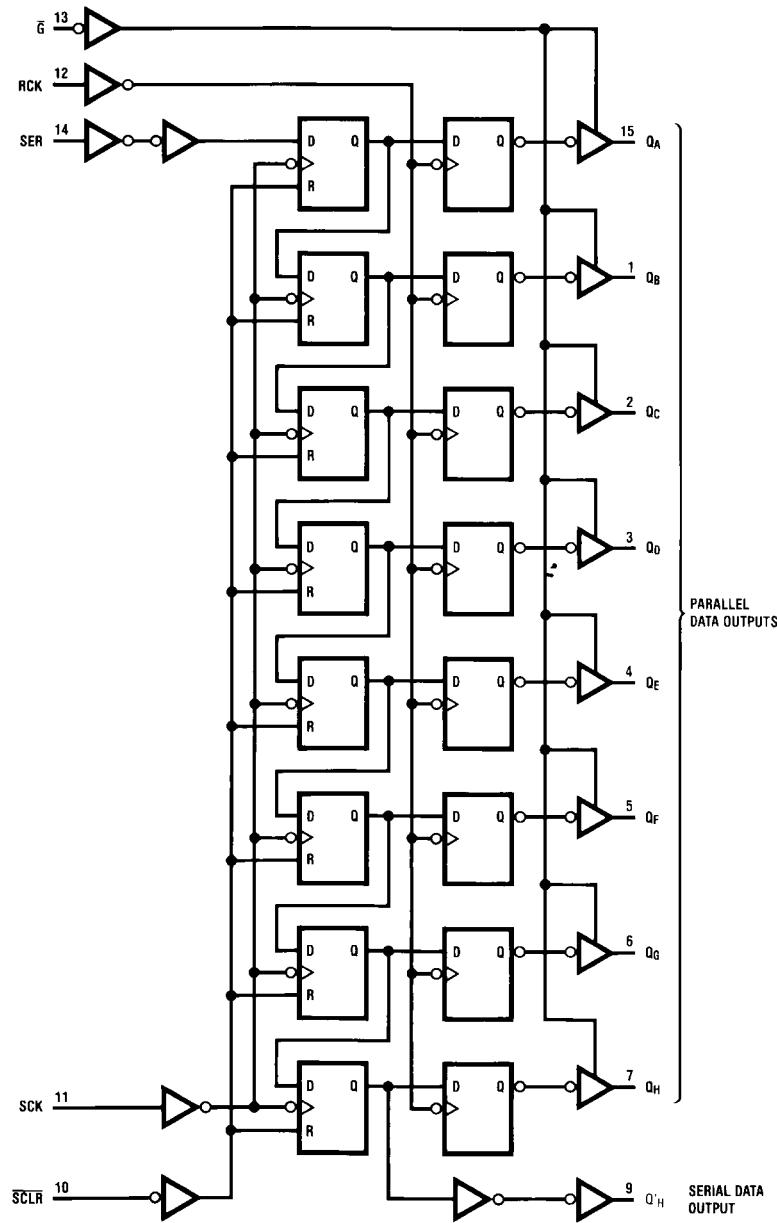
Truth Table

RCK	SCK	SCLR	\bar{G}	Function
X	X	X	H	Q_A thru Q_H = 3-STATE
X	X	L	L	Shift Register cleared $Q'_H = 0$
X	↑	H	L	Shift Register clocked $Q_N = Q_{n-1}$, $Q_0 = SER$
↑	X	H	L	Contents of Shift Register transferred to output latches

MM74HC595

Logic Diagram

(positive logic)



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	-0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Recommended Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})	2	6	V	
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V	
Operating Temperature Range (T_A)	-40	+85	°C	
Input Rise or Fall Times (t_r, t_f)	$V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	1000 500 400	ns	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			$T_A = -40 \text{ to } 85^\circ C$	$T_A = -55 \text{ to } 125^\circ C$	Units
				Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage		2.0V	1.5	1.5	1.5			V
			4.5V	3.15	3.15	3.15			
			6.0V	4.2	4.2	4.2			
V_{IL}	Maximum LOW Level Input Voltage		2.0V	0.5	0.5	0.5			V
			4.5V	1.35	1.35	1.35			
			6.0V	1.8	1.8	1.8			
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9		V
			4.5V	4.5	4.4	4.4	4.4		
			6.0V	6.0	5.9	5.9	5.9		
Q'_H		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0 \text{ mA}$ $ I_{OUT} \leq 5.2 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7		V
			6.0V	5.2	5.48	5.34	5.2		
Q_A thru Q_H		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0 \text{ mA}$ $ I_{OUT} \leq 7.8 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7		V
			6.0V	5.7	5.48	5.34	5.2		
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1		V
			4.5V	0	0.1	0.1	0.1		
			6.0V	0	0.1	0.1	0.1		
Q'_H		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4 \text{ mA}$ $ I_{OUT} \leq 5.2 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4		V
			6.0V	0.2	0.26	0.33	0.4		
Q_A thru Q_H		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0 \text{ mA}$ $ I_{OUT} \leq 7.8 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4		V
			6.0V	0.2	0.26	0.33	0.4		
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0		µA
I_{OZ}	Maximum 3-STATE Output Leakage	$V_{OUT} = V_{CC}$ or GND $G = V_{IH}$	6.0V		±0.5	±5.0	±10		µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160		µA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$, $t_r = t_f = 6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to Q'_H	$C_L = 45\text{ pF}$	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	$C_L = 45\text{ pF}$	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from \bar{G} to Q_A thru Q_H	$R_L = 1\text{ k}\Omega$ $C_L = 45\text{ pF}$	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from \bar{G} to Q_A thru Q_H	$R_L = 1\text{ k}\Omega$ $C_L = 5\text{ pF}$	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
t_S	Minimum Setup Time from SCLR to SCK			20	ns
t_S	Minimum Setup Time from SCK to RCK (Note 5)			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

AC Electrical Characteristics

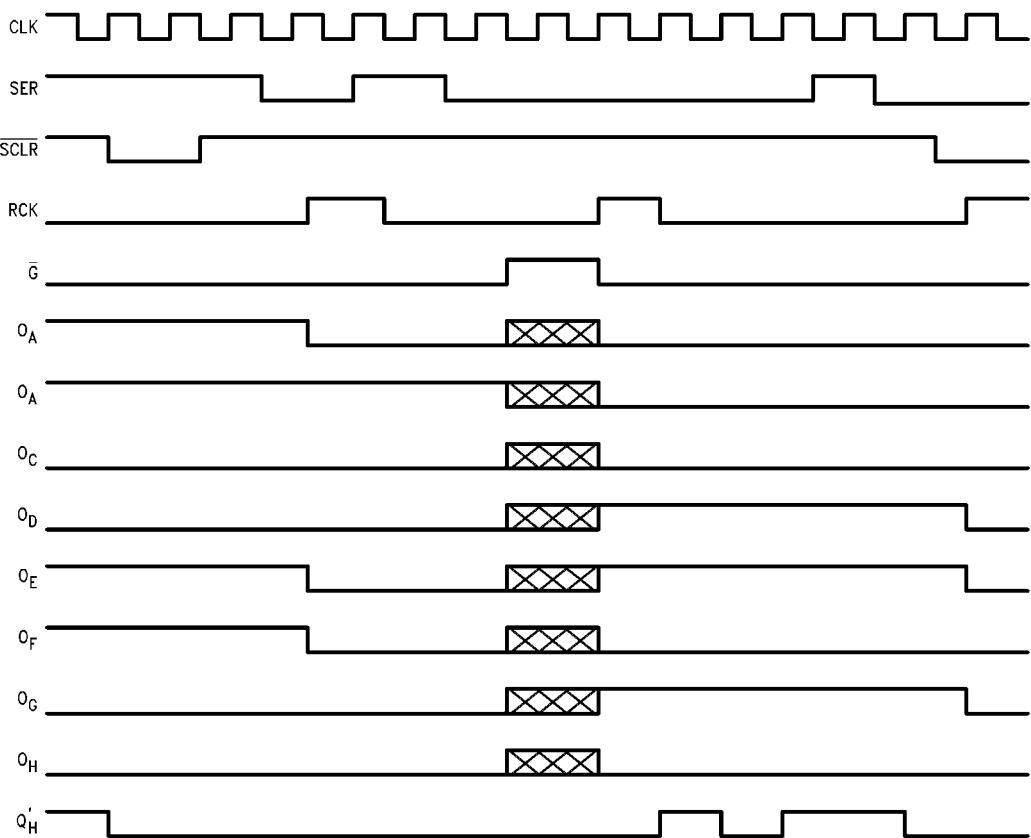
$V_{CC} = 2.0\text{--}6.0V$, $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		$T_A = -40\text{ to }85^\circ C$	$T_A = -55\text{ to }125^\circ C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L = 50\text{ pF}$	2.0V	10	6	4.8	4.0	MHz
			4.5V	45	30	24	20	
			6.0V	50	35	28	24	
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q'_H	$C_L = 50\text{ pF}$	2.0V	58	210	265	315	ns
		$C_L = 150\text{ pF}$	2.0V	83	294	367	441	
		$C_L = 50\text{ pF}$	4.5V	14	42	53	63	ns
		$C_L = 150\text{ pF}$	4.5V	17	58	74	88	
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	$C_L = 50\text{ pF}$	6.0V	10	36	45	54	ns
		$C_L = 150\text{ pF}$	6.0V	14	50	63	76	
		$C_L = 50\text{ pF}$	2.0V	70	175	220	265	ns
		$C_L = 150\text{ pF}$	2.0V	105	245	306	368	
t_{PHL}, t_{PLH}	Maximum Propagation Delay from \bar{G} to Q'_H	$C_L = 50\text{ pF}$	4.5V	21	35	44	53	ns
		$C_L = 150\text{ pF}$	4.5V	28	49	61	74	
		$C_L = 50\text{ pF}$	6.0V	18	30	37	45	ns
		$C_L = 150\text{ pF}$	6.0V	26	42	53	63	
t_{PZH}, t_{PZL}	Maximum Output Enable from \bar{G} to Q_A thru Q_H	$R_L = 1\text{ k}\Omega$	2.0V	75	175	220	265	ns
		$C_L = 50\text{ pF}$	2.0V	100	245	306	368	
		$C_L = 150\text{ pF}$	4.5V	15	35	44	53	ns
		$C_L = 50\text{ pF}$	4.5V	20	49	61	74	
		$C_L = 50\text{ pF}$	6.0V	13	30	37	45	ns
		$C_L = 150\text{ pF}$	6.0V	17	42	53	63	

AC Electrical Characteristics (Continued)

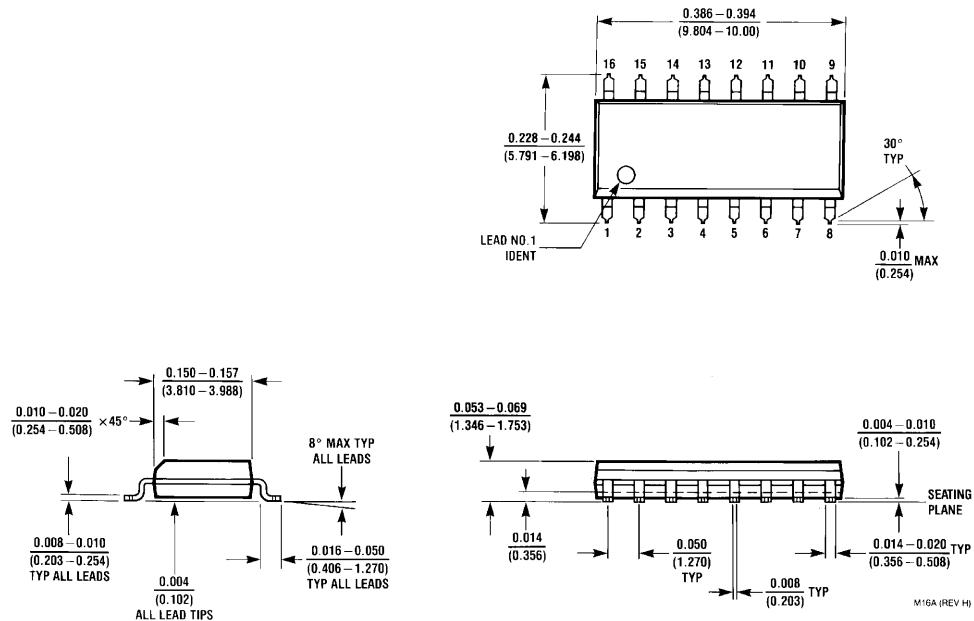
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
				Typ	Guaranteed Limits			
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time from \overline{G} to Q _A thru Q _H	R _L = 1 kΩ C _L = 50 pF	2.0V 4.5V 6.0V	75 15 13	175 35 30	220 44 37	265 53 45	ns
t _S	Minimum Setup Time from SER to SCK		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns
t _R	Minimum Removal Time from SCLR to SCK		2.0V 4.5V 6.0V		50 10 9	63 13 11	75 15 13	ns
t _S	Minimum Setup Time from SCK to RCK		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 26	ns
t _H	Minimum Hold Time SER to SCK		2.0V 4.5V 6.0V		5 5 5	5 5 5	5 5 5	ns
t _W	Minimum Pulse Width of SCK or SCLR		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 22	ns
t _r , t _f	Maximum Input Rise and Fall Time, Clock		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time Q _A -Q _H		2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns
t _{THL} , t _{TLH}	Maximum Output Rise & Fall Time Q' _H		2.0V 4.5V 6.0V		75 15 13	95 19 16	110 22 19	ns
C _{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G} = V_{CC}$ $\overline{G} = GND$		90 150				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF
C _{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 6: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

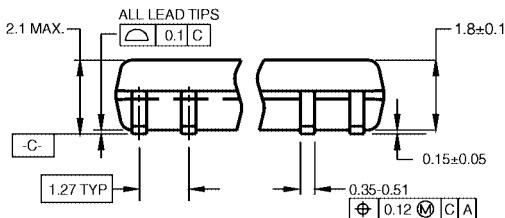
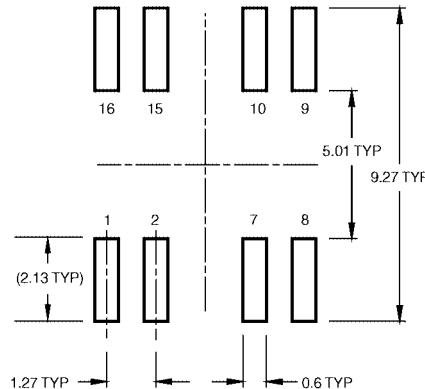
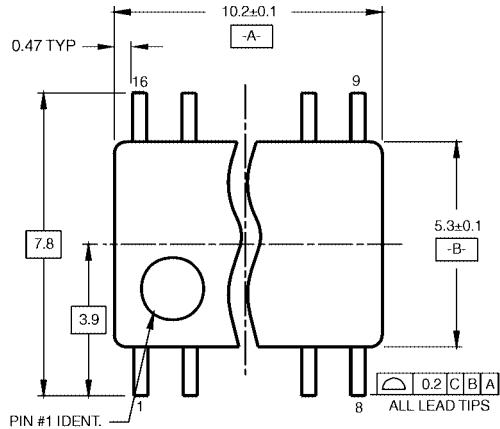
Timing Diagram

NOTE: Implies that the output is in 3 - STATE mode.

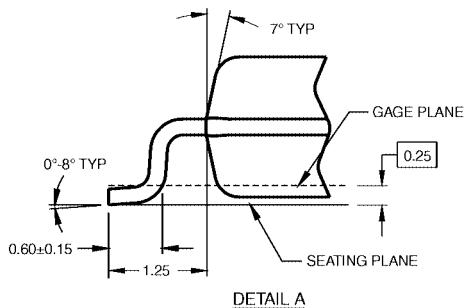
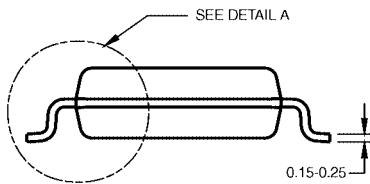
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

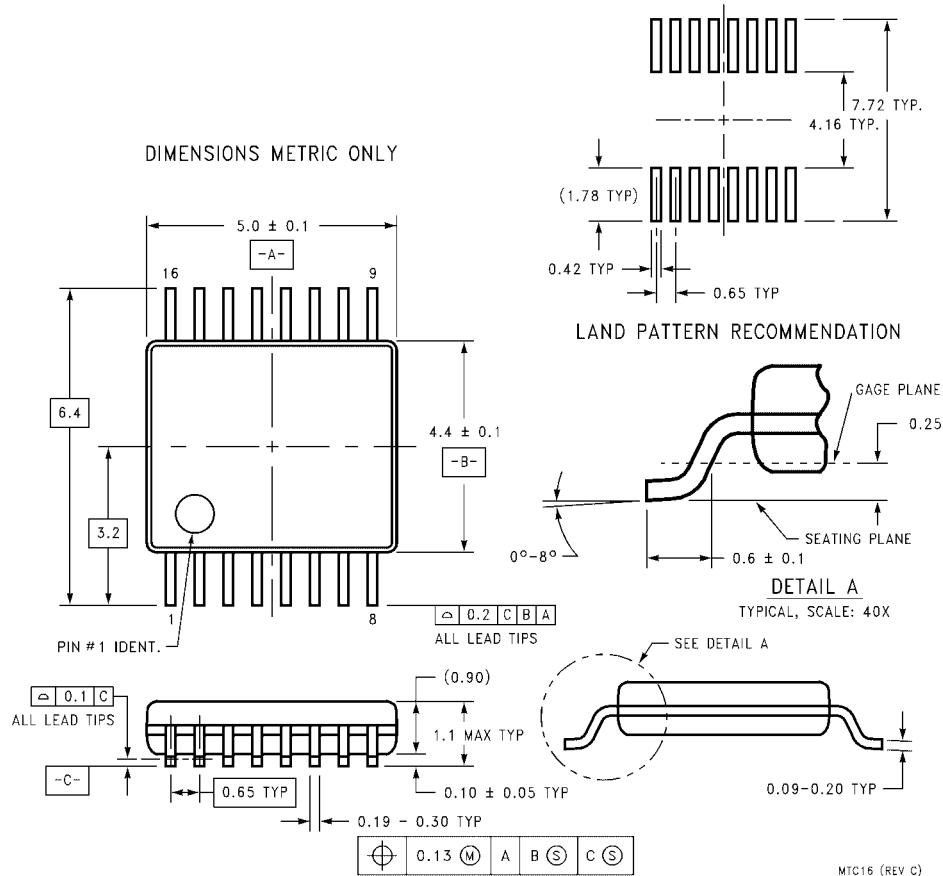
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS



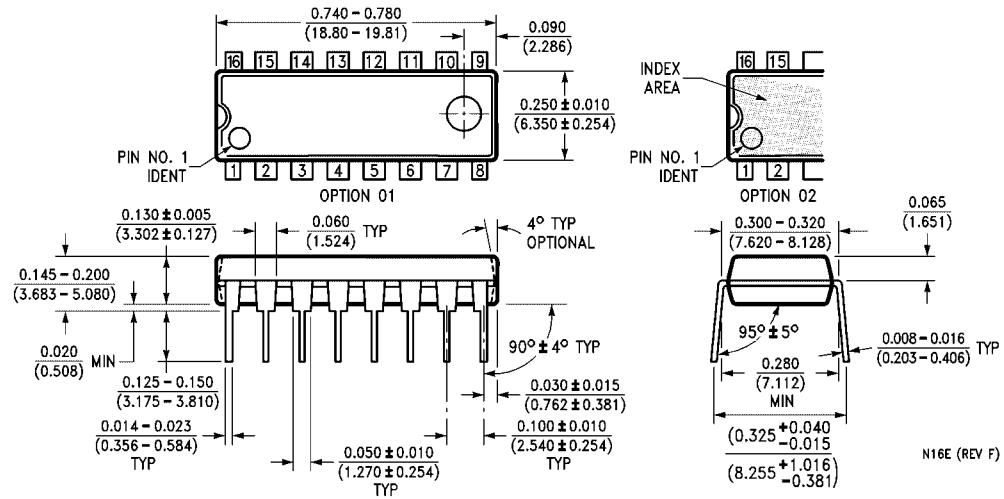
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4514

4-to-16 line decoder/demultiplexer with input latches

Product specification
File under Integrated Circuits, IC06

September 1993

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

FEATURES

- Non-inverting outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with "4514" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3), with latches, a latch enable input (LE), and an active LOW enable input (\bar{E}). The 16 outputs (Q_0 to Q_{15}) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on A_n . When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When \bar{E} is LOW, the selected output, determined by the contents of the latch, is HIGH. At \bar{E} HIGH, all outputs are LOW. The enable input (\bar{E}) does not affect the state of the latch.

When the "4514" is used as a demultiplexer, \bar{E} is the data input and A_0 to A_3 are the address inputs.

QUICK REFERENCE DATA

$GND = 0 \text{ V}$; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	23	26	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	45	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION

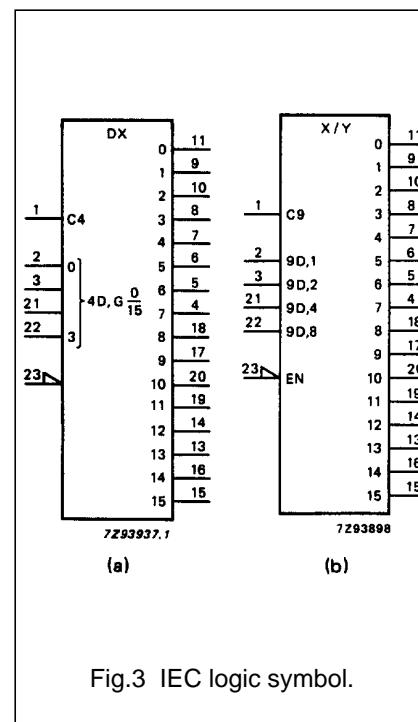
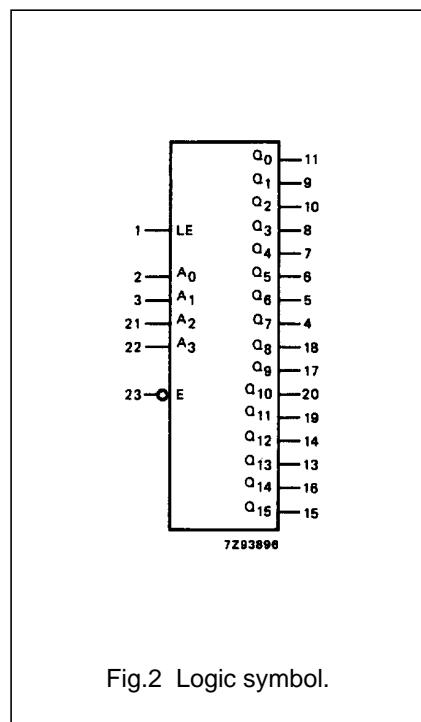
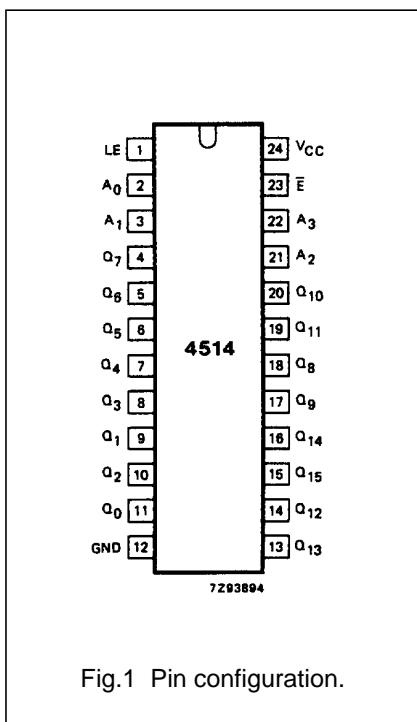
See "[74HC/HCT/HCU/HCMOS Logic Package Information](#)".

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

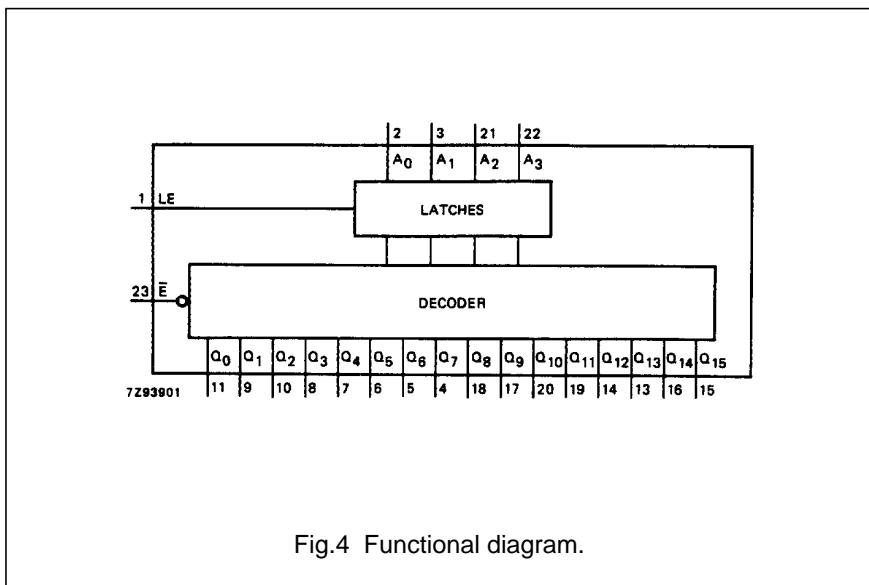
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A ₀ to A ₃	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	Q ₀ to Q ₁₅	multiplexer outputs (active HIGH)
12	GND	ground (0 V)
23	Ē	enable input (active LOW)
24	V _{CC}	positive supply voltage



4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514



APPLICATIONS

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

FUNCTION TABLE

INPUTS					OUTPUTS															
\bar{E}	A ₀	A ₁	A ₂	A ₃	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉	Q ₁₀	Q ₁₁	Q ₁₂	Q ₁₃	Q ₁₄	Q ₁₅
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	H	L	L	L	L	L	H	L	L	L
L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	L	H	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	H	L	L	L	L	H	L	L	H	L

Notes

1. LE = HIGH
H = HIGH voltage level
L = LOW voltage level
X = don't care

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

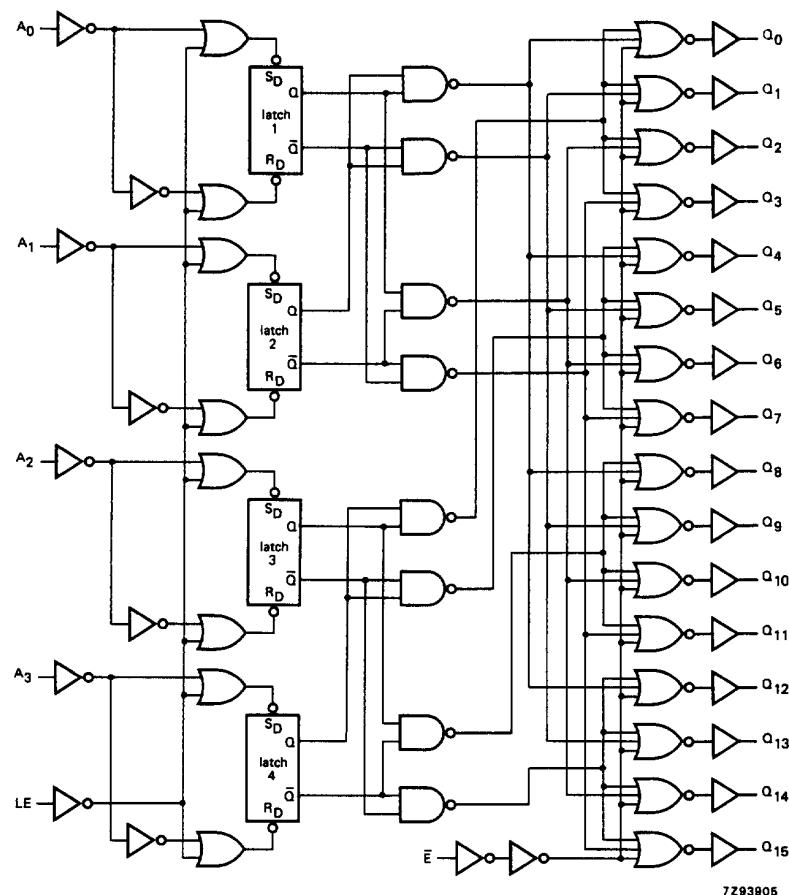


Fig.5 Logic diagram.

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} ($^{\circ}$ C)						UNIT	TEST CONDITIONS			
		74HC							V _{cc} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6	
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6	
t_{PHL}/t_{PLH}	propagation delay \bar{E} to Q_n		41 15 12	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6	
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6	
t_W	latch enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7	
t_{su}	set-up time A_n to LE	90 18 15	25 9 7		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig.7	
t_h	hold time A_n to LE	1 1 1	−11 −4 −3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig.7	

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A_n	0.65
LE	1.40
\bar{E}	1.00

AC CHARACTERISTICS FOR 74HCT

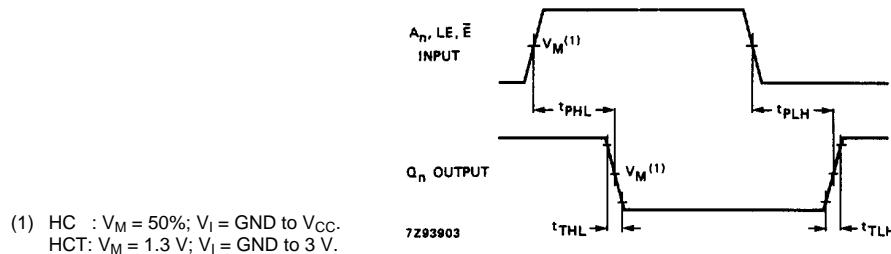
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} ($^{\circ}$ C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n		30	55		69		83	ns	4.5	Fig.6	
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		29	50		63		75	ns	4.5	Fig.6	
t_{PHL}/t_{PLH}	propagation delay \bar{E} to Q_n		17	40		50		60	ns	4.5	Fig.6	
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6	
t_W	latch enable pulse width HIGH	16	4		20		24		ns	4.5	Fig.7	
t_{SU}	set-up time A_n to LE	18	9		23		27		ns	4.5	Fig.7	
t_h	hold time A_n to LE	3	−3		3		3		ns	4.5	Fig.7	

4-to-16 line decoder/demultiplexer with input latches

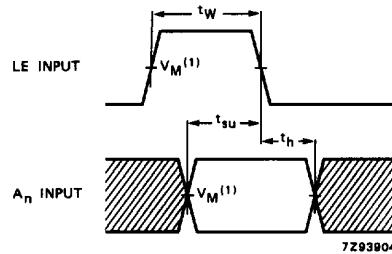
74HC/HCT4514

AC WAVEFORMS

Fig.6 Waveforms showing the input (A_n , LE, \bar{E}) to output (Q_n) propagation delays and the output transition times.

The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n . Set-up and hold times are shown as positive values but may be specified as negative values.

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

APPLICATION INFORMATION

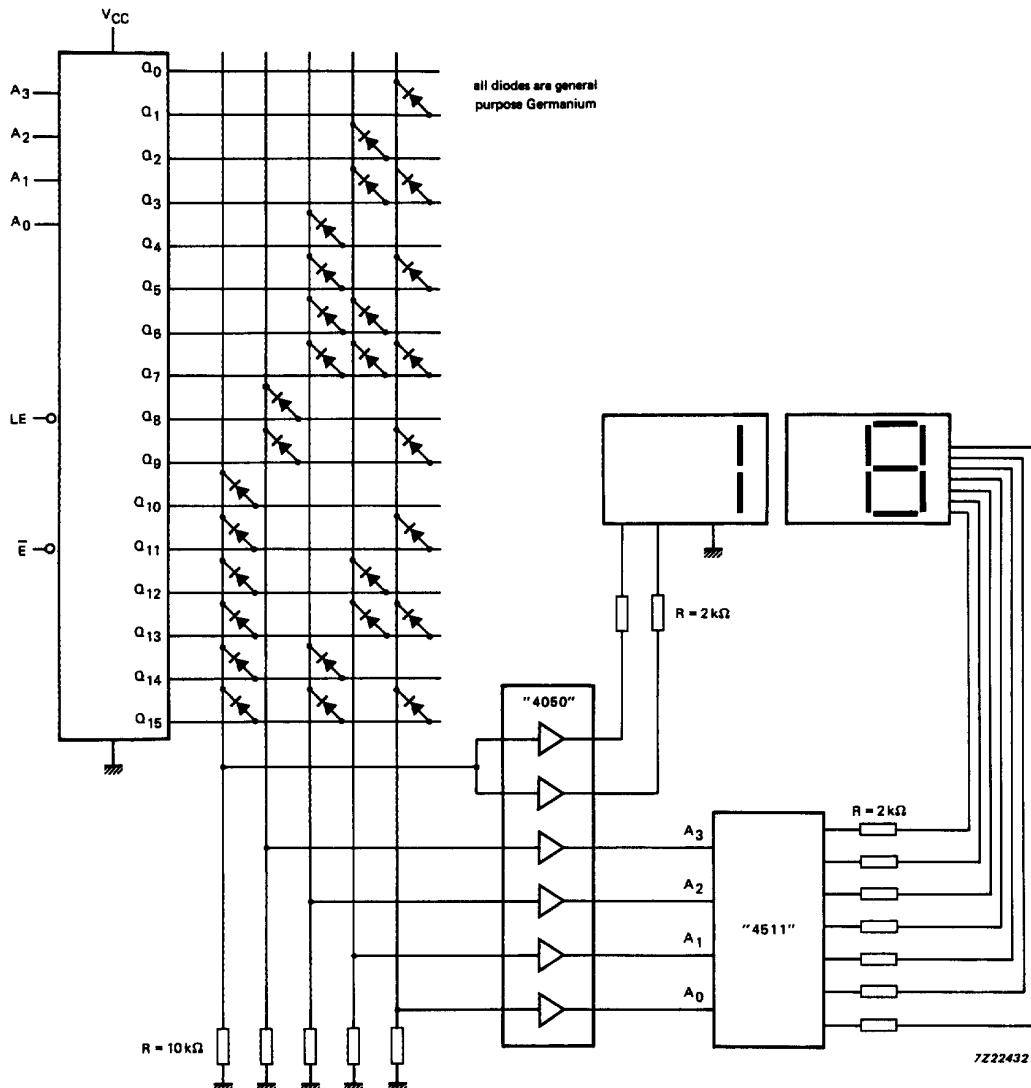


Fig.8 Code-to-code conversion; hexadecimal to BCD.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".



Product Information

74HC/HCT4514; 4-to-16 line decoder/demultiplexer with input latches

Information as of 2002-11-28



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■ General description

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with '4514' of the '4000B' series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3), with latches, a latch enable input (LE), and an active LOW enable input (E). The 16 outputs (Q_0 to Q_{15}) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on A_n . When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When E is LOW, the selected output, determined by the contents of the latch, is HIGH. At E HIGH, all outputs are LOW. The enable input (E) does not affect the state of the latch.

When the '4514' is used as a demultiplexer, E is the data input and A_0 to A_3 are the address inputs.

■ Features

- Non-inverting outputs
- Output capability: standard
- I_{CC} category: MSI

■ Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74HC/HCT4514	4-to-16 line decoder/demultiplexer with input latches	01-Sep-93	Product specification	9	74	Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

Document	Description
1 HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications

■ Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Levels	Output Drive Capability
74HC4514D	SOT137 (SO24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514DB	SOT340-1 (SSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514N	SOT101-1 (DIP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514PW	SOT355-1 (TSSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HC4514U	uncased die	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH	15	5 Volts +	24	Low Power or Battery Applications	CMOS	Low
74HCT4514D	SOT137 (SO24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT4514DB	SOT340-1 (SSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT4514N	SOT101-1 (DIP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low

74HCT4514PW	SOT355-1 (TSSOP24)	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low
74HCT4514U	uncased die	4-of-16 Decoder/Demultiplexer with Input Latches; Outputs LOW at Data Input HIGH; TTL Enabled	15	5 Volts +	24	Low Power or Battery Applications	TTL	Low

■ Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing info	Package	Device status	Buy online
74HC4514D	74HC4514D	9337 156 70652	Standard Marking * Bulk Pack, CECC	SOT137 (SO24)	Full production	BUY ONLINE
	74HC4514D-T	9337 156 70653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT137 (SO24)	Full production	BUY ONLINE
74HC4514DB	74HC4514DB	9351 900 90112	Standard Marking * Bulk Pack	SOT340-1 (SSOP24)	Full production	BUY ONLINE
	74HC4514DB-T	9351 900 90118	Standard Marking * Reel Pack, SMD, 13"	SOT340-1 (SSOP24)	Full production	BUY ONLINE
74HC4514N	74HC4514N	9336 710 40652	Standard Marking * Bulk Pack, CECC	SOT101-1 (DIP24)	Full production	BUY ONLINE
74HC4514PW	74HC4514PW	9352 624 15112	Standard Marking * Bulk Pack	SOT355-1 (TSSOP24)	Full production	BUY ONLINE
	74HC4514PW-T	9352 624 15118	Standard Marking * Reel Pack, SMD, 13"	SOT355-1 (TSSOP24)	Full production	BUY ONLINE
74HC4514U		9338 396 30005	No Marking * Chips on Wafer, Pre-Sawn, On FFC	NAU000	Full production	-
74HCT4514D	74HCT4514D	9337 156 90652	Standard Marking * Bulk Pack, CECC	SOT137 (SO24)	Full production	BUY ONLINE
	74HCT4514D-T	9337 156 90653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT137 (SO24)	Full production	BUY ONLINE
74HCT4514DB	74HCT4514DB	9351 900 80112	Standard Marking * Bulk Pack	SOT340-1 (SSOP24)	Full production	BUY ONLINE
	74HCT4514DB-T	9351 900 80118	Standard Marking * Reel Pack, SMD, 13"	SOT340-1 (SSOP24)	Full production	BUY ONLINE
74HCT4514N	74HCT4514N	9336 710 70652	Standard Marking * Bulk Pack, CECC	SOT101-1 (DIP24)	Full production	BUY ONLINE

74HCT4514PW	74HCT4514PW	9352 624 14112	Standard Marking * Bulk Pack	SOT355-1 (TSSOP24)	Full production	BUY ONLINE	
	74HCT4514PW-T	9352 624 14118	Standard Marking * Reel Pack, SMD, 13"	SOT355-1 (TSSOP24)	Full production	BUY ONLINE	
74HCT4514U		9338 396 40005	No Marking * Chips on Wafer, Pre-Sawn, On FFC	NAU000	Full production	-	-

Products in the above table are all in production. Some variants are discontinued; [click here](#) for information on these variants.

▣ Similar products

[+MORE](#) [74HC/HCT4514](#) links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

▣ Support & tools

[+PDF](#) [HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications](#) (date 01-Mar-98)
[+PDF](#) [HC/T User Guide](#) (date 01-Nov-97)

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LM555 Timer

1 Features

- Direct Replacement for SE555/NE555
 - Timing from Microseconds through Hours
 - Operates in Both Astable and Monostable Modes
 - Adjustable Duty Cycle
 - Output Can Source or Sink 200 mA
 - Output and Supply TTL Compatible
 - Temperature Stability Better than 0.005% per °C
 - Normally On and Normally Off Output
 - Available in 8-pin VSSOP Package

2 Applications

- Precision Timing
 - Pulse Generation
 - Sequential Timing
 - Time Delay Generation
 - Pulse Width Modulation
 - Pulse Position Modulation
 - Linear Ramp Generator

3 Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

Device Information⁽¹⁾

DEVICE INFORMATION		
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM555	SOIC (8)	4.90 mm x 3.91 mm
	PDIP (8)	9.81 mm x 6.35 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Schematic Diagram

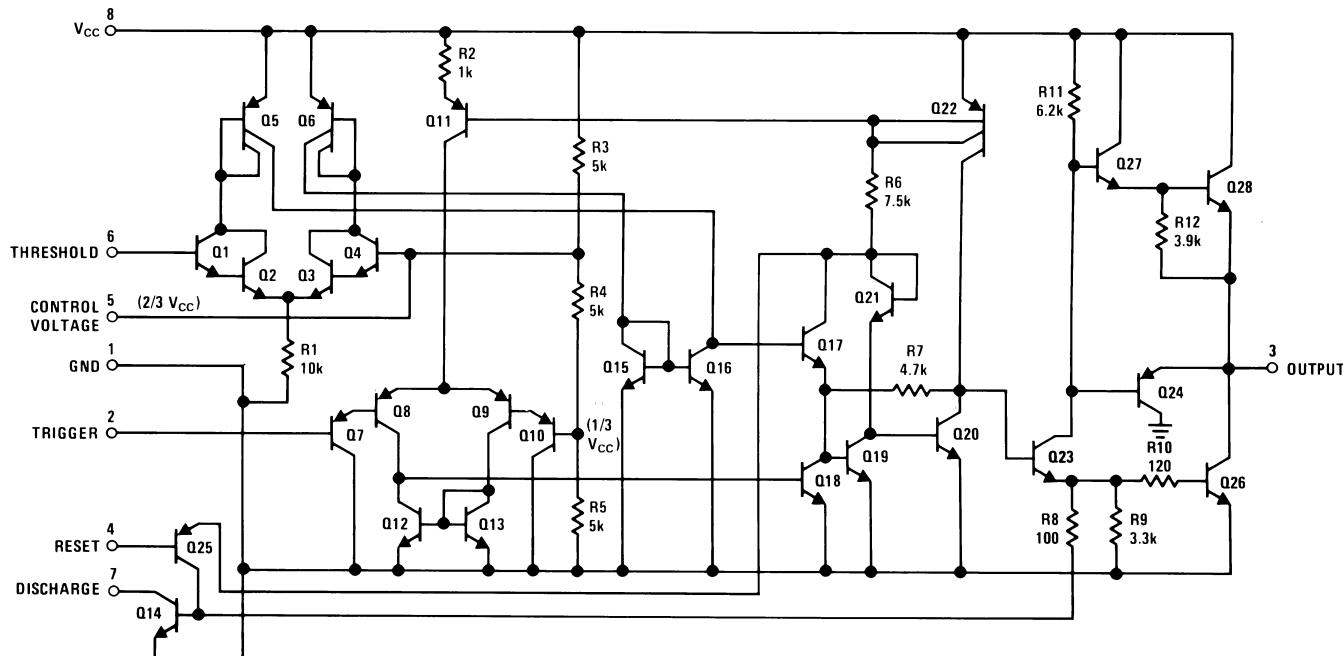


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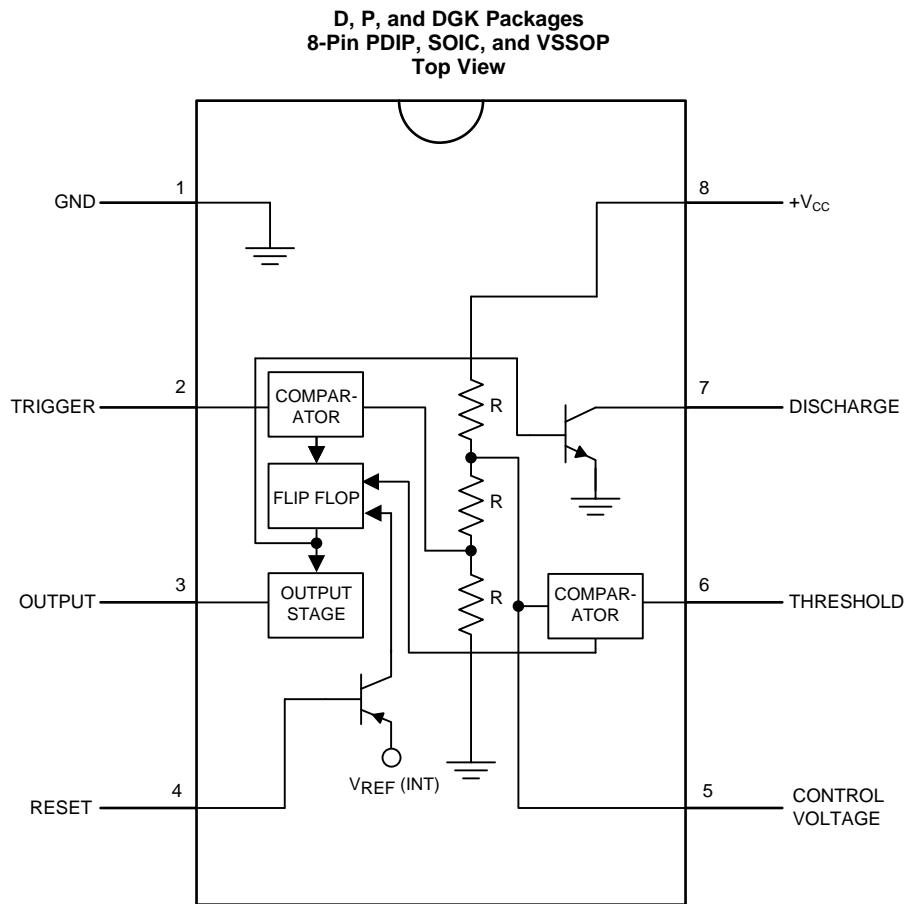
1 Features	1	7.3 Feature Description.....	8
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4 Revision History

Changes from Revision C (March 2013) to Revision D	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
5	Control Voltage	I	Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform
7	Discharge	I	Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of the supply voltage
1	GND	O	Ground reference voltage
3	Output	O	Output driven waveform
4	Reset	I	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to VCC to avoid false triggering
6	Threshold	I	Compares the voltage applied to the terminal with a reference voltage of 2/3 Vcc. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop
2	Trigger	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin
8	V ⁺	I	Supply voltage with respect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

			MIN	MAX	UNIT
Power Dissipation ⁽³⁾	LM555CM, LM555CN ⁽⁴⁾		1180	mW	
	LM555CMM		613	mW	
Soldering Information	PDIP Package	Soldering (10 Seconds)	260	°C	
	Small Outline Packages (SOIC and VSSOP)	Vapor Phase (60 Seconds)	215	°C	
		Infrared (15 Seconds)	220	°C	
Storage temperature, T _{stg}			-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) For operating at elevated temperatures the device must be derated above 25°C based on a 150°C maximum junction temperature and a thermal resistance of 106°C/W (PDIP), 170°C/W (SOIC-8), and 204°C/W (VSSOP) junction to ambient.
- (4) Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500 ⁽²⁾ V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) The ESD information listed is for the SOIC package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage		18	V
Temperature, T _A	0	70	°C
Operating junction temperature, T _J		70	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM555			UNIT
	PDIP	SOIC	VSSOP	
	8 PINS			
R _{θJA} Junction-to-ambient thermal resistance	106	170	204	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

($T_A = 25^\circ\text{C}$, $V_{CC} = 5 \text{ V}$ to 15 V , unless otherwise specified)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		4.5	16		V
Supply Current	$V_{CC} = 5 \text{ V}$, $R_L = \infty$		3	6	mA
	$V_{CC} = 15 \text{ V}$, $R_L = \infty$ (Low State) ⁽³⁾		10	15	
Timing Error, Monostable					
Initial Accuracy			1 %		
Drift with Temperature	$R_A = 1 \text{ k}$ to $100 \text{ k}\Omega$,		50		ppm/ $^\circ\text{C}$
	$C = 0.1 \mu\text{F}$, ⁽⁴⁾				
Accuracy over Temperature			1.5 %		
Drift with Supply			0.1 %		V
Timing Error, Astable					
Initial Accuracy			2.25		
Drift with Temperature	$R_A, R_B = 1 \text{ k}$ to $100 \text{ k}\Omega$,		150		ppm/ $^\circ\text{C}$
	$C = 0.1 \mu\text{F}$, ⁽⁴⁾				
Accuracy over Temperature			3.0%		
Drift with Supply			0.30 %		/V
Threshold Voltage			0.667		$\times V_{CC}$
Trigger Voltage	$V_{CC} = 15 \text{ V}$		5		V
	$V_{CC} = 5 \text{ V}$		1.67		V
Trigger Current		0.5	0.9		μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(5)		0.1	0.25	μA
Control Voltage Level	$V_{CC} = 15 \text{ V}$	9	10	11	V
	$V_{CC} = 5 \text{ V}$	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat ⁽⁶⁾					
Output Low	$V_{CC} = 15 \text{ V}$, $I_7 = 15 \text{ mA}$		180		mV
Output Low	$V_{CC} = 4.5 \text{ V}$, $I_7 = 4.5 \text{ mA}$		80	200	mV
Output Voltage Drop (Low)	$V_{CC} = 15 \text{ V}$				
	$I_{SINK} = 10 \text{ mA}$		0.1	0.25	V
	$I_{SINK} = 50 \text{ mA}$		0.4	0.75	V
	$I_{SINK} = 100 \text{ mA}$		2	2.5	V
	$I_{SINK} = 200 \text{ mA}$		2.5		V
	$V_{CC} = 5 \text{ V}$				
	$I_{SINK} = 8 \text{ mA}$				V
	$I_{SINK} = 5 \text{ mA}$		0.25	0.35	V

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Recommended Operating Conditions*. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (3) Supply current when output high typically 1 mA less at $V_{CC} = 5 \text{ V}$.
- (4) Tested at $V_{CC} = 5 \text{ V}$ and $V_{CC} = 15 \text{ V}$.
- (5) This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total ($R_A + R_B$) is 20 M Ω .
- (6) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Electrical Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ to 15 V , unless otherwise specified)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Drop (High)	$I_{SOURCE} = 200\text{ mA}$, $V_{CC} = 15\text{ V}$			12.5	V
	$I_{SOURCE} = 100\text{ mA}$, $V_{CC} = 15\text{ V}$	12.75	13.3		V
	$V_{CC} = 5\text{ V}$	2.75	3.3		V
Rise Time of Output		100			ns
Fall Time of Output		100			ns

6.6 Typical Characteristics

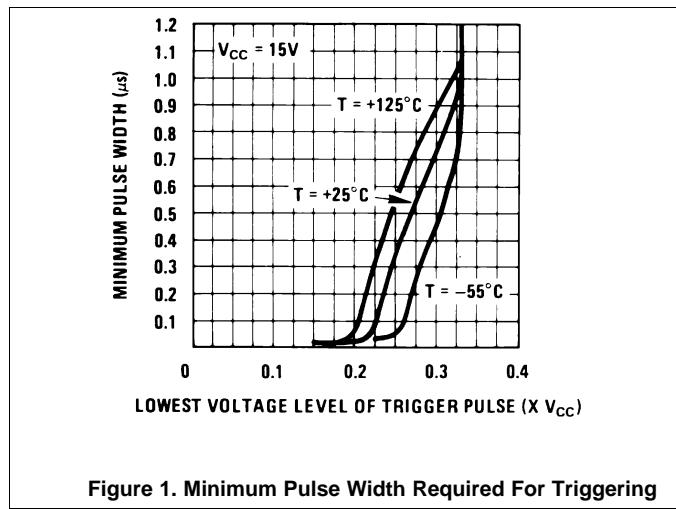


Figure 1. Minimum Pulse Width Required For Triggering

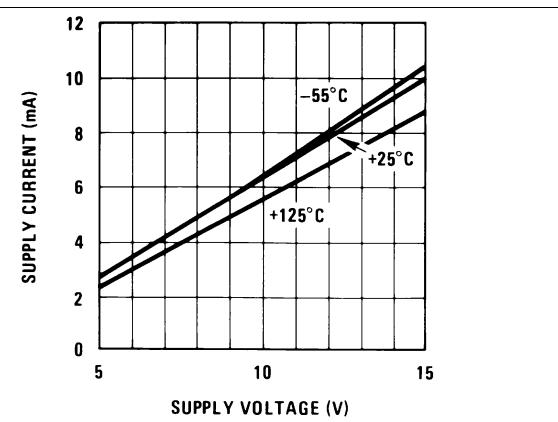


Figure 2. Supply Current vs. Supply Voltage

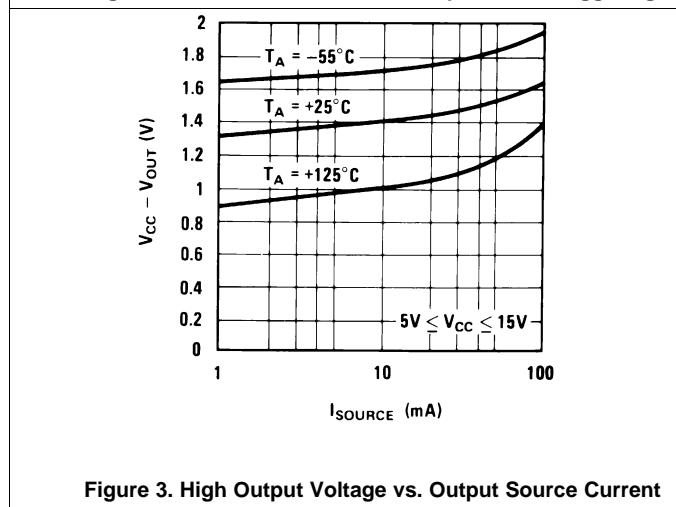


Figure 3. High Output Voltage vs. Output Source Current

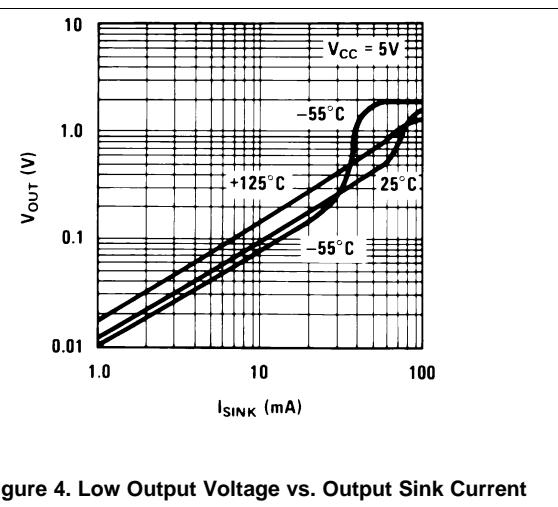


Figure 4. Low Output Voltage vs. Output Sink Current

Typical Characteristics (continued)

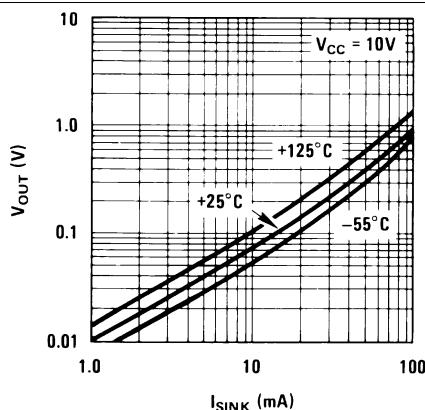


Figure 5. Low Output Voltage vs. Output Sink Current

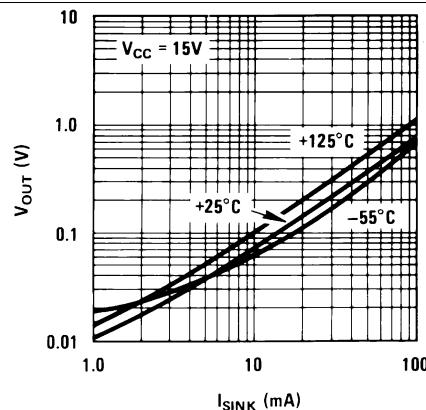


Figure 6. Low Output Voltage vs. Output Sink Current

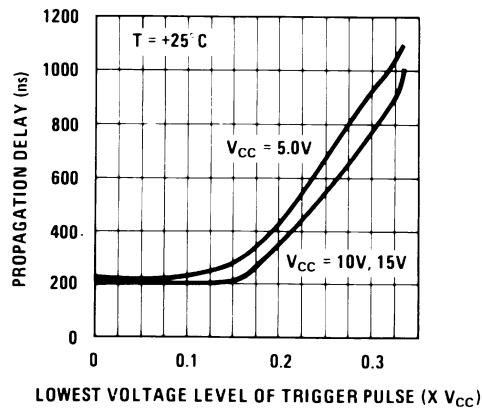


Figure 7. Output Propagation Delay vs. Voltage Level of Trigger Pulse

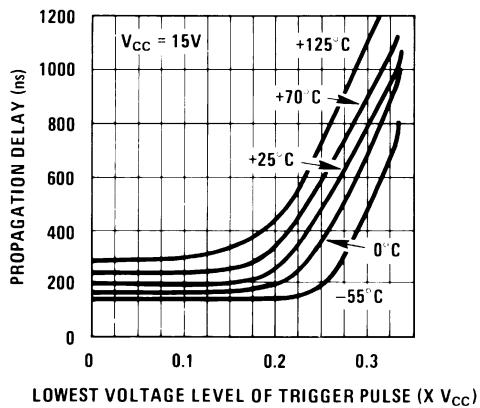


Figure 8. Output Propagation Delay vs. Voltage Level of Trigger Pulse

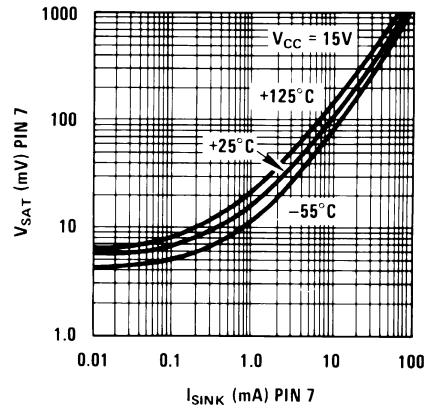


Figure 9. Discharge Transistor (Pin 7) Voltage vs. Sink Current

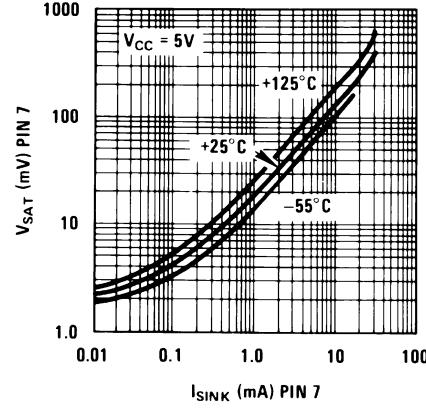


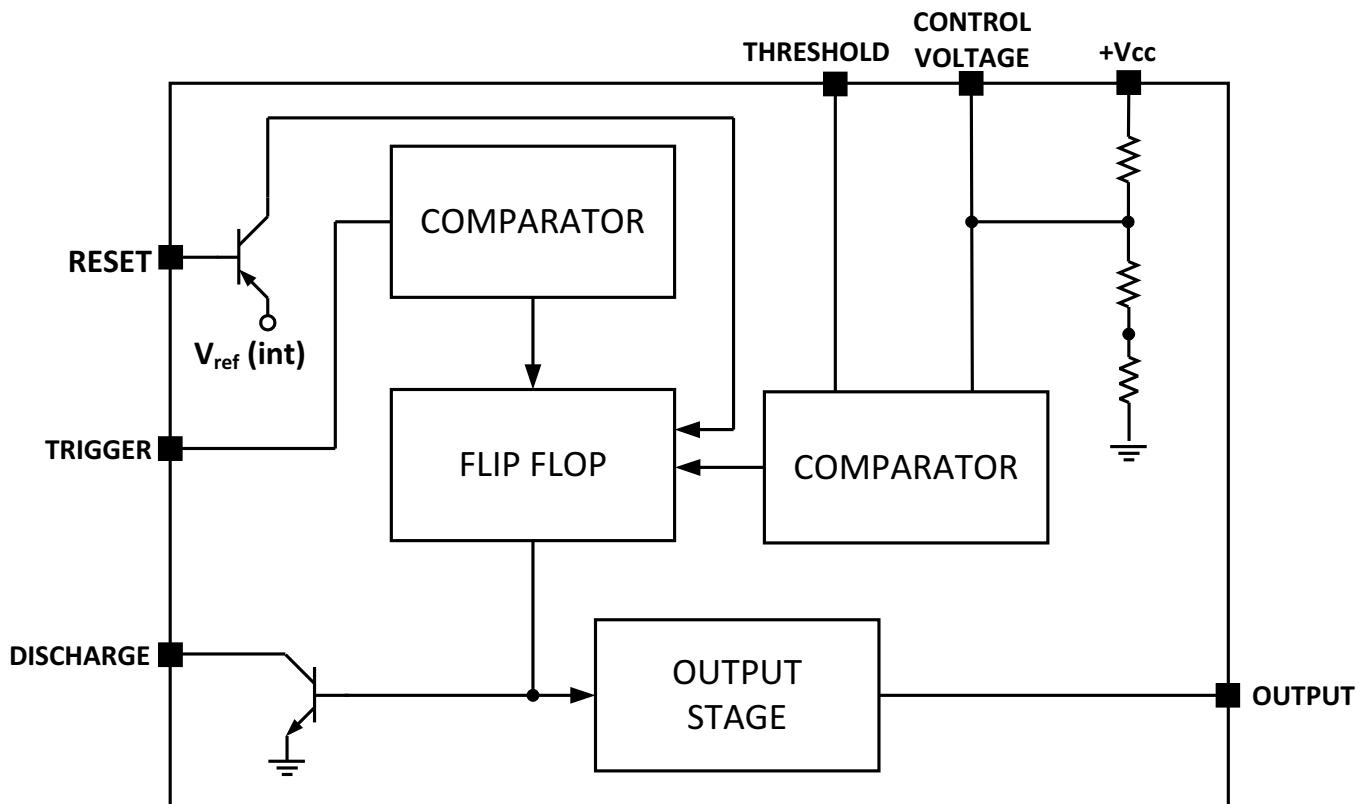
Figure 10. Discharge Transistor (Pin 7) Voltage vs. Sink Current

7 Detailed Description

7.1 Overview

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits. The LM555 are available in 8-pin PDIP, SOIC, and VSSOP packages and is a direct replacement for SE555/NE555.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Direct Replacement for SE555/NE555

The LM555 timer is a direct replacement for SE555 and NE555. It is pin-to-pin compatible so that no schematic or layout changes are necessary. The LM555 come in an 8-pin PDIP, SOIC, and VSSOP package.

7.3.2 Timing From Microseconds Through Hours

The LM555 has the ability to have timing parameters from the microseconds range to hours. The time delay of the system can be determined by the time constant of the R and C value used for either the monostable or astable configuration. A nomograph is available for easy determination of R and C values for various time delays.

7.3.3 Operates in Both Astable and Monostable Mode

The LM555 can operate in both astable and monostable mode depending on the application requirements.

- Monostable mode: The LM555 timer acts as a “one-shot” pulse generator. The pulse begins when the LM555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the

Feature Description (continued)

capacitor equals 2/3 of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.

- Astable (free-running) mode: The LM555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of R_A , R_B , and C .

7.4 Device Functional Modes

7.4.1 Monostable Operation

In this mode of operation, the timer functions as a one-shot (Figure 11). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

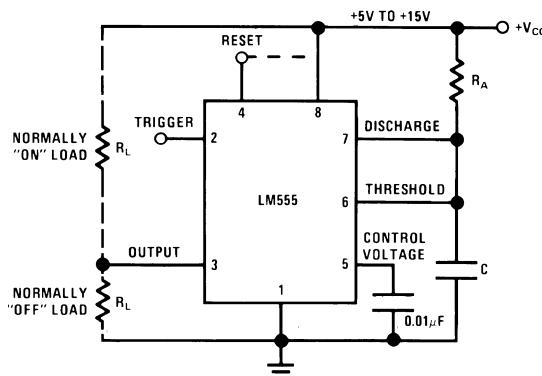


Figure 11. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1 R_A C$, at the end of which time the voltage equals 2/3 V_{CC} . The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 12 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_{CC} = 5\text{ V}$
TIME = 0.1 ms/DIV.
 $R_A = 9.1\text{ k}\Omega$
 $C = 0.01\text{ }\mu\text{F}$

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

Figure 12. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, TI recommends connecting the Reset pin to V_{CC} to avoid any possibility of false triggering.

Device Functional Modes (continued)

Figure 13 is a nomograph for easy determination of R, C values for various time delays.

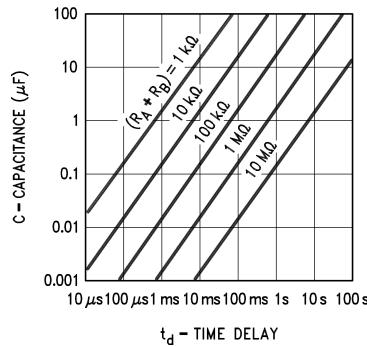


Figure 13. Time Delay

7.4.2 Astable Operation

If the circuit is connected as shown in Figure 14 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B . Thus the duty cycle may be precisely set by the ratio of these two resistors.

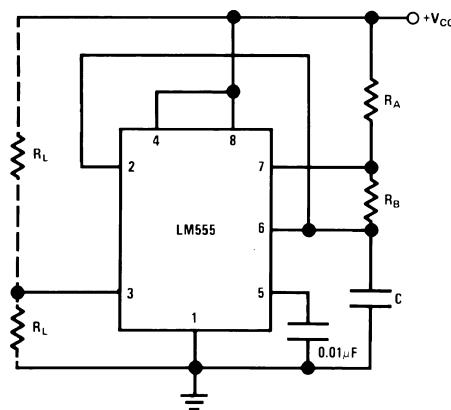
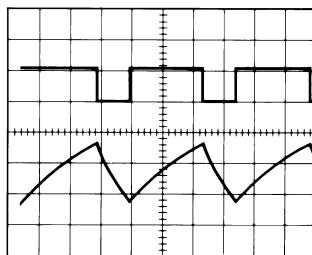


Figure 14. Astable

In this mode of operation, the capacitor charges and discharges between $1/3 V_{CC}$ and $2/3 V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 15 shows the waveforms generated in this mode of operation.

Device Functional Modes (continued)



$V_{CC} = 5 \text{ V}$
TIME = $20\mu\text{s}/\text{DIV.}$
 $R_A = 3.9 \text{ k}\Omega$
 $R_B = 3 \text{ k}\Omega$
 $C = 0.01 \mu\text{F}$
Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

Figure 15. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C} \quad (4)$$

Figure 16 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

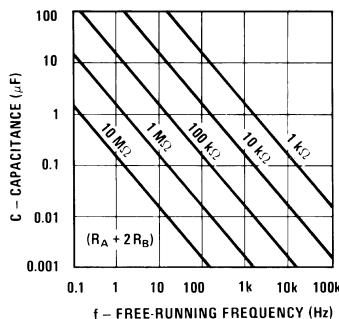


Figure 16. Free Running Frequency

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM555 timer can be used in various configurations, but the most commonly used configuration is in monostable mode. A typical application for the LM555 timer in monostable mode is to turn on an LED for a specific time duration. A pushbutton is used as the trigger to output a high pulse when trigger pin is pulsed low. This simple application can be modified to fit any application requirement.

8.2 Typical Application

[Figure 17](#) shows the schematic of the LM555 that flashes an LED in monostable mode.

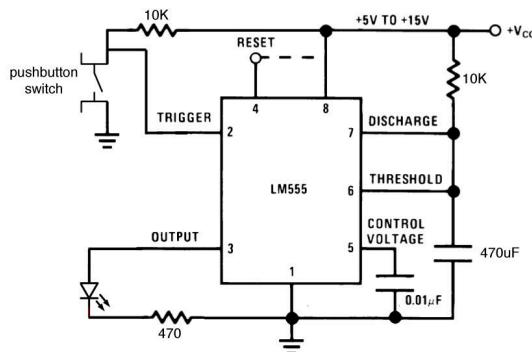


Figure 17. Schematic of Monostable Mode to Flash an LED

8.2.1 Design Requirements

The main design requirement for this application requires calculating the duration of time for which the output stays high. The duration of time is dependent on the R and C values (as shown in [Figure 17](#)) and can be calculated by:

$$t = 1.1 \times R \times C \text{ seconds} \quad (6)$$

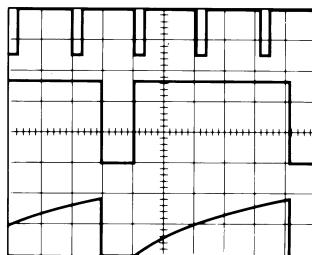
8.2.2 Detailed Design Procedure

To allow the LED to flash on for a noticeable amount of time, a 5 second time delay was chosen for this application. By using [Equation 6](#), RC equals 4.545. If R is selected as 100 kΩ, C = 45.4 μF. The values of R = 100 kΩ and C = 47 μF were selected based on standard values of resistors and capacitors. A momentary push button switch connected to ground is connected to the trigger input with a 10-K current limiting resistor pullup to the supply voltage. When the push button is pressed, the trigger pin goes to GND. An LED is connected to the output pin with a current limiting resistor in series from the output of the LM555 to GND. The reset pin is not used and was connected to the supply voltage.

8.2.2.1 Frequency Divider

The monostable circuit of [Figure 11](#) can be used as a frequency divider by adjusting the length of the timing cycle. [Figure 18](#) shows the waveforms generated in a divide by three circuit.

Typical Application (continued)



$V_{CC} = 5 \text{ V}$ Top Trace: Input 4 V/Div.
 TIME = 20 $\mu\text{s}/\text{DIV}$. Middle Trace: Output 2V/Div.
 $R_A = 9.1 \text{ k}\Omega$ Bottom Trace: Capacitor 2V/Div.
 $C = 0.01 \mu\text{F}$

Figure 18. Frequency Divider

8.2.2.2 Additional Information

Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs , typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

8.2.3 Application Curves

The data shown below was collected with the circuit used in the typical applications section. The LM555 was configured in the monostable mode with a time delay of 5.17 s. The waveforms correspond to:

- Top Waveform (Yellow) – Capacitor voltage
- Middle Waveform (Green) – Trigger
- Bottom Waveform (Purple) – Output

As the trigger pin pulses low, the capacitor voltage starts charging and the output goes high. The output goes low as soon as the capacitor voltage reaches 2/3 of the supply voltage, which is the time delay set by the R and C value. For this example, the time delay is 5.17 s.

Typical Application (continued)

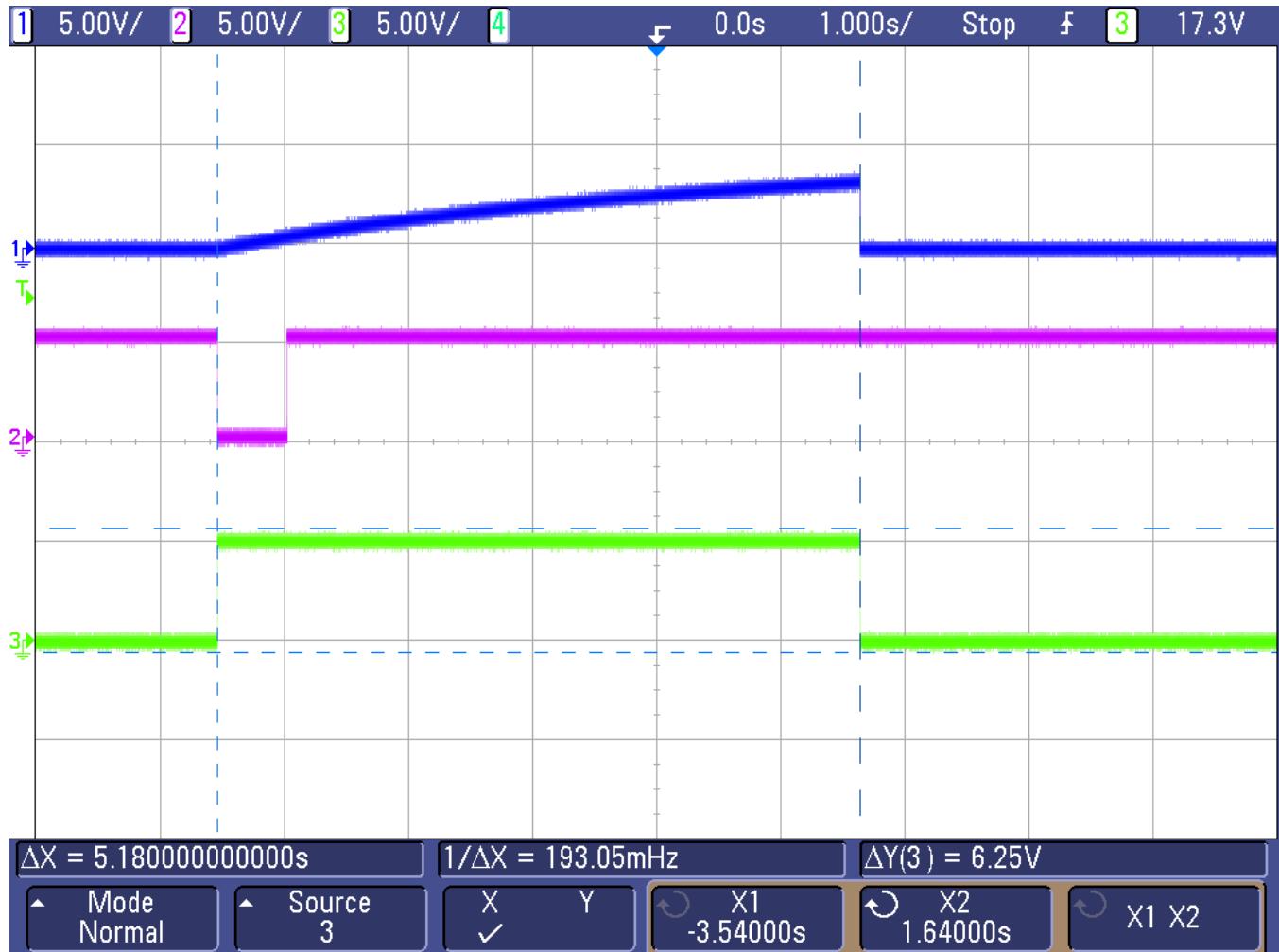


Figure 19. Trigger, Capacitor Voltage, and Output Waveforms in Monostable Mode

9 Power Supply Recommendations

The LM555 requires a voltage supply within 4.5 V to 16 V. Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended capacitor value is 0.1 μ F in parallel with a 1- μ F electrolytic capacitor. Place the bypass capacitors as close as possible to the LM555 and minimize the trace length.

10 Layout

10.1 Layout Guidelines

Standard PCB rules apply to routing the LM555. The 0.1- μ F capacitor in parallel with a 1- μ F electrolytic capacitor should be as close as possible to the LM555. The capacitor used for the time delay should also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 20 is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01- μ F bypass capacitor for control voltage pin
- C3 – 0.1- μ F bypass ceramic capacitor
- C4 – 1- μ F electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

10.2 Layout Example

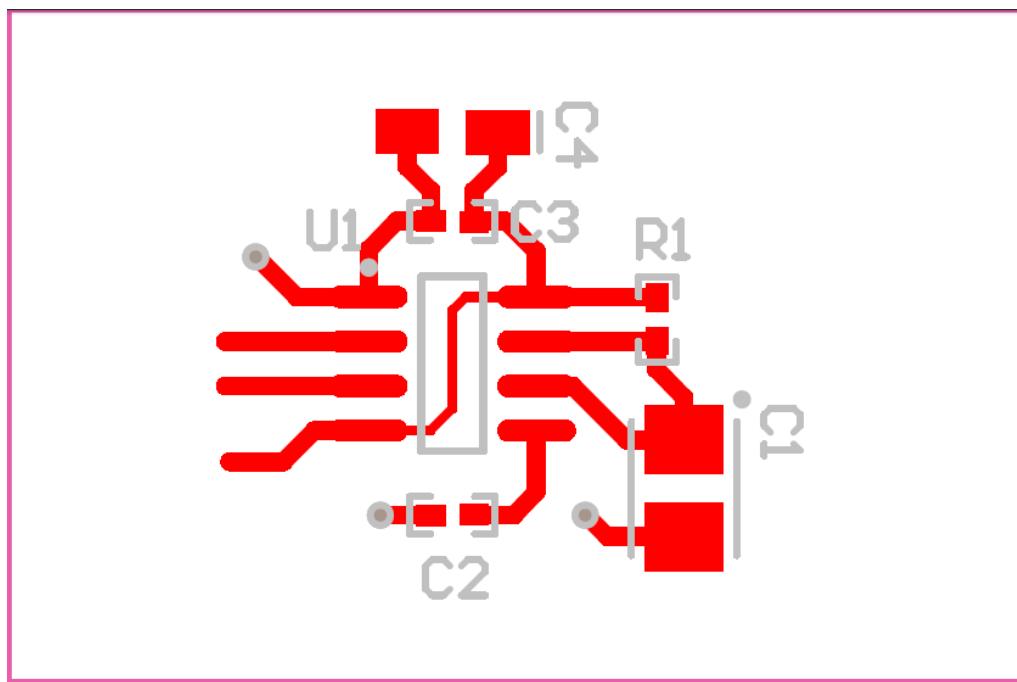


Figure 20. Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM555CM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 555CM	
LM555CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 555CM	Samples
LM555CMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	0 to 70	Z55	
LM555CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	Z55	Samples
LM555CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	Z55	Samples
LM555CMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM 555CM	
LM555CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 555CM	Samples
LM555CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 555CN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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PACKAGE OPTION ADDENDUM

29-Jun-2017

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

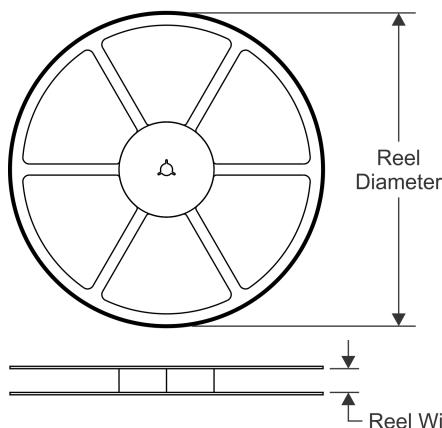
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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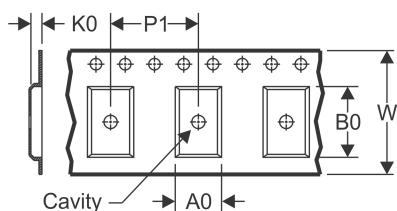
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

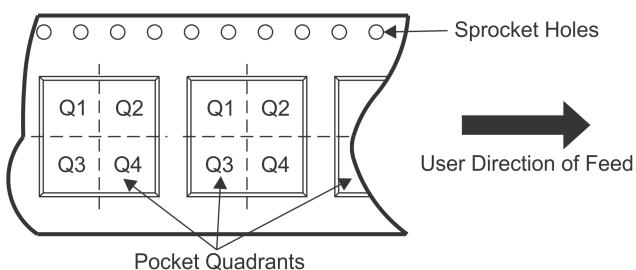


TAPE DIMENSIONS



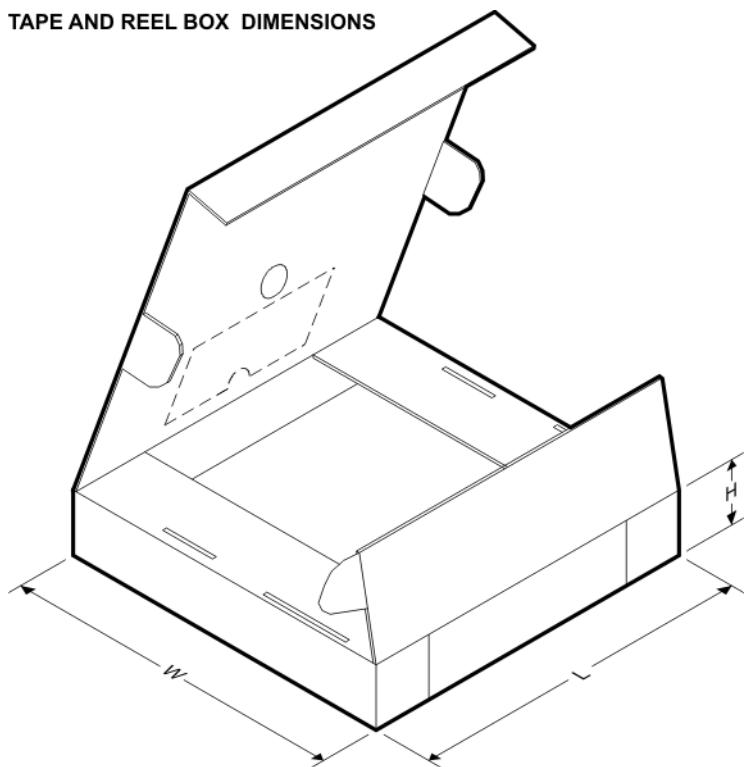
A_0	Dimension designed to accommodate the component width
B_0	Dimension designed to accommodate the component length
K_0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A_0 (mm)	B_0 (mm)	K_0 (mm)	P_1 (mm)	W (mm)	Pin1 Quadrant
LM555CMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM555CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

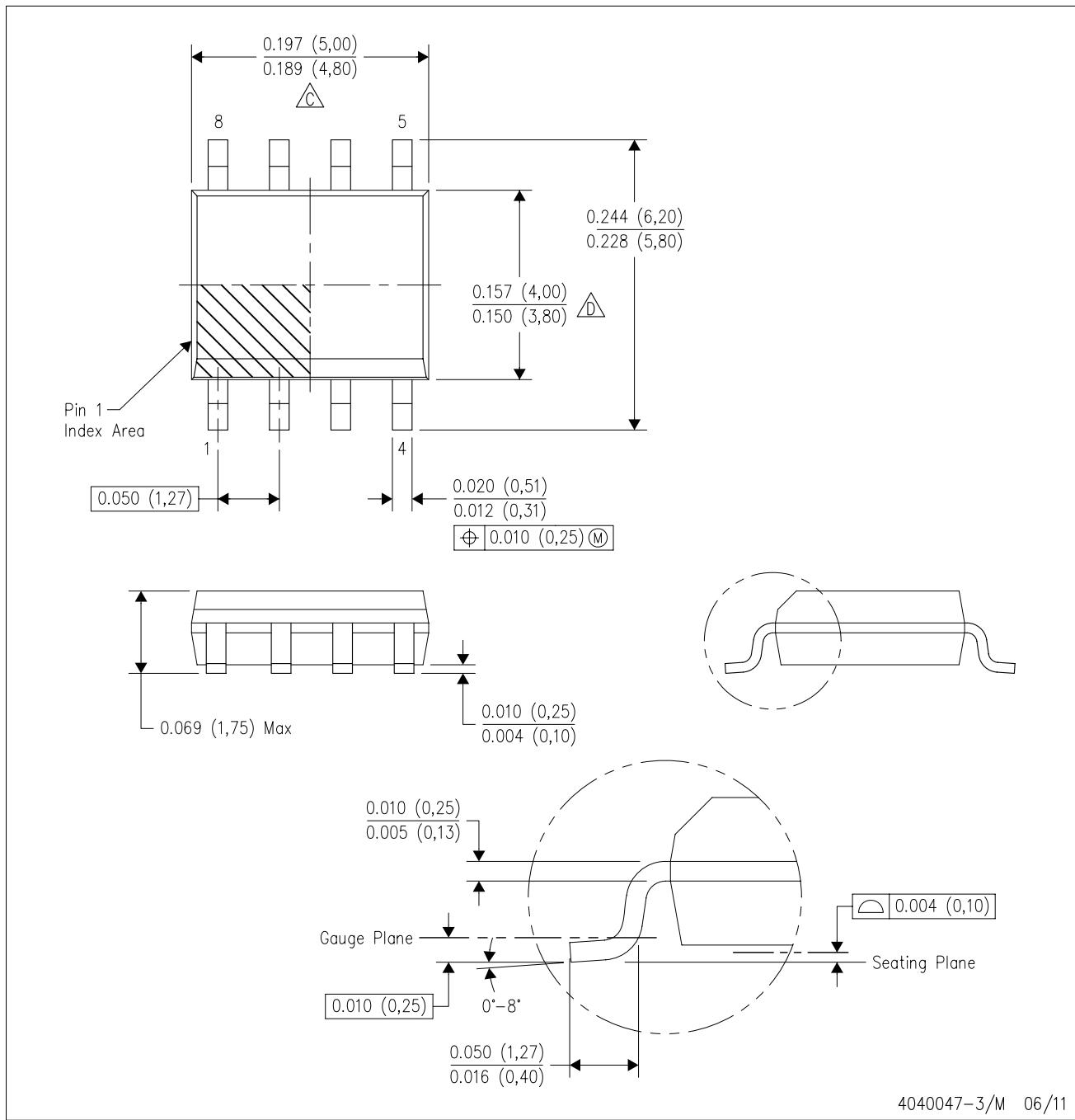
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM555CMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM555CMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM555CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM555CMX	SOIC	D	8	2500	367.0	367.0	35.0
LM555CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

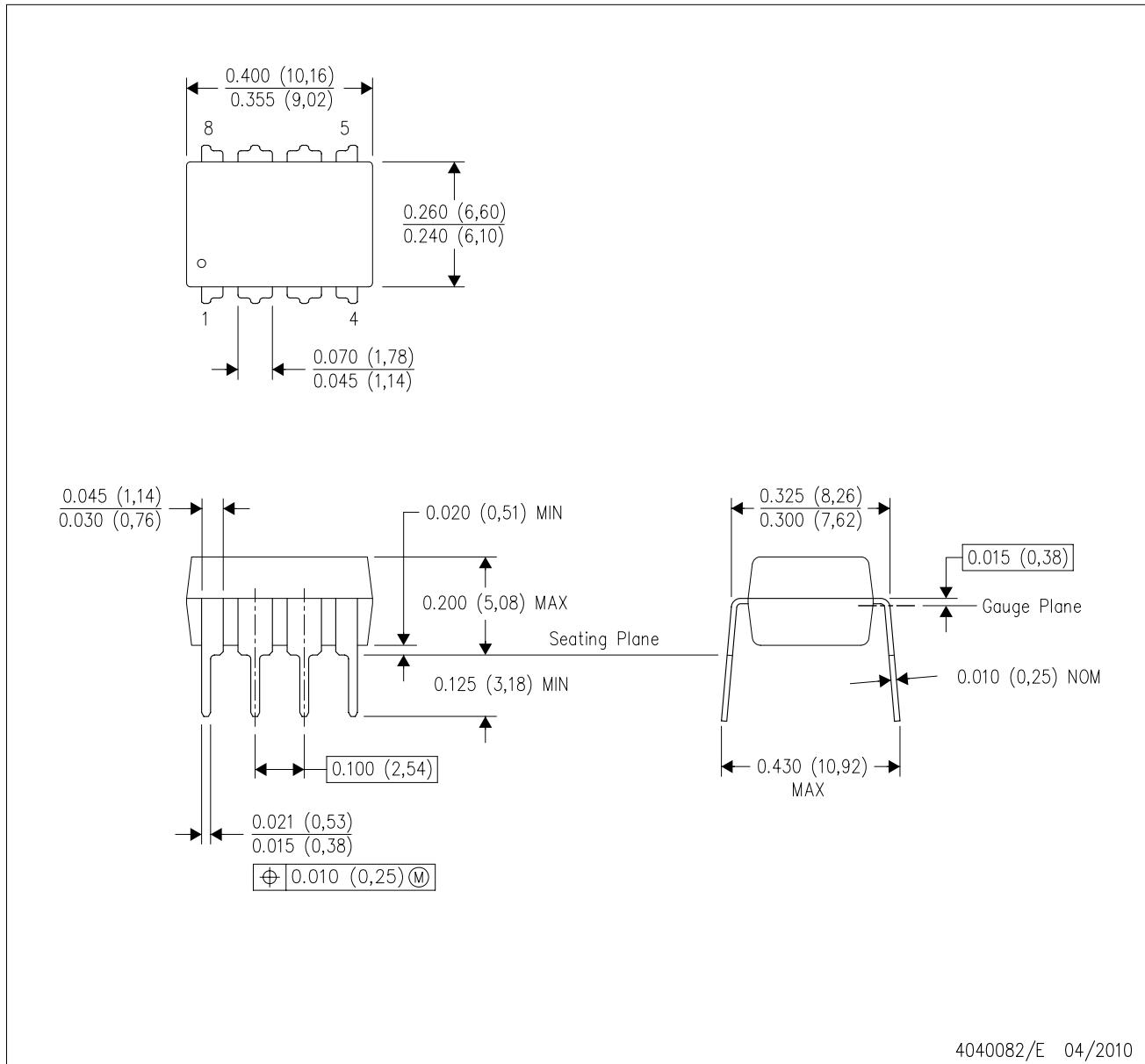
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

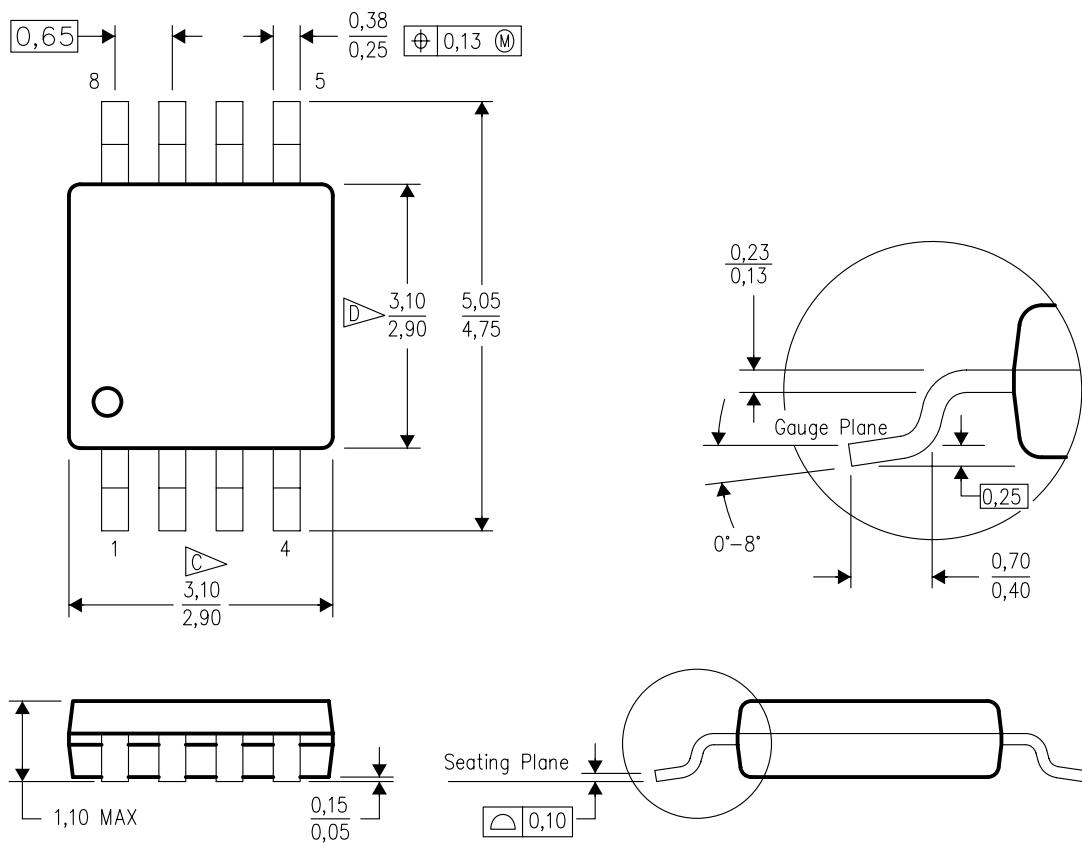


4040082/E 04/2010

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

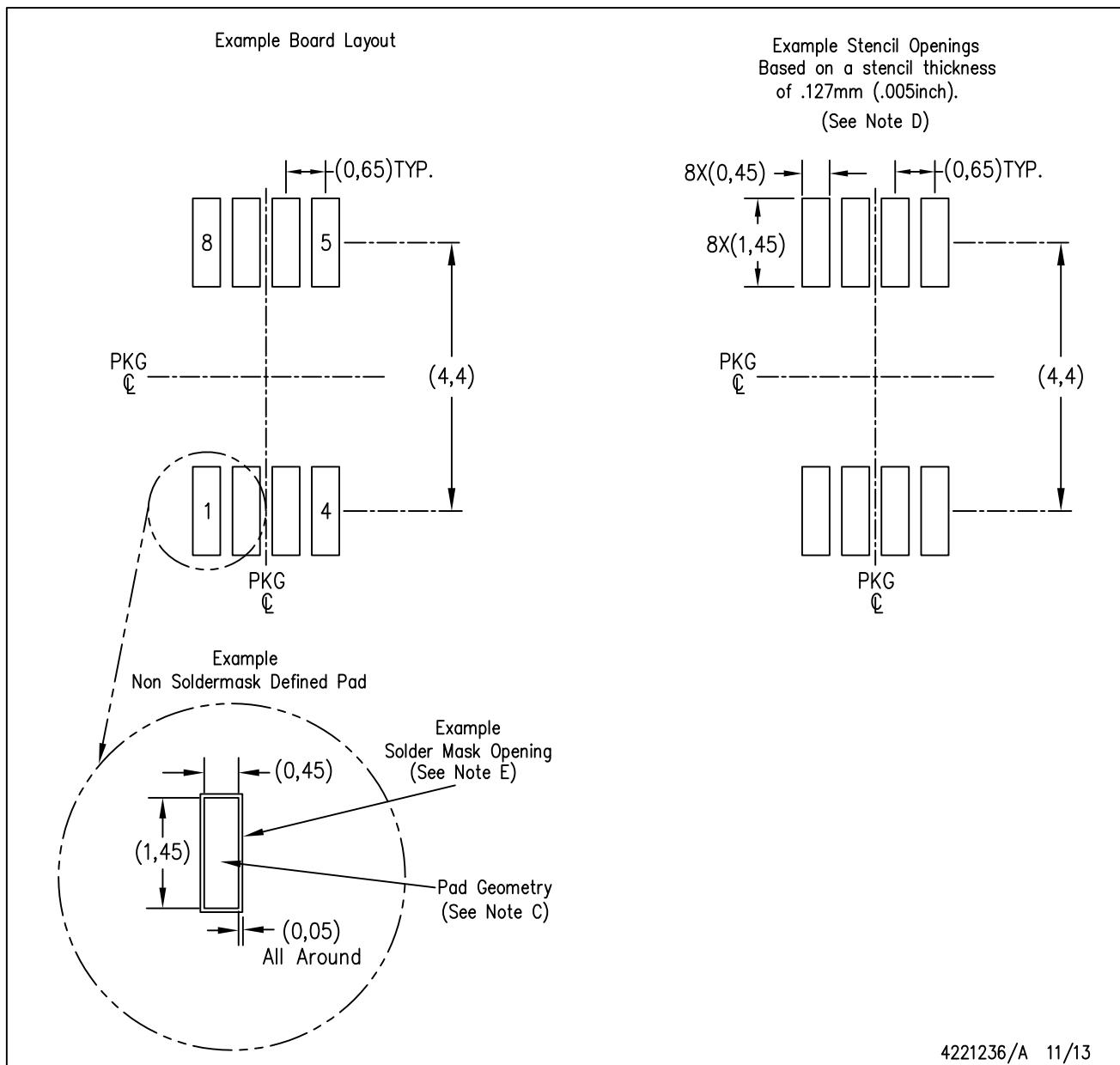
Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

LAND PATTERN DATA

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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High Speed Super Low Power SRAM

32K-Word By 8 Bit

HM62256

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
1.0	Initial issue	Jan.19,2005	
2.0	Add green code in order information	May.12,2005	



High Speed Super Low Power SRAM

32K-Word By 8 Bit

HM62256

■ GENERAL DESCRIPTION

The HM62256 is a high performance, high speed and super low power CMOS Static Random Access Memory organized as 32,768 words by 8bits and operates for a single 4.5 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 55/70ns in 5.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE).

The HM62256 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The HM62256 is available in JEDEC standard 28-pin SOP (330 mil) and PDIP (600 mil) packages.

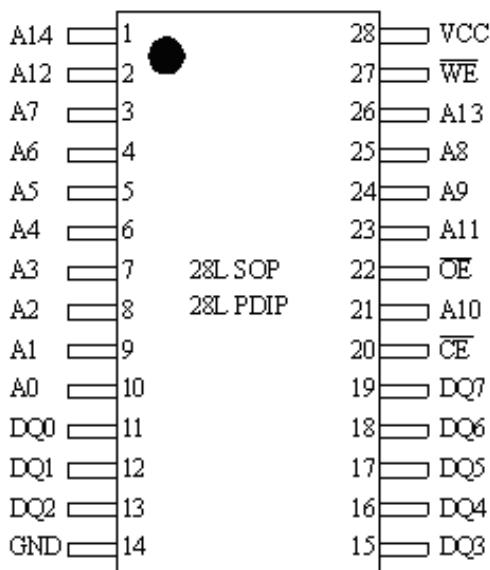
■ FEATURES

- Wide operation voltage : 4.5 ~ 5.5V
- Ultra low power consumption : 2mA@1MHz (Max.) , Vcc=5.0V.
1.0 uA (Typ.) CMOS standby current
- High speed access time : 55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE and /OE options.

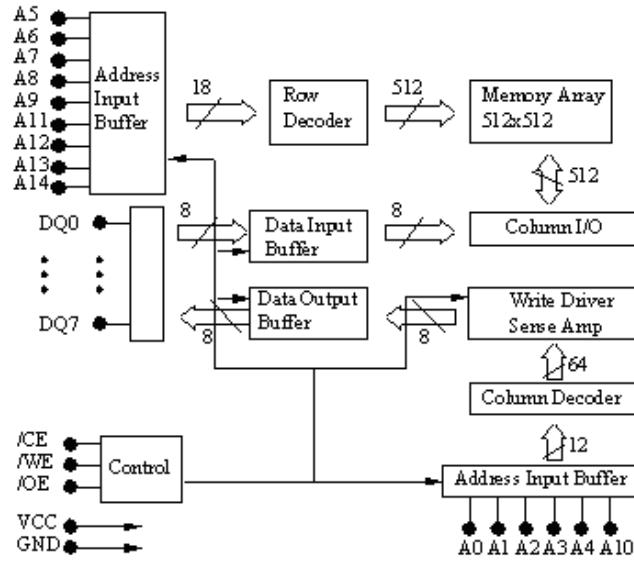
■ PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Speed (ns)	Standby Current(Typ.) I_{CCSB1}	Package Type
HM62256	0~70°C	4.5~5.5V	55/70	1.0 uA (Vcc = 5.0V)	28 SOP
					28 PDIP

■ PIN CONFIGURATIONS



■ FUNCTIONAL BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Type	Function
A0 – A14	Input	Address inputs for selecting one of the 32,768 x 8 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground



High Speed Super Low Power SRAM

32K-Word By 8 Bit

HM62256

■ TRUTH TABLE

Mode	/CE	/WE	/OE	DQ0~7	Vcc Current
Standby	H	X	X	High Z	I _{CCSB} , I _{CCSB1}
Output Disabled	L	H	H	High Z	I _{CC}
Read	L	H	L	D _{OUT}	I _{CC}
Write	L	L	X	D _{IN}	I _{CC}

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Rating	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{BIA} S	Temperature Under Bias	-40 to +125	°C
T _{STG}	Storage Temperature	-60 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0~70°C	4.5~5.5V

■ CAPACITANCE⁽¹⁾(TA=25°C,f=1.0MHz)

Symbol	Parameter	Conduction	MAX.	Unit
C _{IN}	Input Capacitance	V _{IN} =0V	6	pF
C _{DQ}	Input/Output Capacitance	V _{I/O} =0V	8	pF

1. This parameter is guaranteed, and not 100% tested.



High Speed Super Low Power SRAM

32K-Word By 8 Bit

HM62256

■ DC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, Vcc = 5.0V)

Name	Parameter	Test Condition	MIN	TYP ⁽¹⁾	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage ⁽²⁾	Vcc=5.0V	-0.5		0.8	V
V_{IH}	Guaranteed Input High Voltage ⁽²⁾	Vcc=5.0V	2.5		Vcc+0.2	V
I_{IL}	Input Leakage Current	V _{CC} =MAX, V _{IN} =0 to V _{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V _{CC} =MAX, /CE=V _{IN} , or /OE=V _{IN} , V _{IO} =0V to V _{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V _{CC} =MAX, I _{OL} = 1mA			0.4	V
V_{OH}	Output High Voltage	V _{CC} =MIN, I _{OH} = -1mA	2.2			V
I_{CC}	Operating Power Supply Current	/CE=V _{IL} , I _{DQ} =0mA, F=F _{MAX} =1/ t _{RC}			20	mA
I_{CCSB}	TTL Standby Supply	/CE=V _{IH} , I _{DQ} =0mA,			1	mA
I_{CCSB1}	CMOS Standby Current	/CE ≥ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V,		1.0	10	uA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.

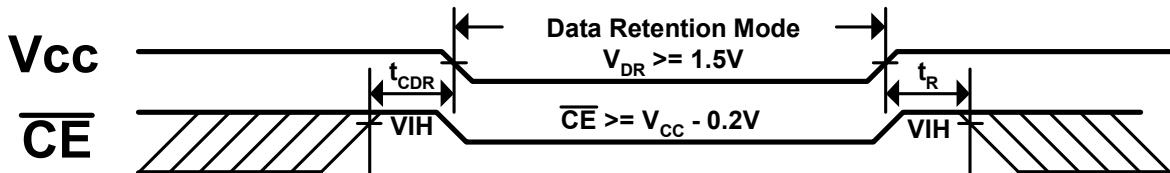
■ DATA RETENTION CHARACTERISTICS (TA = 0° ~70°C)

Name	Parameter	Test Condition	MIN	TYP ⁽¹⁾	MAX	Unit
V_{DR}	V _{CC} for Data Retention	/CE ≥ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE ≥ V _{CC} -0.2V, V _{CC} =2V V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V		0.5	3	uA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t _{RC} (2)			ns

1. TA = 25°C.

2. t_{RC}= Read Cycle Time.

■ LOW Vcc DATA RETENTION WAVEFORM (/CE Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

■ KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
____	MUST BE STEADY	MUST BE STEADY
\\\\\\	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
/\\\\\\	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
XXXXXX	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
==><==	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

■ AC TEST LOADS AND WAVEFORMS

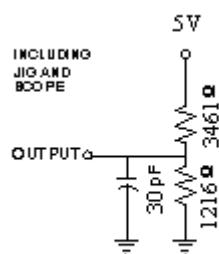


FIGURE 1A

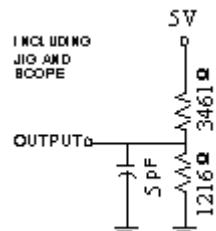


FIGURE 1B

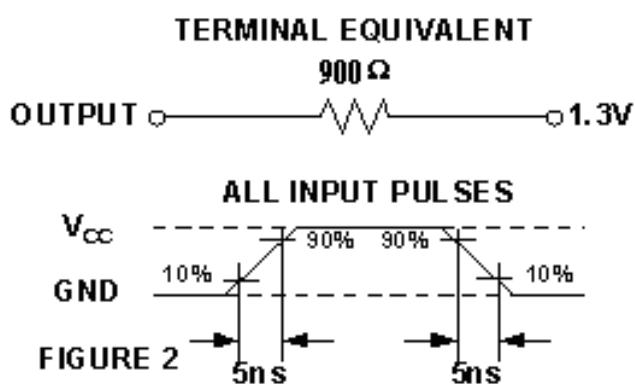


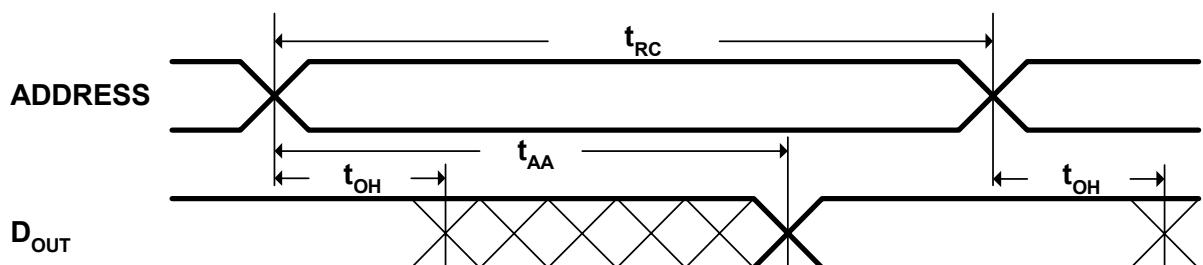
FIGURE 2

■ AC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, Vcc = 5.0V)
< READ CYCLE >

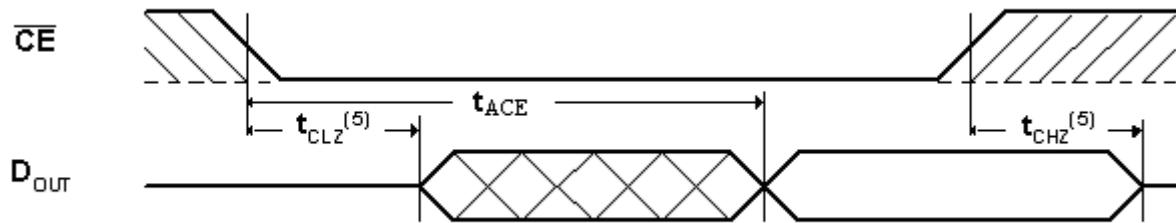
JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{ACE}	Chip Select Access Time		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		30		50	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10		10		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0	35	0	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
t_{AXOX}	t_{OH}	Address Change to Out Disable	10		10		ns

■ SWITCHING WAVEFORMS (READ CYCLE)

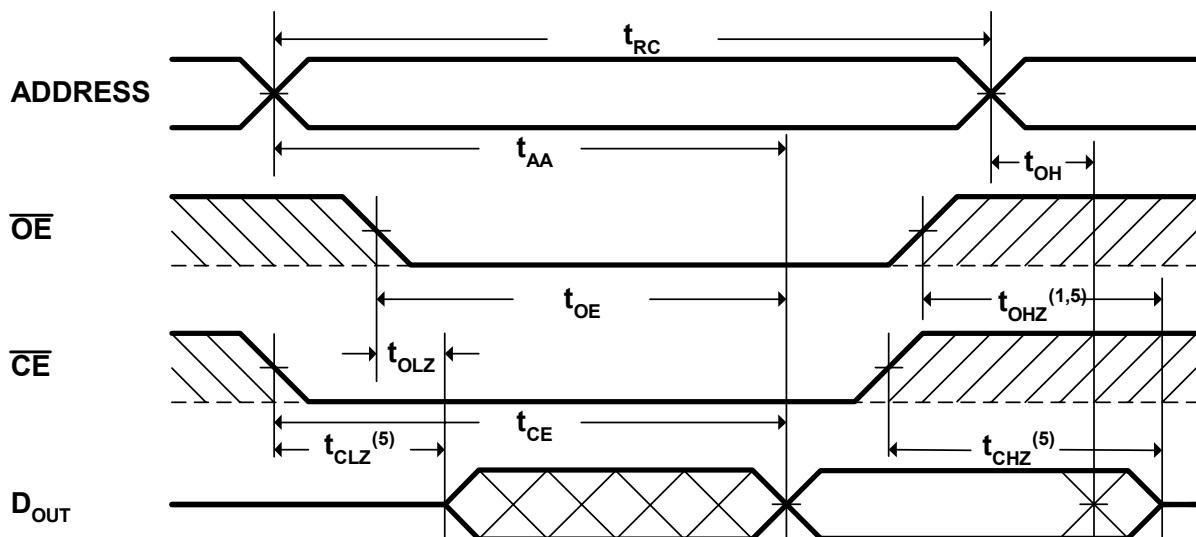
READ CYCLE1 ^(1,2,4)



READ CYCLE2 ^(1,3,4)



READ CYCLE3 ^(1,4)



NOTES:

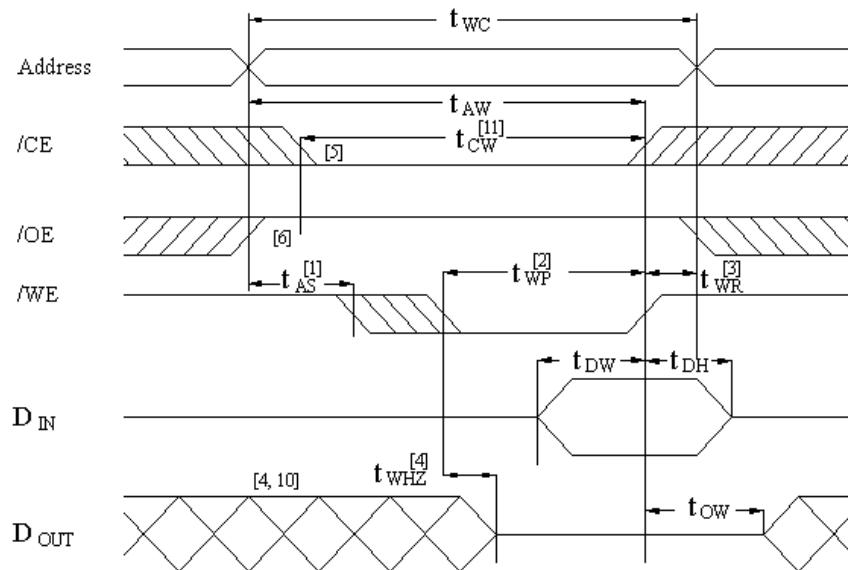
1. /WE is high in read Cycle.
2. Device is continuously selected when /CE = V_{IL}.
3. Address valid prior to or coincident with CE transition low.
4. /OE = V_{IL}.
5. Test conditions assume signal transition times of 5ns or less, timing reference levels of 0.5VCC, input pulse levels of 0V to VCC and output loading specified in Figure 1A.
6. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, Vcc = 5.0V)
< WRITE CYCLE >

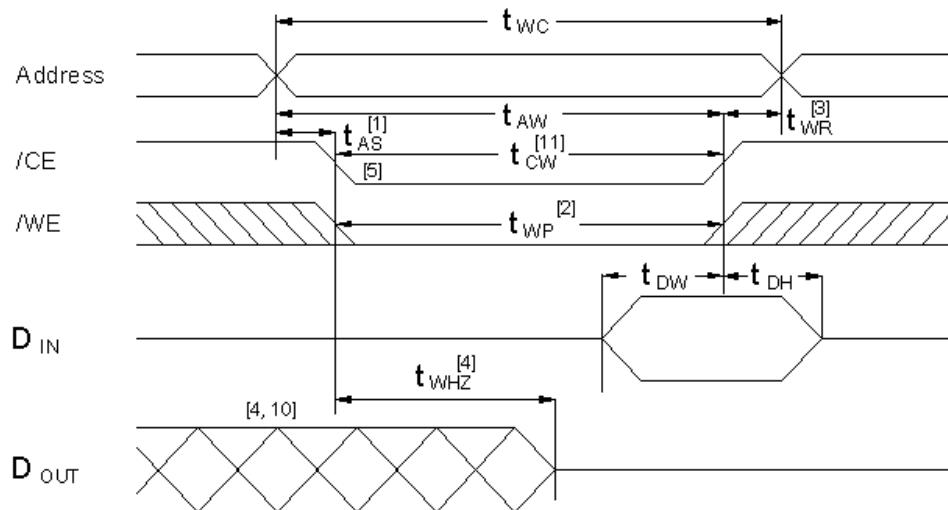
JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	55		70		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	55		70		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time	0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		25		35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	20		30		ns
t_{WHDX}	t_{DH}	Data Hold for Write End	0		0		ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (Write Enable Controlled)



WRITE CYCLE2 (Chip Enable Controlled)



NOTES:

1. /WE must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of /CE or /WE going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.
6. It's recommended to keep /OE at high (/OE = VIH) as /WE Controlled WRITE CYCLE.
7. D_{OUT} is the read data of next address.
8. If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Test conditions assume signal transition times of 5ns or less, timing reference levels of 0.5VCC, input pulse levels of 0V to VCC and output loading specified in Figure 1A.
10. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of /CE going low to the end of write.

■ ORDER INFORMATION

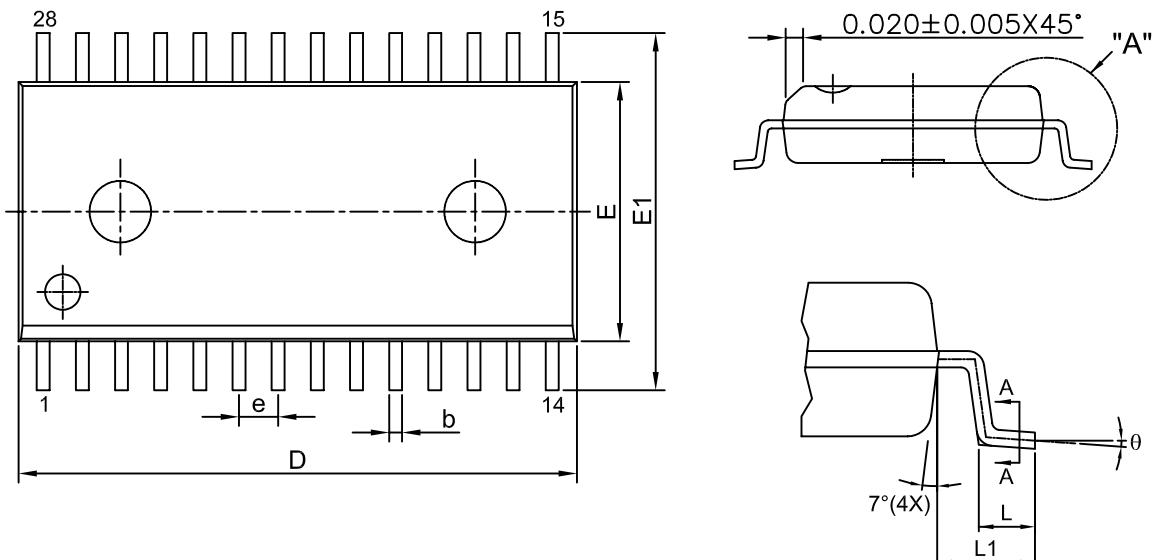
HM62256 XX X - XXX

Package:
ALF : 28SOP -330mil
ALP : 28L PDIP-600 mil

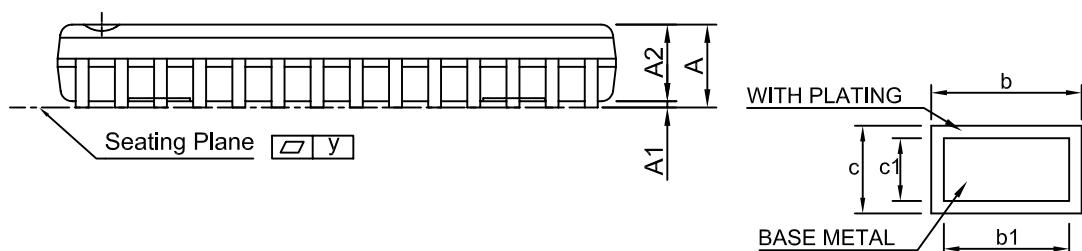
Speed:
55: 55ns
70: 70ns

Package Material
Blank: Normal
G: Lead & Halogen Free

■ PACKAGE DIMENSIONS - 28L SOP -330mil

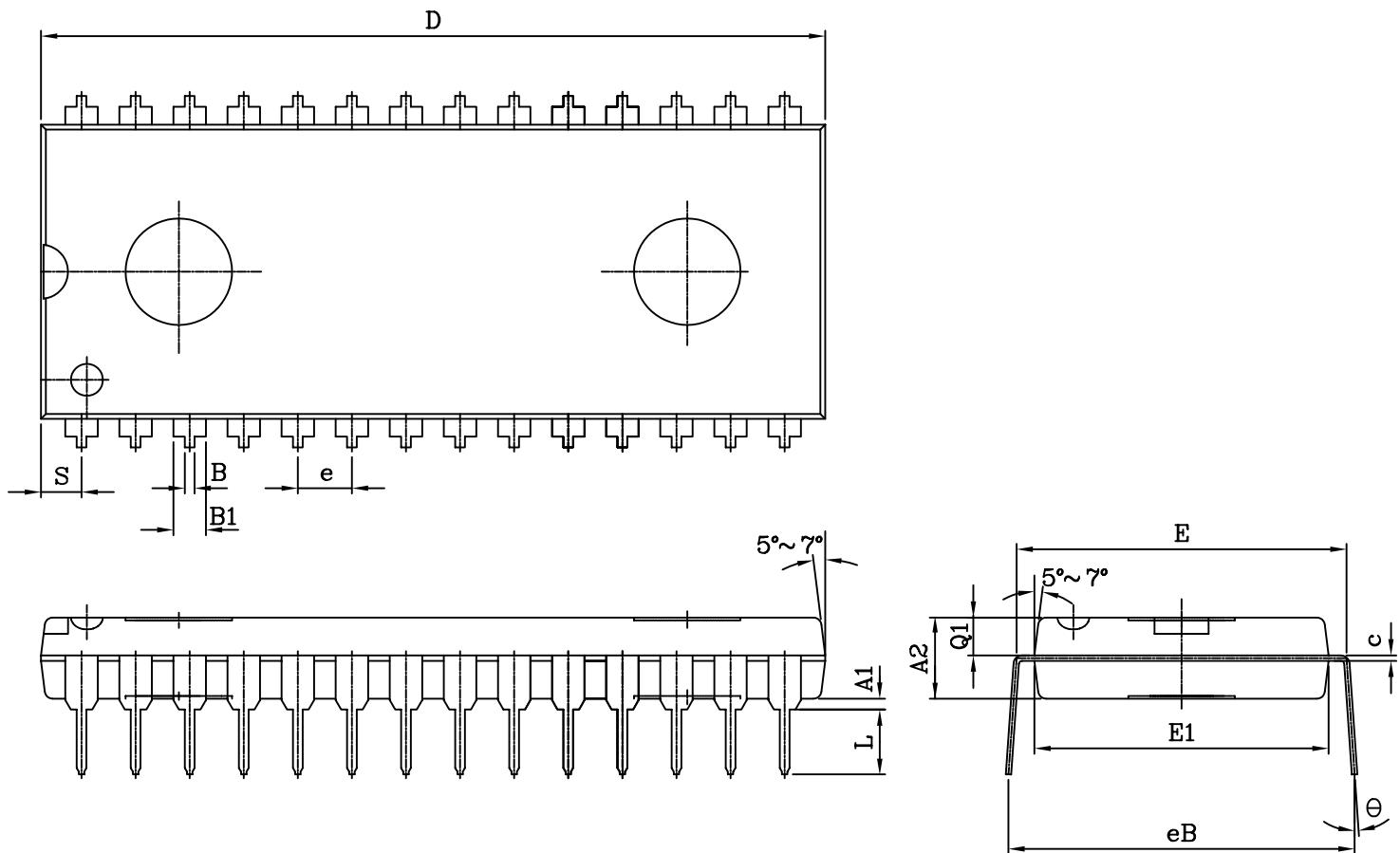


DETAIL "A" (2:1)



SECTION A-A

SYMBOL UNIT	A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ	
mm	Min.	2.540	0.102	2.362	0.35	0.35	0.20	0.20	17.983	8.280	11.506	1.118	0.700	1.520	—	0°
	Nom.	2.692	0.226	2.489	—	—	—	—	18.110	8.407	11.811	1.270	0.964	1.720	—	—
	Max.	2.844	0.350	2.616	0.50	0.45	0.32	0.28	18.237	8.534	12.116	1.422	1.228	1.920	0.1	10°
inch	Min.	0.100	0.004	0.093	0.014	0.014	0.008	0.008	0.708	0.326	0.453	0.044	0.0276	0.0598	—	0°
	Nom.	0.106	0.009	0.098	—	—	—	—	0.713	0.331	0.465	0.050	0.0380	0.0677	—	—
	Max.	0.112	0.014	0.103	0.020	0.018	0.012	0.011	0.718	0.336	0.477	0.056	0.0484	0.0756	0.004	10°

■ PACKAGE DIMENSIONS - 28L PDIP -600mil


SYMBOL UNIT	A1	A2	B	B1	c	D	E	E1	e	eB	L	S	Q1	Θ	
mm	Min.	0.254	3.683	0.330	1.270	0.152	36.957	14.986	13.716	2.540 (TYP)	15.748	3.048	1.778	1.651	3°
	Nom.	—	3.810	0.457	1.524	0.254	37.084	15.240	13.818		16.256	3.302	2.032	1.778	6°
	Max.	—	3.937	0.584	1.778	0.356	37.211	15.494	13.920		16.764	3.556	2.286	1.905	9°
inch	Min.	0.010	0.145	0.013	0.050	0.006	1.455	0.590	0.540	0.100 (TYP)	0.620	0.120	0.070	0.065	3°
	Nom.	—	0.150	0.018	0.060	0.010	1.460	0.600	0.544		0.640	0.130	0.080	0.070	6°
	Max.	—	0.155	0.023	0.070	0.014	1.465	0.610	0.548		0.660	0.140	0.090	0.075	9°

Features

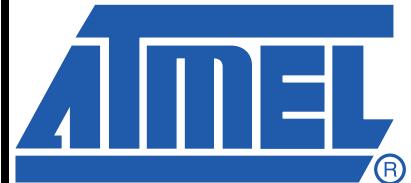
- **Fast Read Access Time – 150 ns**
- **Automatic Page Write Operation**
 - Internal Address and Data Latches for 64 Bytes
- **Fast Write Cycle Times**
 - Page Write Cycle Time: 10 ms Maximum (Standard)
 - 2 ms Maximum (Option – Ref. AT28HC64BF Datasheet)
 - 1 to 64-byte Page Write Operation
- **Low Power Dissipation**
 - 40 mA Active Current
 - 100 µA CMOS Standby Current
- **Hardware and Software Data Protection**
- **DATA Polling and Toggle Bit for End of Write Detection**
- **High Reliability CMOS Technology**
 - Endurance: 100,000 Cycles
 - Data Retention: 10 Years
- **Single 5V ±10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-wide Pinout**
- **Industrial Temperature Ranges**
- **Green (Pb/Halide-free) Packaging Option Only**

1. Description

The AT28C64B is a high-performance electrically-erasable and programmable read-only memory (EEPROM). Its 64K of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 220 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

The AT28C64B is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C64B has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.



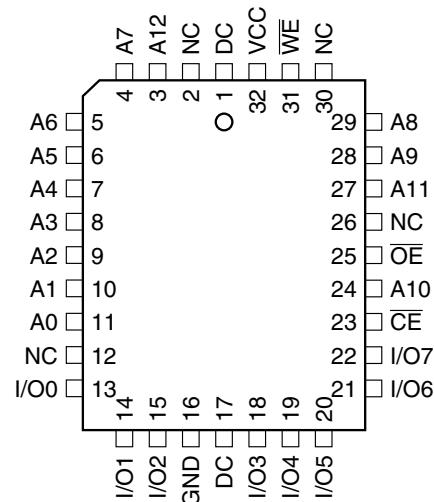
64K (8K x 8) Parallel EEPROM with Page Write and Software Data Protection

AT28C64B

2. Pin Configurations

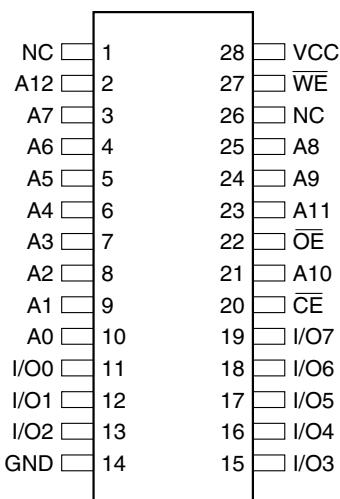
Pin Name	Function
A0 - A12	Addresses
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

2.2 32-lead PLCC Top View

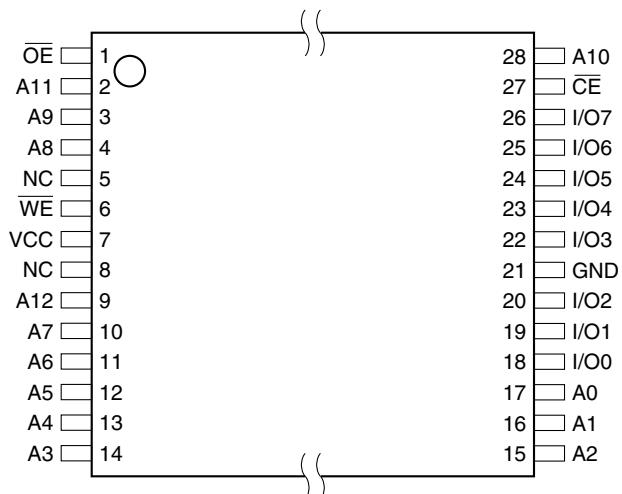


Note: PLCC package pins 1 and 17 are Don't Connect.

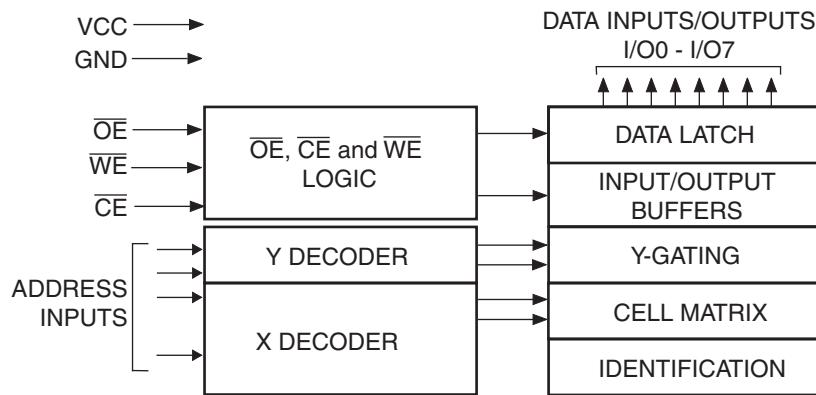
2.1 28-lead PDIP, 28-lead SOIC Top View



2.3 28-lead TSOP Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT28C64B is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state when either \overline{CE} or \overline{OE} is high. This dual line control gives designers flexibility in preventing bus contention in their systems.

4.2 Byte Write

A low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high initiates a write cycle. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

4.3 Page Write

The page write operation of the AT28C64B allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; after the first byte is written, it can then be followed by 1 to 63 additional bytes. Each successive byte must be loaded within $150\ \mu s$ (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C64B will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 to A12 inputs. For each \overline{WE} high to low transition during the page write operation, A6 to A12 must be the same.

The A0 to A5 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

4.4 DATA Polling

The AT28C64B features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at any time during the write cycle.

4.5 Toggle Bit

In addition to DATA Polling, the AT28C64B provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Toggle bit reading may begin at any time during the write cycle.

4.6 Data Protection

If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel® has incorporated both hardware and software features that will protect the memory against inadvertent writes.

4.6.1 Hardware Data Protection

Hardware features protect against inadvertent writes to the AT28C64B in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8 V (typical), the write function is inhibited; (b) V_{CC} power-on delay – once V_{CC} has reached 3.8 V, the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of \overline{OE} low, \overline{CE} high, or \overline{WE} high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a write cycle.

4.6.2 Software Data Protection

A software controlled data protection feature has been implemented on the AT28C64B. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C64B is shipped from Atmel with SDP disabled.

SDP is enabled by the user issuing a series of three write commands in which three specific bytes of data are written to three specific addresses (see “Software Data Protection Algorithms” on [page 10](#)). After writing the 3-byte command sequence and waiting t_{WC} , the entire AT28C64B will be protected against inadvertent writes. It should be noted that even after SDP is enabled, the user may still perform a byte or page write to the AT28C64B by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP remains active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP protects the AT28C64B during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not actually written into the device; their addresses may still be written with user data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device. However, for the duration of t_{WC} , read operations will effectively be polling operations.

4.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5 V and using address locations 1FC0H to 1FFFH, the additional bytes may be written to or read from in the same manner as the regular memory array.

5. DC and AC Operating Range

	AT28C64B-15
Operating Temperature (Case)	-40°C - 85°C
V _{CC} Power Supply	5V ±10%

6. Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	D _{IN}
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z
Chip Erase	V _{IL}	V _H ⁽³⁾	V _{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.

2. See "AC Write Waveforms" on page 8.

3. V_H = 12.0V ±0.5V.

7. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins)	
with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V _{CC} + 0.6V
Voltage on \overline{OE} and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

8. DC Characteristics

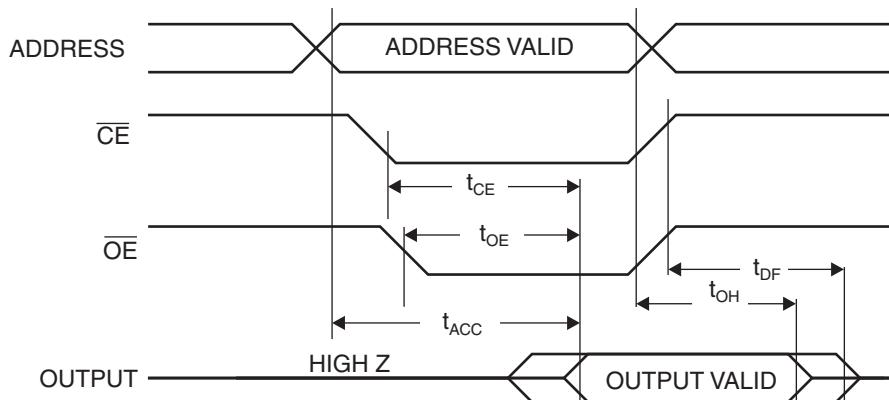
Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC} + 1V		10	µA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	µA
I _{SB1}	V _{CC} Standby Current CMOS	\overline{CE} = V _{CC} - 0.3V to V _{CC} + 1V		100	µA
I _{SB2}	V _{CC} Standby Current TTL	\overline{CE} = 2.0V to V _{CC} + 1V		2	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA		40	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.40	V
V _{OH}	Output High Voltage	I _{OH} = -400 µA	2.4		V



9. AC Read Characteristics

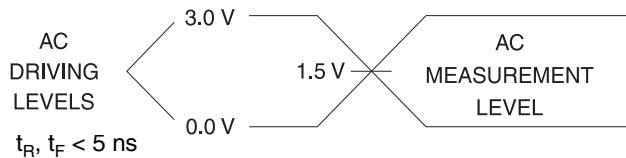
Symbol	Parameter	AT28C64B-15		Units
		Min	Max	
t_{ACC}	Address to Output Delay		150	ns
$t_{CE}^{(1)}$	\overline{CE} to Output Delay		150	ns
$t_{OE}^{(2)}$	\overline{OE} to Output Delay	0	70	ns
$t_{DF}^{(3)(4)}$	\overline{CE} or \overline{OE} to Output Float	0	50	ns
t_{OH}	Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	0		ns

10. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

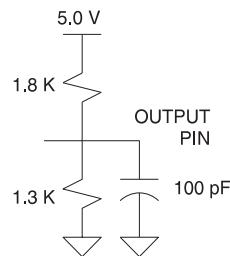


- Notes:
1. \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 3. t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first ($C_L = 5 \text{ pF}$).
 4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

$f = 1 \text{ MHz}, T = 25^\circ\text{C}$ ⁽¹⁾

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

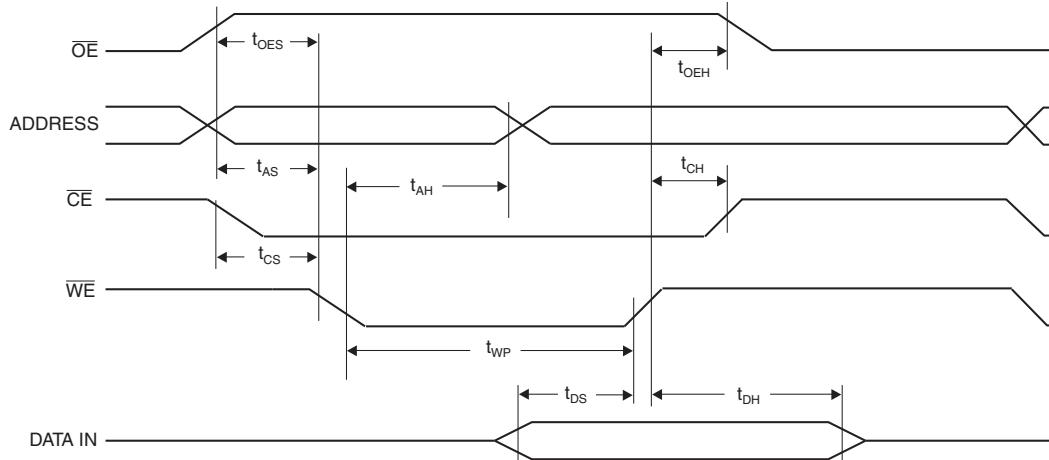
Note: 1. This parameter is characterized and is not 100% tested.

14. AC Write Characteristics

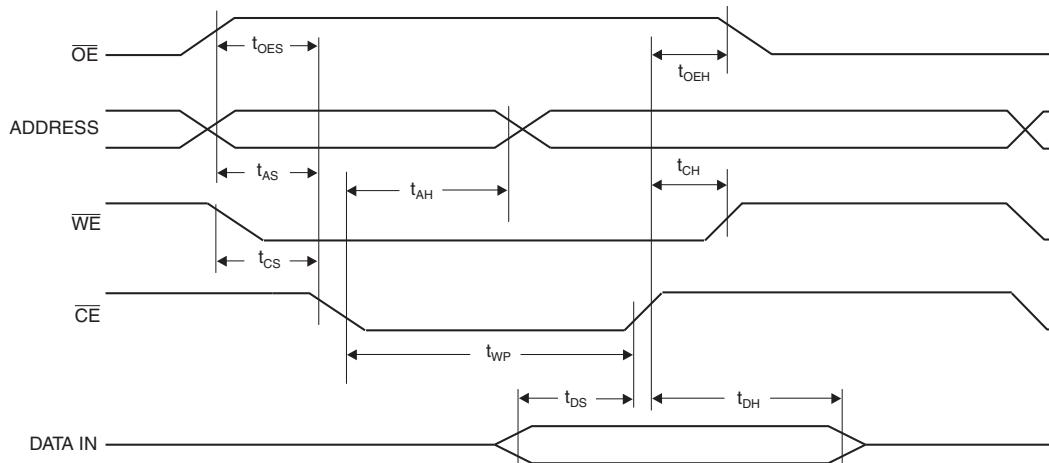
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, \overline{OE} Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (\overline{WE} or \overline{CE})	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, \overline{OE} Hold Time	0		ns

15. AC Write Waveforms

15.1 \overline{WE} Controlled



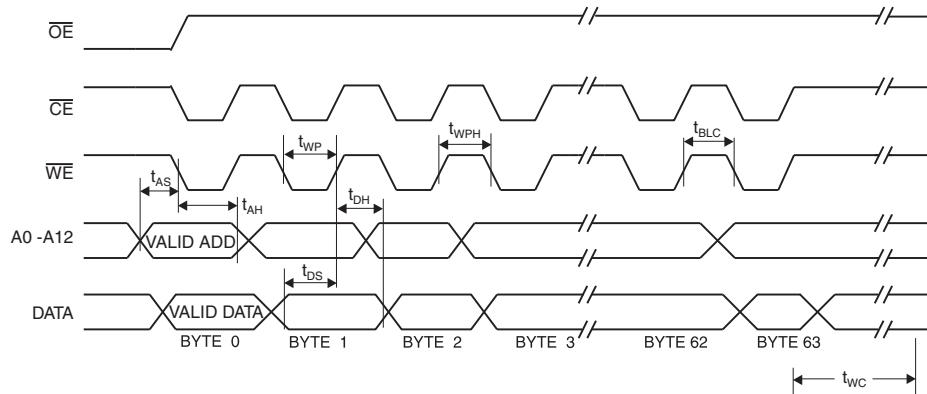
15.2 \overline{CE} Controlled



16. Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{WC}	Write Cycle Time (option available – Ref. AT28HC64BF datasheet)		2	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	μs
t_{WPH}	Write Pulse Width High	50		ns

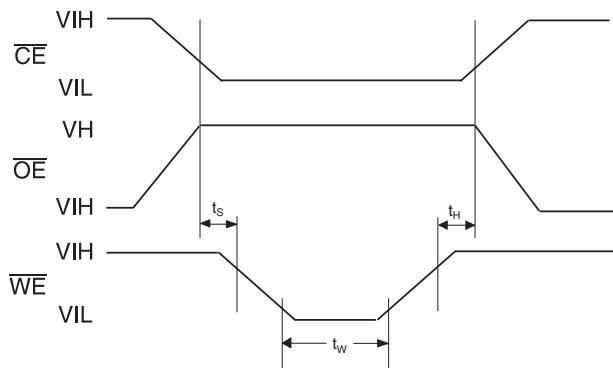
17. Page Mode Write Waveforms⁽¹⁾⁽²⁾



Notes:

1. A6 through A12 must specify the same page address during each high to low transition of \overline{WE} (or \overline{CE}).
2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

18. Chip Erase Waveforms

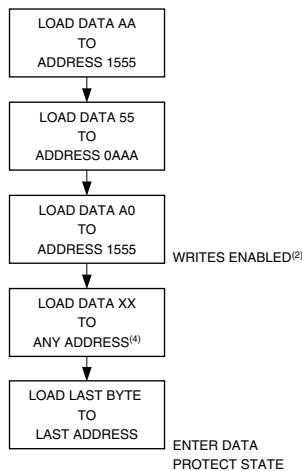


$$t_S = t_H = 1 \mu s \text{ (min.)}$$

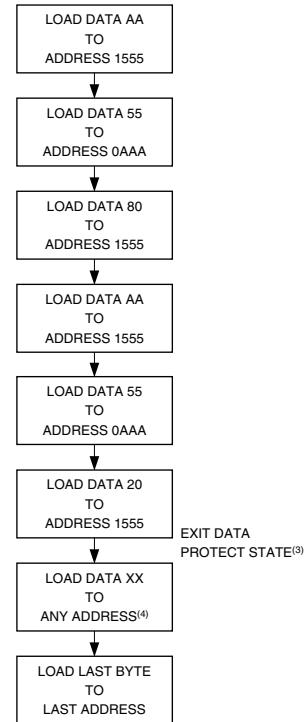
$$t_W = 10 \text{ ms (min.)}$$

$$V_H = 12.0V \pm 0.5V$$

19. Software Data Protection Enable Algorithm⁽¹⁾



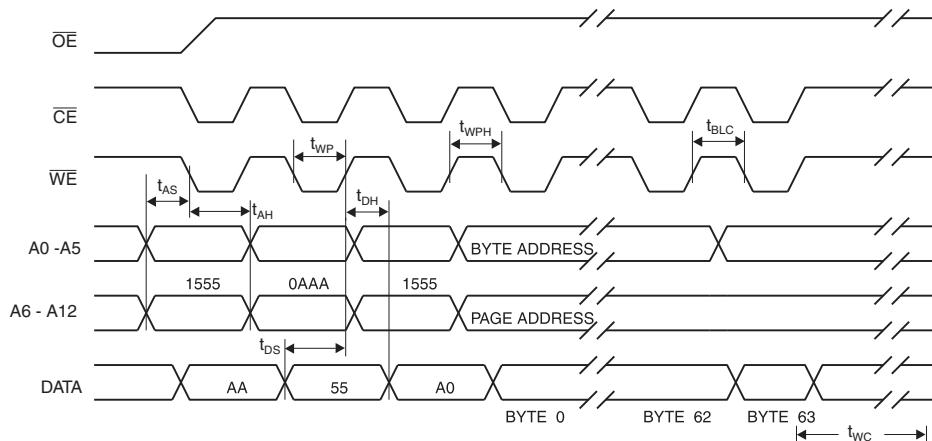
20. Software Data Protection Disable Algorithm⁽¹⁾



- Notes:
1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A12 - A0 (Hex).
 2. Write Protect state will be activated at end of write even if no other data is loaded.
 3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
 4. 1 to 64 bytes of data are loaded.

- Notes:
1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A12 - A0 (Hex).
 2. Write Protect state will be activated at end of write even if no other data is loaded.
 3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
 4. 1 to 64 bytes of data are loaded.

21. Software Protected Write Cycle Waveforms⁽¹⁾⁽²⁾



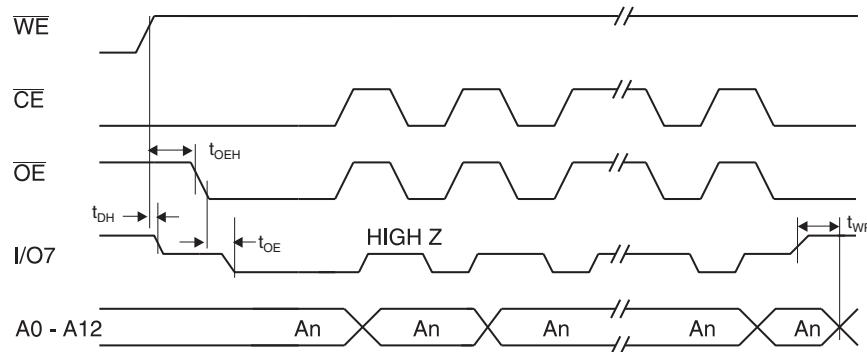
- Notes:
1. A6 through A12 must specify the same page address during each high to low transition of **WE** (or **CE**) after the software code has been entered.
 2. **OE** must be high only when **WE** and **CE** are both low.

22. Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	\overline{OE} Hold Time	0			ns
t_{OE}	\overline{OE} to Output Delay ⁽¹⁾				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. See "AC Read Characteristics" on page 6.

23. Data Polling Waveforms



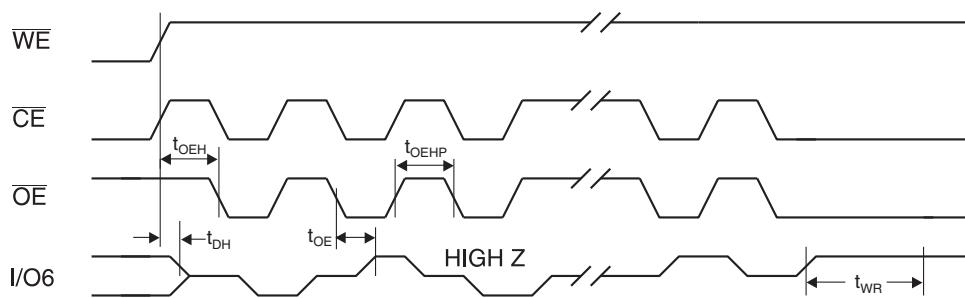
24. Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	\overline{OE} Hold Time	10			ns
t_{OE}	\overline{OE} to Output Delay ⁽²⁾				ns
t_{OEH}	\overline{OE} High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.

2. See "AC Read Characteristics" on page 6.

25. Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾



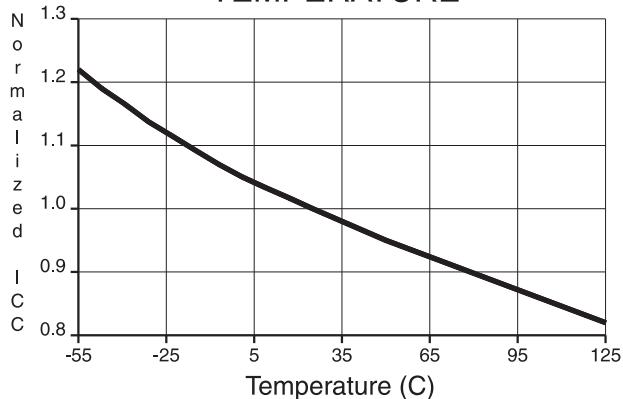
Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.

2. Beginning and ending state of I/O6 will vary.

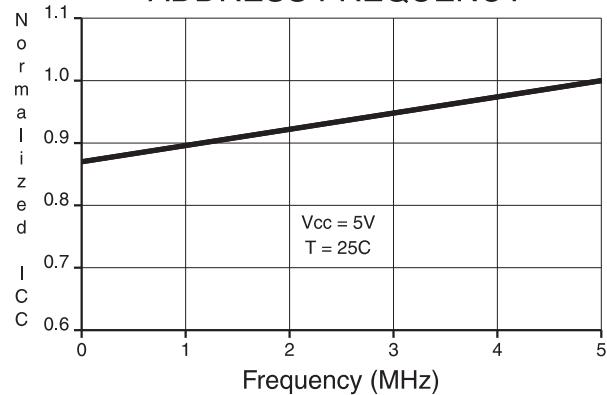
3. Any address location may be used but the address should not vary.

26. Normalized I_{CC} Graphs

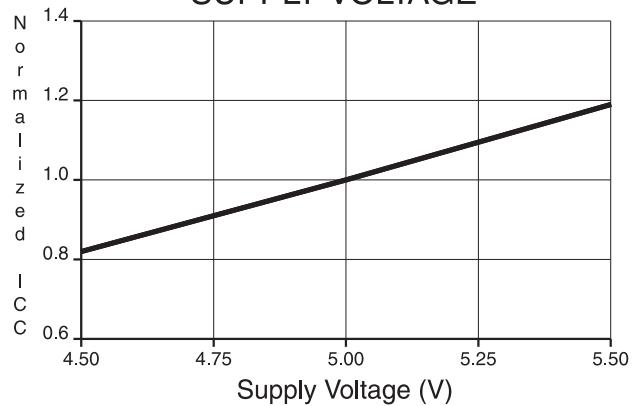
NORMALIZED SUPPLY CURRENT vs.
TEMPERATURE



NORMALIZED SUPPLY CURRENT vs.
ADDRESS FREQUENCY



NORMALIZED SUPPLY CURRENT vs.
SUPPLY VOLTAGE



27. Ordering Information

27.1 Green Package Option (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	0.1	AT28C64B-15JU	32J	Industrial (-40°C to 85°C)
			AT28C64B-15SU	28S	
			AT28C64B-15TU	28T	
			AT28C64B-15PU	28P6	

27.2 Die Products

Contact Atmel Sales for die sales options.

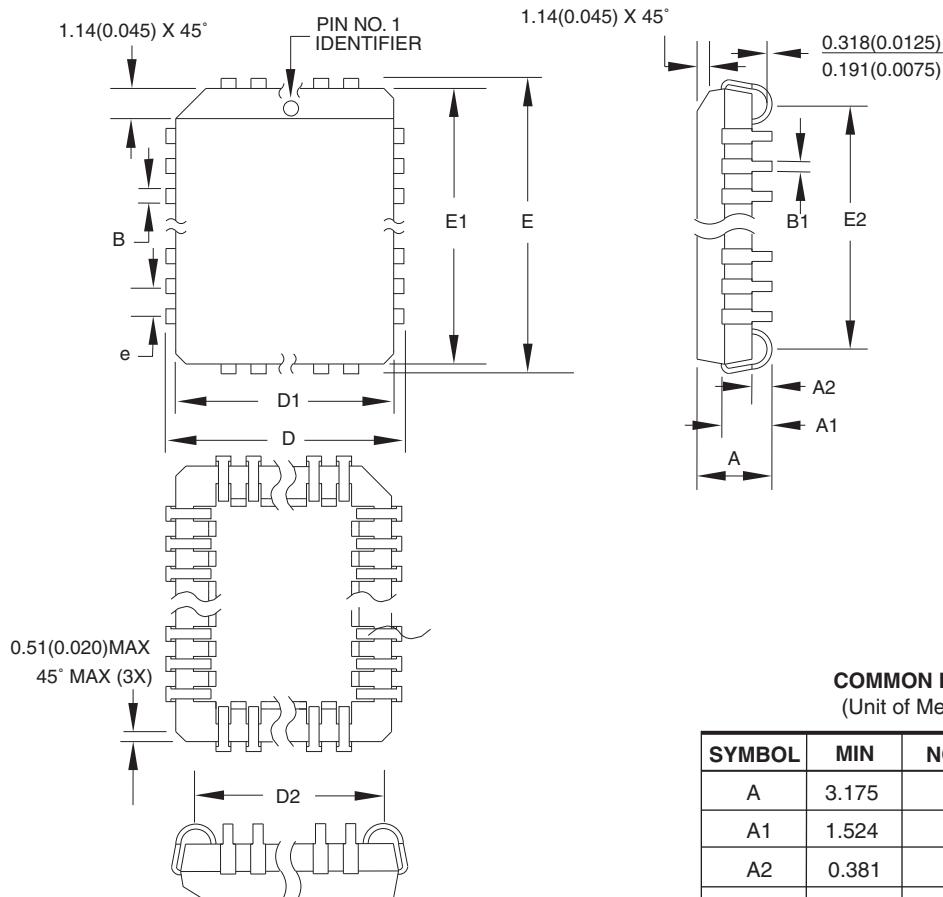
Package Type

32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)



28. Packaging Information

28.1 32J – PLCC



- Notes:
- This package conforms to JEDEC reference MS-016, Variation AE.
 - Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 - Lead coplanarity is 0.004" (0.102 mm) maximum.

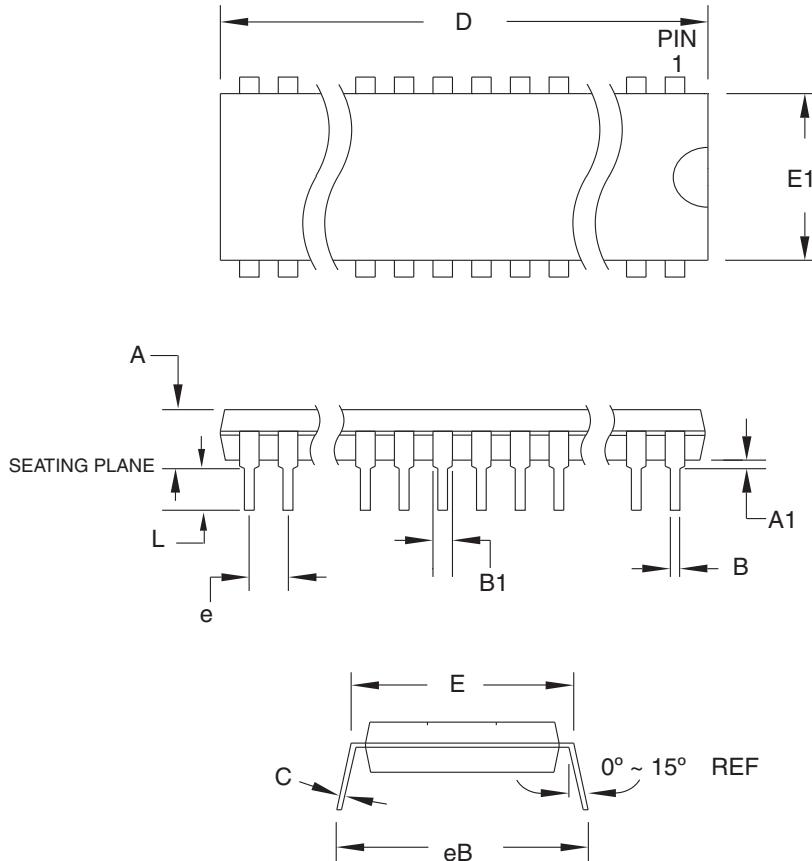
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

10/04/01

ATMEL	2325 Orchard Parkway San Jose, CA 95131	TITLE 32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	DRAWING NO. 32J	REV. B
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28.2 28P6 – PDIP



- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AB.
 2. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

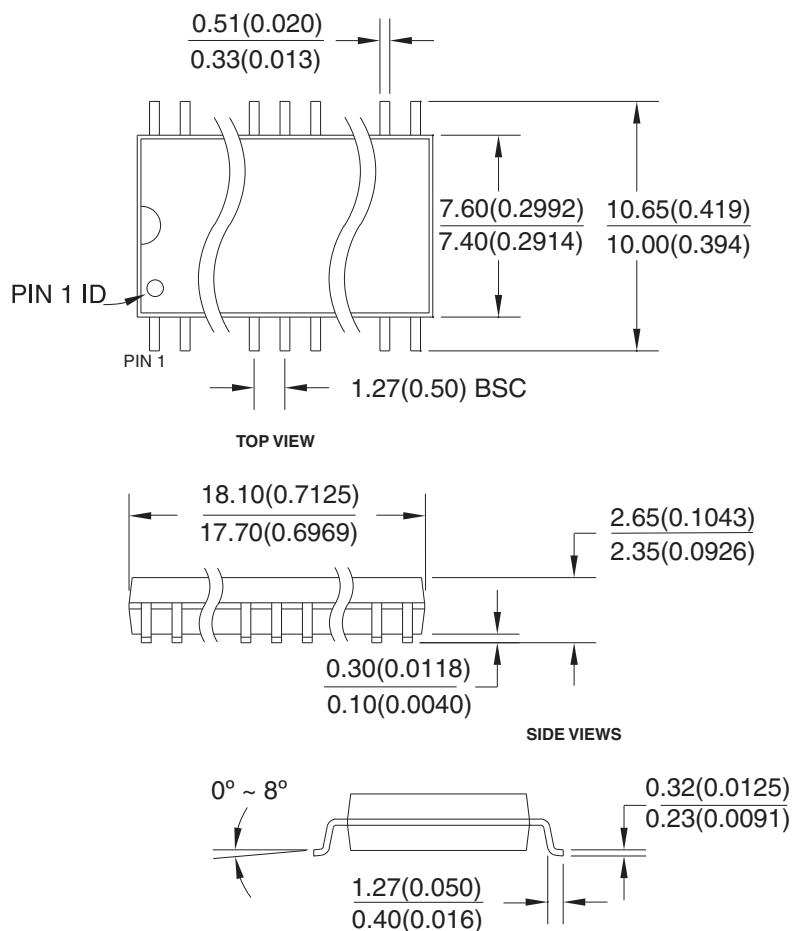
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	4.826	
A1	0.381	—	—	
D	36.703	—	37.338	Note 2
E	15.240	—	15.875	
E1	13.462	—	13.970	Note 2
B	0.356	—	0.559	
B1	1.041	—	1.651	
L	3.048	—	3.556	
C	0.203	—	0.381	
eB	15.494	—	17.526	
e	2.540 TYP			

09/28/01

ATMEL 2325 Orchard Parkway San Jose, CA 95131	TITLE 28P6, 28-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO. 28P6	REV. B
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28.3 28S – SOIC

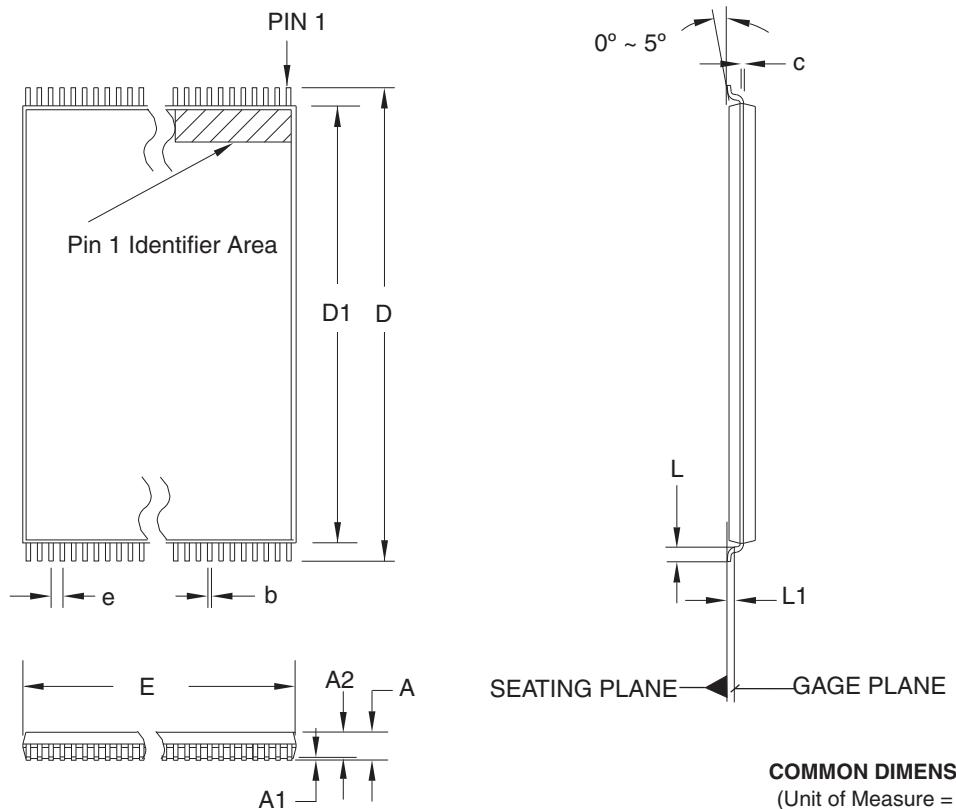
Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.



8/4/03

ATMEL	2325 Orchard Parkway San Jose, CA 95131	TITLE 28S, 28-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC) JEDEC Standard MS-013	DRAWING NO.	REV.
			28S	B

28.4 28T – TSOP



Notes:

1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

12/06/02

AMEL	2325 Orchard Parkway San Jose, CA 95131	TITLE 28T, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)	DRAWING NO.	REV.
			28T	C



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Literature Requests
www.atmel.com/literature

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SC56-11SRWA

SUPER BRIGHT RED

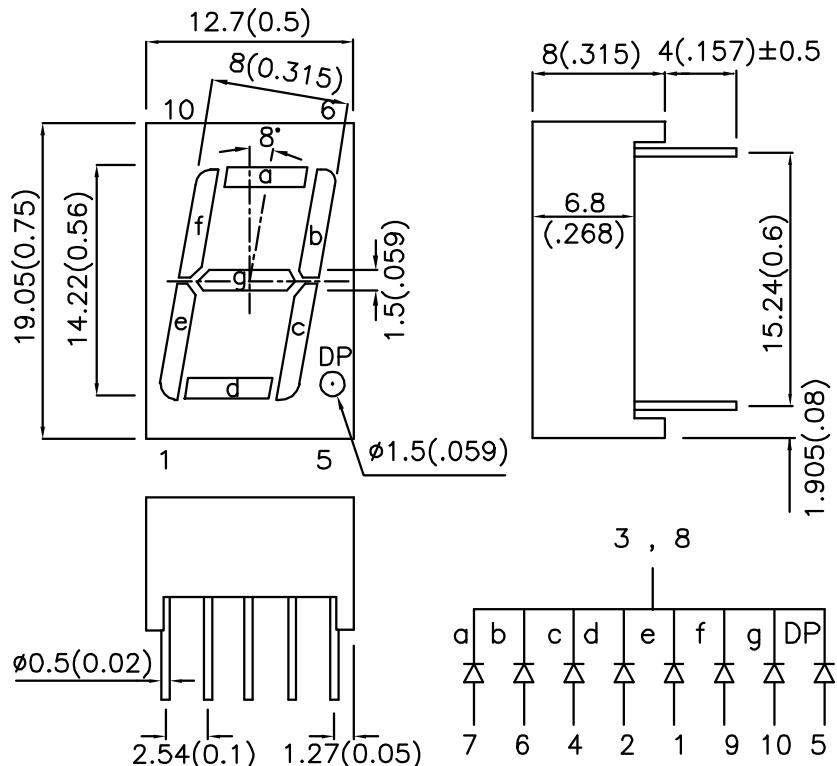
Features

- 0.56 INCH DIGIT HEIGHT.
- LOW CURRENT OPERATION.
- EXCELLENT CHARACTER APPEARANCE.
- EASY MOUNTING ON P.C. BOARDS OR SOCKETS.
- I.C. COMPATIBLE.
- MECHANICALLY RUGGED.
- STANDARD : GRAY FACE, WHITE SEGMENT.
- RoHS COMPLIANT.

Description

The Super Bright Red source color devices are made with Gallium Aluminum Arsenide Red Light Emitting Diode.

Package Dimensions & Internal Circuit Diagram



Notes:

1. All dimensions are in millimeters (inches), Tolerance is $\pm 0.25(0.01")$ unless otherwise noted.
2. Specifications are subject to change without notice.

Kingbright

Selection Guide

Part No.	Dice	Lens Type	I _V (ucd) @ 10mA		Description
			Min.	Typ.	
SC56-11SRWA	SUPER BRIGHT RED (GaAlAs)	WHITE DIFFUSED	4700	24000	Common Cathode, Rt. Hand Decimal.

Electrical / Optical Characteristics at T_A=25°C

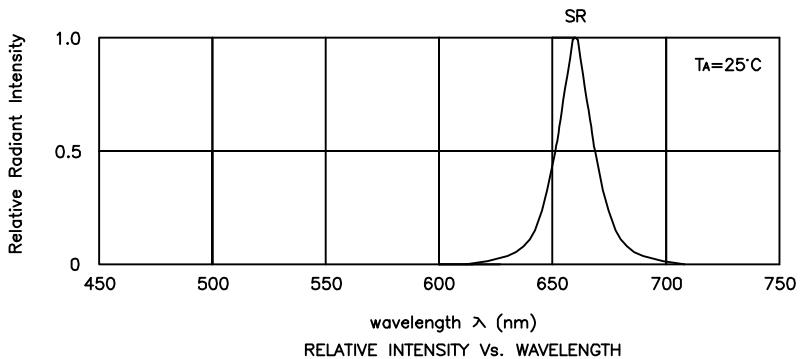
Symbol	Parameter	Device	Typ.	Max.	Units	Test Conditions
λpeak	Peak Wavelength	Super Bright Red	660		nm	I _F =20mA
λD	Dominant Wavelength	Super Bright Red	640		nm	I _F =20mA
Δλ1/2	Spectral Line Half-width	Super Bright Red	20		nm	I _F =20mA
C	Capacitance	Super Bright Red	45		pF	V _F =0V;f=1MHz
V _F	Forward Voltage	Super Bright Red	1.85	2.5	V	I _F =20mA
I _R	Reverse Current	Super Bright Red		10	uA	V _R = 5V

Absolute Maximum Ratings at T_A=25°C

Parameter	Super Bright Red	Units
Power dissipation	100	mW
DC Forward Current	30	mA
Peak Forward Current [1]	155	mA
Reverse Voltage	5	V
Operating / Storage Temperature	-40°C To +85°C	
Lead Solder Temperature [2]	260°C For 5 Seconds	

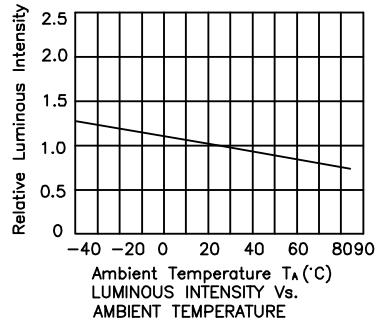
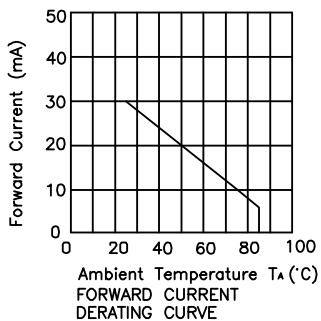
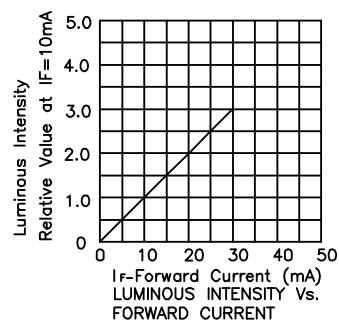
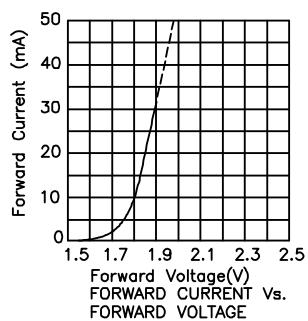
Notes:

1. 1/10 Duty Cycle, 0.1ms Pulse Width.
2. 2mm below package base.



Super Bright Red

SC56-11SRWA



Remarks:

If special sorting is required (e.g. binning based on forward voltage, luminous intensity or wavelength), the typical accuracy of the sorting process is as follows:

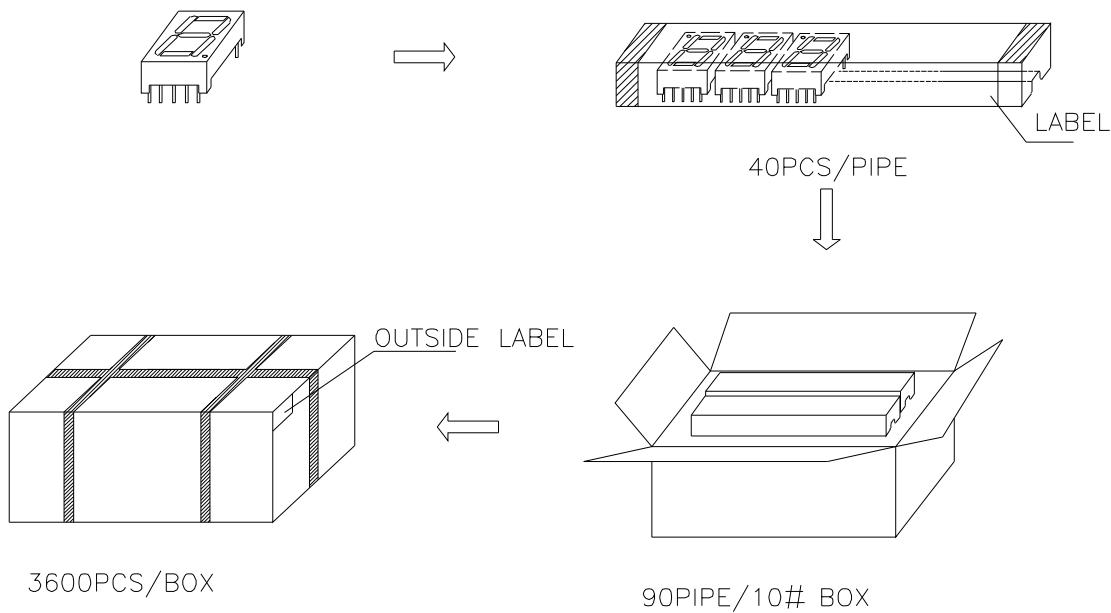
1. Wavelength: +/-1nm
2. Luminous Intensity: +/-15%
3. Forward Voltage: +/-0.1V

Note: Accuracy may depend on the sorting parameters.

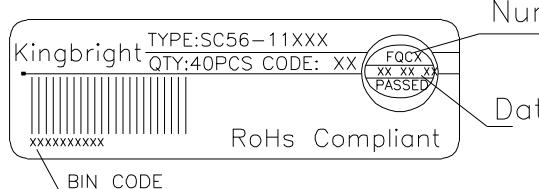
Kingbright

PACKING & LABEL SPECIFICATIONS

SC56-11SRWA



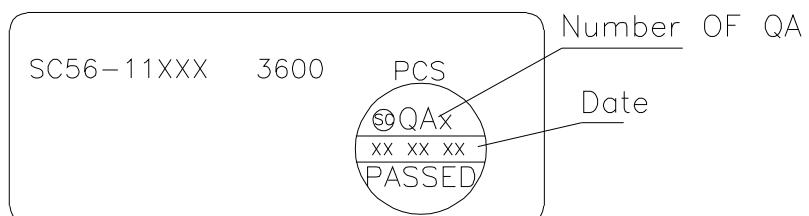
Inside LABEL Paste On The IC-pipe



Number OF FQC

Date

Outside LABEL Paste On The Box



Number OF QA

Date