## LC3 Quick Reference Guide

## Instruction Set

		Thistraction Set	
Op	Format	Description	Example
ADD	ADD DR, SR1, SR2	Adds the values in SR1 and	ADD R1, R2, #5
	ADD DR, SR1, imm5	SR2/imm5 and sets DR to that	The value 5 is added to the value in
		value.	R2 and stored in R1.
AND	AND DR, SR1, SR2	Performs a bitwise and on the	AND R0, R1, R2
	AND DR, SR1, imm5	values in SR1 and SR2/imm5	A bitwise and is preformed on the
		and sets DR to the result.	values in R1 and R2 and the result
			stored in R0.
BR	BR(n/z/p) LABEL	Branch to the code section	BRz LPBODY
	Note: (n/z/p) means	indicated by LABEL, if the bit	Branch to LPBODY if the last
	any combination of	indicated by (n/z/p) has been set	instruction that modified the
	those letters can appear	by a previous instruction. n:	condition codes resulted in zero.
	there, but must be in	negative bit, z: zero bit, p:	BRnp ALT1
	that order.		Branch to ALT1 if last instruction
	that order.	positive bit. Note that some	
		instructions do not set condition	that modified the condition codes
		codes bits.	resulted in a positive or negative
			(non-zero) number.
JMP	JMP SR1	Unconditionally jump to the	JMP R1
JIVII	JIVIF SKI	instruction based upon the	Jump to the code indicated by the
		address in SR1.	address in R1.
ICD	JSR LABEL		JSR POP
JSR	JSK LABEL	Put the address of the next	
		instruction after the JSR	Store the address of the next
		instruction into R7 and jump to	instruction into R7 and jump to the
		the subroutine indicated by	subroutine POP.
		LABEL.	
JSRR	JSSR SR1	Similar to JSR except the	JSSR R3
		address stored in SR1 is used	Store the address of the next
		instead of using a LABEL.	instruction into R7 and jump to the
			subroutine indicated by R3's value.
LD	LD DR, LABEL	Load the value indicated by	LD R2, VAR1
		LABEL into the DR register.	Load the value at VAR1 into R2.
LDI	LDI DR, LABEL	Load the value indicated by the	LDI R3, ADDR1
		address at LABEL's memory	Suppose ADDR1 points to a
		location into the DR register.	memory location with the value
			x3100. Suppose also that memory
			location x3100 has the value 8. 8
			then would be loaded into R3.
LDR	LDR DR, SR1, offset6	Load the value from the memory	LDR R3, R4, #-2
LUK	22K 2K, 5K1, 011500	location found by adding the	Load the value found at the address
		value of SR1 to offset6 into DR.	(R4 –2) into R3.
LEA	LEA DR, LABEL	Load the address of LABEL into	LEA R1, DATA1
LEA	LLA DI, LADEL		Load the address of DATA1 into
		DR.	
NOT	NOT DR, SR1	Performs a bitwise not on SR1	R1. NOT R0, R1
NOI	NOI DK, SKI	and stores the result in DR.	· · · · · · · · · · · · · · · · · · ·
		and stores the result in DK.	A bitwise not is preformed on R1
	D.F.III		and the result is stored in R0.
RET	RET	Return from a subroutine using	RET
		the value in R7 as the base	Equivalent to JMP R7.
		address.	

RTI	RTI	Return from an interrupt to the code that was interrupted. The address to return to is obtained by popping it off the supervisor stack, which is automatically done by RTI.	RTI  Note: RTI can only be used if the processor is in supervisor mode.
ST	ST SR1, LABEL	Store the value in SR1 into the memory location indicated by LABEL.	ST R1, VAR3 Store R1's value into the memory location of VAR3.
STI	STI SR1, LABEL	Store the value in SR1 into the memory location indicated by the value that LABEL's memory location contains.	STI R2, ADDR2 Suppose ADDR2's memory location contains the value x3101. R2's value would then be stored into memory location x3101.
STR	STR SR1, SR2, offset6	The value in SR1 is stored in the memory location found by adding SR2 and offest6 together.	STR R2, R1, #4 The value of R2 is stored in memory location (R1 + 4).
TRAP	TRAP trapvector8	Performs the trap service specified by trapvector8. Each trapvector8 service has its own assembly instruction that can replace the trap instruction.	TRAP x25 Calls a trap service to end the program. The assembly instruction HALT can also be used to replace TRAP x25.

Symbol Legend

Symbol	Description	Symbol	Description
SR1, SR2	Source registers used by instruction.	LABEL	Label used by instruction.
DR	Destination register that will hold	trapvector8	8 bit value that specifies trap service
	the instruction's result.		routine.
imm5	Immediate value with the size of 5	offset6	Offset value with the size of 6 bits.
	bits.		

## TRAP Routines

Trap Vector	Equivalent Assembly	Description
	Instruction	
x20	GETC	Read one input character from the keyboard and store it into R0
		without echoing the character to the console.
x21	OUT	Output character in R0 to the console.
x22	PUTS	Output null terminating string to the console starting at address
		contained in R0.
x23	IN	Read one input character from the keyboard and store it into R0 and
		echo the character to the console.
x24	PUTSP	Same as PUTS except that it outputs null terminated strings with
		two ASCII characters packed into a single memory location, with
		the low 8 bits outputted first then the high 8 bits.
x25	HALT	Ends a user's program.

Pseudo-ops

Pseudo-op	Format	Description
		Para Para
.ORIG	.ORIG#	Tells the LC-3 simulator where it should place the segment of
		code starting at address #.
.FILL	.FILL#	Place value # at that code line.
.BLKW	.BLKW #	Reserve # memory locations for data at that line of code.
.STRINGZ	.STRINGZ " <string>"</string>	Place a null terminating string <string> starting at that location.</string>
.END	.END	Tells the LC-3 assembler to stop assembling your code.