REV	Description	Date
V1.0	First Release	2016-11-12

AX7020 Schematics

黑金ZYNQ硬件平台

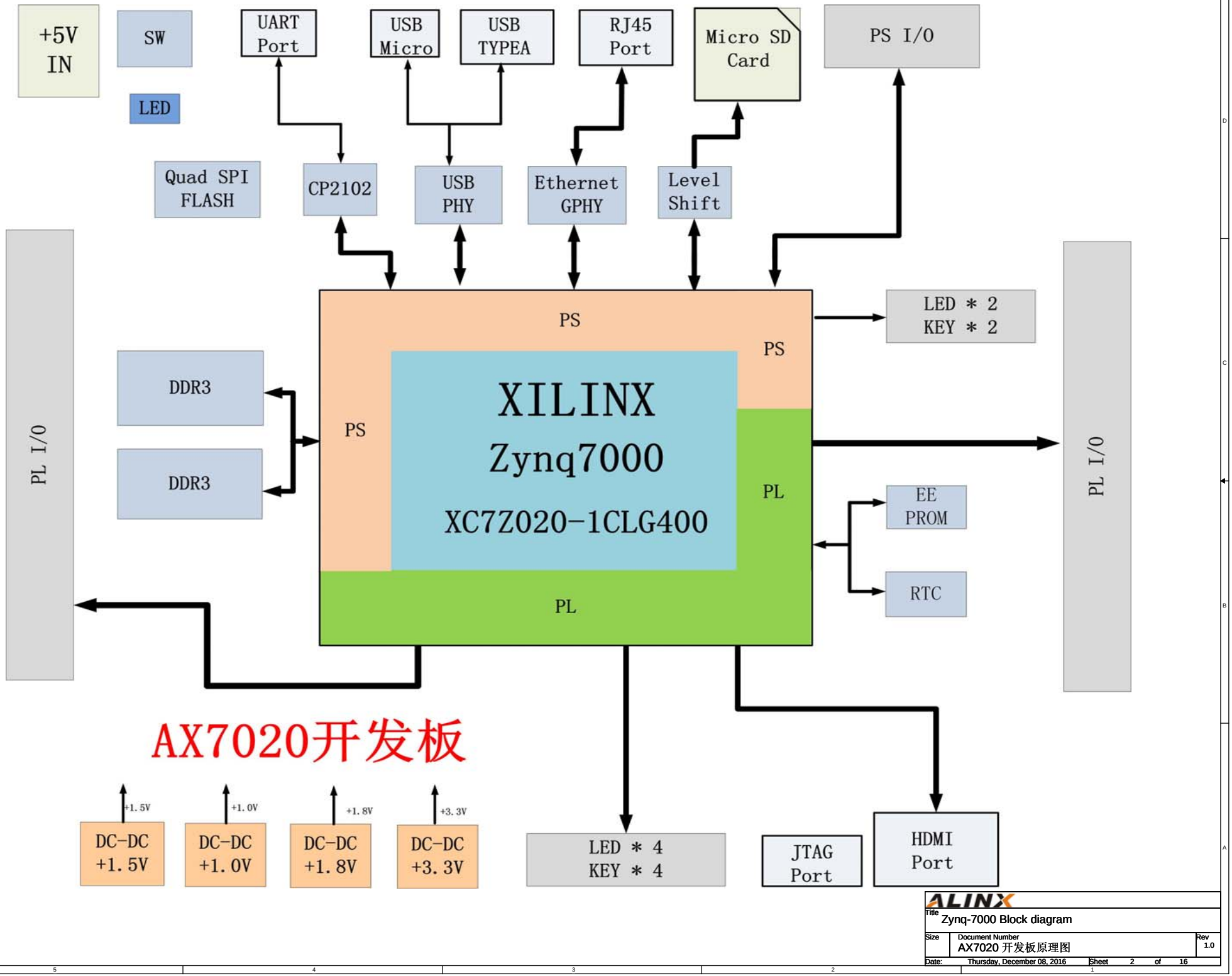
Page Number	Description
Page01	Cover Page
Page02	Block Diagram
Page03	Zynq-7000 JTAG & Bank0
Page04	Zynq-7000 MIO Config
Page05	Zynq-7000 Bank13-34-35
Page06	Zynq-7000 Bank502
Page07	Zynq-7000 Power
Page08	DDR3
Page09	GPHY
Page10	USB OTG
Page11	FLASH, RTC, EEPROM
Page12	LED, KEY
Page13	UART, SD
Page14	HDMI
Page15	EXTEND IO
Page16	POWER

ALINX

Title: Zynq-7000 Cover Page

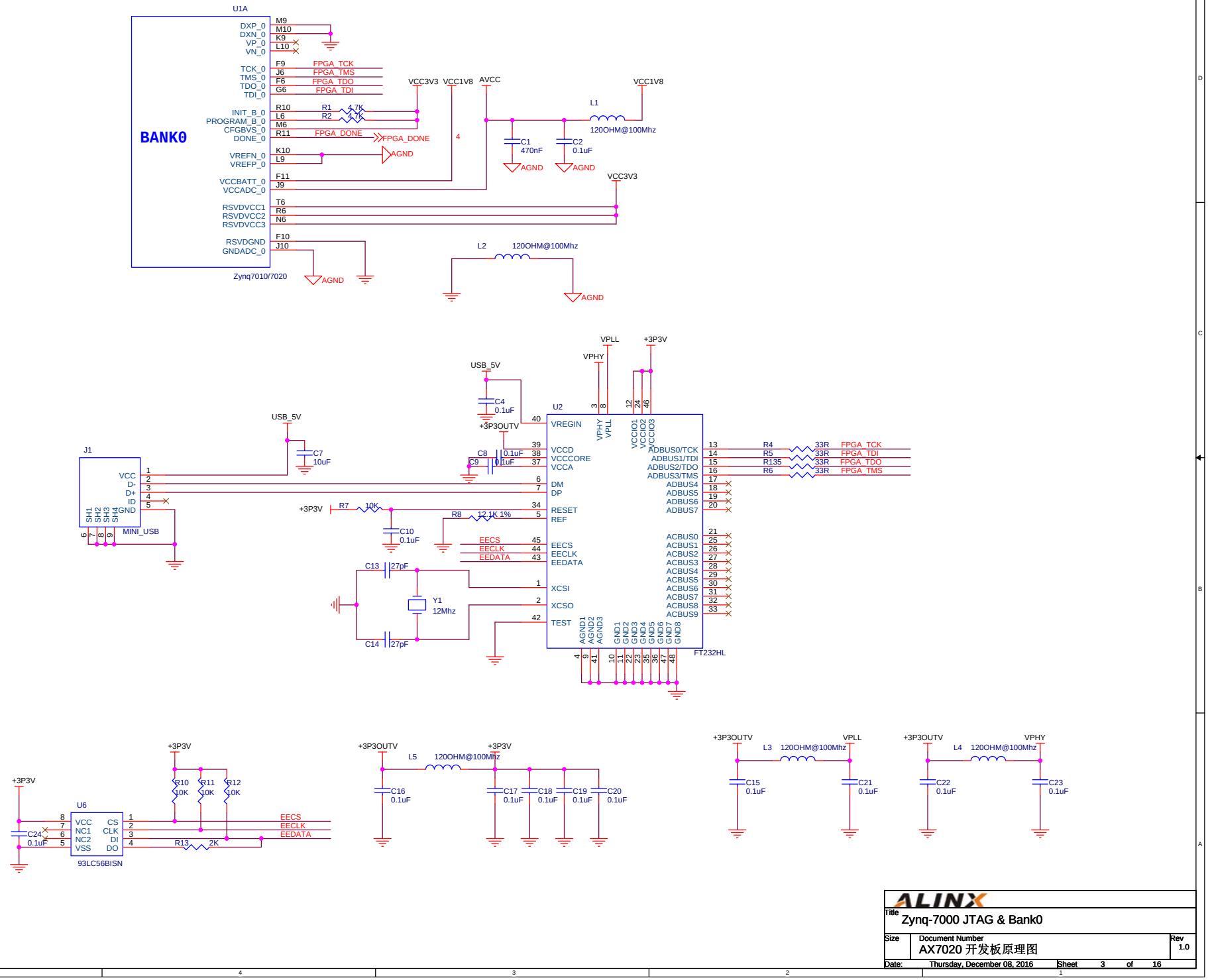
Size | Document Number: AX7020 开发板原理图 | Rev: 1.0

Date: Thursday, December 08, 2016 | Sheet 1 of 16



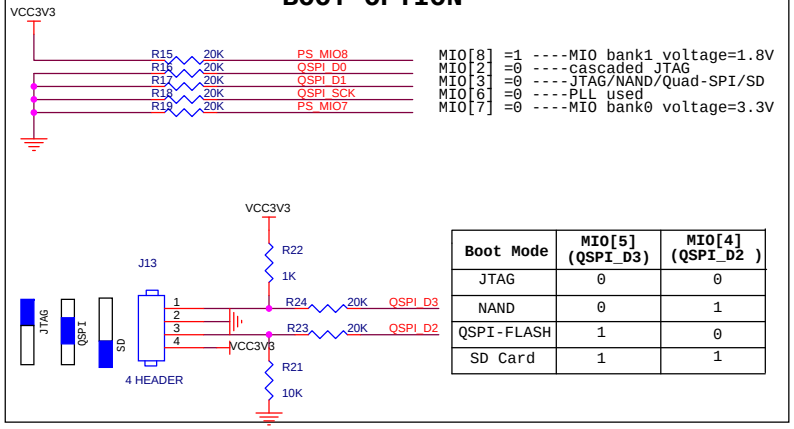
ALINX

Title	Zynq-7000 Block diagram	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 2 of 16	



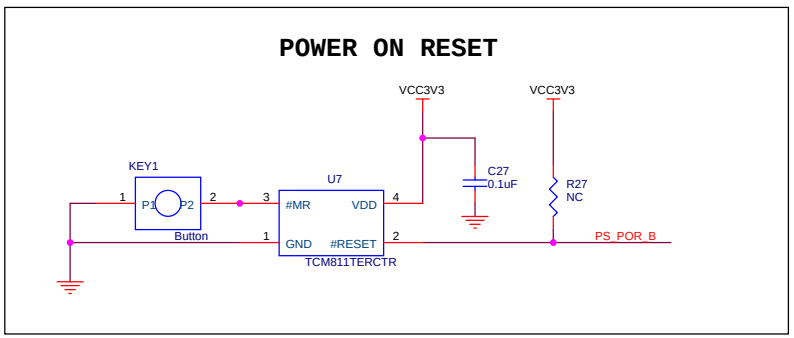
Title	Zynq-7000 JTAG & Bank0		
Size	Document Number: AX7020 开发板原理图		Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 3 of 16		

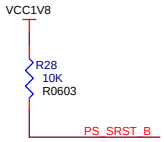
BOOT OPTION

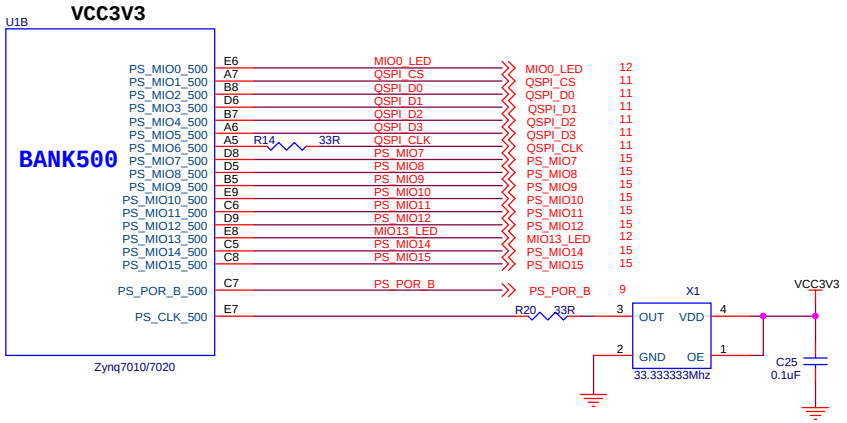


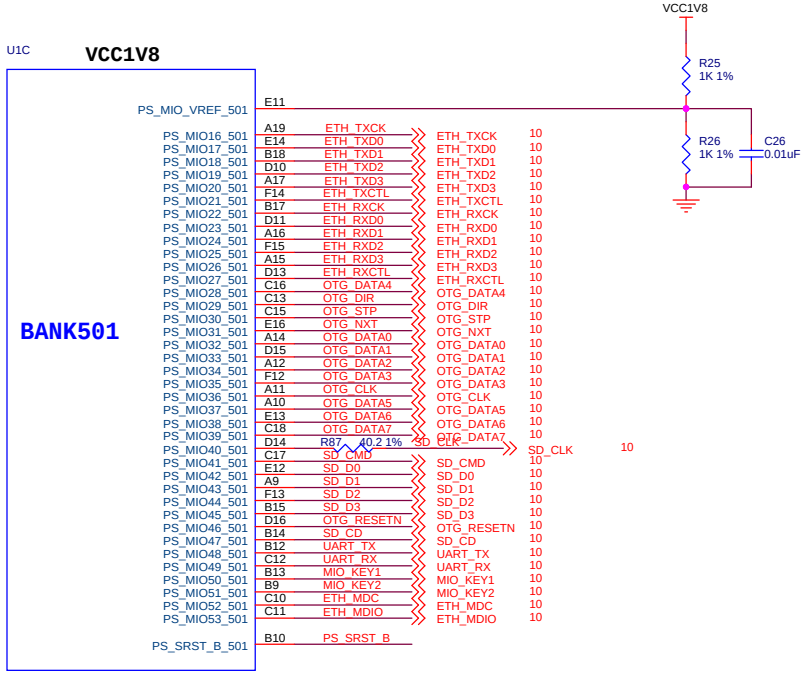
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET



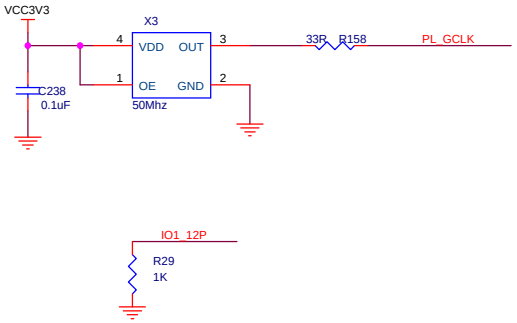


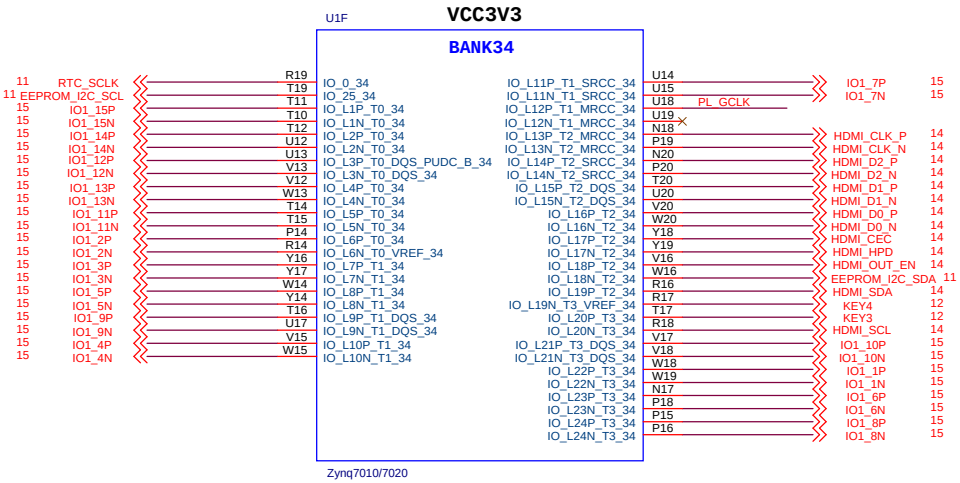


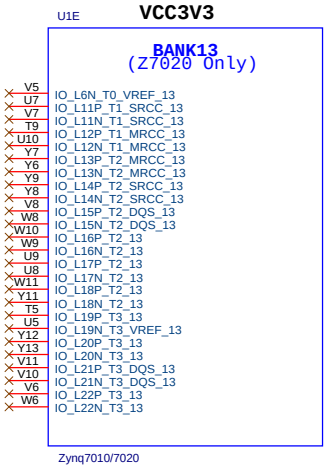


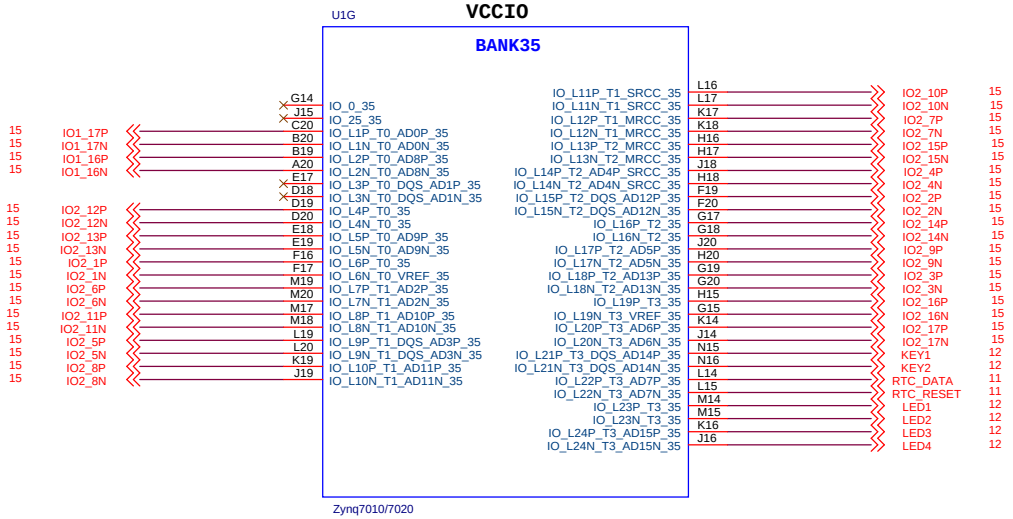
ALINX

Title	Zynq-7000 PS MIO	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 4 of 16	







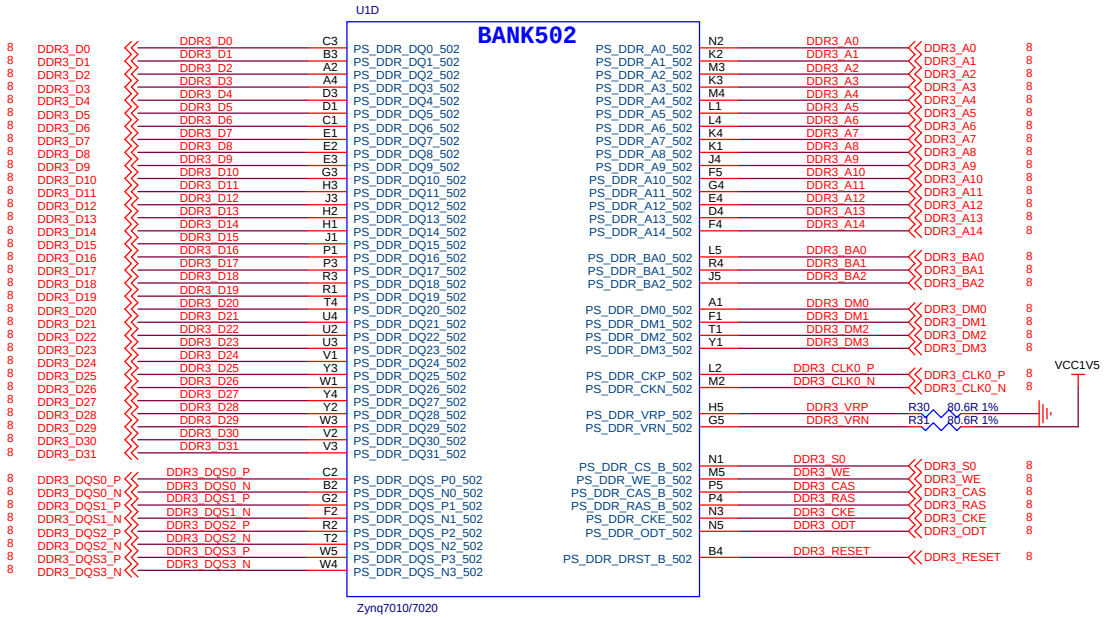


ALINX

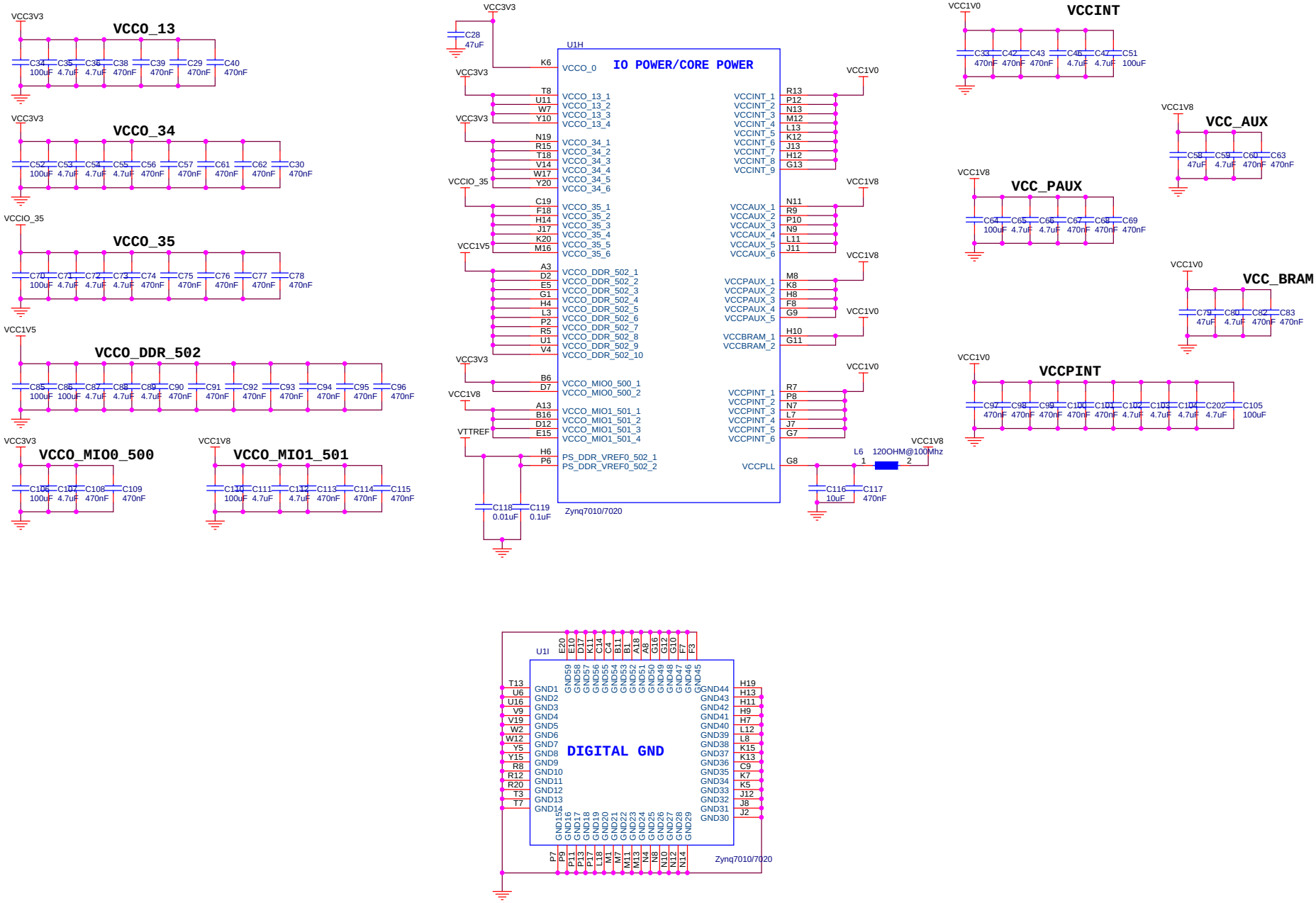
Title: Zynq-7000 Bank13 & 34 & 35

Size	Document Number	Rev
	AX7020 开发板原理图	1.0

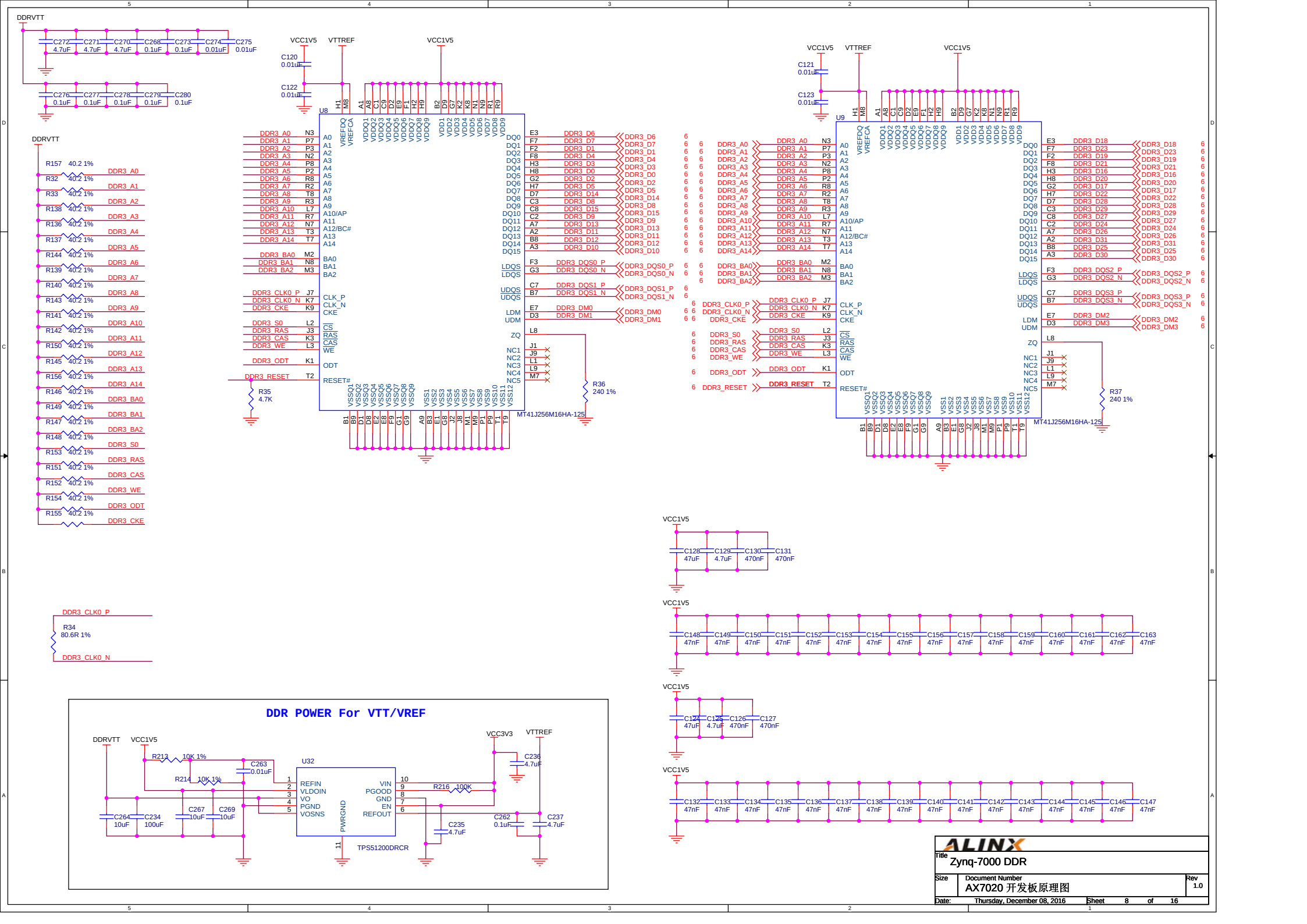
Date: Thursday, December 08, 2016 Sheet 5 of 16

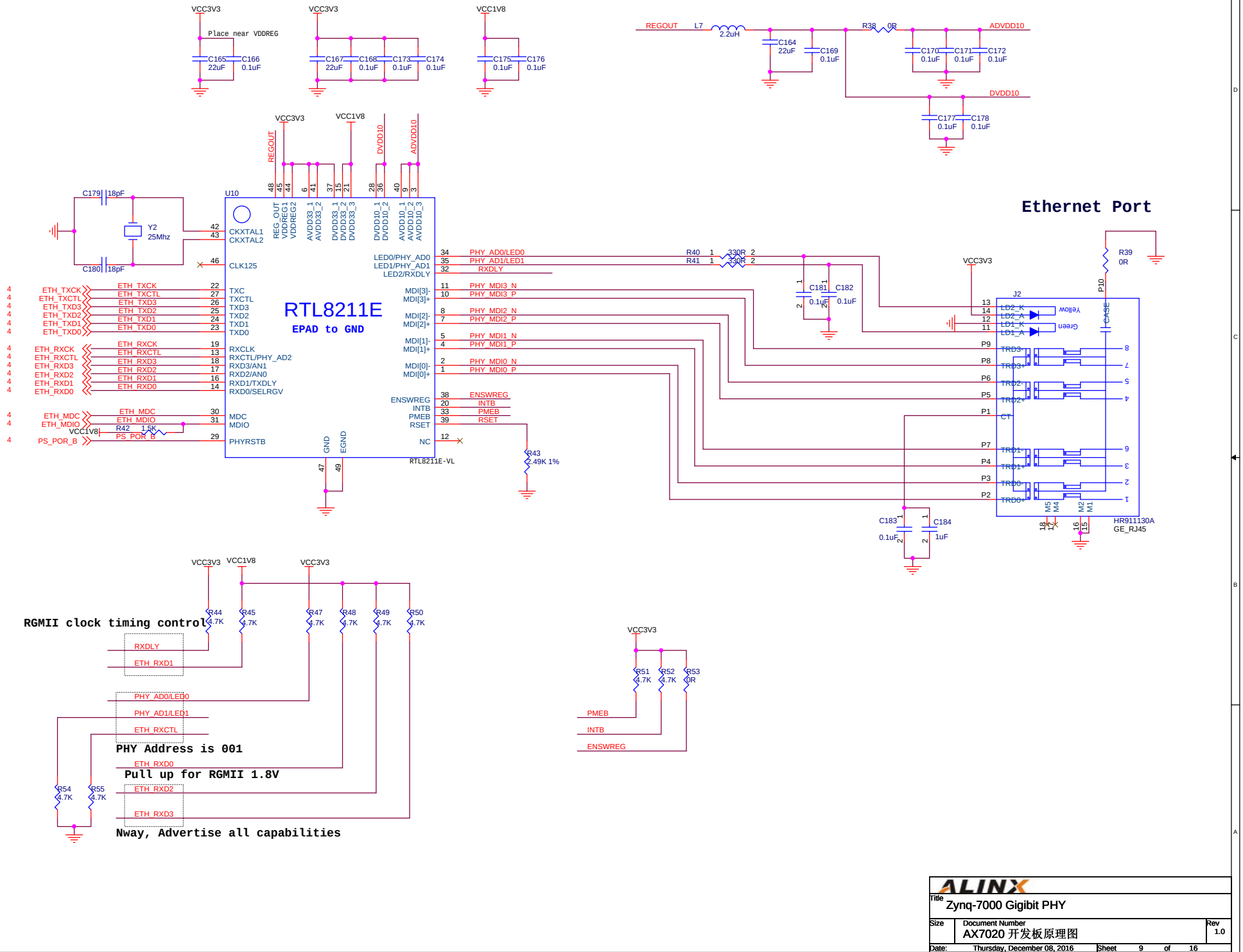


Title	Zynq-7000 Bank502	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 6 of 16	

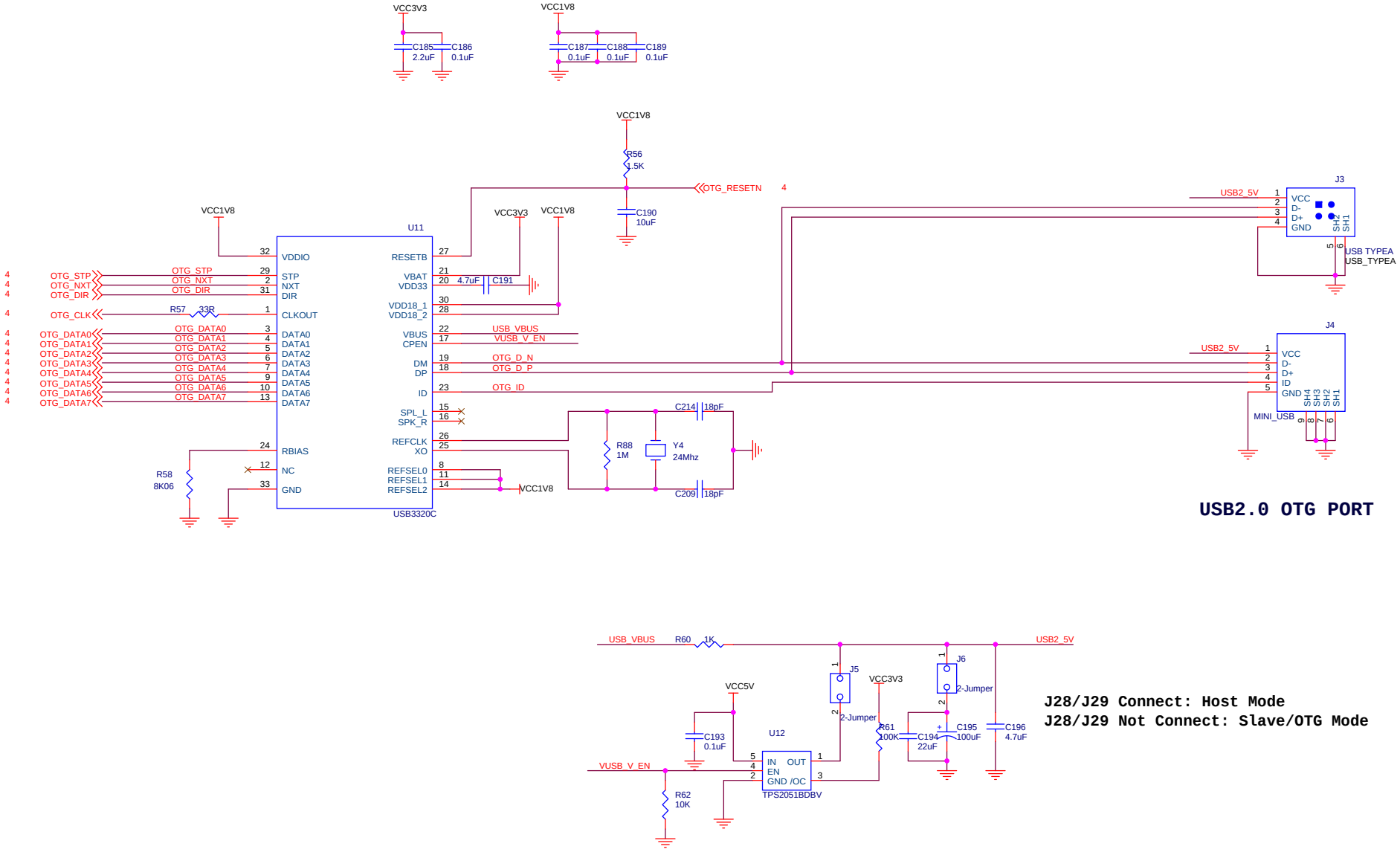


Title	Zynq-7000 Cover Page		
Size	Document Number AX7020 开发板原理图		Rev 1.0
Date: Thursday, December 08, 2016	Sheet 7 of 16		

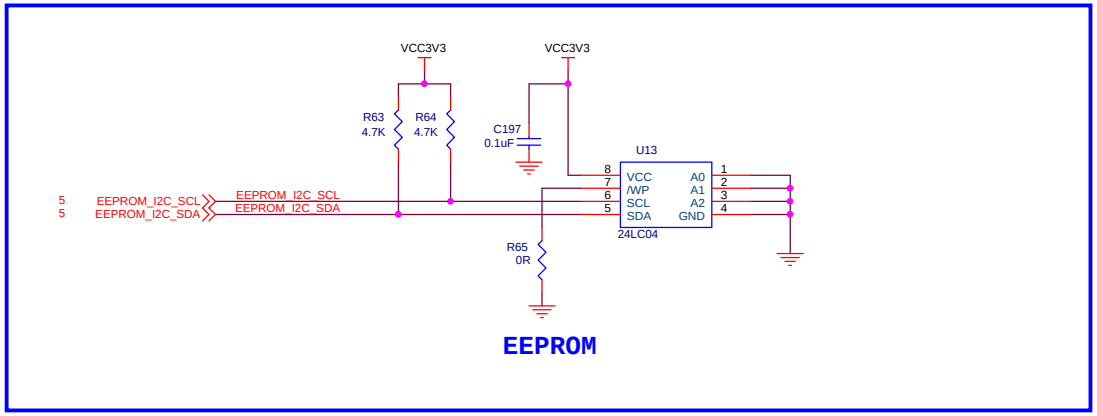

DDRVTT
C272 4.7uF
C271 4.7uF
C270 4.7uF
C268 0.1uF
C273 0.1uF
C274 0.01uF
C275 0.01uF
C276 0.1uF
C277 0.1uF
C278 0.1uF
C279 0.1uF
C280 0.1uF
VCC1V5
VTTREF
C120 0.01uF
C122 0.01uF
U8
MT41J256M16HA-125
R35 4.7K
R36 240 1%
C121 0.01uF
C123 0.01uF
U9
MT41J256M16HA-125
R37 240 1%
R157 40.2 1%
R32 40.2 1%
R33 40.2 1%
R138 40.2 1%
R136 40.2 1%
R137 40.2 1%
R144 40.2 1%
R139 40.2 1%
R140 40.2 1%
R143 40.2 1%
R141 40.2 1%
R142 40.2 1%
R150 40.2 1%
R145 40.2 1%
R156 40.2 1%
R146 40.2 1%
R149 40.2 1%
R147 40.2 1%
R148 40.2 1%
R153 40.2 1%
R151 40.2 1%
R152 40.2 1%
R154 40.2 1%
R155 40.2 1%
DDR3_CLK0_P
R34 80.6R 1%
DDR3_CLK0_N
C128 47uF
C129 4.7uF
C130 470nF
C131 470nF
C148 47nF
C149 47nF
C150 47nF
C151 47nF
C152 47nF
C153 47nF
C154 47nF
C155 47nF
C156 47nF
C157 47nF
C158 47nF
C159 47nF
C160 47nF
C161 47nF
C162 47nF
C163 47nF
C124 47uF
C125 4.7uF
C126 470nF
C127 470nF
C132 47nF
C133 47nF
C134 47nF
C135 47nF
C136 47nF
C137 47nF
C138 47nF
C139 47nF
C140 47nF
C141 47nF
C142 47nF
C143 47nF
C144 47nF
C145 47nF
C146 47nF
C147 47nF
DDR POWER For VTT/VREF
VCC3V3
C263 0.01uF
R213 10K 1%
R214 10K 1%
U32
TPS51200DRCR
R216 100K
C236 4.7uF
C264 10uF
C234 100uF
C267 10uF
C269 10uF
C235 4.7uF
C262 0.1uF
C237 4.7uF
ALINX
Title
Zynq-7000 DDR
Size
Document Number
AX7020 开发板原理图
Rev
1.0
Date: Thursday, December 08, 2016
Sheet 8 of 16

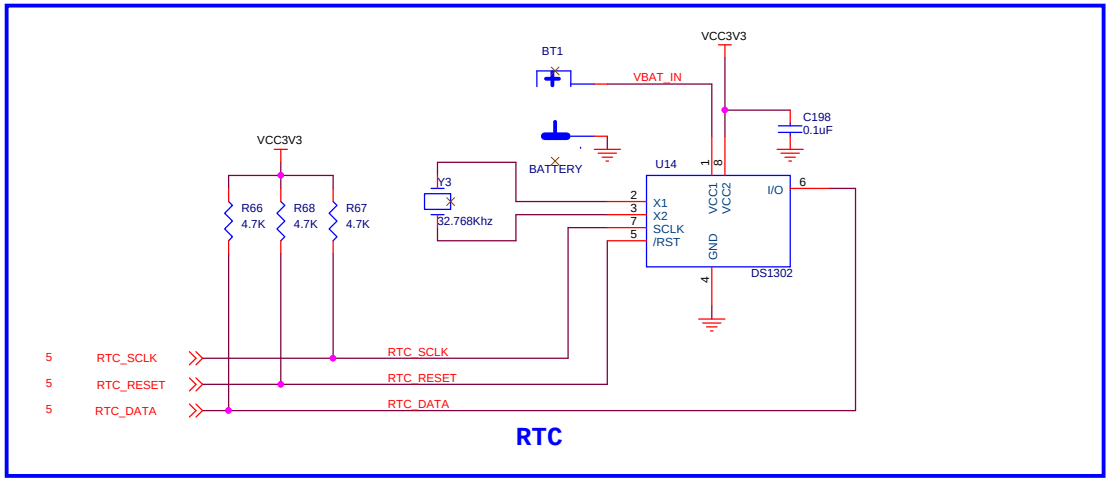


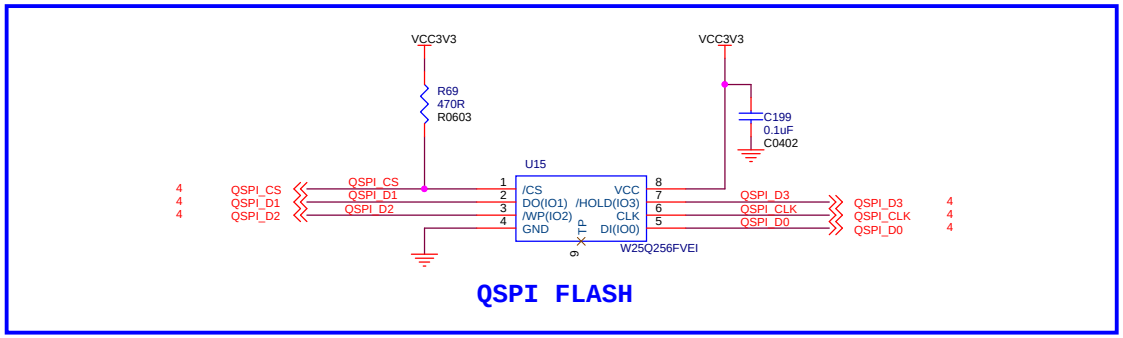
Title	Zynq-7000 Gigibit PHY	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 9 of 16	



Title	Zynq-7000 OTG USB	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 10 of 16	





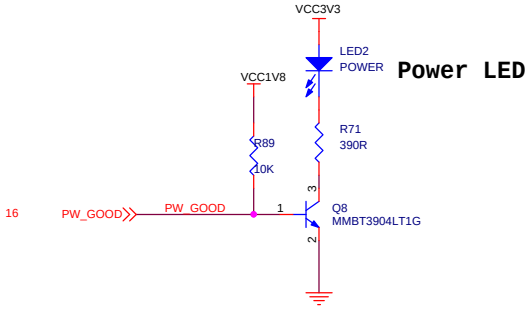


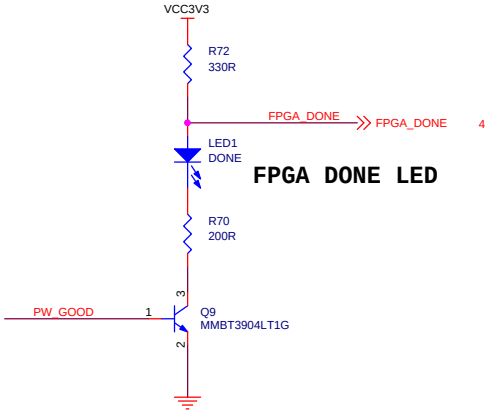
ALINX

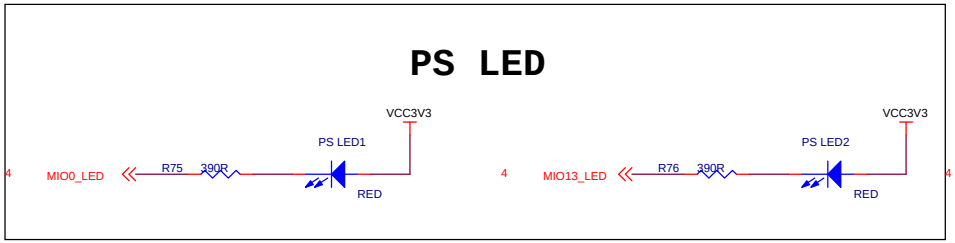
Title: Zynq-7000 QSPI & RTC & EEPROM

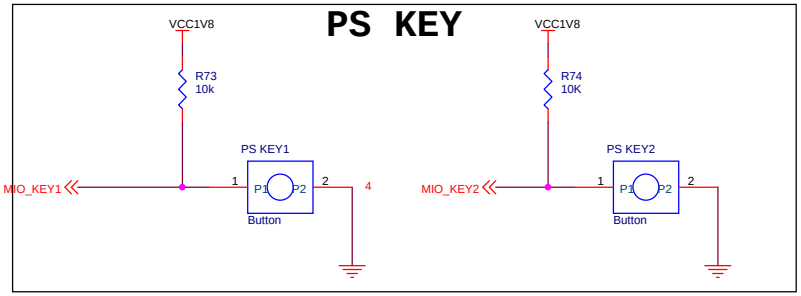
Size	Document Number	Rev
	AX7020 开发板原理图	1.0

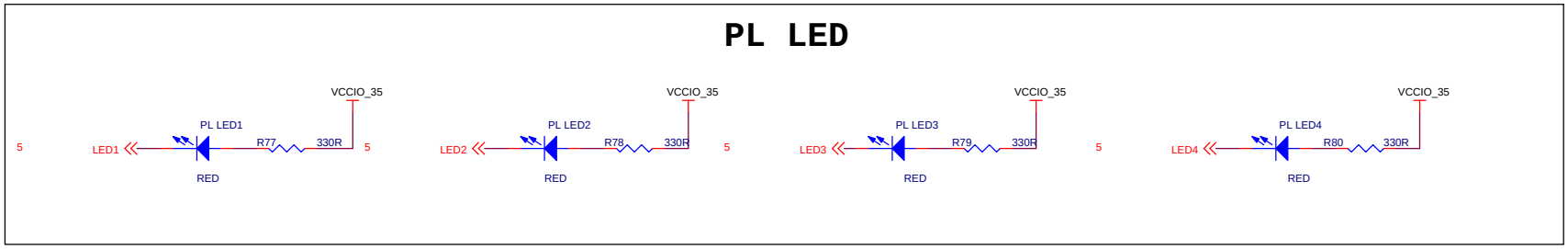
Date: Thursday, December 08, 2016 Sheet 11 of 16

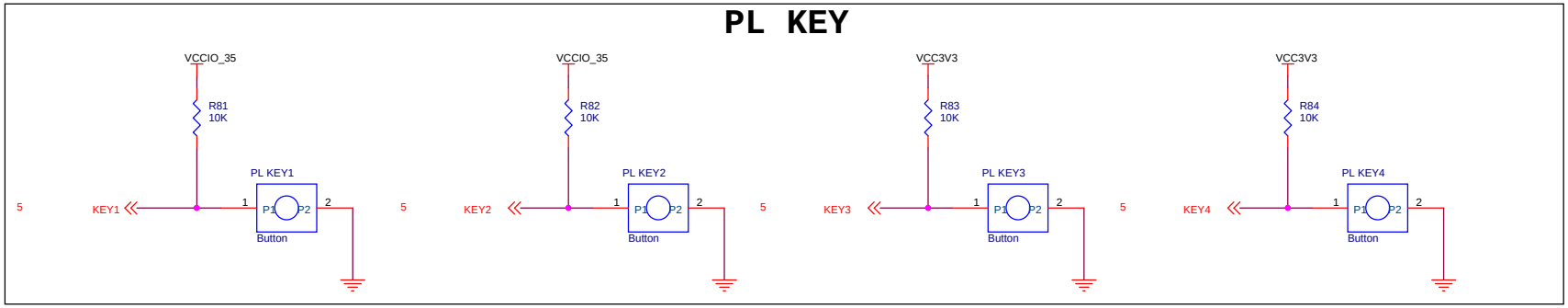








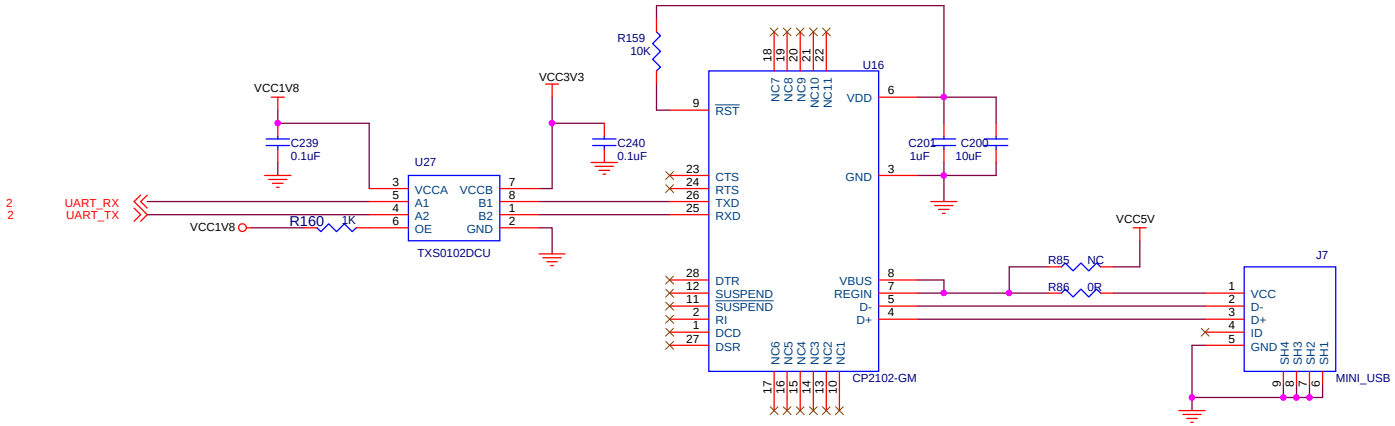




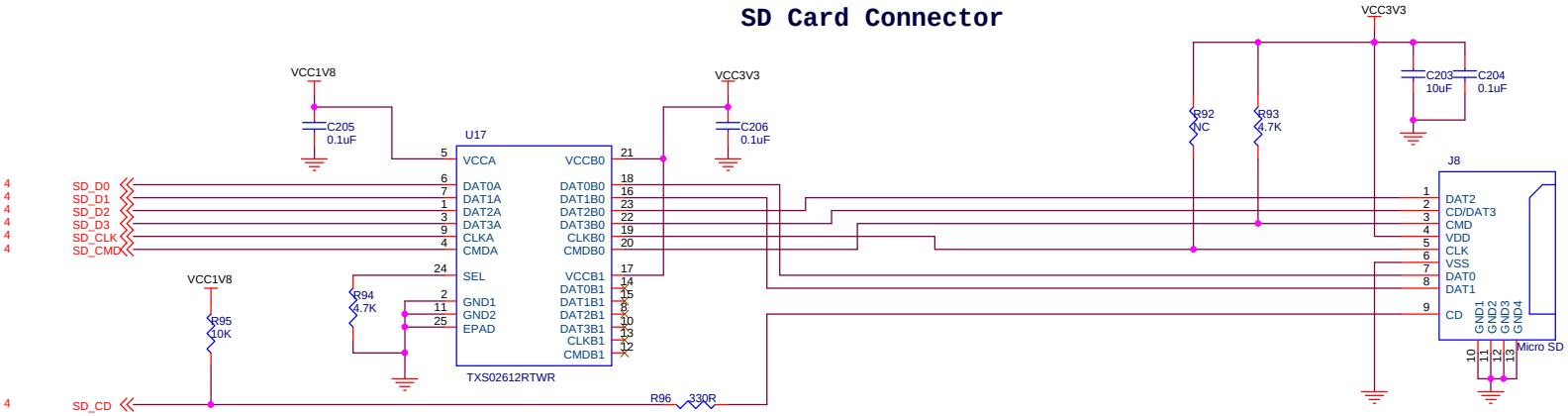
ALINX

Title	Zynq-7000 LED & KEY	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 12 of 16	

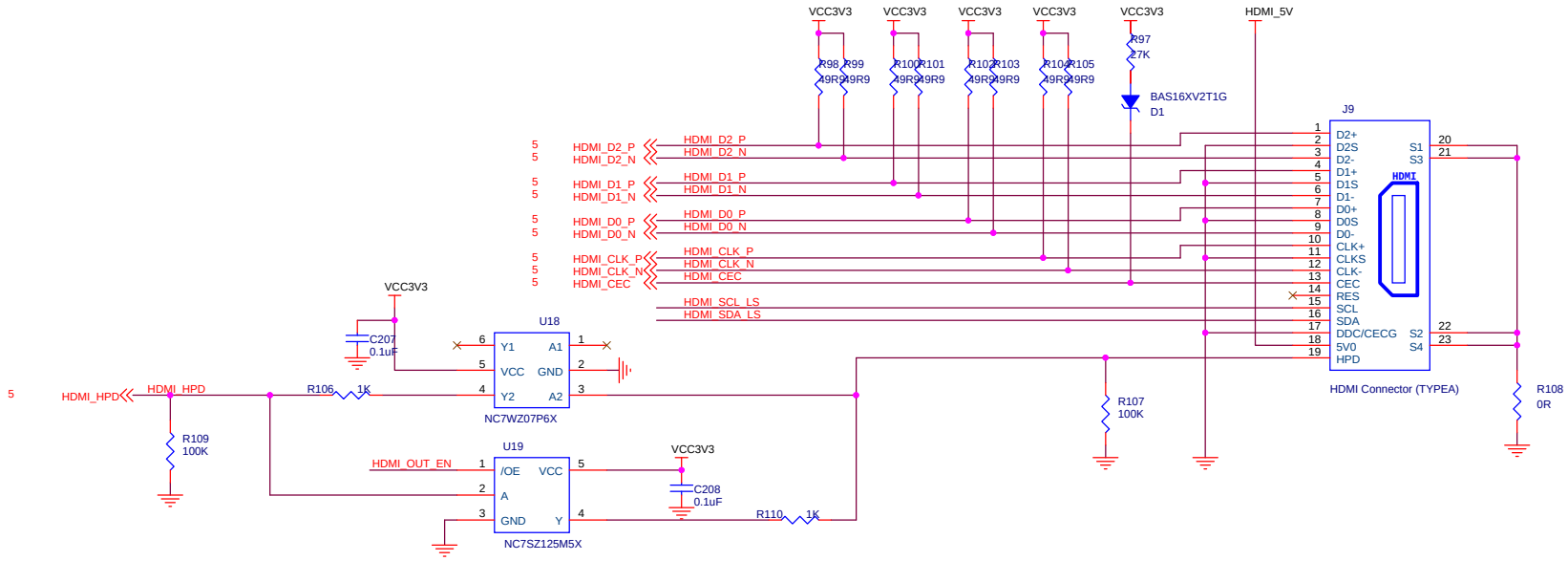
USB Uart

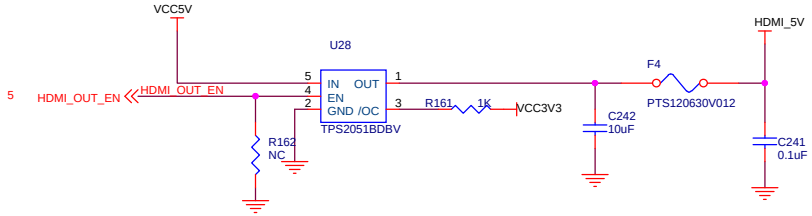


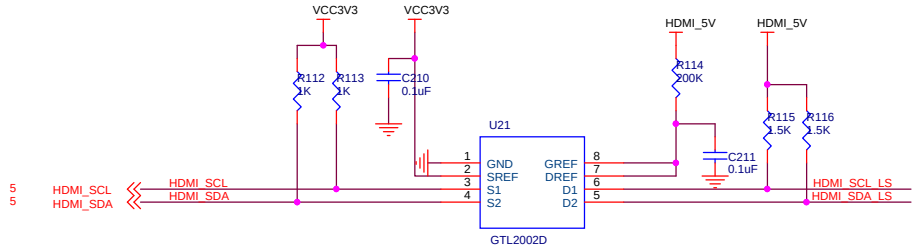
SD Card Connector



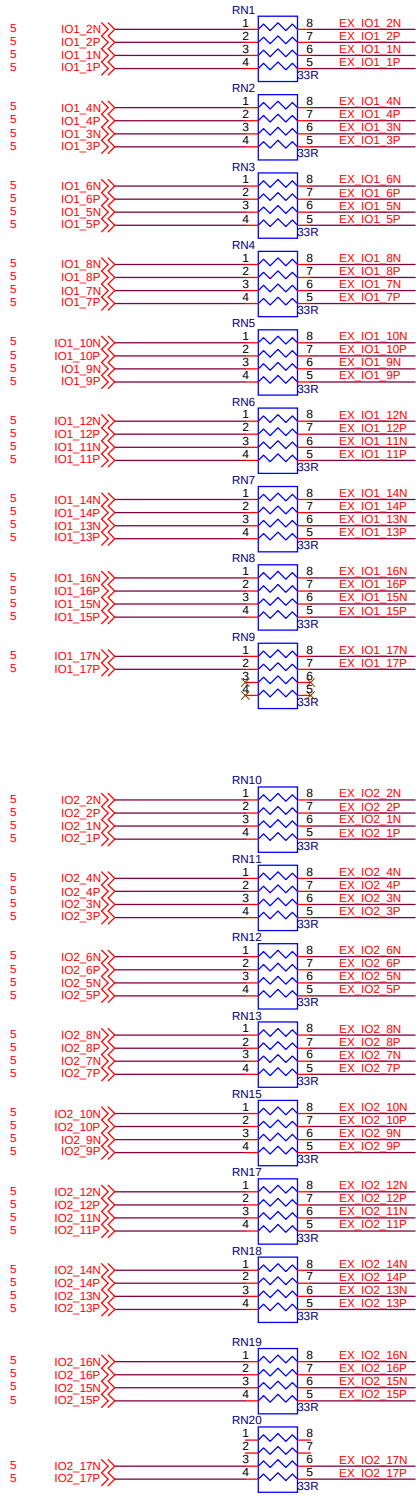
Title	Zynq-7000 UART & SD	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 13 of 16	



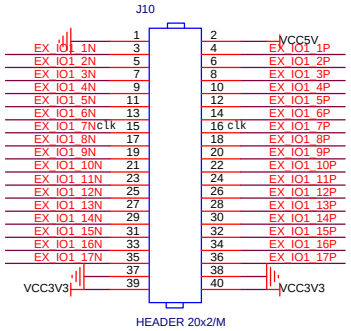


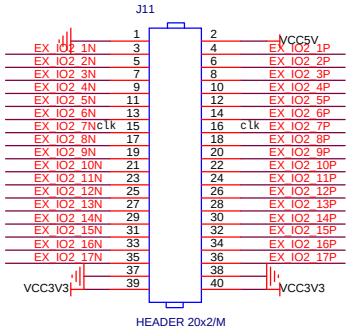


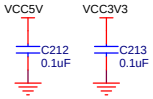
Title	Zynq-7000 HDMI		
Size	Document Number AX7020 开发板原理图		Rev 1.0
Date: Thursday, December 08, 2016	Sheet 14 of 16		

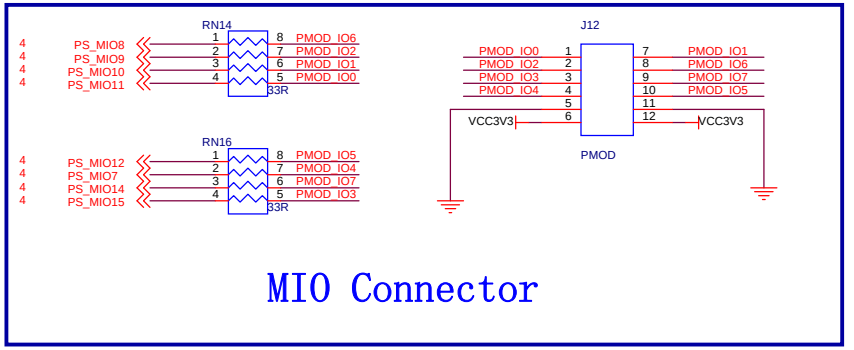


FPGA 40 PIN External IO

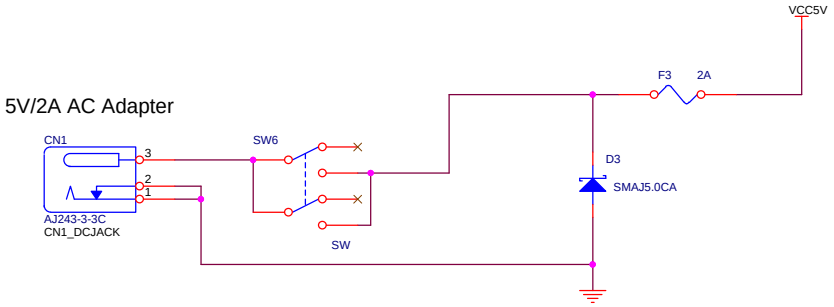


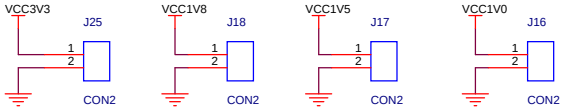


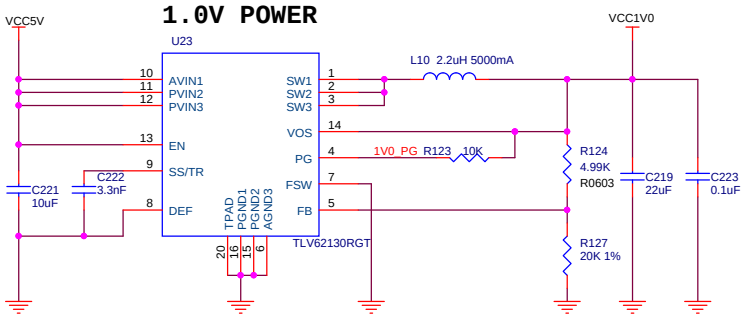


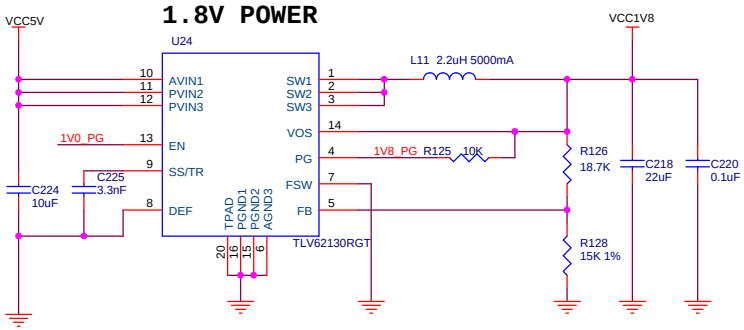


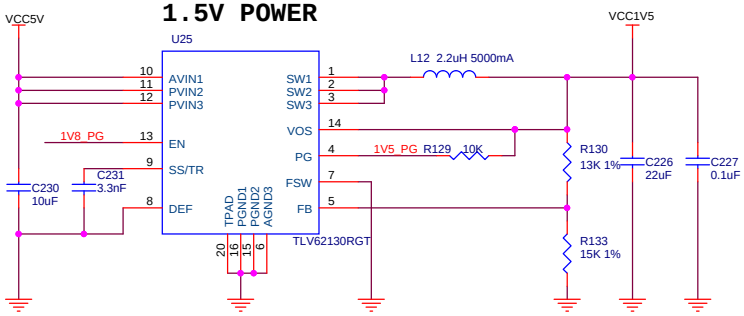
ALINX		
Title	Zynq-7000 LED & KEY & IO	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 15 of 16	

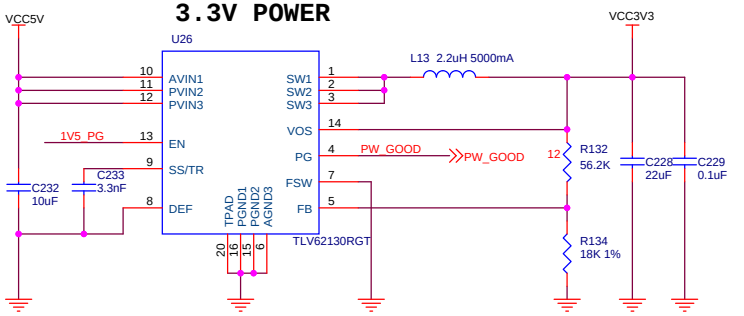






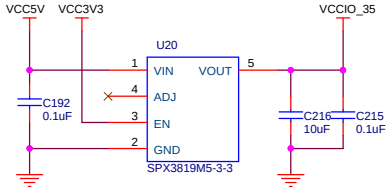






Power On Sequnce:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO



ALINX

Title	Power	
Size	Document Number: AX7020 开发板原理图	Rev: 1.0
Date: Thursday, December 08, 2016	Sheet 16 of 16	