

The Advanced Threats Evolution: REsearchers Arm Race

@matrosov

Offensive Security REsearch at

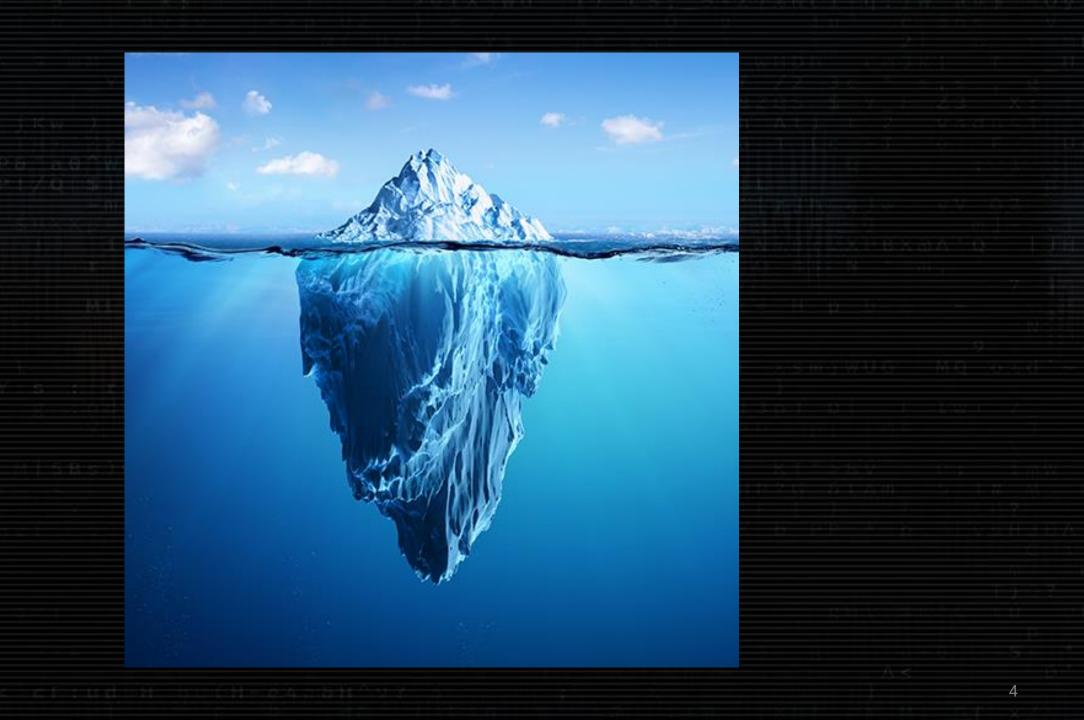


Former Principal Security Researcher @Cylance @Intel @ESET

Doing Security REsearch since 1997



How I got the idea to talk about evolution of persistence techniques?



Security Industry Visibility Point



Modern Persistence Techniques



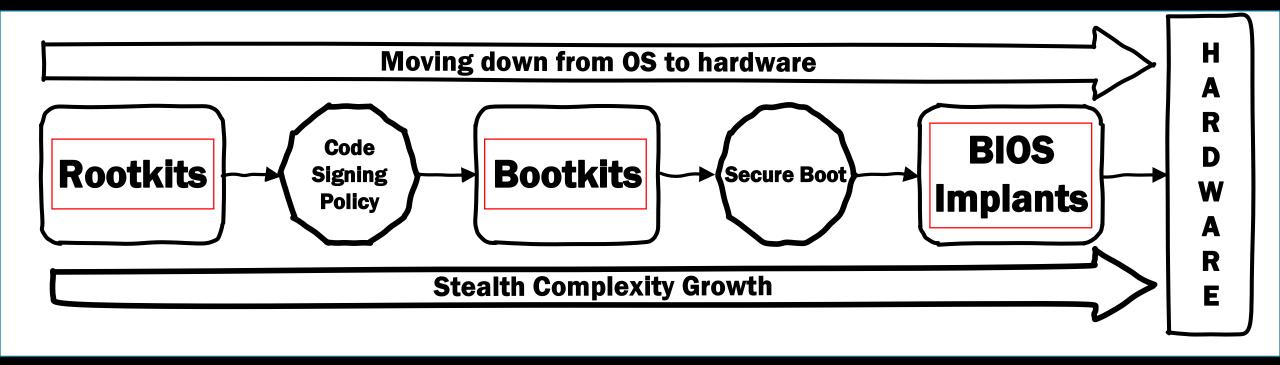


Evolution of persistence techniques

Mitigations against malware persistence techniques are raising the bar of complexity, but the bar is always covered only the most common ones.

More mitigations, more persistence complexity





Types of Persistence



blindspot

Hardware

Firmware

HW/OS change Persistence

Endpoints

AV/EDR

Boot Sectors

Boot Loaders

File System

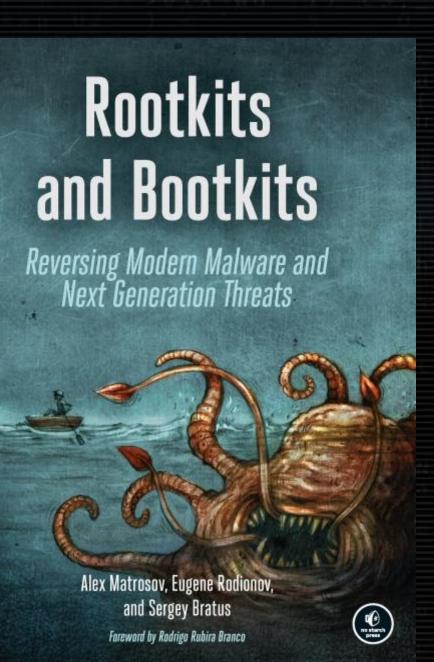
OS Kernel

OS User Space

Memory

Reboot/Shutdown Persistence

Sleep/Hibernate Persistence



Rootkits



Golden Age of Rootkits (2006 - 2012) Bootkits (2011 - 2015)



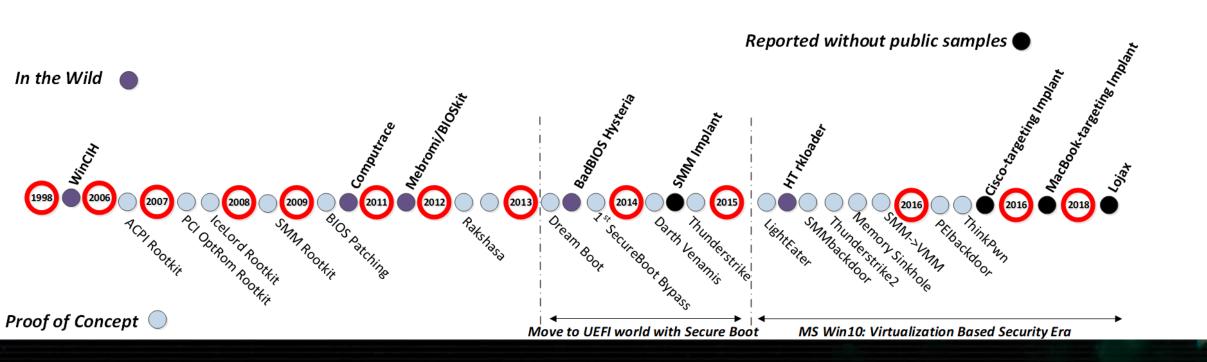
- ☐ Cybercrime actors persistence goals
 - ☐ Long term infection rate
 - ☐ Spam bots
 - □ DDoS bots

- □ State-sponsored actors persistence goals
 - ☐ Long term covered operations
 - ☐ Espionage, gathering data
 - ☐ Attack specific target in specific time

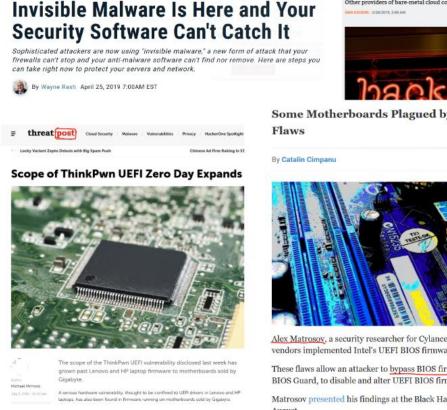
https://github.com/bootkitsbook/rootkits

Golden Age of Firmware/Hardware Implants is happening right now!

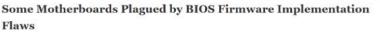
The retrospective of incidents with BIOS implants



Number of incidents with firmware increases every year









Alex Matrosov, a security researcher for Cylance, has discovered several flaws in how some motherboard vendors implemented Intel's UEFI BIOS firmware into their products.

These flaws allow an attacker to <u>bypass BIOS</u> firmware protections, such as Intel BIOS Guard and Intel BIOS Guard, to disable and alter UEFI BIOS firmware, such as placing a rootkit.

Matrosov presented his findings at the Black Hat USA 2017 security conference held in Las Vegas in August.





Bloomberg Businessweek

The Big Hack: The Software Side of China's Supply Chain Attack

 It wasn't just hardware. An online portal for firmware updates hid and distributed malware.

"Firmware attacks are hard to detect by current antivirus and

other security software because firmware resides at architectural levels of the device that are not usually accessible to current tools"

Tech buyer rights raised in Cisco vulnerability

The seriousness of the Cisco vulnerability, Thrangycat, raises the question of tech buyers' rights when dealing with such a serious flaw in a vendor's hardware.



A network vulnerability as hard to fix as the recently disclosed Thrangrycat flaw in 150 varieties of Cisco switches and routers raises the question of a tech buyer's rights when repairing a

OS Kernel-Mode (Ring 0)

- Mitigations: PatchGuard, Code Signing Policy
- Prevention: AV HIPS, EDR

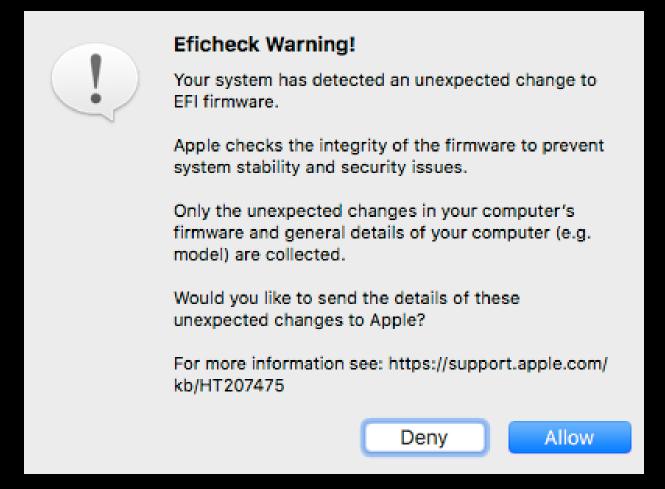
Boot code (MBR/VBR)

- Mitigations: Secure/Measured Boot, Boot Guard
- Prevention: AV HIPS, EDR

BIOS/UEFI Firmware SMM (Ring -2)

- Mitigations: limited (Intel BIOS/Boot Guard? STM?)
- Prevention: not exist

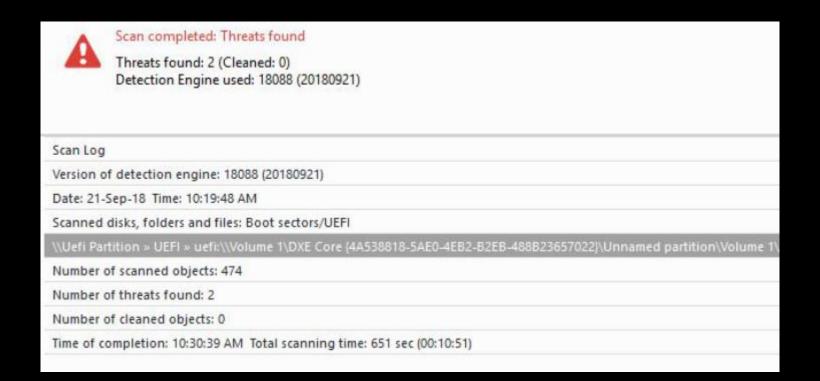






Integrity check works only with fixed dataset!

In large-scale integrity, pre-check/post-check has problems to detect supply chain attacks.





Dump and scan approach for UEFI images from OS has visibility limitations.

Most of AV endpoints just detect known UEFI threats and identify unusual DXE/PEI images by simple heuristics.

BIOS challenge for AV Endpoint solutions



- ☐ Limits of gathering information after OS boot
 - ✓ Everything can be a fake after OS boot
 - ✓ BIOS Rootkit/Implant can disable any AV endpoint solution
 - ✓ All the BIOS updates can be reinfected or just blocked
- □ No trusted path between AV and UEFI Firmware
 - ✓ Only cooperation between Firmware and AV can help to protect
 - √ Hashing UEFI drivers or SPI flash dump don't guarantee much
 - √ Who guarantee BIOS updates from hardware vendor not infected?
- □ Blind spot of supply chain attacks
 - ✓ Physical access not in scope of the most of security features

Who watch the watchers?



☐ Microarchitectural attacks — Hardware is new Software!

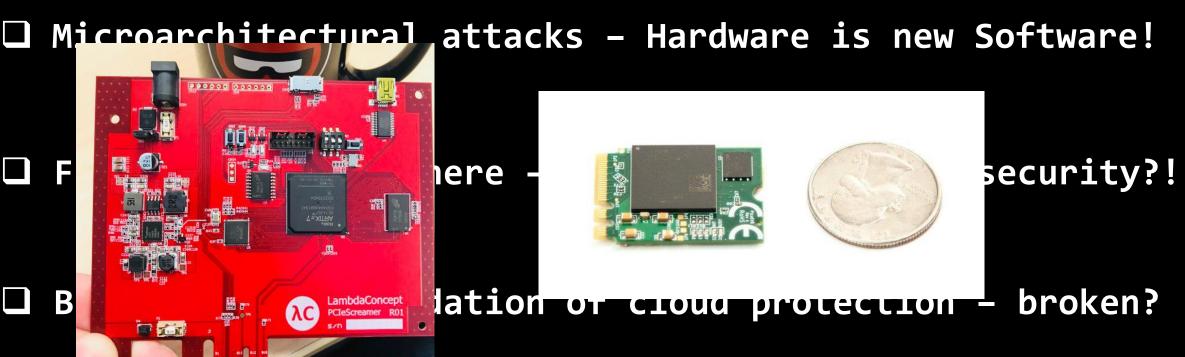
☐ Firmware is everywhere – Who cares about its security?!

■ BIOS became a foundation of cloud protection - broken?

☐ Supply Chain attacks - become mainstream?

Who watch the watchers?





☐ Supply Chain attacks — become mainstream?

Who wa





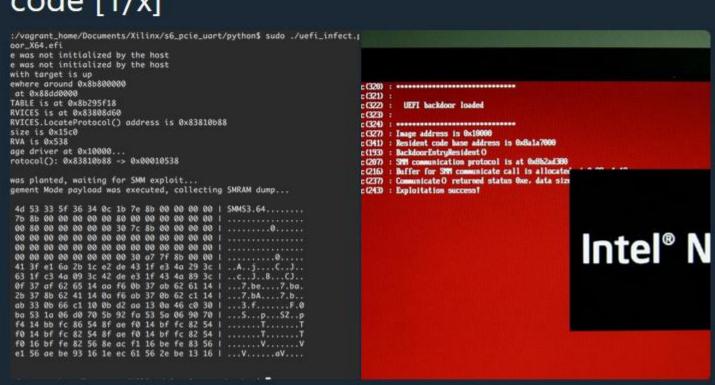


Rogue PCI-E/FireWire/Thunderbolt/etc. device can exploit platform firmware vulns to execute arbitrary System Management Mode code [1/x]

security?!

v Software!

- broken?



□ Microa

B

☐ Supply

7:41 PM - 21 Jun 2017

Win10 has active security measurement inside BIOS



- ☐ MS HW Security Testability Specification (HSTI)
 - HstiSiliconDxe Secure Boot, Signed Updates ...
 - HstiPlatformDxe DMA, Rollback Protection ...
 - HstiResultDxe store results in locked EFI variable
- ☐ MS Device Guard has direct FW feedback
 - DeviceGuardDxe runtime check for security features dependencies is enabled correctly in firmware

□ Device security

Security that comes built into your device.

Core isolation

Virtualization-based security is running to protect the core parts of your device.

Core isolation details

Security processor

Your security processor, called the trusted platform module (TPM), is providing additional encryption for your device.

Security processor details

Secure boot

Secure boot is on, preventing malicious software from loading when your device starts up.

Learn more

But Gigabyte/ASUS/MSI/ASROCK/Samsung don't care about security!

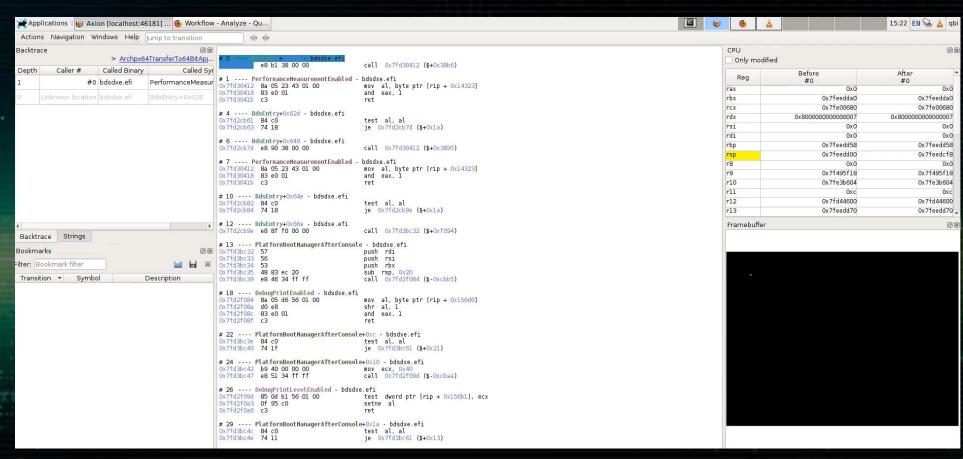
```
BiosInterfaceLockDown (BILD) control = 1
[*] BIOS Top Swap mode is disabled (TSS = 0)
[*] RTC TopSwap control (TS) = 0
[+] PASSED: BIOS Interface is locked (including Top Swap Mode)
[*] running module: chipsec.modules.common.bios wp
    Module path: c:\Chipsec\chipsec\modules\common\bios wp.pyc
   BC = 0x08 \ll BIOS Control (b:d.f 00:31.0 + 0xDC)
    [00] BIOSWE
                          = 0 << BIOS Write Enable
                  = 2 << SPI Read Configuration
= 0 << Top Swap Status
= 0 << SWM DIAG
    [01] BLE
                    = 0 << BIOS Lock Enable
    [02] SRC
    [04] TSS
    [05] SMM BWP
                          = 0 << SMM BIOS Write Protection
[*] BIOS Region: Base = 0x00A00000, Limit = 0x00FFFFFF
SPI Protected Ranges
PRx (offset) | Value
                                      Limit
PR0 (74)
                          00000000
                                      00000000
PR1 (78)
                                                       0
PR2 (7C)
               00000000
                          00000000
                                      00000000
PR3 (80)
                           00000000
                                      00000000
                                                       0
PR4 (84)
               00000000
                           00000000
                                      00000000
```

2019

Tools limitations for UEFI firmware RE

- □ Full system simulation (like Simics) don't provide hardware-vendor specific environment and EFI protocols which is create a lot of limitations.
- UEFI emulation (like QEMU) to execute specific DXE driver even with multiple stubs will have very limited code coverage. In some cases, it will be helpful but in most of them just a waste of time.
- □ Hardware-level debugging (over Intel DCI) isn't available on the most of enterprise platforms (DCI unlock sometimes possible over vulnerabilities). Executing DXE driver on not native hardware create the same limitations as simulation or emulation.

Tools limitations for UEFI firmware RE



https://blog.tetrane.com/2019/From-UEFI-to-Windows-Boot.html

You can also debug the UEFI firmware part of the boot process or even custom UEFI modules with source level debugging. Please check our XNU kernel debugging howto for more details on this feature.

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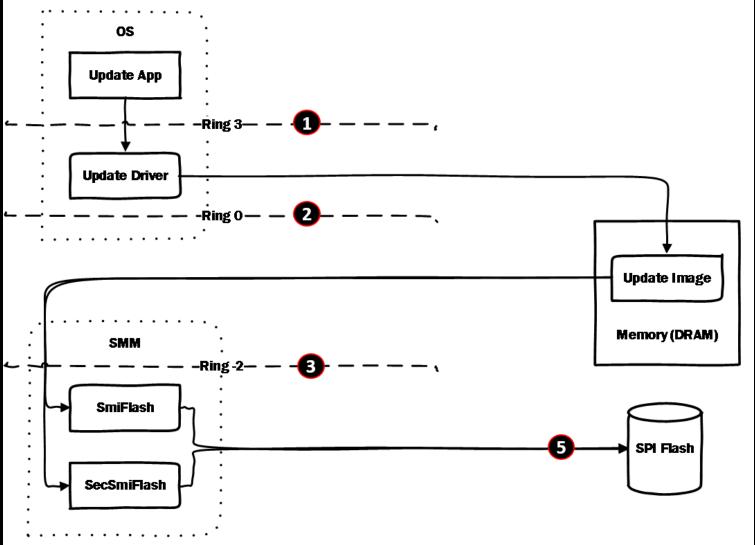
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UEFI update process chaos: too many tools, too many problems





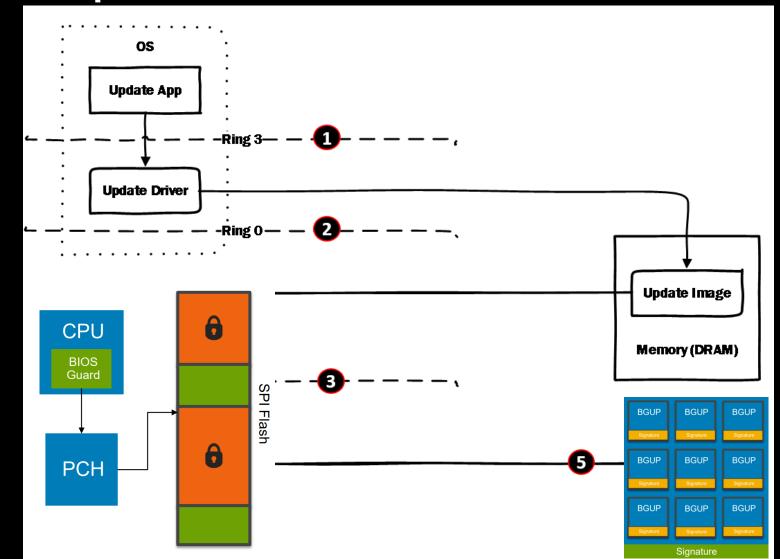
https://embedi.org/blog/nuclear-explotion/

https://medium.com/@matrosov/dangerous-update-tools-c246f7299459

https://www.blackhat.com/us-19/briefings/schedule/#breaking-through-another-side-bypassing-firmware-security-

boundaries-from-embedded-controller-15902

UEFI update process chaos: too many tools, too many problems



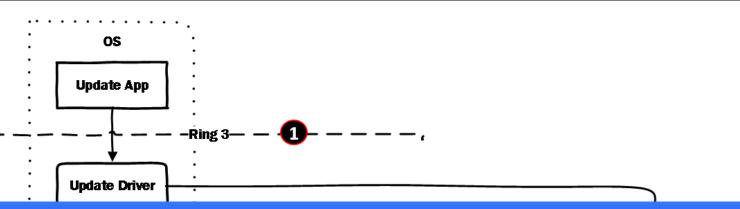


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UEFI update process chaos: too many tools, too many problems





Upgrading to Windows 10 Version 1709

Running action: Disable Bootguard

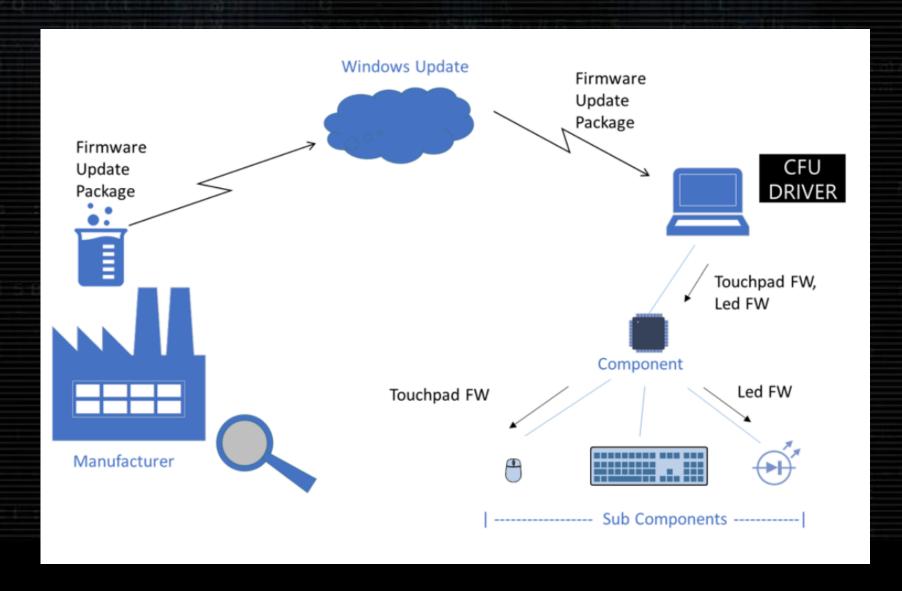


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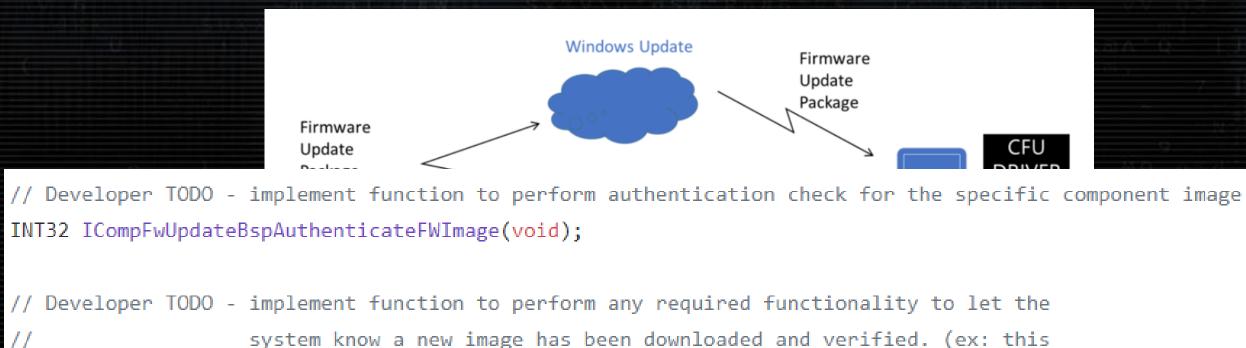
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MS Component Firmware Update



MS Component Firmware Update

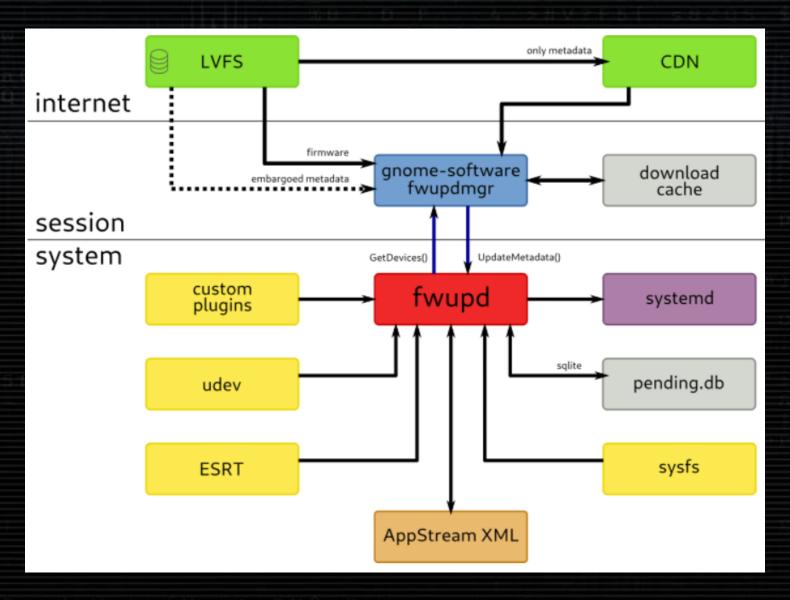


void ICompFwUpdateBspSignalUpdateComplete(void);

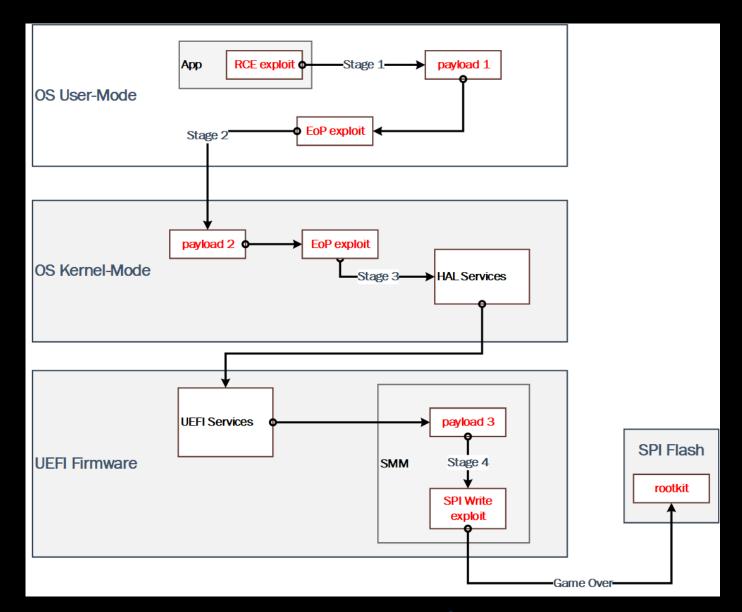
Sub Components -----

could be where the boot loader is modified to point to the new image)

Linux Vendor Firmware Service



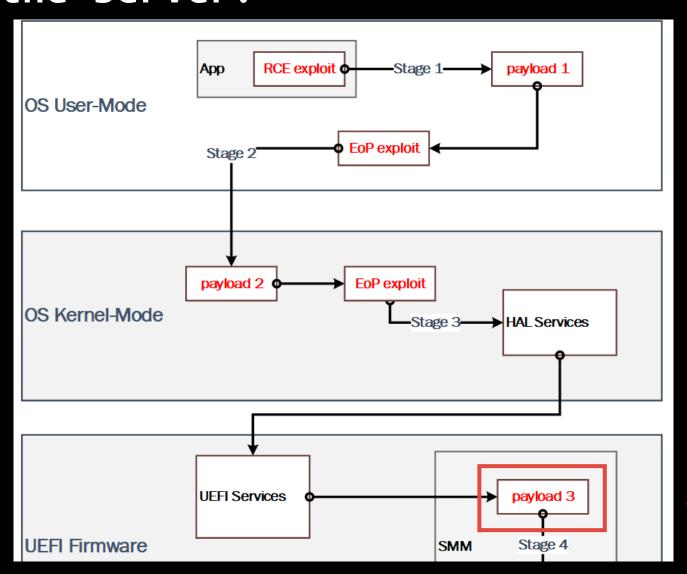
How many steps you need to gain BIOS persistence?



2019

Is it really important to have SPI persistent on the server?





SMM Runtime Persistence

Why the golden age of Firmware/Hardware Implants is happening right now?!

Why firmware is a new big thing for the attacker?

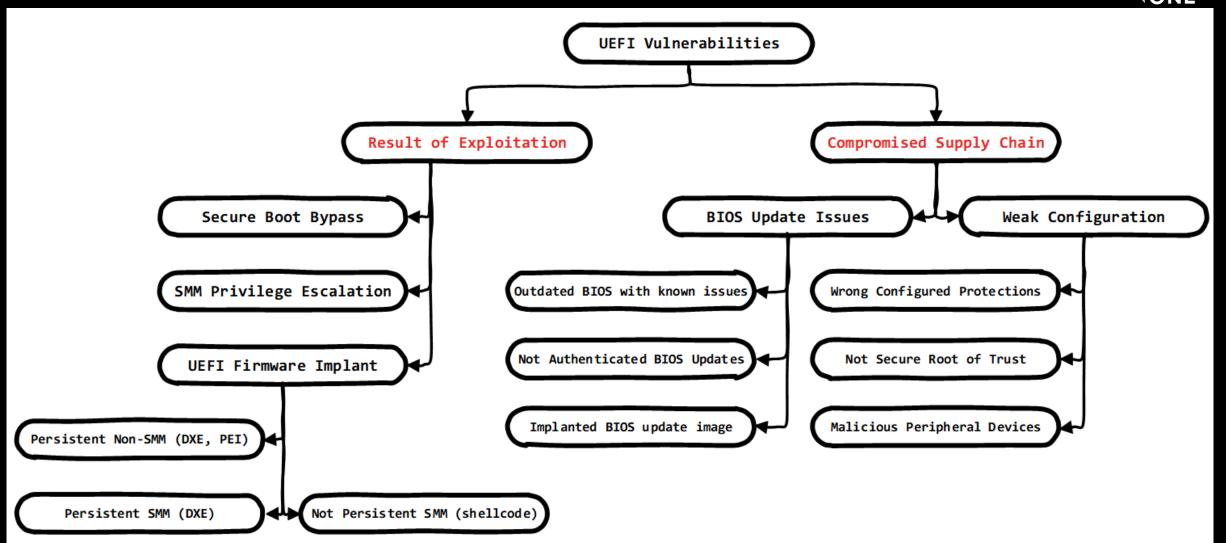


- ☐ Firmware was not considered as a critical security asset for a long time
 - Firmware is patchable and can be updated in many cases in the field
 - The cost for firmware update is much lower vs hardware recall
 - Bring-up of the new hardware is hard. Many vendors by mistake misconfigured security features in the production stage.

- ☐ Everything goes to the cloud include firmware and hardware
 - In most of the cases cloud providers don't control firmware and hardware
 - Supply Chain attacks become a huge problem (nobody control all HW components)
 - Isolated VM instances can be attacked too (persistence in the guest instances)

UEFI persistence classification





Average time of vulnerability disclosure in firmware 6-9 months!

(1-day exploit lifetime almost a year or longer!!)

Challenge of understanding attacker tactics or creating the right mitigations is related to mindset difference between attacker and architect.

Offensive Research != Security Research

Mitigations Design != Security Architecture

It's why is important to have an internal offensive research team to uncover the real reality, not the one which is created by architects of mitigations.

June 18

11:00 - 12:00

Inside the Machine: How Offensive Security is Defining the Way we Compute Data

•

First Track



English

TBA



Rodrigo Branco

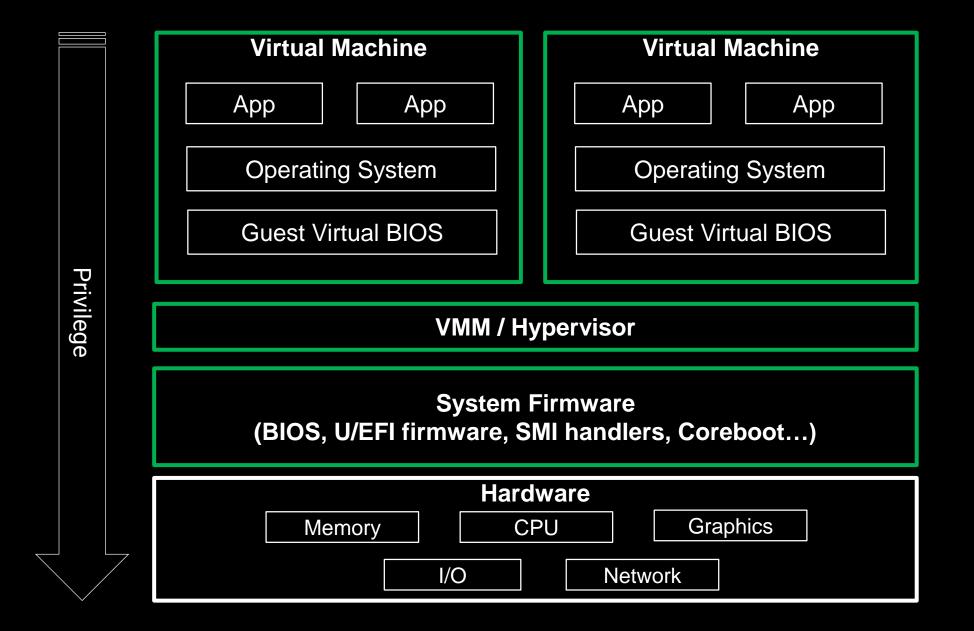
Chief Security Researcher, Strategic Offensive Research & Mitigations (STORM) Team

Let's go back to the cloud w



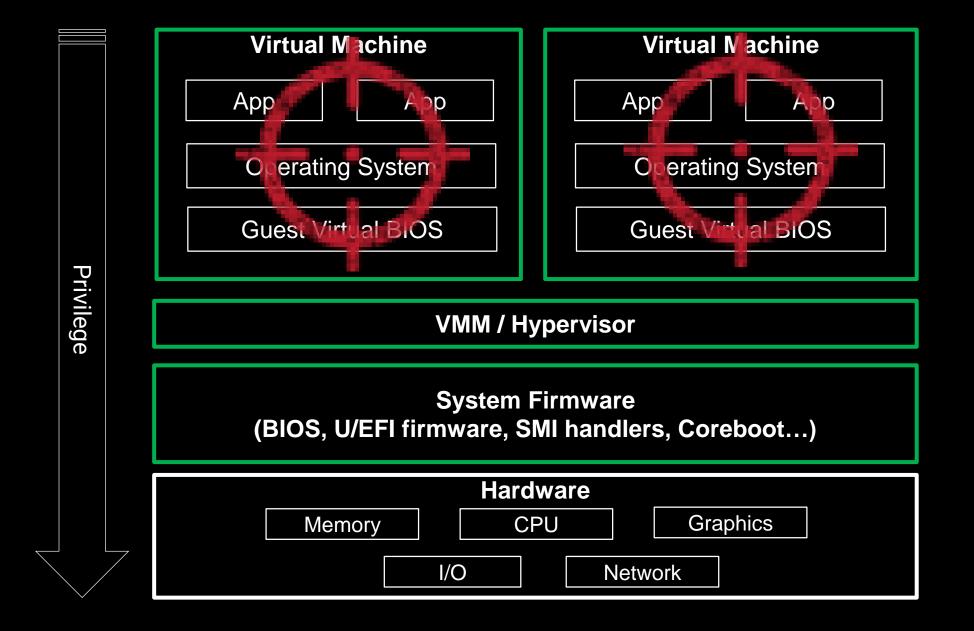
What can go wrong with the cloud?





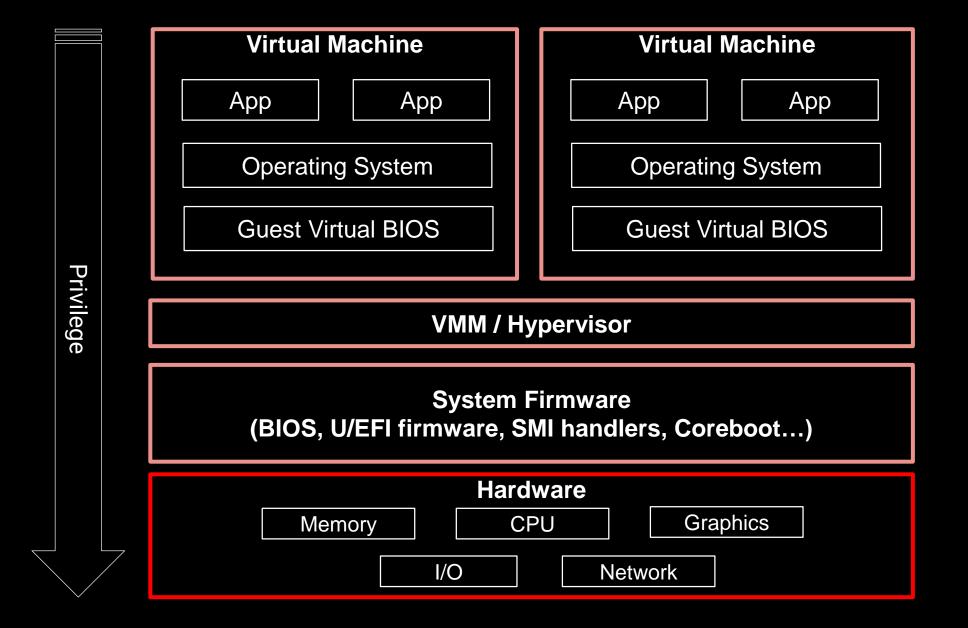
What can go wrong with the cloud?





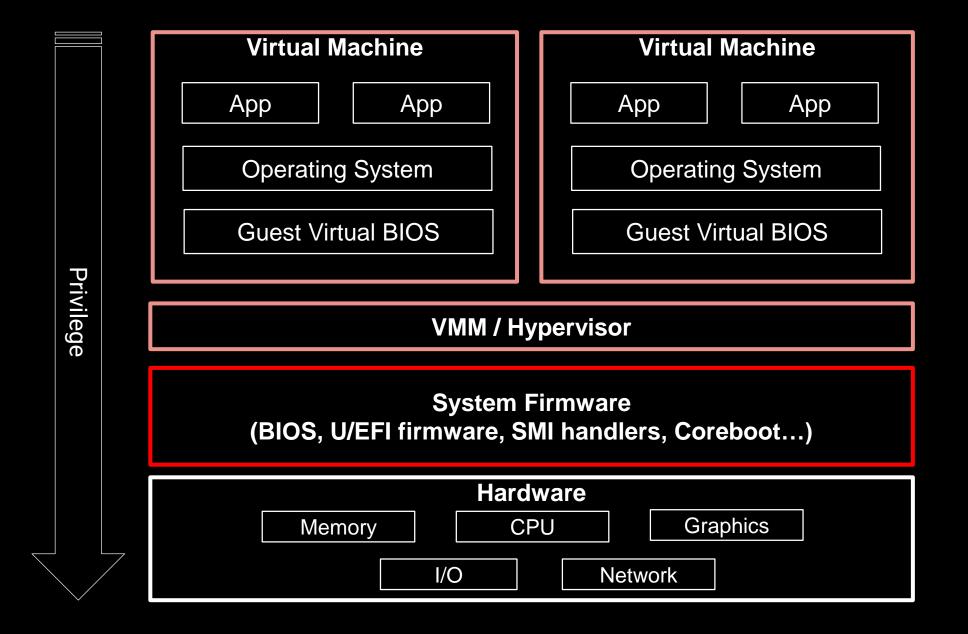
If BIOS is compromised it's game cloud over





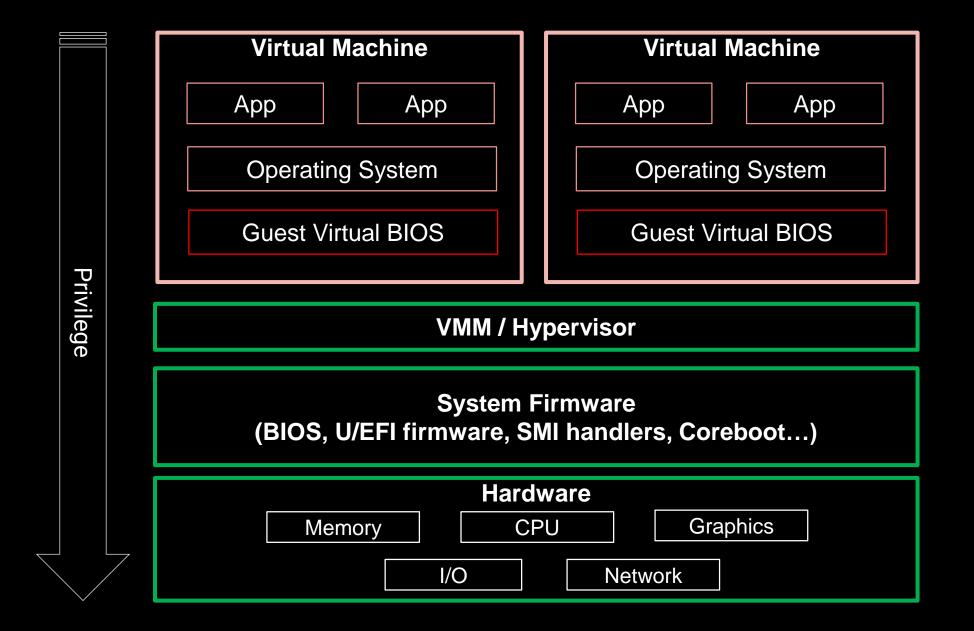
If BIOS is compromised it's game cloud over





What if attacker gain persistence only in guest BIOS?





SeaBIOS/Coreboot in the cloud (in some cases)



```
[x][ Module: SPI Flash Descriptor Security Override Pin-Strap
←[39m[*] HSFS = 0x0000 << Hardware Sequencing Flash Status Register (SPIBAR + 0x4)</p>
   [00] FDONE
                    = 0 << Flash Cycle Done
   [01] FCERR
                    = 0 << Flash Cycle Error
   [02] AEL
                    = 0 << Access Error Log
   [03] BERASE
                    = 0 << Block/Sector Erase Size
   [05] SCIP
                    = 0 << SPI cycle in progress
   [13] FDOPSS
                    = 0 << Flash Descriptor Override Pin-Strap Status
   [14] FDV
                    = 0 << Flash Descriptor Valid
   [15] FLOCKDN
                    = 0 << Flash Configuration Lock-Down ←[0m
←[31m[-] FAILED: SPI Flash Descriptor Security Override is enabled←[0m]
```

SeaBIOS/Coreboot in the cloud (in some cases)



```
x][ Module: BIOS Region Write Protection
-[39m[*] BC = 0x00 << BIOS Control (b:d.f 00:31.0 + 0xDC)
   [00] BIOSWE = 0 << BIOS Write Enable
  [01] BLE = 0 << BIOS Lock Enable
  [02] SRC = 0 << SPI Read Configuration
  [04] TSS = 0 << Top Swap Status
  [05] SMM_BWP = 0 << SMM BIOS Write Protection ←[0m
-[31m[-] BIOS region write protection is disabled!←[0m
-[39m
*| BIOS Region: Base = 0x000000000, Limit = 0x00000FFF+[0m
-[39mSPI Protected Ranges←[0m
[39mPRx (offset) | Value | Base
                                  Limit
| 00000000 | 00000000 | 00000000 | 0
-[39mPR0 (74)
                                                  0 ←[0m
               00000000
                          00000000
                                    00000000 0
-[39mPR1 (78)
                                                  0 ←[0m
               00000000
                          00000000
                                                 0 ←[0m
-[39mPR2 (7C)
                          00000000
                                    00000000 0 0 ←[0m
-[39mPR3 (80)
               00000000
                          00000000
                                    00000000 0
-[39mPR4 (84)
               00000000
                                                 | 0 ←[0m
-[39m←[0m
-[31m[!] None of the SPI protected ranges write-protect BIOS region←[0m
-[39m←[0m
-[31m[!] BIOS should enable all available SMM based write protection mechanisms or configure SPI protected ranges
-[31m[-] FAILED: BIOS is NOT protected completely+[0m
```

SeaBIOS/Coreboot in the cloud (in some cases)



```
[*] running module: chipsec.modules.common.spi_access+[0m
[x][ Module: SPI Flash Region Access Control
←[39mSPI Flash Region Access Permissions←[0m]
←[39m[*] FRAP = 0x000000000 << SPI Flash Regions Access Permissions Register (SPIBAR + 0x50)</p>
   [00] BRRA
                    = 0 << BIOS Region Read Access
   [08] BRWA
                  = 0 << BIOS Region Write Access
            = 0 << BIOS Master Read Access Grant
   [16] BMRAG
                = 0 << BIOS Master Write Access Grant ←[0m
   [24] BMWAG
←[39m←[0m
←[39mBIOS Region Write Access Grant (00):←[0m
←[39m FREGO_FLASHD: 0←[0m
←[39m FREG1 BIOS : 0←[0m
←[39m FREG2_ME
               : 0←[0m
←[39m FREG3 GBE : 0←[0m
←[39m FREG4_PD
               : 0←[0m
←[39m FREG5
               : 0←[0m
←[39m FREG6
               : 0←[0m
←[39mBIOS Region Read Access Grant (00):←[0m
←[39m FREG0 FLASHD: 0←[0m
←[39m FREG1_BIOS : 0←[0m
←[39m FREG2_ME
               : 0←[0m
←[39m FREG3_GBE : 0←[0m
←[39m FREG4_PD
               : 0←[0m
←[39m FREG5
               : 0←[0m
               : 0←[0m
←[39m FREG6
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←[39m FREG0 FLASHD: 0←[0m
←[39m FREG1 BIOS : 0←[0m
←[39m FREG2_ME
               : 0←[0m
←[39m FREG3 GBE : 0←[0m
←[39m FREG4 PD
               : 0←[0m
←[39m FREG5
               : 0←[0m
←[39m FREG6
               : 0←[0m
←[39mBIOS Region Read Access (00):←[0m
```

Big cloud providers like Amazon/Google/MS are not that bad

FF ONE 2019

Shielded VM can help you protect your system from attack vectors like:

- Malicious guest OS firmware, including malicious UEFI extensions
- Boot and kernel vulnerabilities in guest OS
- · Malicious insiders within your organization

To guard against these kinds of advanced persistent attacks, Shielded VM uses:

- Unified Extensible Firmware Interface (UEFI): Ensures that firmware is signed and verified
- Secure and Measured Boot: Help ensure that a VM boots an expected, healthy kernel
- Virtual Trusted Platform Module (vTPM): Establishes a root-of-trust, underpins
 Measured Boot, and prevents exfiltration of vTPM-sealed secrets
- Integrity Monitoring: Provides tamper-evident logging, integrated with Stackdriver, to help you quickly identify and remediate changes to a known integrity state

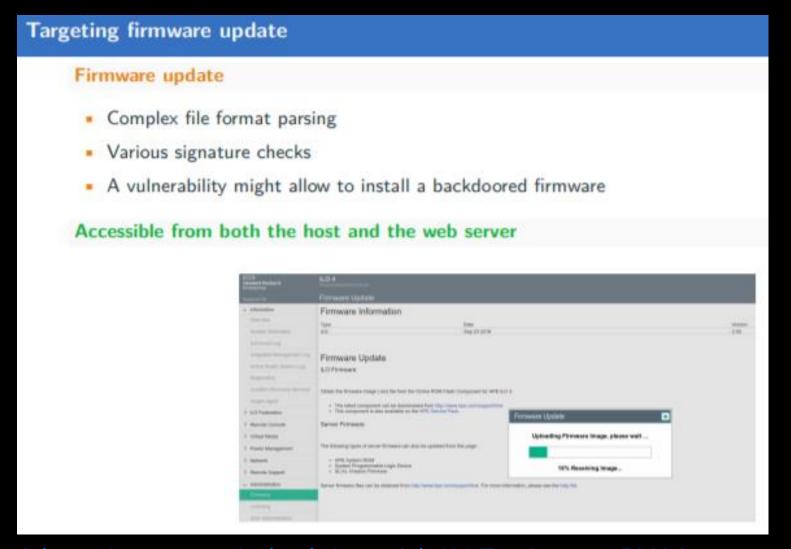
https://cloud.google.com/blog/products/identity-security/shielded-vm-your-ticket-to-guarding-against-rootkits-and-exfiltration

https://docs.microsoft.com/en-us/windows-server/security/guarded-fabric-shielded-vm/guarded-fabric-and-shielded-vms

VM guest BIOS persistence out of scope for existing security solutions!

BMC is a key from Data Center internal network

BMC in many cases expose different path to update BIOS



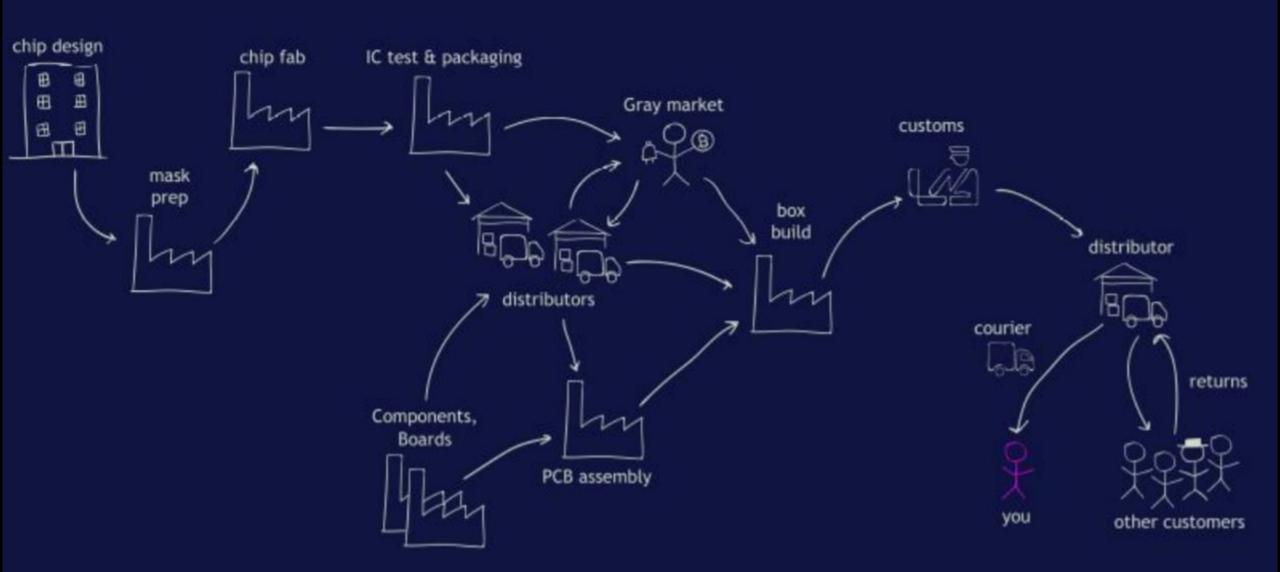
https://2018.zeronights.ru/wp-content/uploads/materials/01-Turning-your-BMC-into-a-revolving-door.pdf
https://www.sstic.org/media/SSTIC2019/SSTIC-actes/iDRACKAR/SSTIC2019-Slides-iDRACKAR-iooss.pdf
https://www.immunityinc.com/downloads/The-Unbearable-Lightness-of-BMC-wp.pdf

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2019

Supply Chain Attacks on HW/FW: growing problems

It's A Huge Attack Surface...



Halvar Flake's wisdom



Scaling, firmware engines, and inspectability

Nobody has a good way to assure that a given device is reset into a "known-good" state, **especially** if the hardware was under physical attacker control.



We can't check the transistors.

We can't check the firmware origin.

Establishing "who is in control" is near-impossible against strong adversaries.

Why for hardware vendors security is not on the first place?

WTF Hardware Root of Trust?



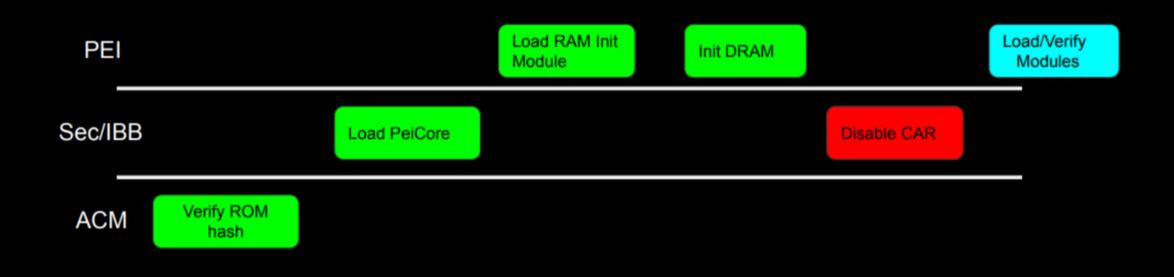
- ☐ Root of Trust baked in pure Hardware?
 - Cant be extracted/modified from software (developed in RTL)?
 - not flexible with OEM's
 - hard to support in the field (updates and etc.)
 - hard to implement secure way to cooperate with firmware on the same chip
- ☐ In most of the cases Hardware Root of Trust it's a mix between firmware and locked in the FUSE value or by specific bit.

☐ Secure state transition between hardware and firmware is hard. It's always something missing.

TOCTOU on SPI Flash open the doors



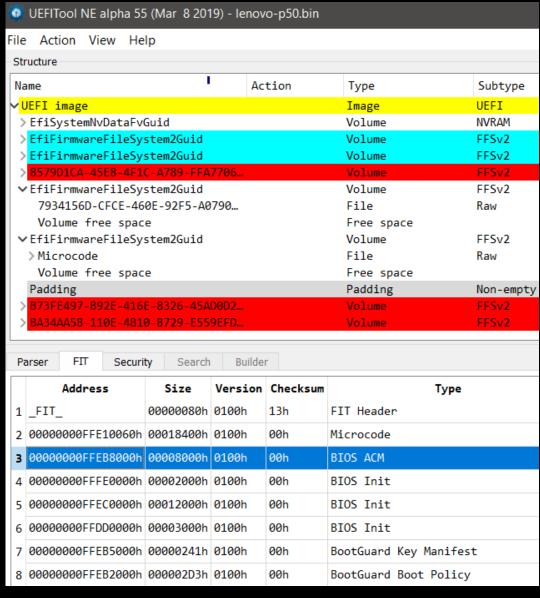
Early Boot: ACM, Sec and PEI Phases



Code in CAR RAM XIP

Intel ACM's and Microcode downgrade





Intel ACM's and Microcode downgrade





Alex Matrosov @matrosov · Jun 14

Intel microcode downgrade is a huge supply-chain problem. Even after the patch problem still exists in many platforms. Btw ACM's downgrade is also possible (a bit more tricky but downgrade both Microcode + ACM is a key to success).

Great job @flothrone and the team!



Alexander Ermolov @flothrone · Jun 13

Our team (@ttbr0, @undermarble and me) walks through UEFI BIOS again, as a result:

- 6 Escalation of Privileges to SMM
- microcode downgrade vulnerability, allowing to bypass hardware root-oftrusts.

Details coming soon! intel.com/content/www/us...

Halvar Flake's wisdom



Scaling, firmware engines, and inspectability

Scaling has yielded the performance gains of the last decades, but scaling made physical inspection impossible.

Universal computation has replaced many formerly-simpler components in your computer with full CPUs + firmware - usually without mechanism for inspection.

Current approach for firmware security is based on "ensuring nobody can get in" (code signing), but transient faults can be locally induced to bypass, and signing keys get stolen with regularity.



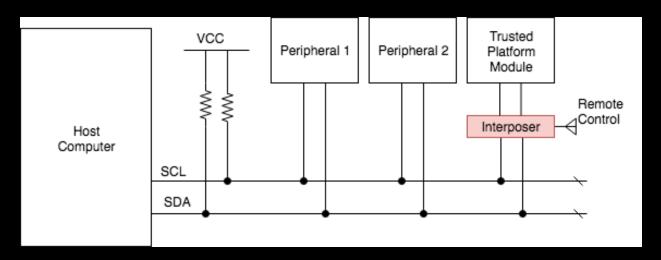
3rd party components is part of Supply Chain hell

Supply Chain attack vectors extend attack surface which always been out of scope for HW/FW vendors.

TPM – Root of Trust Problems

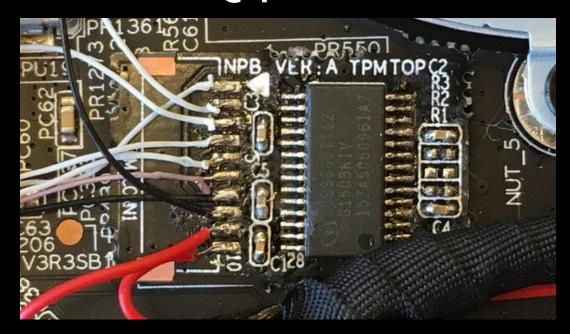


@uffeux



https://github.com/nccgroup/TPMGenie

@qrs



Major vendors trying to fix the Root



Google Titan



Apple T2



Microsoft Cerberus

Amzon Greengrass

https://cloud.google.com/blog/products/gcp/titan-in-depth-security-in-plaintext

https://www.apple.com/mac/docs/Apple_T2_Security_Chip_Overview.pdf

https://github.com/opencomputeproject/Project_Olympus/tree/master/Project_Cerberus https://aws.amazon.com/greengrass/

Any of hardware vendors doesn't have a full supply chain control

(a lot of 3rd party FW come as binary blobs)

Operation ShadowHammer (ASUS Live Update compromise) demonstrate security gaps in current whole update delivery process

REsearchers Arm Race never stops!

Thank you!

