USB-to-High-Speed Serial Port Chip CH343

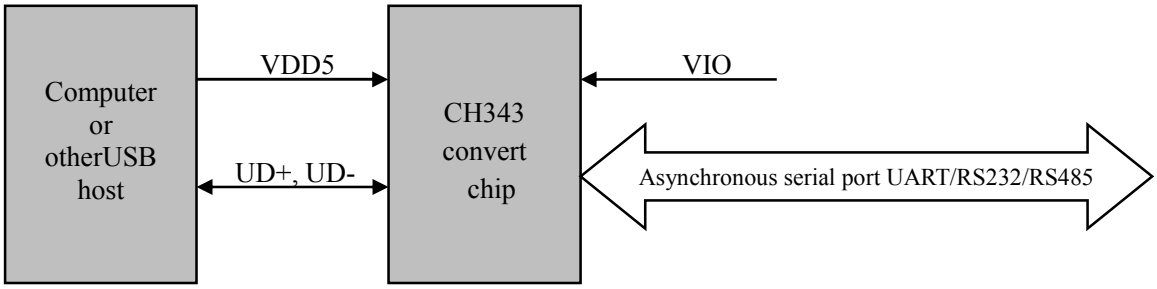
DataSheet

Version: 1B

http://wch.cn

1. Introduction

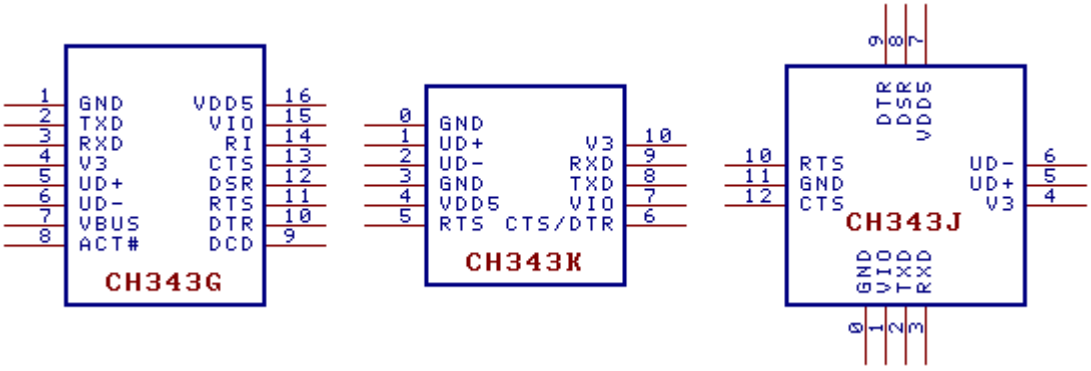
CH343 is a USB bus converter chip realizing USB to high-speed asynchronous serial port. It supports automatic recognition and dynamic self-adaptation of communication baud rate of 115200bps and below, and provides commonly used MODEM interface signals to expand asynchronous serial ports for the computer, or upgrade ordinary serial device or MCU directly to USB bus.



2. Features

- Full-speed USB device interface, USB 2.0 compatible.
- Intergrated firmware, emulate standard UART interface, used to upgrade the original serial peripherals, or expand additional serial UART via USB.
- Original serial applications are totally compatible without any modification.
- Supports built-in CDC driver in operating system or multi-functional high-speed VCP manufacture driver.
- Hardware ful-duplex serial UART interface, intergrated separate transmit-receive buffer, supports communication baud rate varies from 50bps to 4Mbps.
- Optional automatic recognition and dynamic self-adaption for common communication baud rate of 115200bps and below.
- Supports 5, 6, 7 or 8 data bits, and supports odd parity, even parity, blank, mark and no parity.
- Supports common MODEM control signals RTS, DTR, DCD, RI, DSR and CTS.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provide sending status TNOW supports RS485 switch.
- Supports RS232 interface through external level converter device.
- Supports 5V and 3.3Vpower supply voltages.
- The serial port interface I/O powered independently, supports 5V, 3.3V, 2.5V, 1.8V power supply voltages.
- Intergrated power-on reset, intergrated clock, no external crystal required.
- RoHS compliant SOP-16, ESSOP-10 and QFN-12 lead-free packages.

3. Packages



Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH343G
ESSOP-10	3.9mm	150mil	1.00mm	39mil	Narrow pitch 10-pin patch with bottom plate	CH343K
QFN12_2X2	2*2mm		0.5mm	19.7mil	Ultra-small square leadless 12-pin	CH343J

Note:

The backplane of the CH343K and CH343J is 0# pin GND, which is an optional connection, but suggested connection; other GND are necessary connections.
The package form of CH343J only supports batch quantity and needs to be reserved.

4. Pin Out

SOP16 Pin No.	ESSOP10 Pin No.	QFN12 Pin No.	Pin Name	Pin Type	Pin Description
16	4	7	VDD5	POWER	The positive power input of the power regulator requires an external decoupling capacitor
15	7	1	VIO	POWER	I/O port power input, requires an external decoupling capacitor
1	3,0	11,0	GND	POWER	The common ground needs to be connected to the ground wire of the USB bus
4	10	4	V3	POWER	Internal power regulator output and core and USB power input, When VDD5 voltage is less than 3.6V, connect VDD5 to input the external power supply, An external decoupling capacitor is required to be connected when the VDD5 voltage is greater than 3.6V
NONE	NONE	NONE	RST	IN	Input of external reset, active low, intergrated pull-up resistor
5	1	5	UD+	USB signal	Connect to USB D+ Signal directly
6	2	6	UD-	USB signal	Connect to USB D- Signal directly
7	NONE	NONE	VBUS	IN	VBUS status detection input of USB bus, intergrated pull-down resistor
2	8	2	TXD	OUT	Transmit asynchronous data output of serial port, idle state is high level

3	9	3	RXD	IN	Receive asynchronous data input of serial port , integrated pull-up resistor
13		12	CTS	IN	MODEM input signal, clear sending, active low
	6		CTS or DTR	Default input It can be automatically transferred to output	The default is MODEM input signal; clear sending, active low, when DTR is set as effective at the computer software, it will automatically switch to MODEM output signal, data terminal ready, active low
12	NONE	8	DSR	IN	MODEM input signal, data set ready, active low
14	NONE	NONE	RI	IN	MODEM input signal, ring indicator, active low
9	NONE	NONE	DCD	IN	MODEM input signal, data carrier detect, active low
10	NONE	9	DTR TNOW	OUT	MODEM output signal, data terminal ready, active low, if an external pull-down resistor is detected during power-on, it will switch to serial port sends ongoing status indication, active at high level
11	5	10	RTS	OUT	MODEM output signal, request to send, active low
8	NONE	NONE	ACT#	OUT	USB configuration completion status output, active low, inactive when suspended. If an external pull-down resistor is detected during power-on, it will switch to the communication baud rate self-adaption mode, which can also be enable by software

5. Function Description

5.1. Power and Power Consumption

CH343 has 3 power supplies and a intergrated voltage regulator which generates 3.3V. VDD5 is the input power regulator. V3 is the output of the voltage regulator and USB transceiver and core power supply input, and VIO is the I/O pins power supply.

CH343 supports 5V or 3.3V power supply voltages, and the V3 pin should be externally connect to a power decoupling capacitor with a capacity of about 0.1uf. When using 5V power supply (greater than 3.8V), VDD5 inputs external 5V power supply (for example, the USB bus power supply), the internal voltage regulator generates 3.3V on V3 which used by USB transceivers. When using 5V power supply(greater than 3.8V), VDD5 inputs external 5V power supply (for example, the USB bus power supply), the internal voltage regulator generate 3.3V on V3 which used by USB transceivers. When using 3.3V power supply. V3 still requires an external decoupling capacitor.

VIO pin of CH343 provides I/O power supply for serial port I/O and RST pins. It supports 1.8V~5V power supply voltages. VIO should use the same power supply as MCU and other peripherals. UD+, UD- and VBUS pins use V3 power supply, not VIO power supply.

CH343 automatically supports USB device suspension to save power consumption. In the USB suspend state, if the I/O output pin has no external load and the I/O input pin is float(internally pulled up) or in a high level state, the VIO power supply will not consume current. In addition, when V3 and VDD5 lose power and are at a voltage of 0V, the current consumption of VIO is the same as above, and VIO will not flow current backwards to VDD5 or V3.

VBUS should be connected to USB power supply, and when the loss of USB power is detected, CH343 will turn off the USB and sleep (suspend). The CH343K/J chip has no VBUS pin, so it is assumed that there is always a USB power supply.The intergrated pull-down resistor of the VBUS pin can be controlled by the

computer software by setting the OUT1 signal in the serial port MCR register (SERIAL_IOC_MCR_OUT1). When OUT1 is invalid, the pull-down resistor will be turned on (default status). When OUT1 is valid, the pull-down resistor will be turned off.

When the VBUS pin is connected with a resistor in series and then used to control the VIO power supply through PMOS, CH343 will provide a VIO low voltage protection mechanism. During the period when the VBUS pull-down resistor is turned off, if the VIO voltage is detected to be lower than about 1.4V, the CH343 will automatically absorb about 300uA discharge current at the VBUS pin until the VIO voltage rises to end the discharge current and automatically turn on the pull-down resistor.

The following are several power connection schemes for reference.

<table>
<tr><td rowspan="2">Power supply scheme</td><td>UART signals voltage
MCU operating voltage</td><td>VDD5 pin</td><td>V3 pin</td><td>VIO pin</td><td>MCU or peripheral power supply</td></tr>
<tr><td>No lower than V3 pin’s voltage</td><td>Rated voltage: about 3.3 V</td><td colspan="2">Both use the same power supply, 1.8V-5V</td></tr>
<tr><td rowspan="4">All USB Power Supply</td><td>5V</td><td>USB power supply 5V</td><td>Only connected to the capacitor</td><td colspan="2">USB power supply 5V</td></tr>
<tr><td>3.3V</td><td>USB power supply 5V</td><td>External capacitor</td><td colspan="2">Powered by V3 for 3.3V, up to 10 mA</td></tr>
<tr><td>3.3V</td><td colspan="4">USB 5V power stepped down to 3.3V via external LDO power regulator,V3 connects to external capacitor.</td></tr>
<tr><td>1.8V～4V</td><td>USB power supply 5V</td><td>Only connected to the capacitor</td><td colspan="2">The USB power supply is reduced in voltage through an external LDO regulator</td></tr>
<tr><td>USB+ self-powered dual power supply</td><td>1.8V～5V</td><td>USB power supply 5V</td><td>Only connected to the capacitor</td><td colspan="2">Self-powered 1.8V～5V
（1.8V,2.5V,3.3V,5V）</td></tr>
<tr><td rowspan="2">All self-powered</td><td>4V～5V</td><td>Self-powered 4V- 5V</td><td>Only connected to the capacitor</td><td colspan="2">Self-powered 4V- 5V</td></tr>
<tr><td>1.8V～5V</td><td colspan="2">Self-powered, rated voltage 3.3V, external capacitor</td><td colspan="2">Self-powered 1.8V～5V</td></tr>
</table>

5.2. Serial Port

The pins of CH343 in asynchronous serial port mode include: data transmission pins, MODEM contact signal pins and auxiliary pins.

Data transmission pins include: TXD pin and RXD pin. When the serial port input is idle, RXD will be at high level. When the serial port output is idle, TXD will be at high level.

The MODEM control signal pins include: CTS pin, DSR pin, RI pin, DCD pin, DTR pin and RTS pin. All these MODEM control signals are controlled by the computer application program and their purposes can be defined.

The DTR pin of the CH343 is used as a configuration input pin during power-on or reset. It can be connected to a 4.7KΩ (3～8KΩ) pull-down resistor to generate a default low level to make the serial port enter half-duplex mode and switch the original DTR pin to TNOW output pin, for indicating that the serial port is sending data. In half-duplex mode, TNOW can be used to directly control the receiving and transmitting switch of RS485 transceiver.

The CTS/DTR pin of the CH343K automatically switches from CTS to DTR (the default idle status is high level) when the computer software is set to DTR valid, and remains as DTR output until the chip is

re-powered on or reset. The DTR does not support the half-duplex mode input.

Auxiliary pins include: ACT# pins. The ACT# pin is the status output of the USB device configuration completion, which can be used to notify the MCU or drive the LED connected to the VIO after the current limiting resistor is connected in series. The ACT# pin is used as a configuration input pin during power-on or reset. It can be connected to a 4.7KΩ (3～8KΩ) pull-down resistor to generate a default low level, so that the serial port will enter the communication baud rate self-adaption mode and can automatically and dynamically identify common communication baud rate of 115200bps and below. It mainly supports common communication baud rates such as 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 115200 and special high-speed communication baud rates such as 10K, 20K, 30K, 50K, 100K, 150K, 250K, 300K and 500K.

The asynchronous serial port of CH343 supports CTS and RTS hardware automatic flow control, which can be enabled by software. If enabled, the serial port will continuously send the next data only when it detects that the CTS pin input is valid (active at low level). Otherwise, the serial port transmission will be suspended; when the receiving buffer area is null, the serial port will automatically validate RTS pin (active at low level), and the serial port will automatically invalidate the RTS pin until the data in the receiving buffer area is full, and the RTS pin will be revalidated again when the buffer area is null. You can connect your own CTS pin to the other party's RTS pin through the hardware automatic rate control, and can connect your own RTS pin to the other party's CTS pin.

CH343 has intergrated separate transmit-receive buffer and supports simplex, half-duplex or full duplex asynchronous serial communication. Serial data includes 1 low-level start bit, 5, 6, 7 or 8 data bits, 1 or 2 high-level stop bits, and supports odd/even/mark/blank checking. CH343 supports common communication baud rates: 50, 75, 100, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 256000, 307200, 460800, 921600, 1M, 1.5M, 2M, 3M, 4M and 6M, etc.

In applications with high communication baud rate, it is recommended to enable hardware automatic flow control. The full-speed USB is only 12Mbps. Considering the factors such as protocol overhead, the serial port shouldnot be in a continuous or full-duplex high-speed communication status of 3Mbps and above in the practical applications.

The allowable baud rate error of the CH343 serial port receiving signalisnot more than 2%, and the baud rate error of the serial port transmitting signal shall be less than 1.5%.

In the Windows operating system of the computer, CH343 supports the CDC drive program that comes with the system. The high-speed VCP vendor drive program can be also installed to simulate the standard serial ports, so most of serial port applications are fully compatible and usually no any modification is required.

CH343 can be used to upgrade the original serial peripheral device, or to add additional serial ports to the computer through the USB bus. RS232, RS485, RS422 and other interfaces can be further provided through the external level conversion device.

5.3. Clock, Reset and Others

CH343 has the intergrated USB pull-up resistors, and the UD+ and UD- pins should be directly connected to the USB bus.

CH343 has a intergrated power-on reset circuit and a low-voltage reset circuit. It monitors the voltages of the V3 pin and the VIO pin at the same time. When the V3 voltage is lower than VRV3 or the VIO voltage is lower than VRVIO, the chip will be automatically reset by hardware.

CH343 has a intergrated clock generator, without external crystal and oscillation capacitor.

In large batch applications, the manufacturer identification code VID and product identification code PID of CH343 and product information can be customized.

6. Parameters

6.1. Absolute Maximum Ratings

(critical state or exceeding maximum can cause chip to not work or even be damaged)

Name	Parameter Description	Min	Max	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage temperature	-55	105	℃
VDD5	USB power supply voltage (VDD5 pin power supply, GND pin grounded)	-0.5	6.0	V
VIO	Serial port I/O power supply voltage (VIO pin power supply, GND pin grounded)	-0.5	6.0	V
VVBUS	Voltage on the VBUS pin	-0.5	6.5	V
VUSB	Voltage on the USB signals pin	-0.5	V3+0.5	V
VUART	Voltage on the serial port and other pins	-0.5	VIO+0.5	V

6.2. Electrical Parameters

(Test Conditions: TA=25℃, VDD5=5V or VDD5=V3=3.3V, VIO=1.8V～5V, Excluding USB Pins)

Name	Parameter Description			Min	Typ	Max	Unit
VDD5	USB Power supply voltage	V3 pin is not connected to VDD5 and V3 is connected to the capacitor		4.0	5	5.5	V
		V3 pin is connected to VDD5, VDD5=V3		3.0	3.3	3.6	
VIO	VIO power supply voltage on the serial port and other I/O			1.7	5	5.5	V
IVDD	VDD5 or V3 supply current during operation				3	15	mA
IVIO	VIO supply current during operation				0	10	mA
ISLP	Operating Supply Current(USB Suspend)	VDD5 power supply =5V			0.09	0.16	mA
		VDD5=V3 power supply=3.3V			0.005	0.015	mA
		VIO power supply, no I/O load/ pull-up			0.002	0.05	mA
ILDO	External load capacity of internal power regulator					10	mA
VIL	Low level input voltage		VIO=5V	0		1.5	V
			VIO=3.3V	0		0.9	V
			VIO=1.8V	0		0.5	V
VIH	High level input voltage		VIO=5V	2.5		VIO	V
			VIO=3.3V	1.9		VIO	V
			VIO=1.8V	1.2		VIO	V
VIHVBS	High level voltage of VBUS pin		VIO= 1.8V～5V	1.7		5.8	V
VOL	Low level Output voltage	VIO=5V, 15mA draw current			0.4	0.5	V
		VIO=3.3V, 8mA draw current			0.3	0.4	V
		VIO=1.8V, 3mA draw current			0.3	0.4	V

VOH	High level Output voltage Non-reset status	VIO=5V, 10mA output current	VIO-0.5	VIO-0.4		V
		VIO=3.3V, 5mA output current	VIO-0.4	VIO-0.3		V
		VIO=1.8V, 2mA output current	VIO-0.4	VIO-0.3		V
IPUP	Serial port and RST pin pull-up current (Pulled up to VIO voltage)	VIO=5V	35	150	220	uA
		VIO=3.3V	15	60	90	uA
		VIO=1.8V	3	14	21	uA
IPDN	Pull-down current of VBUS pin	VBUS>1.6V	6	10	16	uA
		VBUS<1.3V	50	140	200	uA
VRV3	Power-on reset / low-voltage reset voltage threshold of V3 power		2.5	2.7	2.9	V
VRVIO	Low-voltage reset voltage thredshold of VIO power		0.8	1.0	1.15	V
VESD	HBM ESD withstand voltage on USB or I/O pins		5	6		KV

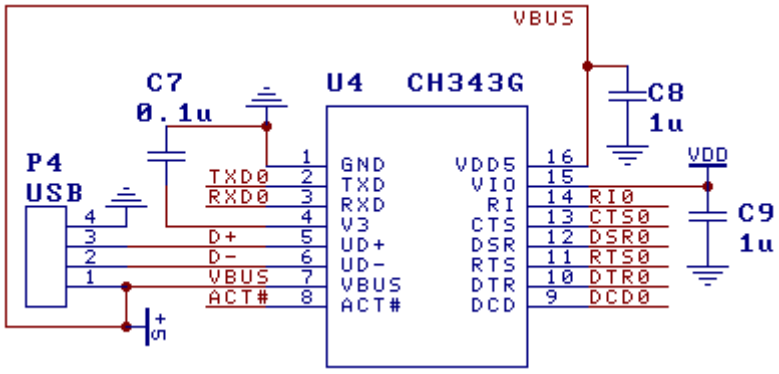
6.3. Timing Parameters

(Test Conditions: TA=25℃, VDD5=5V or VDD5=V3=3.3V, VIO=1.8V～5V)

Name	Parameter Description		Min	Typ	Max	Unit
FD	Error of internal clock (Comparative influenced baud rate)	TA=-15℃～60℃	-1.0	±0.5	+1.0	%
		TA=-40℃～85℃	-1.5	±0.8	+1.5	%
TRSTD	Reset delay after power-on or external reset input		9	15	25	mS
TSUSP	USB automatic suspend time		3	5	9	mS
TWAKE	Wake-up completion time after chip sleep		1.2	1.5	5	uS

7. Applications

7.1. USB to 9-wire TTL Serial Port (Figure below)



The figure above shows the USB to TTL serial port realized by CH343G. The signal wires in the figure can only be connected to RXD, TXD and the common ground wire. Other signal lines can be selected as needed, and can be left suspended when not needed.

P4 is a USB port. The USB bus includes a pair of 5V power lines and a pair of data signal lines. Generally,

the +5V power line is red, the ground line is black, the D+ signal line is green, and the D- signal line is white. The supply current provided by the USB bus can reach 500mA, and the VBUS pin detects the USB power supply status here.

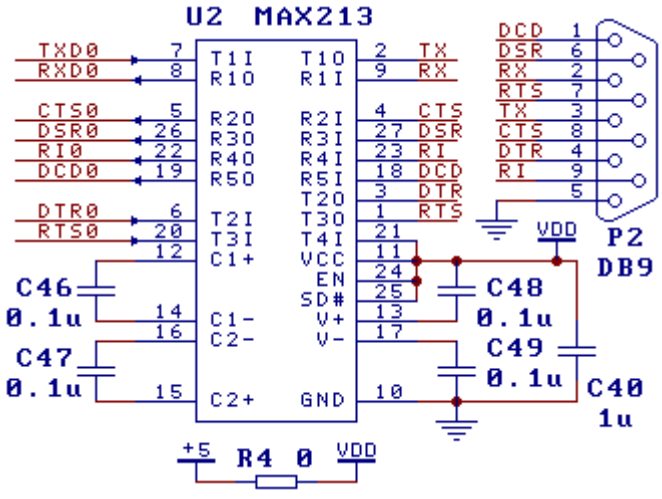
Three power supply schemes: Firstly, all USB power supplies; USB bus is directly used to provide 5V power supply for CH343 chip and USB products, i.e., 5V power supply for VDD5=VBUS=USB, 5V for VIO=VMCU=USB or 1.8V～4V after voltage reduction; secondly, separate and independent power supply; the self-supplied standing power VDD is used for VIO of CH343 and the MCU of the product together, and the USB power is used for CH343. VDD5 is connected to the USB power VBUS, that is, VDD5=VBUS=USB=5V power supply, and self-supplied power of VIO=VMCU=VDD=1.8V-5V; thirdly, all self-supplied power, the USB power is only detected but not used. USB product provides standing power VDD through self-powered mode; mainly VDD5=VIO=VMCU=VDD=self-supplied 5V or VDD5=V3=VIO=VMCU=VDD=self-supplied 3.3V two kinds.

The capacitor C7 of the V3 pin is 0.1uF, and is used for the decoupling of the internal 3.3V power supply node decoupling of CH343, and C8 and C9 are used for the decoupling of the external power supply.

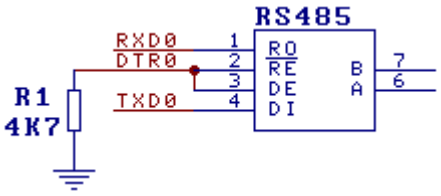
It should be noticed that the decoupling capacitors C7, C8 and C9 should be as close as possible to the connected pins of CH343 when the printed circuit board PCB is designed; the D+ and D- signal lines should be close to parallel wiring, and ground wire or covered copper should be provided on both sides to reduce the external signal interference;

7.2. USB to 9-wire RS232 Serial Port (Figure below)

CH343G provides commonly used serial port signals and MODEM signals. In the figure, the TTL serial port is converted to RS232 serial port through the external level conversion circuit U2. Port P2 is a DB9 pin, and its pins and functions are the same as those of the ordinary 9-pin serial port of the computer. The similar models of U2 include MAX213/ADM213/SP213/MAX211 and so on. USB bus uniformly supplies power to U2 in the figure through R4.

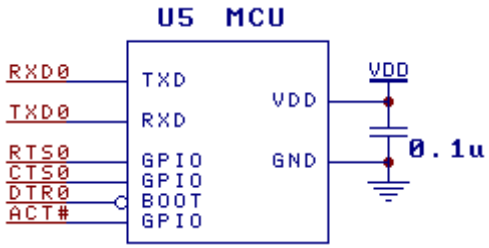


7.3. USB to RS485 (Figure below)



In the figure, the DTR pin is externally connected to the pull-down resistor, so as to switch to the TNOW pin, which is used to control the DE (high active transmission enabling) and RE# (low active transmission enabling) pins of the RS485 transceiver. The RS485 transceiver and VIO should share the same power.

7.4. Connection to MCU Serial Port to Supply Power Respectively (Figure below)



The figure above shows the reference circuit of MCU connected to CH343 chip through TTL serial port to realize USB communication under dual power supply mode. CH343 is powered by USB bus. Another self-supplied power VDD is used for VBUS, MCU and VIO. VDD supports 5V, 3.3V, 2.5V and 1.8V.

Except for RXD and TXD, other pins are optional for connection.

If the serial port speed is high, then the MCU can realize hardware automatic flow control through CTS and RTS.

If necessary, VBUS (OUT1) can also be used to control the PMOS power switch for supplying power to MCU from the USB power supply, as shown in the following figure: +5 is the USB power supply, VDD is the VIO power supply and MCU power supply of CH343. By default, the pull-down resistor of VBUS is turned on to generate a pull-down current, so that the PMOS grid electrode has enough voltage for switching on, and VBUS supplies power to VIO. After RTS and DTR are set in the computer software, it is valid when OUT1 is set. Then, the pull-down resistor of VBUS will be turned off, so that the grid electrode of PMOS will lose voltage and be turned off. Eventually, the VIO voltage drop leads to the MCU low voltage reset. When the VIO voltage drops to about 1.4V, the VIO low-voltage protection mechanism will be triggered, VBUS will automatically sink the pull-down current and recover the pull-down resistor, so that the PMOS will be turned on again and the VIO will be restored to supply power. The VIO voltage drop and MCU reset are realized in the whole process.