

BP233XJ Application Guide

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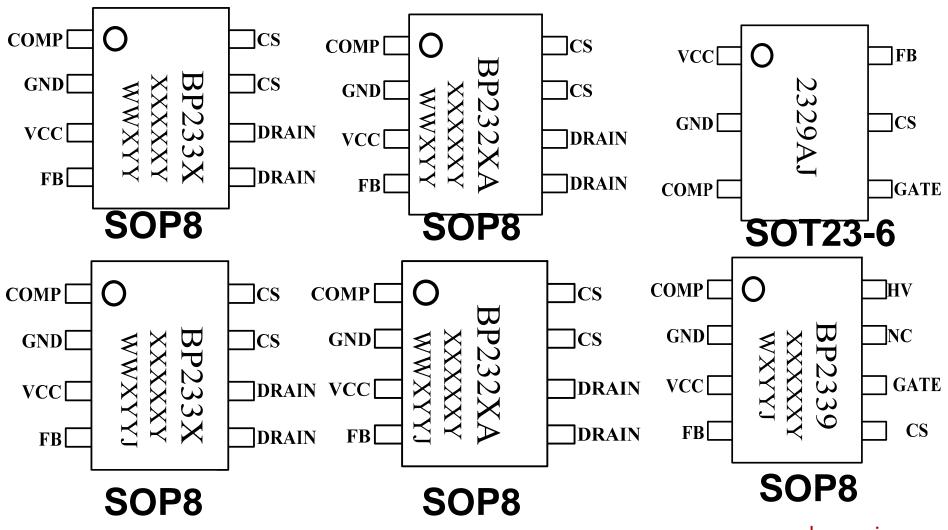


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BP23XX Products description

上海晶丰明源半导体有限公司 Bright Power Semiconductor

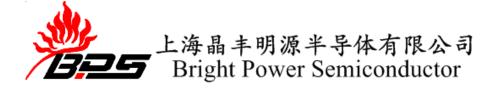
Products description:

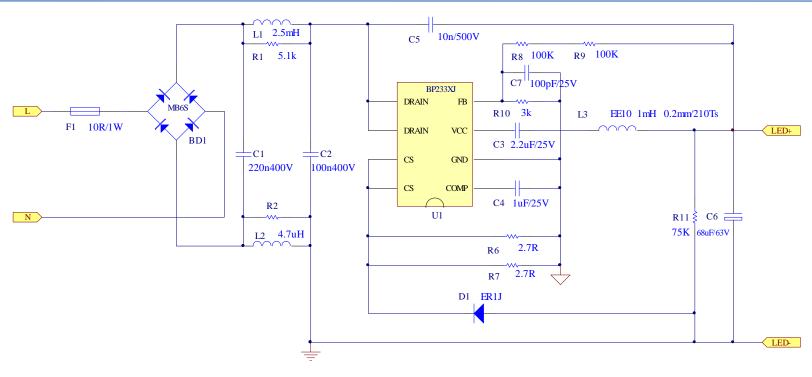


BP23XX Products descriptio 上海晶丰明源半导体有限公司 Bright Power Semiconductor

	BP23XX	BP233XJ
Spec change	Max on time:20us	Max on time:30us
Improved performance	When thermal fold back triggers ,it well have flicker	Improved ,it has no flicker if it has thermal fold back
Improved performance	OVP is easily be triggered ,leading to flicker	With 100PF in parallel with FB resistor, the application with be anti-humidity, high temp and less sensitive to layout
Application Notices (application parameters	If original	Recommend to have 100PF capacitor in parallel with FB resistors
needs to be checked if replace BP233X with BP233XJ)	If original	Recommend to have 1mA dummy load
51 233/01	If original	Recommend to have VCC capacitor be 2.2uF

Typical Design

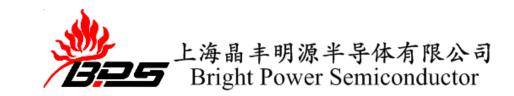




	Package	BV/V	Rds(on)/Ω
BP2335J	SOP8	550	6
BP2336J	SOP8	500	3
BP2338J	SOP8	600	2
BP2339J	SOP8	/	/

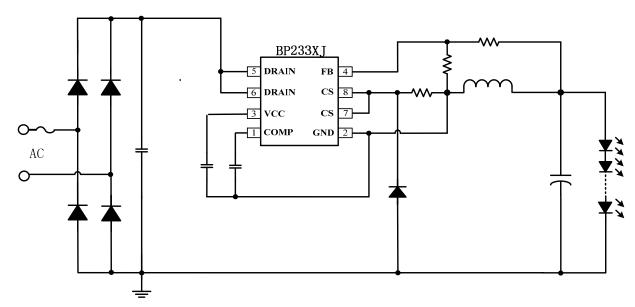
- If more power, invite BP2339J. The controller; external drive MOS, can push more power.
- FB add 100pF with chip optimized to enhance the anti-jamming capability.

Operation



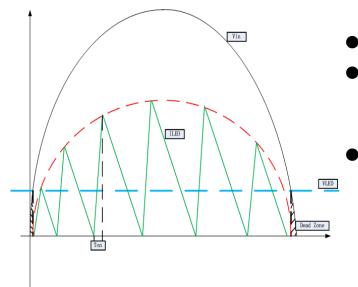
BP233XJ family feature:

- 1. Utilizes floating ground buck structure
- 2. Constant Ton to achieve high power factor
- 3. Fast start up and power supply with HV JFET
- 4. critical conduction mode operation
- 5. The average current sampling
- 6. Internal LED open protection/short protection
- 7. Internal Thermal Regulation Function

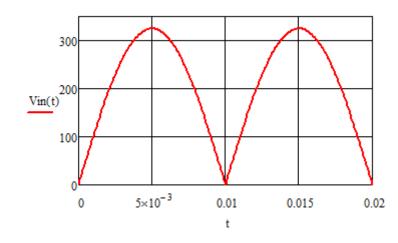


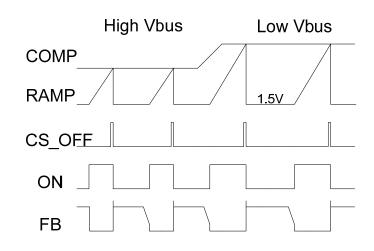
Operation





- Constant Ton PFC control with line compensation
- Operates in Critical Conduction Mode, the inductor current is sensed during the whole switching cycle and limited cycle by cycle.
 - COMP compensation ensure constant control and line regulation 。







Suggestion for Design Tool

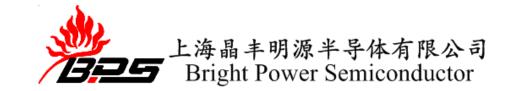
key parameters

The minimum system working frequency: suggested that selection in the 40~50KHz (Lowest operating frequency appears in full the minimum input voltage at peak), The operating frequency is too high PF value will deteriorate, low operating frequencies will require greater or more of the transformer primary side of the transformer to ensure that the number of turns of unsaturated to ensure at the minimum input voltage do not exceed the maximum on-time 30uS_o

Fsw_min: >40kHz, Ton_max<30us @ Vin_min

The maximum magnetic flux density: suggested that selection <0.3T, Because the system will reach the maximum peak current at the lowest input voltage peaks and, in some extreme applications can increase the Bm, get a better price

Bmax<0.3T



COMP Pin Design

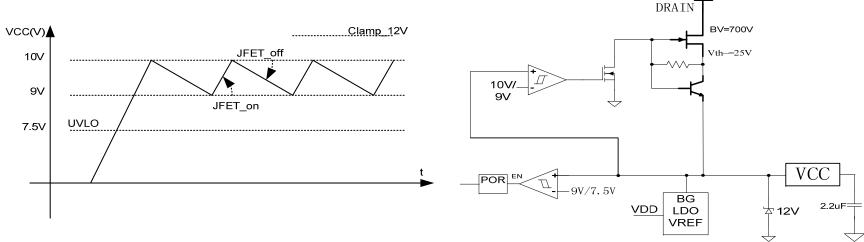
- Put C_COMP close to the COMP Pin and short trace in Layout.
- Typical value for C_COMP is 1uF to getting better startup.
 Too larger C_COMP, the start ability will be weaker, the power factor will be better.

for LTHD requirements, RC can be increased control loop compensation.



VCC Pin Design

• Power supply with HV JFET, Higher operation frequency need more supply.

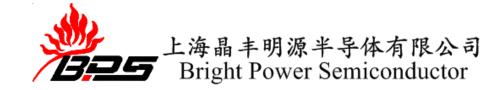


- VCC_Clamp at 12V;
- The more larger C_VCC, the more littler input voltage;
- VCC capacitor should not exceed 4.7uf (including 4.7uf), recommended 2.2uf;

VCC capacitor can not select more than 4.7uf reasons: In steady state operation, the VCC capacitor greater than or equal 4.7uF, JFET in to VCC capacitor charging time will be longer, giving VCC capacitor charging time, the instantaneous power consumption of the chip will increase,

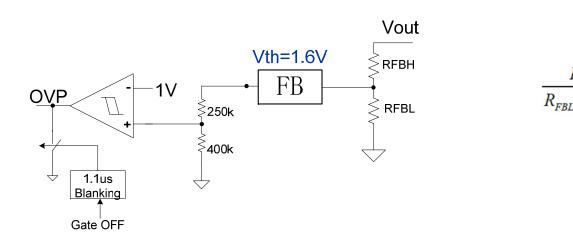
Cause fever becomes large chip, chip thermal regulation causes the output current is reduced when the JFET after the end of charging, reduce heat chip, chip thermal regulation of the output current. So when JFET charge to VCC, the output current will cause fluctuations, When this frequency fluctuation less than 100Hz (equivalent to the VCC capacitor charging frequencies), and enters the human visual range, you will see lights flashing or jitter. Reduce the VCC capacitor, the output current rippled frequency (VCC charging frequency) is greater than 100Hz, the human eye can not see the flashing lights or the phenomenon of jitter.

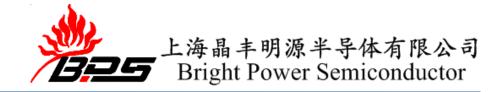
10 www.bpsemi.com



FB Pin parameters design(Important!)

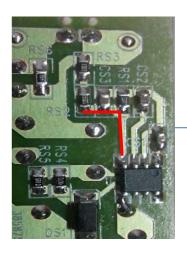
- R_L for FB is typical 3K to avoid interruptions;
- Set V_FB about 1V during normal operation, keep margin for OVP and Vo_min(FB OVP threshold is 1.6V).
- R_H could stand with BV voltage as result of two 1206 package.
- Add 100pF on FB pin to avoid interruption.





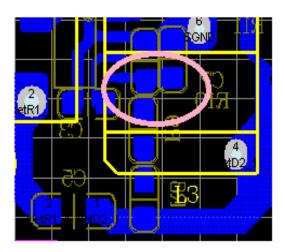
FB Pin Layout Design(Put all three resistors close to the FB pin.)

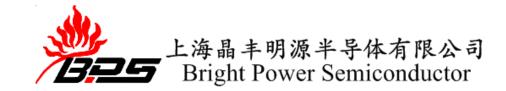
- FB upper arm connection foil between the two resistors must be short.
- FB node between the two resistors and down close to the FB Pin, The point takes away from the switching node, to prevent interference,
- If it is double-sided board, FB sampling end do not go to any top line



Recommendations for improvement

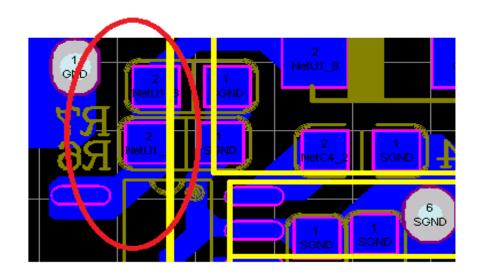






CS Pin Design

• CS connection GND Pin too long to be as short as possible resistance line, connected to the IC output will lead to deterioration of the current regulation



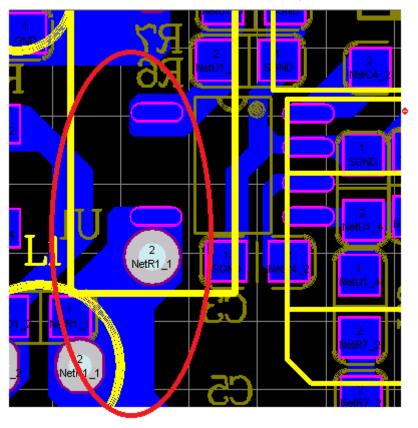


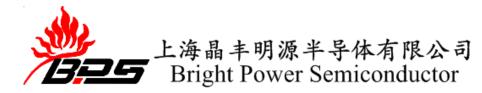
Drain/GND Pin Design

• Copper area of Drain give clearance space under Pin7. Too much copper on Drain weak the EMI but helpful a lot on thermal dissipation.

• In PCB Library, the package for SOP8 should at least remove Pin7, better as well as

Pin6 to extend the safety space.



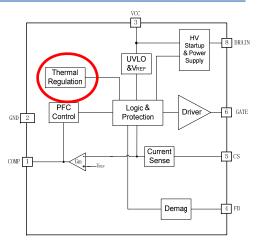


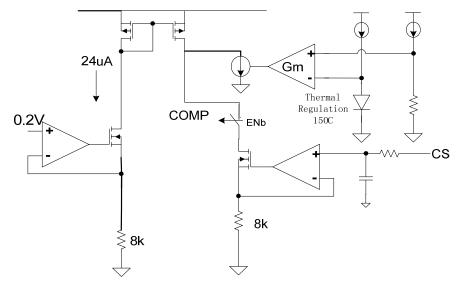
Thermal regulation when IC into thermal regulation ,the IC will adjust the COMP voltage to reduce output current, and at the same time ,the IC will adjust the Toff to reduce frequency ,ensure that output current will not decline too large to flicker when IC enter the thermal regulation.

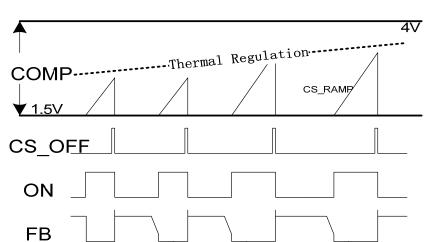
Suggestions:

Key consideration when designing the IC temperature to prevent premature entry into the thermal regulation:

- 1. Reduce working frequency can decline the IC temperature:
- 2. Appropriate increase in PCB chip Drain / CS pin copper area to enhance the cooling effect;



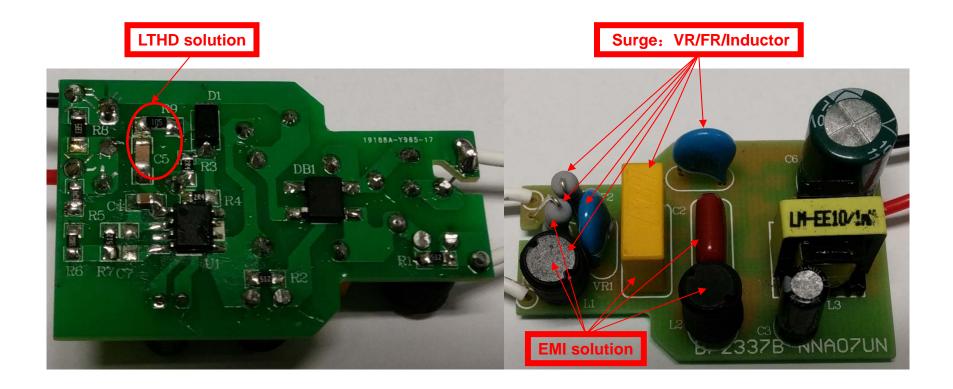






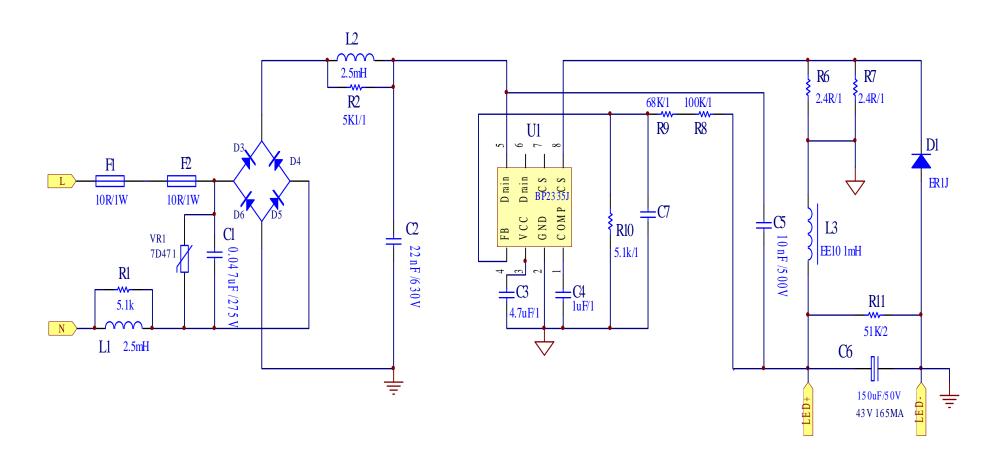
For India and Brazil

- More safety margin requested.
- 2.5kV surge.



For India and Brazil

2.5KV scheme schematic:





For India and Brazil

2.5KV test results:

With BP2335J, for example.

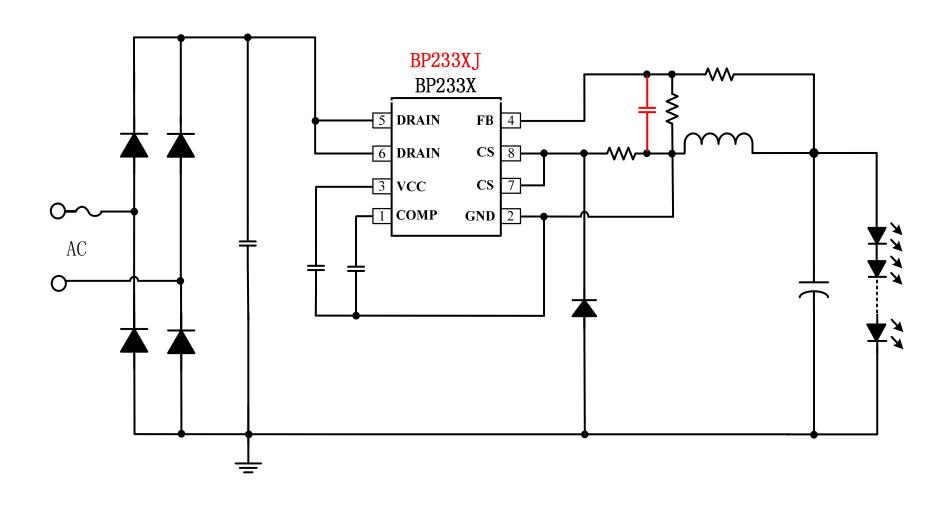
		BP2335J 2.5KV	
NO.	surge	+ 90°	- 270°
	1kV	PASS	PASS
	1.5kV	PASS	PASS
#1	2kV	PASS	PASS
	2.5kV	PASS	PASS
	2.6kV	PASS	PASS
	1kV	PASS	PASS
	1.5kV	PASS	PASS
#2	2kV	PASS	PASS
#2	2.5kV	PASS	PASS
	2.6kV	PASS	PASS
	3kV	PASS	PASS
	1.5kV	PASS	PASS
	2kV	PASS	PASS
#3	2.5kV	PASS	PASS
	2.6kV	PASS	PASS
	3kV	PASS	PASS



BP233XJ &BP23XX Replacement Guide

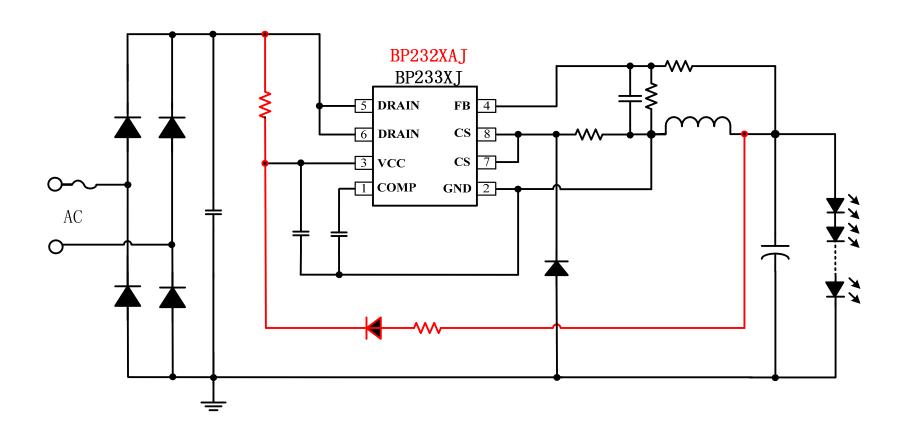


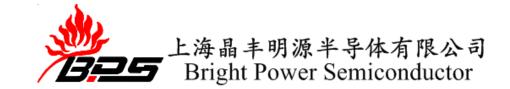
BP233XJ &BP233X replace schematic





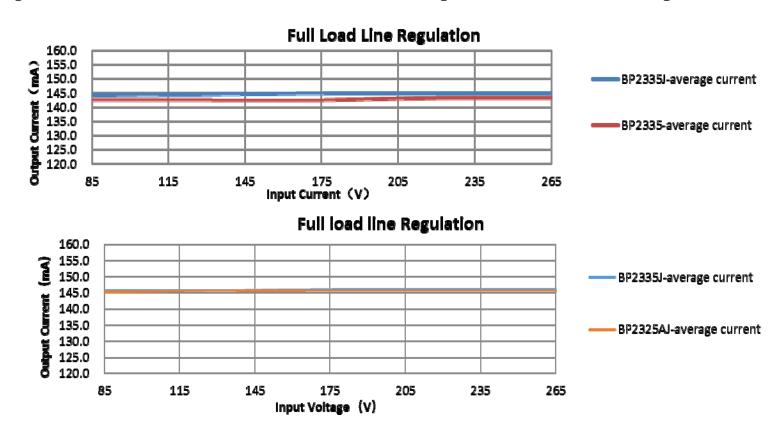
BP233XJ &BP233X replace schematic





After Replacement

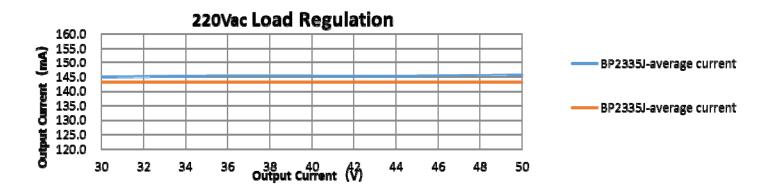
• Output current is consistent (with BP2335J comparison test as an example)

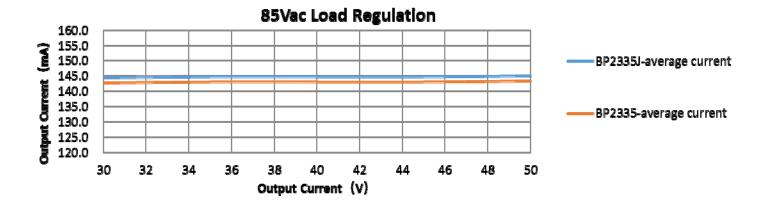


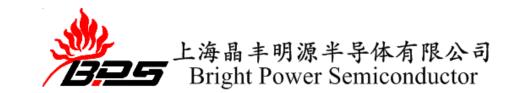


After replacement

Same load regulation

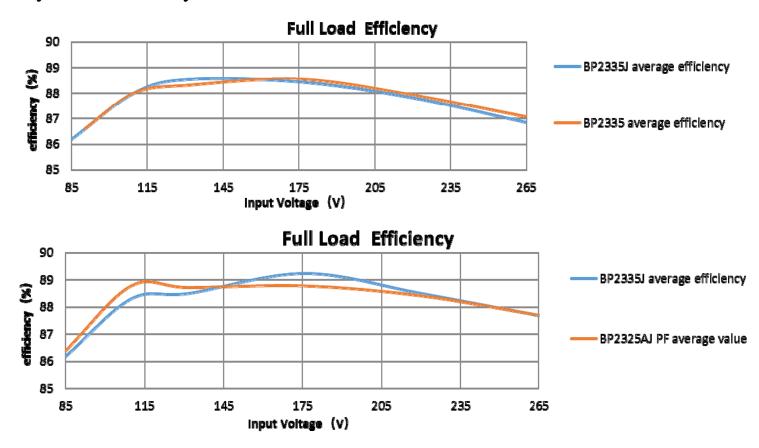


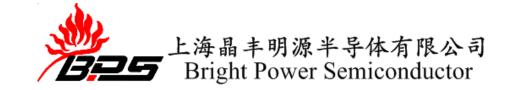




After replacement

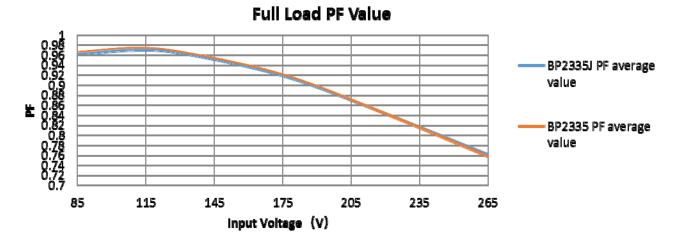
• Same system efficiency

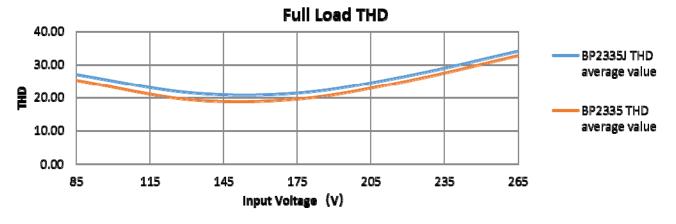


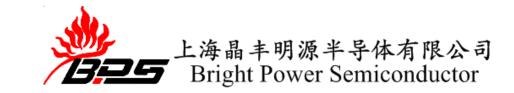


After replacement

• Systems PF, THD is a little low (BP2335J and BP2335 comparative data)

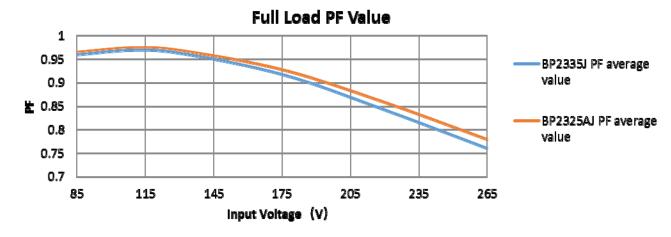


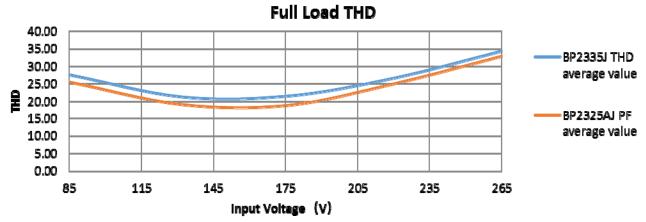


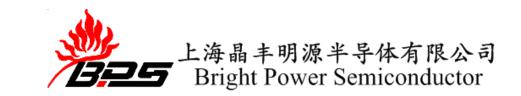


After replacement

• Systems PF, THD is a little low (BP2335J and BP2325AJ comparative data)



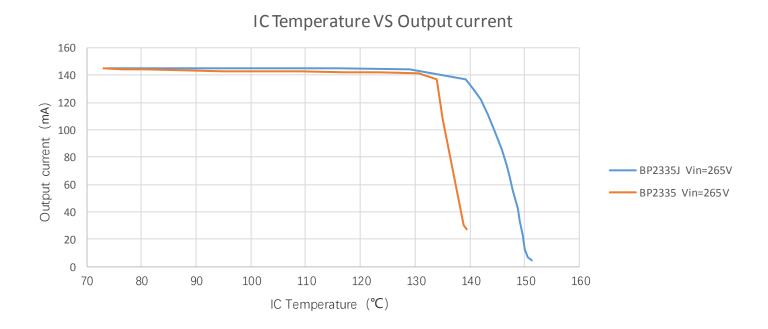


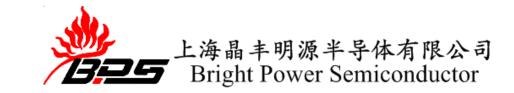


After replacement

• Thermal regulation

BP233XJ based on the current temperature curve improvement, BP233XJ slow decline in the current version when entering the thermal regulation Improved ,it has no flicker if it has thermal fold back .





Replacement consideration

• The reason of BP233XJ Systems PF, THD is a little low

BP233XJ version Tonmax about 30us, and BP233X / BP232XAJ Tonmax version of 20,Tonmaxrelative increase, Increase The gain of the whole system (COMP voltage decreases also can achieve the same output changes); Because the system of compensation main pole unchanged (Determined by the COMP current and COMP capacitance), The phase margin will be worse (Equivalent to increase system bandwidth, the 100 hz frequency ripple suppression of variation), so BP233XJ version of PF/THD relative BP233X and BP232XAJ is less。

Improvement Strategy: 1. Increase COMP capacitance

- 2. The COMP pin can plus RC compensation
- 3. Reduce system working frequency (increase on time)



- 1. Increase COMP capacitance
- Increase COMP capacitance

265

0.754

0.758

0.757

Under different comp capacitance BP2335J contrast BP2325AJ/BP2335 PF 。

Input	F	BP2325AJ The	C_COMP is 1	.uF	Input	BP2335J The C_COMP is 1uF			
voltage (V)	age (1) 1# 2# 3# average	average	voltage (V)	1#	2#	3#	average		
90	0.97	0.97	0.97	0.970	90	0.964	0.965	0.965	0.965
110	0.975	0.975	0.975	0.975	110	0.968	0.97	0.97	0.969
132	0.967	0.967	0.968	0.967	132	0.962	0.963	0.962	0.962
176	0.924	0.924	0.926	0.925	176	0.915	0.916	0.918	0.916
220	0.854	0.853	0.856	0.854	220	0.84	0.839	0.841	0.840
265	0.775	0.774	0.776	0.775	265	0.758	0.757	0.761	0.759
Input		BP2335 The (C_COMP is 1u	F	Input voltage	ВР	2335J The C	_COMP is 2.2	uF
voltage (V)	1#	2#	3#	average	(V)	1#	2#	3#	average
90	0.969	0.969	0.97	0.969	90	0.968	0.968	0.968	0.968
110	0.973	0.974	0.973	0.973	110	0.974	0.974	0.974	0.974
132	0.964	0.965	0.965	0.965	132	0.97	0.97	0.969	0.970
176	0.916	0.92	0.919	0.918	176	0.933	0.932	0.933	0.933
220	0.837	0.845	0.842	0.841	220	0.866	0.863	0.864	0.864

0.756

265

0.785

0.783

0.787

0.785

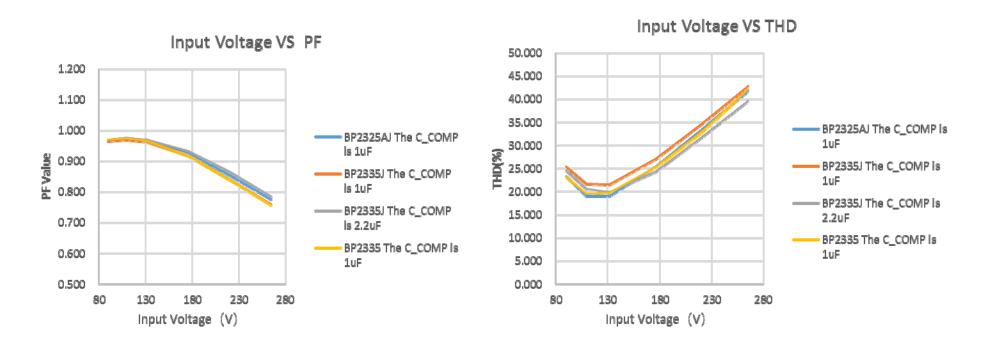


Replacement consideration

• The choice of COMP capacitance

Under different comp capacitance BP2335J contrast BP2325AJ/BP2335 PF and THD.

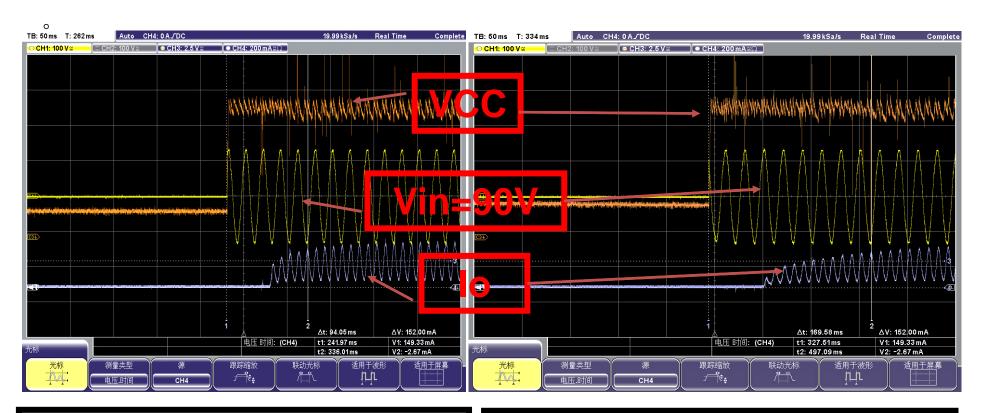
Comp capacitance can significantly increase PF, reduce THD system.





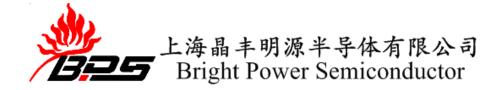
Increasing COMP capacitance, then start time longer

COMP capacitance increases easy to cause the change of the startup time, the greater the capacitance the slower startup time



1uf C_COMP the BP2335J startup time is 94.05us

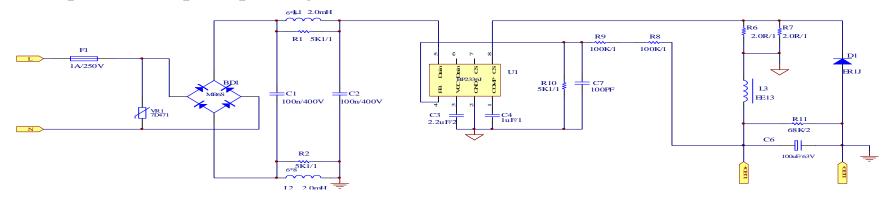
2.2uf C_COMP the BP2335J startup time is 169.58us



2. The COMP pin can plus RC compensation

LTHD Plan: The following plan BP2336J, for example

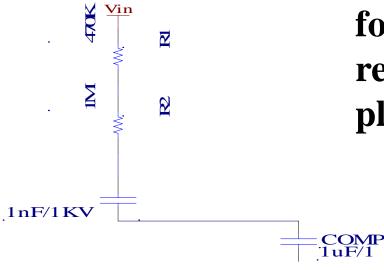
Before optimization principle diagram:



Vin (V)	lo (mA)	Vo (V)	Pin (W)	η (%)	PF	THD (%)
90	198	51.4	11.46	88.81	0.963	27.2
110	198	51.3	11.33	89.65	0.976	20.8
132	198	51.1	11.24	90.02	0.979	17.9
176	198	51	11.21	90.08	0.965	19.5
220	198	51	11.27	89.60	0.938	23.6
265	198	51	11.37	88.81	0.898	28



Vin (V)	lo (mA)	Vo (V)	Pin (W)	η (%)	PF	THD (%)
90	198	51.3	11.41	89.02	0.963	27.4
110	198	51.3	11.29	89.97	0.98	19.7
132	198	51	11.21	90.08	0.985	16.3
176	198	51	11.22	90.00	0.988	12.3
220	198	51.1	11.33	89.30	0.987	11.2
265	198	51	11.49	87.89	0.976	16.5



The COMP pin can plus RC compensation

for THD to under 20% meet the requirements if The COMP pin can plus RC compensation



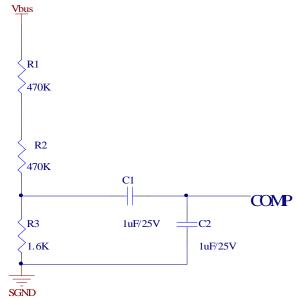
About the COMP plus compensation problems:

Our laboratory for high pressure, high temperature and high humidity not found the problem; But detailed FAE confirmed, because of High voltage THD RC compensation, and in wet environment, there will be a rising power phenomenon.

Strategy: Parallel resistance to partial pressure on Vbus, at that moment, from Vbus voltage to the COMP become low, thus making the voltage on Vbus is not due to the high pressure leakage directly to the COMP.

Test data and some schematic diagram:

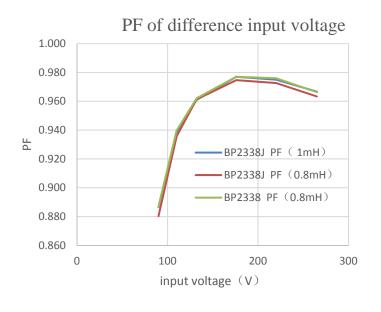
Vin (V)	lo (mA)	Vo (V)	Pin (W)	η (%)	PF	THD (%)
90	199	51.5	11.54	88.81	0.963	27.4
110	199	51.3	11.39	89.63	0.979	19.9
132	199	51.1	11.33	89.75	0.985	16.1
176	199	51	11.31	89.73	0.987	13.1
220	199	50.9	11.44	88.54	0.983	13.5
265	199	50.8	11.62	87.00	0.969	20

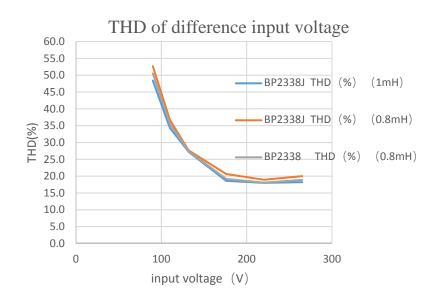


Compensation to improve the circuit part

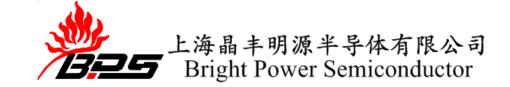


- 3. Reduce system working frequency (increase on time)
- Reduce the influence of the working frequency of PF/THD system





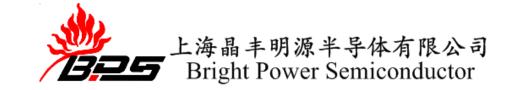
Under the different inductor, the big inductor, the system working frequency will be reduced, the PF/THD improved. So, reduce the system working frequency can improve PF and THD.



• The PF influence of Reduce working frequency (the following data is BP2338J, as an example)

ıc		BP2338J PF (1mH)						
IC	90Vac	110Vac	132Vac	176Vac	220Vac	265Vac	load (V)	
BP2338J-1#	0.883	0.938	0.962	0.979	0.976	0.969	80	
BP2338J-2#	0.883	0.938	0.963	0.979	0.976	0.968	80	
BP2338J-3#	0.894	0.938	0.958	0.973	0.973	0.963	80	
BP2338J PF	0.887	0.938	0.961	0.977	0.975	0.067	90	
average value	0.887	0.938	0.961	0.977	0.975	0.967	80	
10	BP2338J PF (0.8mH)						load (\/)	
IC	90Vac	110Vac	132Vac	176Vac	220Vac	265Vac	load (V)	
BP2338J-1#	0.879	0.935	0.961	0.974	0.971	0.963	80	
BP2338J-2#	0.883	0.935	0.962	0.976	0.974	0.965	80	
BP2338J-3#	0.879	0.937	0.961	0.974	0.973	0.962	80	
BP2338AJ PF	0.000	0.026	0.061	0.075	0.072	0.062	00	
average value	0.880	0.936	0.961	0.975	0.973	0.963	80	

IC	BP2338 PF (0.8mH)						
IC	90Vac	110Vac	132Vac	176Vac	220Vac	265Vac	load (V)
BP2338-1#	0.887	0.940	0.963	0.977	0.976	0.966	80
BP2338-2#	0.887	0.940	0.962	0.977	0.976	0.966	80
BP2338-3#	0.887	0.939	0.961	0.977	0.976	0.967	80
BP2338 PF average value	0.887	0.940	0.962	0.977	0.976	0.966	80

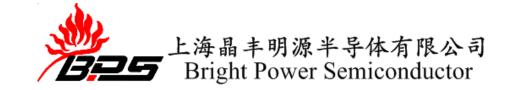


Replacement consideration

• The THD influence of Reduce working frequency (the following data is BP2338J, as an example)

IC		BP.	2338J THD	(%) (1mH	1)		load ()()
IC IC	90Vac	110Vac	132Vac	176Vac	220Vac	265Vac	load (V)
BP2338J-1#	56.7	36.0	27.4	18.5	17.8	18.7	80
BP2338J-2#	51.8	36.0	26.9	18.8	18.0	18.9	80
BP2338J-3#	48.4	34.3	27.2	18.6	18.0	18.2	80
BP2338J THD	E2 2	25.4	27.2	18.6	17.0	18.6	00
average value	52.3	35.4	21.2	10.0	17.9	18.0	80
IC		BP2	338J THD	(%) (0.8m	H)		load (\/)
IC	90Vac	BP2 110Vac	338J THD 132Vac	(%) (0.8m 176Vac	H) 220Vac	265Vac	load (V)
IC BP2338J-1#	90Vac 53.1	1	1	, ,	·	265Vac 20.2	load (V)
		110Vac	132Vac	176Vac	220Vac		` ′
BP2338J-1#	53.1	110Vac 36.7	132Vac 27.3	176Vac 20.5	220Vac 19.2	20.2	80
BP2338J-1# BP2338J-2#	53.1 51.9	110Vac 36.7 37.1	132Vac 27.3 27.6	176Vac 20.5 19.5	220Vac 19.2 18.3	20.2 19.5	80

IC		load (V)						
IC	90Vac	110Vac	132Vac	176Vac	220Vac	265Vac	load (V)	
BP2338-1#	50.3	35.5	27.0	19.0	18.0	18.7	80	
BP2338-2#	50.7	35.2	27.1	19.1	17.8	18.9	80	
BP2338-3#	50.6	35.8	28.0	19.4	18.4	19.0	80	
BP2338 THD average value	50.53	35.50	27.37	19.17	18.07	18.87	80	



After replacement

• At the Room Temperature (C_VCC is 2.2uf)

			After Temperature stability							
Input Voltage (V)	Environment temperature (°C)	BP2335J	BP2335	BP2335J and BP2335 temperature difference	BP2325AJ	BP2335J and BP2325AJ temperature difference				
		IC Temperature (°C)	IC Temperature (°C)		IC Temperature (°C)					
90	28	77. 5	73. 8		77. 2					
Rising temperatur	re device△T (°C)	49. 5	45. 8	-3.7	48. 2	-1.3				
176	28	70	71. 2		68					
Rising temperatur	re device△T (°C)	42	43. 2	1.2	40	-2				
220	28	73. 5	75. 8		70					
Rising temperatur	e device \triangle T ($^{\circ}$ C)	45. 5	47.8	2.3	42	-3.5				
265	27	78	81. 5		74. 2					
Rising temperatur	re device△T (°C)	51	54. 5	3.5	46. 2	-4.8				
300	29	90. 2	93. 9		81. 1					
Rising temperatur	re device△T (°C)	61. 2	64. 9	3.7	51. 1	-10.1				

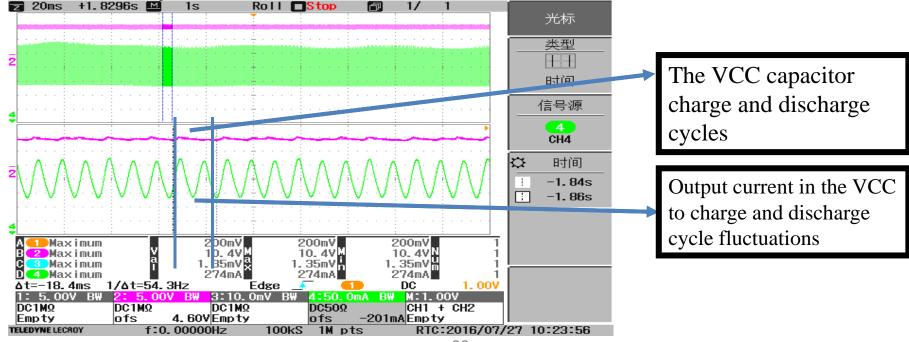


Replacement consideration

• The choices of C_VCC

Compare with BP233X, C_VCC recommended less than 4.7uf;

1、When enter thermal regulation, the BP233XJ into DCM mode, the IC will adjusted Toff according to the temperature of the IC. if the VCC capacitor is too big,JFET to recharge cycle longer VCC。 That frequency about 100HZ, When enter thermal regulation, due to JFET fever caused output current in the VCC to charge and discharge cycle fluctuations, we can see the flicker clearly.

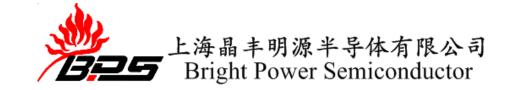




Replacement consideration

- The choice of C_VCC
- VCC capacitor should not exceed 4.7uf (including 4.7uf), recommended 2.2uf; VCC capacitor can not select more than 4.7uf reasons: In steady state operation, the VCC capacitor greater than or equal 4.7uF, JFET in to VCC capacitor charging time will be longer, giving VCC capacitor charging time, the instantaneous power consumption of the chip will increase,

Cause fever becomes large chip, chip thermal regulation causes the output current is reduced when the JFET after the end of charging, reduce heat chip, chip thermal regulation of the output current. So when JFET charge to VCC, the output current will cause fluctuations, When this frequency fluctuation less than 100Hz (equivalent to the VCC capacitor charging frequencies), and enters the human visual range, you will see lights flashing or jitter. Reduce the VCC capacitor, the output current rippled frequency (VCC charging frequency) is greater than 100Hz, the human eye can not see the flashing lights or the phenomenon of jitter.

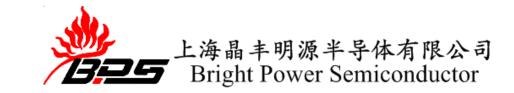


Replacement consideration

- OVP
- 1. Compare with BP232XAJ, FB anti-interference enhancement (must be 100pF capacitor resistor in parallel with FB), Without 100pF capacitor with FB, if BP233X add interference on FB, that will be flicker.
- 2. The whole lamp test IC after be affected with damp, high temperature and high pressure test, the BP233XJ has not been flicker.

	Open circuit protection voltage (V)						
IC	FB without interference, with 100pf capacitor OVP calculated value is Vovp=64.3V						
	90Vac	110Vac	132Vac	176Vac	220Vac	265Vac	
BP2335J-1#	75	74. 1	73. 7	73. 7	69. 5	66. 6	
BP2335J-2#	77	75.8	74. 1	71.6	69. 1	69. 1	
BP2335J-3#	80. 4	78.7	76. 2	76.6	72.5	71. 2	

	Open circuit protection voltage (V)						
IC	FB with interference ,with 100pf capacitor OVP calculated value is Vovp=64.3V						
	90Vac	110Vac	132Vac	176Vac	220Vac	265Vac	
BP2335J-1#	98.7	80.4	75	73. 7	70.8	67. 5	
BP2335J-2#	98. 7	78. 7	76. 2	73. 3	69. 1	68. 3	
BP2335.J-3#	100	79. 5	77. 9	76. 2	71.6	71. 2	
		O	pen circuit protect				
IC	FB withou	O at interference, w		ion voltage (V)			
	FB withou			ion voltage (V)			
		ıt interference 🔻 v	vithout 100pf capa	ion voltage(V) citor OVP calcula	ated value is Vovp	=64.3V	
IC	90Vac	at interference, w 110Vac	vithout 100pf capa 132Vac	ion voltage (V) acitor OVP calcula 176Vac	ated value is Vovp 220Vac	265 Vac	



Replacement consideration

OVP

Compare with BP233X, OVP will change with the input voltage, input low voltage, high OVP, When FB side add interference, low voltage input, OVP will follow input voltage; The input voltage increases, OVP gradually returned to normal.

Reason: When input voltage is low, input and output difference is small, the peak current is very small, demagnetization time is lesser, at this time that cloud not detection OVP, so when output is open, the V_OVP will be following with input voltage; with input voltage rising, The V_OVP will gradually returned to normal.

Improvement: maybe we can increase dummy load current.

$$\frac{R_{FBL}}{R_{FBL} + R_{FBH}} = \frac{1.6V}{V_{OVP}}$$



Replacement consideration

• The same surge (The following data in BP2335J, as an example) the surge of cool MOS is poor.

(one pi+one 10Ω fuse resistance)							
NO.	surge	BP2335J Vds	BP2335J	BP2335 Vds	BP2335		
#1	250V	656V	PASS		PASS		
	300V	681V	PASS		PASS		
	350V	687V	PASS	687V	PASS		
	400V	712V	PASS	712V	PASS		
	450V	731V	PASS	725V	PASS		
	500V	756V	PASS				
	550V	768V	PASS	743V	PASS		
	600V	762	1stFail	406V	1stFail		
#2	300V	668V	PASS		PASS		
	350V	693V	PASS	687V	PASS		
	400V	712V	PASS	706V	PASS		
	450V	731V	PASS	725V	PASS		
	500V	743V	PASS	750V	PASS		
	550V	762V	PASS	762V	PASS		
	600V	762V	1st Fail	750V	1st Fail		
#3	300V	668V	PASS				
	350V	693V	PASS	681V	PASS		
	400V	712V	PASS	706V	PASS		
	450V	737V	PASS	731V	PASS		
	500V	750V	PASS	743V	PASS		
	550V	768V	1st Fail	762V	PASS		
	600V			758V	1st Fail		



Replacement consideration

The same EMI

The following data is BP2338J ,as an example (input voltage is 220V, output is 80V220mA, inductance 0.8mH):

