

DEVELOPMENT OF LOGICAL CIRCUITRY USING SILICON CARBIDE SUBSTRATES FOR CONTROL CIRCUITS IN HARSH ENVIRONMENTS

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Title of Research Opportunity: SiC CIRCUIT AND DEVICE DESIGN AND FABRICATION

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1. STATEMENT OF PROBLEM

Recently, NASA has begun prioritizing an exploratory mission to Venus [1], including a surface lander [2]. Previous landers from the Venera program by the USSR were only able to last, at most, two hours on the unforgiving Venusian surface [3]. The extreme temperatures and oxidative atmosphere of the planet's surface mean it is very difficult for current electronic systems to perform for extended periods. While a wealth of new high temperature and pressure sensing instruments have been developed as part of the Venus Exploration Analysis Group (VEXAG), the glue electronics to control and operate such a lander are still elusive [4].

The development of silicon carbide (SiC) semiconductor devices has gained increasing popularity in the past 20 years, yet the technology lacks the wide breadth of available devices which competing substrates currently offer. Far from the first light emitting diode [5, 6] which was originally made in SiC, today SiC can be found in many high power applications. Recent developments have even allowed the creation of power switching devices with high-voltage junction temperature tolerance up to 1200 V in both JFET and MOSFET designs [7, 8]. Current SiC logical devices are produced using JFET technology. Core logic gates such as the inverter, NAND, and NOR have been demonstrated in both depletion mode [9] and enhancement mode [10] SiC JFET. Despite recent demonstrations of a ring oscillator [?] and development of 100's scale transistor level logic using SiC JFET technology [11], there

is a dearth of advanced logic designs for SiC circuits which would further the NASA Venus lander objectives. The goal of this proposed work is to develop discrete digital logic devices using SiC substrates and patterning.

2. BACKGROUND AND RELEVANCE TO PREVIOUS WORK

Silicon carbide has several interesting properties that make it an attractive semiconductor platform for devices intended to withstand harsh environments. At standard atmospheric pressures, SiC remains crystalline with no defects at temperatures up to 2760 °C before partial sublimation [12]. At higher pressures, this temperature stability increases. Under 100 atm, similar to the pressure at the surface of Venus, SiC remains solid up to 2830 °C before melting. Individual junctions of p-doped and n-doped SiC material have a much higher tolerance for heat than more commonly used substrates such as Si. This is because the optimum working temperature of SiC is very close to the highest normal mode vibrational temperature, or band gap [13]. Microelectromechanical systems (MEMS) based on SiC have been established as a viable device for some time [14], and some developed MEMS devices are pushing temperature limits in sensors [15]. Logic gates manufactured from SiC can take advantage of this property by creating devices which tolerate high voltage switching, a task which produces a large amount of heat [16]. The converse can be true as well: it is possible to make low power logic gates that tolerate extreme temperatures.

Additionally, SiC has been shown to be particularly resilient against radiation damage. Circuits made of SiC have been reported to exhibit much lower rates of carrier damage due to deep material defects caused by neutron flux, with McGarrity et al. reporting $\frac{1}{3}$ of the damage compared to Si based devices at doses of 10^{16} neutrons/cm² [17]. This makes SiC technology attractive for radiation heavy environments, including satellites and exploratory vehicles. The large gate sizes in current SiC technology compared to modern CMOS feature sizes makes the SiC further resistant to radiation effects [18]. If this material is used for the sensitive electronic equipment, it is possible to have reduced failure rates with current design specifications. Furthermore, it is possible that future devices using this technology may

require less device redundancy for radiation hardening purposes, making it possible to create exploratory vehicles with greater computational power and reduced power consumption.

Logical units for SiC are designed by the NASA Silicon Carbide Electronics and Sensors group using depletion mode JFET technology on both 4H-SiC and 6H-SiC wafers. At the simplest level of description, an n-type JFET, the most durable and stable type for high temperature operation [11], is a transistor gate with the drain and source connected to an n-type substrate with a p-type gate separated by a depletion layer. A detailed diagram of the current archetypal SiC JFET layers can be found in the literature [19]. These JFETs are normally ON devices which switch OFF when a voltage applied to the gate passes a certain threshold in a reverse biased regime. Due to this design, the source requires a negative voltage, making the HIGH and LOW bits ground and a negative voltage, respectively. As certain parts of a logical array require a positive voltage, a JFET logic circuit is necessarily more complex to design due to the presence of an additional power rail. Further complications arise from the body bias effect based on the substrate voltage [20] and radially dependent resistivity observed in printed wafers [19].

As a physical chemist, I have an outside perspective on device function at the gate interface level which allows for a critical approach to the challenges posed by innovative logic design. My previous experience with silicon based control systems has demonstrated that I am capable at computer aided design (CAD) of electronic systems [21]. In addition to my design experience, I have also used modeling programs such as SPICE to characterize the behavior of a Fourier transform device for monitoring sample conductivity. Modern developments in microcontroller prototyping boards allow for integration of one device to test another. My previous work gave me experience with prototype evaluation of electronic systems and bringing a scientific approach to an engineering problem. Particularly, previous designs for sensors deployed in unpredictable climates have made me conscious of the need for devices built to tolerate these conditions including temperature dependent conductivity sensors [22]. As a scientist who enjoys developing devices for monitoring and evaluating physical and

chemical properties, the challenges posed by SiC JFET design appeal to my desire to broaden my skills.

3. GENERAL METHODOLOGY, PROCEDURES TO BE FOLLOWED, AND TIMELINE FOR COMPLETION OF EACH STEP

The goal of this proposed work is to develop logic circuits required for a low power monitoring device tolerant to harsh conditions by application of known computing architecture to the emerging silicon carbide technology. At the highest level of abstraction, a device of this nature requires a central processing unit (CPU), level shifters, analog to digital converters (ADC), switched power supply units (PSU), and memory. Certain portions of this list, including level shifters [9], ADC [23], and PSU [24], have been demonstrated in previous research. In the case of a modern application, a single package microprocessor can handle most of these tasks. However, minimal work has been done creating complex logic for the CPU in SiC. The development of this device must start from a basic level, designing the subcomponents of the CPU individually.

A CPU can be generalized as a combination of individual logic units, primarily these are registers and arithmetic logic units (ALU). The goal of this proposal is to develop the technology in SiC JFET for both of these logic units to create a functional 8-bit microprocessor.

3.1. Register. The register is a logic unit which is included in many important CPU and device components such as the primary register, memory, instruction set, and program counter. To construct this unit, we must reduce this piece down to its relatively simpler components. The register is a series of clock synchronized flip-flops, a flip-flop is a pair of latches, a latch is simply a pair of NOR gates connected in a certain manner, and a NOR gate is constructed from a few individual transistors. Figure 1 shows the decreasing levels of abstraction from the register of a popular integrated circuit to the layers and doping of a single NOR gate designed for CMOS technology. The transistor technology for JFET SiC gates have been previously demonstrated for NOR gates, making the technology scale up possible.

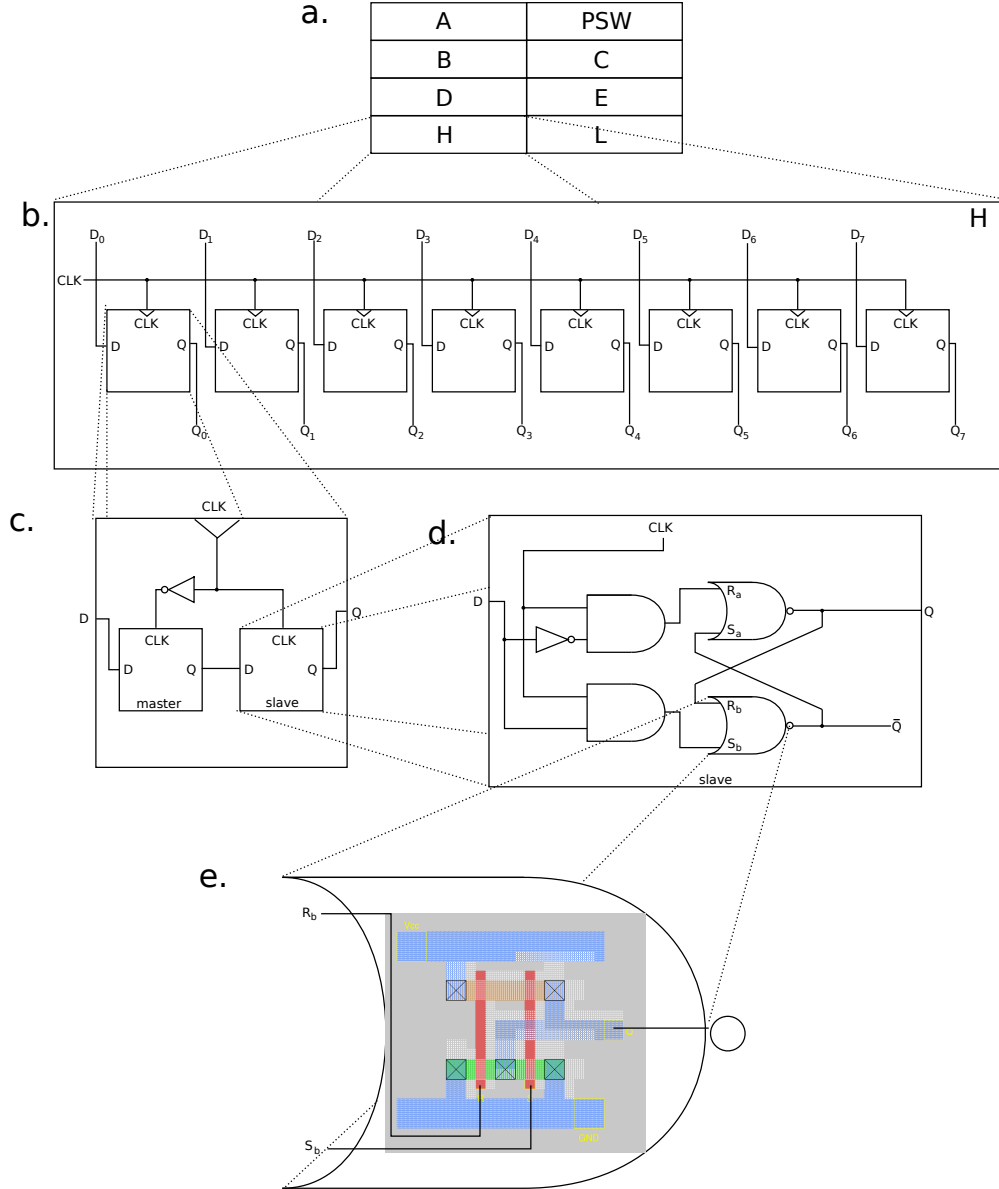


FIGURE 1. This is an example register design showing the design hierarchy. Part *a* shows the primary user accessible 8-bit registers included in the design of the popular Intel 8085 chip [25]. Part *b* shows detail of one register from part *a* [26, 27]. Each bit of the register is a flip-flop which adjusts the value from D to Q for each bit on in a clock cycle. Part *c* shows one of these flip-flops. A flip-flop is composed of two latches, a master and a slave, which copy D to Q on the rising edge of the clock cycle. This saves the state of the flip-flop at all other times. Part *d* shows one of the latches, a simple logic circuit consisting of one NOT, two ANDs, and two NORs in a bistable arrangement. Part *e* shows a diagram of one CMOS NOR gate depicted in part *d* as they would be designed for patterning on the SiC surface using the program MAGIC [28]. In short: multiple of *e* make up *d*, which make up *c*, which make up *b*, which make up *a*.

Due to the synchronous nature of the register and the importance of timing in computing, each device will be rigorously analyzed as it is created and tested. As it is impractical to directly measure single gate delay, a value which is often on the scale of picoseconds, it is useful to estimate the rise and fall of a signal through a gate using computational models and values of capacitance and current for each interconnect [29]. The delay for multiple equivalent gates is additive at scale, making the averaged delay over multiple gates in a device a calculable quantity with simple instrumentation. The averaged gate speed can be measured by construction of an array of latches acting asynchronously. This will be used to verify computationally calculated values.

Keeping with the “bottom-up” approach to design on the SiC substrate, the first task will be designing and verifying a single bit flip-flop, which has not been reported in literature. The patterned device will be characterized by tests to determine the ability to retain and replace the bit over multiple clock cycles. As SiC devices are being sought to operate in harsh conditions, tests will be undertaken to determine the bit retention ability of the flip-flop at a range of temperatures from standard conditions to $>500^{\circ}\text{C}$. Testing of the device can take place with a voltage monitor (capable of determining bit state) at short time scales and a local RC oscillator (as oscillators must be close to the circuit to prevent return current, making an external crystal oscillator impractical for high temperature tests). The second task will be to scale this device up to a full 8-bit register. Findings from the first task will be used to determine the design of this circuit, and it will be tested and verified in a similar manner.

3.2. Arithmetic Logic Unit. Another essential component of the CPU is the Arithmetic Logic Unit (ALU). This is an umbrella term for portion of the processor which performs simple arithmetic operations such as addition, subtraction, multiplication, division, and comparison. Each of these operations requires a distinct circuit. The addition and subtraction circuitry will be designed in the form of a carry-lookahead adder (chosen for the ability to perform faster calculations than many other adder circuits, a property which will be valuable in lifetime-limited missions), using two’s complement values for subtraction operations. The

multiplication and division operations will be performed on circuitry designed using logical and arithmetic shifters. Equality comparators are simple ANDs of a number of XNOR gates, which can be constructed from the NAND and NOR gates available in SiC JFET. Magnitude comparators are a variant of subtractors. All of these have well documented logical designs which can be applied to SiC systems.

Simple arithmetic circuits are used throughout the computer system. For example, operations are performed based on orders delivered by Operation Codes (Opcodes) from the program register. These instructions must be interpreted by the logic of the device by arithmetic means. For example, an adder is used to determine the address of the next instruction from the program counter, and a control ALU is utilized to compute the memory address of data to be operated upon by the CPU. With a working register established, it will be necessary to develop a way to utilize the register directly by furnishing it with operations. The development goal of designing a working ALU furthers the overarching goal of creating a working processor, as the individual components of the ALU are used in many places.

The first task of the ALU portion of this proposal is to demonstrate a simple half-adder circuit patterned in SiC. The half-adder will be fed alternating values of HIGH and LOW on both inputs to determine if a correct value is generated for the output and/or the carry of the circuit. The input for this circuit will be generated by an external microcontroller such as an Arduino prototyping board timed to send the signal pulses at regular intervals and check the answers. The Arduino will log the inputs, output, and carry from this circuit to check for errors. This experiment will be repeated in both standard conditions and harsh conditions in excess of 500 °C to simulate real operation. The Si based Arduino signal generation and logging can be isolated from the elevated temperature conditions since HIGH and LOW signals are not subject to the same trace length constraints as oscillators. Success of the circuit will be determined by continuous operation without errors with a lifetime to match previously explored logical units [30], discussed further in Section 5. The next task will be to scale up to an 8-bit full adder, then to a carry-lookahead adder which will be tested in the same manner.

Comparators and shifters will be tested in a similar “bottom-up” manner and constraints as the adder. For the comparator, initial tests will be performed on a simple 2-bit comparator, then scaled up to a full 8-bit comparator. The first bit shifter will be a simple array shifter of 2-bits, tested by cycling the bit shift by one unit over time. The scaled up version of the shifter will be tasked with performing full 8-bit shift operations. Tests will be performed at a range of temperature conditions and deemed successful for continuous operation without errors, similar to the other proposed units of the ALU.

4. EXPLANATION OF NEW OR UNUSUAL TECHNIQUES

The proposed work is unique in that it uses SiC for logical device fabrication. There are very few devices which use this technology, and use of substrate materials outside of Si in CMOS design is uncommon due to industry focus on small feature sizes and high computational power. While this is a new and exciting area of research, there will be few novel techniques implemented at this stage. The design flow for computers at the Si level is so well documented that many university level research institutions offer courses on the most up-to-date processes available. However, the technology for SiC devices is young compared to Si devices, many of these modern methods make use of architecture and design technology not prepared for the simplicity of SiC. Therefore, a “back-to-basics” approach is more suitable for this project. The “back-to-basics” approach will favor the use of the original VLSI work pioneered by Mead and Conway, and their contemporaries [31, 32, 33].

While much of the design for modern integrated circuits is handled by computational algorithms, few such mathematical models are available for the SiC substrate. The current state of circuit simulation makes use of NMOS SPICE models with certain parameters ignored [11]. Instead, a more traditional approach to device design must be considered. Masks for experimental devices will require manual generation based on traditional standard for VLSI device production pioneered by Mead and Conway [31]. Previous work by the SiC group at NASA has produced some important values for device modeling including size constraints. Physical constants observed in this work will be used to further develop a custom

technology profile for SiC in a VLSI design program such as MAGIC [28]. By recording these parameters, it is possible to approach the algorithmic simplicity enjoyed by traditional substrate devices, establishing Electronic Design Automation (EDA). The modularity and regularity inherent to the nature of computer design makes these values extremely valuable as the overarching project scales up. Furthermore, VLSI EDA programs can be used in conjunction with SPICE to simulate the designed circuits at the pattern level [34].

5. EXPECTED RESULTS AND THEIR SIGNIFICANCE AND APPLICATION

The qualifications for an individual circuit success were previously mentioned in Section 3. Generally, these success criteria can be divided into data retention time for register devices and continuous error-free operation time for ALU related devices. Some electronic properties are temperature dependent, such as resistance [19] and band-gap [35]. Therefore, it is critical to test circuits designed for optimal operation at one temperature over the range of possible operations temperatures. These tests are to be replicated at both standard temperatures and temperatures found in harsh conditions, such as the surface of Venus, using lab ovens.

A successful register is a device which can retain the stored data over many clock cycles, and change each bit in a timely manner on the rising edge of a single clock cycle. To determine the size of this clock cycle, we look to a reference point, such as a previous lander. The Sojourner Rover utilized a variant of the Intel 8085 chip, the 80C85, running at a clock speed of 2 MHz [36]. The manufacturer reported maximum clock speed of this CPU is 5 MHz [37]. Therefore, for the purposes of this test, the success factor will assume an acceptable operation speed of 2 MHz with an optimum operation speed of 5 MHz. If we assume that the bit stored in the flip-flop is either modified on each clock cycle or stored for the clock cycle, and we assume that the chance for a bit to be either 0 or 1 is equal, then we can be 99% confident the longest a bit will be stored in a single flip-flop is 7 clock cycles. Therefore, the produced register will be adequately successful if it can retain a bit for 350 ns and exceed success if it can retain a bit for 1.4 μ s.

A successful ALU is a device which can perform the requested operation quickly, with no errors. In a surface level lab with minimal radioactive sources, it should be expected that an adder or bit shifter would work consistently. However, no device is perfect, and chip manufacturers are hesitant to publish failure rates in their devices. Certain failure modes, such as electromigration, are tested for using temperature acceleration. However, the original draw of SiC circuits is the high temperature stability, reducing the likelihood of this failure path [38]. With the lack of benchmarks for ALU failure and the high temperature stability expectation which can accelerate further testing, the success metric will be based on the previous performance reported by the Hunter group, including a thousand hour lifetime of an oscillator at 500 °C [30]. The ALU produced in the course of the work in this proposal will be considered a success if the error-free lifetime exceeds 1000 h, the time reported by Spry et al.

In the event the devices fail to pass benchmarks for the register, ALU, or their preceding variants, efforts will be made to determine the cause of the issue. Previous circuit issues which have been a cause of concern in the past, such as the micropipe defects in SiC devices [38], have been analyzed in detail [39] based on “failed” experiments. This provides much needed data for future improvements on the material. Circuits which do not meet benchmark expectations will be analyzed by electron microscopic techniques for sources of damage, much like the previously mentioned failure was determined to be due to oxide cracking in the thousand hour test [30]. These sources of failure can provide more evidence to shed light on the cause of such defects in SiC systems.

The technology developed for this work has far-reaching applications. There have been few complicated logic devices made in SiC [30]. A successful register and ALU would open the doors to further development in this material, eventually leading to the eventual development of a single-cycle microprocessor CPU with high temperature and radiation resistance. Processors in this material would be very attractive for future space-faring missions and use in extreme terrestrial environments. The individual building blocks produced by this work can also be used as a basis for other SiC devices. For example, the development of a successful 8-bit register would naturally lead to the development of ROM and RAM with

similar configurations. The modularity and repeatability of these devices makes it relatively simple to drop a successful gate design from one project to the next. By designing these devices in a prevalent, open-source VLSI EDA environment, the parameters explored in these designs would be available to future designers working with this technology.

6. REFERENCES/CITATIONS

REFERENCES

- [1] R Herrick, K Baines, M Bullock, G Chin, B Grimm, W Kiefer, S Mackwell, K McGouldrick, B Sharpton, S Smerkar, and others. Goals Objectives and Investigations for Venus Exploration. *Venus Exploration Analysis Group (VEXAG)*, 2014.
- [2] T Kremic, GW Hunter, PG Neudeck, DJ Spry, GE Ponchak, GM Beheim, RS Okijie, MC Scardelletti, JD Wrbanek, DM Vento, and others. Long-Life In-Situ Solar System Explorer (LLISSE) Probe Concept and Enabling High Temperature Electronics. In *Lunar and Planetary Science Conference*, volume 48, 2017.
- [3] Donald M Hunten. *Venus*. University of Arizona Press, 1983.
- [4] Jeff Balcerski. Venus Science Priorities for Laboratory Measurements and Instrument Definition Workshop Report. Technical report, National Institute of Aerospace, Langley, VA, April 2015.
- [5] H. J. Round. A Note on Carborundum. *Electrical World*, 49(6):309, February 1907.
- [6] O. V. Losev. Luminous carborundum detector and detection with crystals. *Telegrafiya i Telefoniya bez Provodov*, 44, 1927.
- [7] R. Siemienieć and U. Kirchner. The 1200V direct-driven SiC JFET power switch. In *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, pages 1–10, August 2011.

- [8] K. Mino, S. Herold, and J. W. Kolar. A gate drive circuit for silicon carbide JFET. In *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, volume 2, pages 1162–1166 Vol.2, November 2003.
- [9] M.J. Krasowski. *N Channel JFET Based Digital Logic Gate Structure*. Google Patents, March 2010.
- [10] H. Habib, N.G. Wright, and A.B. Horsfall. Complementary JFET Logic for Low-Power Applications in Extreme Environments. In *Silicon Carbide and Related Materials 2012*, volume 740 of *Materials Science Forum*, pages 1052–1055. Trans Tech Publications, March 2013.
- [11] Phillip G. Neudeck, David J. Spry, and Liangyu Chen. First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits, May 2016.
- [12] Vera Haase, Gerhard Kirschstein, Hildegard List, Sigrid Ruprecht, Raymond Sangster, Friedrich Schröder, Wolfgang Töpfer, Hans Vanecek, Werner Heit, Jürgen Schlichting, and Hartmut Katscher. The Si-C Phase Diagram. In Vera Haase, Gerhard Kirschstein, Hildegard List, Sigrid Ruprecht, Raymond Sangster, Friedrich Schröder, Wolfgang Töpfer, Hans Vanecek, Werner Heit, Jürgen Schlichting, Hartmut Katscher, Raymond Sangster, and Friedrich Schröder, editors, *Si Silicon: System Si-C. SiC: Natural Occurrence. Preparation and Manufacturing Chemistry. Special Forms. Manufacture. Electrochemical Properties. Chemical Reactions. Applications. Ternary and Higher Systems with Si and C*, pages 1–5. Springer Berlin Heidelberg, Berlin, Heidelberg, 1985.
- [13] V.E. Chelnokov and A.L. Syркин. High temperature electronics using SiC: Actual situation and unsolved problems. *E-MRS 1996 Spring Meeting, Symposium A: High Temperature Electronics: Materials, Devices and Applications*, 46(1):248–253, April 1997.

- [14] Pasqualina M Sarro. Silicon carbide as a new MEMS technology. *Sensors and Actuators A: Physical*, 82(1–3):210–218, May 2000.
- [15] R. S. Okojie, C. Blaha, D. Lukco, V. Nguyen, and E. Savrun. Zero offset drift suppression in SiC pressure sensors at 600 x00B0C. In *2010 IEEE Sensors*, pages 2269–2274, November 2010.
- [16] C. E. Weitzel, J. W. Palmour, C. H. Carter, K. Moore, K. K. Nordquist, S. Allen, C. Thero, and M. Bhatnagar. Silicon carbide high-power devices. *IEEE Transactions on Electron Devices*, 43(10):1732–1741, October 1996.
- [17] J. M. McGarrity, F. B. McLean, W. M. DeLancey, J. Palmour, C. Carter, J. Edmond, and R. E. Oakley. Silicon carbide JFET radiation response. *IEEE Transactions on Nuclear Science*, 39(6):1974–1981, December 1992.
- [18] Quming Zhou and Kartic Mohanram. Transistor sizing for radiation hardening. In *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, pages 310–315. IEEE, 2004.
- [19] Philip G Neudeck, David J Spry, and Liang-Yu Chen. First-order SPICE modeling of extreme-temperature 4H-SiC JFET integrated circuits. *Additional Papers and Presentations*, 2016(HiTEC):000263–000271, 2016.
- [20] Philip G Neudeck, David J Spry, and Liangyu Chen. Experimental and theoretical study of 4H-SiC JFET threshold voltage body bias effect from 25° C to 500° C. 2015.
- [21] Wesley T. Honeycutt. *Development and Applications of Chemical Sensors for the Detection of Atmospheric Carbon Dioxide and Methane*. Dissertation, Oklahoma State University, Stillwater, Oklahoma, May 2017.

- [22] Wesley T. Honeycutt, M. Tyler Ley, and Nicholas F. Materer. A Comparison of the Properties of Selected Commercially Available, Low-cost Carbon Dioxide and Methane Gas Concentration Sensors. *Sensors Journal IEEE*, 2017 [Submitted].
- [23] Raheleh Hedayati, Luigia Lanni, Bengt Gunnar Malm, Ana Rusu, and Carl-Mikael Zetterling. A 500° C 8-b Digital-to-Analog Converter in Silicon Carbide Bipolar Technology. *IEEE Transactions on Electron Devices*, 63(9):3445–3450, 2016.
- [24] Saleh Kargarrazi, Luigia Lanni, Stefano Saggini, Ana Rusu, and Carl-Mikael Zetterling. 500° C bipolar SiC linear voltage regulator. *IEEE Transactions on Electron Devices*, 62(6):1953–1957, 2015.
- [25] Intel Corporation. *8080/8085 Assembly Language Programming Manual*. Intel Corporation, Santa Clara, 1978.
- [26] David Harris and Sarah Harris. *Digital Design and Computer Architecture*. Elsevier, 2012.
- [27] David A. Patterson and John L. Hennessy. *Computer Organization and Design: The Hardware/Software Interface*. Newnes, 2013.
- [28] John K Ousterhout, Gordon T Hamachi, Robert N Mayo, Walter S Scott, and George S Taylor. The magic VLSI layout system. *IEEE Design & Test of Computers*, 2(1):19–30, 1985.
- [29] Brajesh Kumar Kaushik, Sankar Sarkar, and R.P. Agarwal. Waveform analysis and delay prediction for a CMOS gate driving RLC interconnect load. *System-Level Interconnect Prediction*, 40(4):394–405, July 2007.
- [30] David J Spry, Philip G Neudeck, Liang-Yu Chen, Dorothy Lukco, Carl W Chang, Glenn M Beheim, Michael J Krasowski, and Norman F Prokop. Processing and characterization

- of thousand-hour 500° C durable 4H-SiC JFET integrated circuits. *Additional Papers and Presentations*, 2016(HiTEC):000249–000256, 2016.
- [31] Carver Mead and Lynn Conway. *Introduction to VLSI Systems*, volume 1080. Addison-Wesley Reading, MA, 1980.
- [32] Douglas A. Pucknell and Kamran Eshraghian. *Basic VLSI Design: Systems and Circuits*. Prentice-Hall, Inc., 1988.
- [33] Michael Slater. *Microprocessor-Based Design: A Comprehensive Guide to Effective Hardware Design*. Prentice-Hall, Inc., 1987.
- [34] Laurence W. Nagel and D.O. Pederson. SPICE (Simulation Program with Integrated Circuit Emphasis). Technical report, EECS Department, University of California, Berkeley, April 1973.
- [35] Y. P. Varshni. Temperature dependence of the energy gap in semiconductors. *Physica*, 34(1):149 – 154, 1967.
- [36] null. Mars Pathfinder FAQs - Sojourner. https://mars.nasa.gov/MPF/rover/faqs_sojourner.html#cpu, April 1997.
- [37] OKI Semiconductor. MSM80C85AHRG/GS/JS, January 1998.
- [38] J. B. Casady and R. W. Johnson. Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review. *Solid-State Electronics*, 39(10):1409 – 1422, 1996.
- [39] P. G. Neudeck and J. A. Powell. Performance limiting micropipe defects in silicon carbide wafers. *IEEE Electron Device Letters*, 15(2):63–65, February 1994.