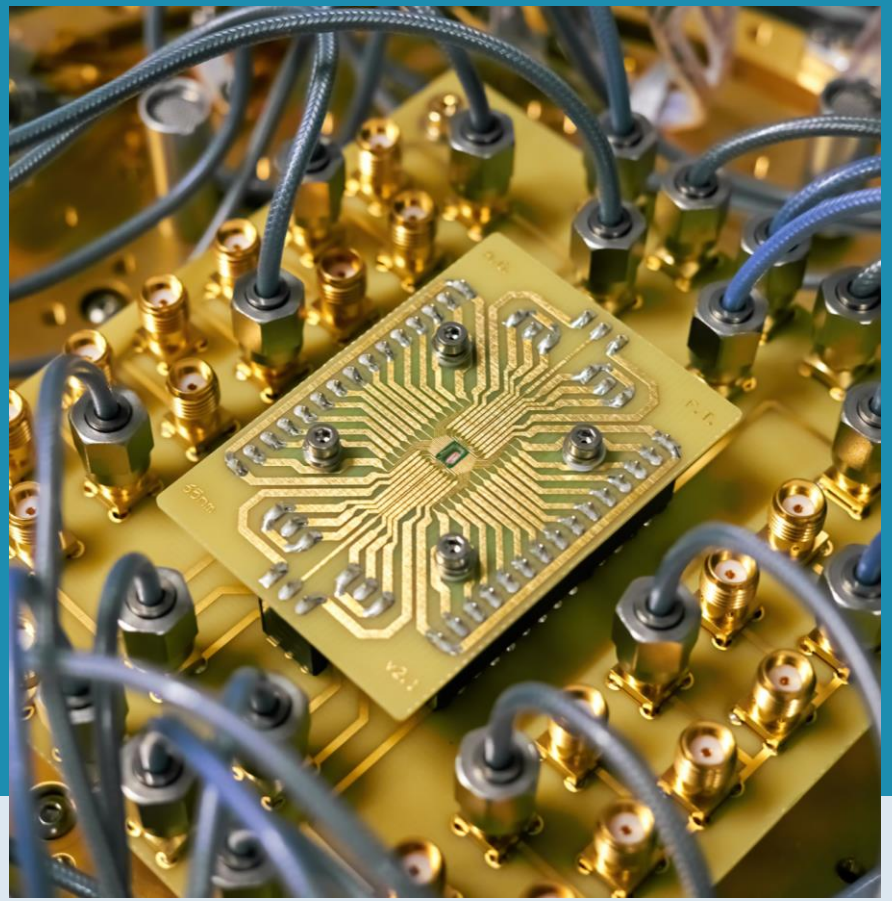
KU LEUVEN

Design of Analog and Mixed-Signal Integrated Circuits B-KUL-H05E3A

Design Project Introduction



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KU LEUVEN

DAMSIC

Filip Tavernier

Tim Piessens

Professors

Teaching Assistants

Alberto

Jun

Shuangmu

Prayag

DAMSIC

Professors

- Many topics + many slides
- Oral exam (10/20 points)

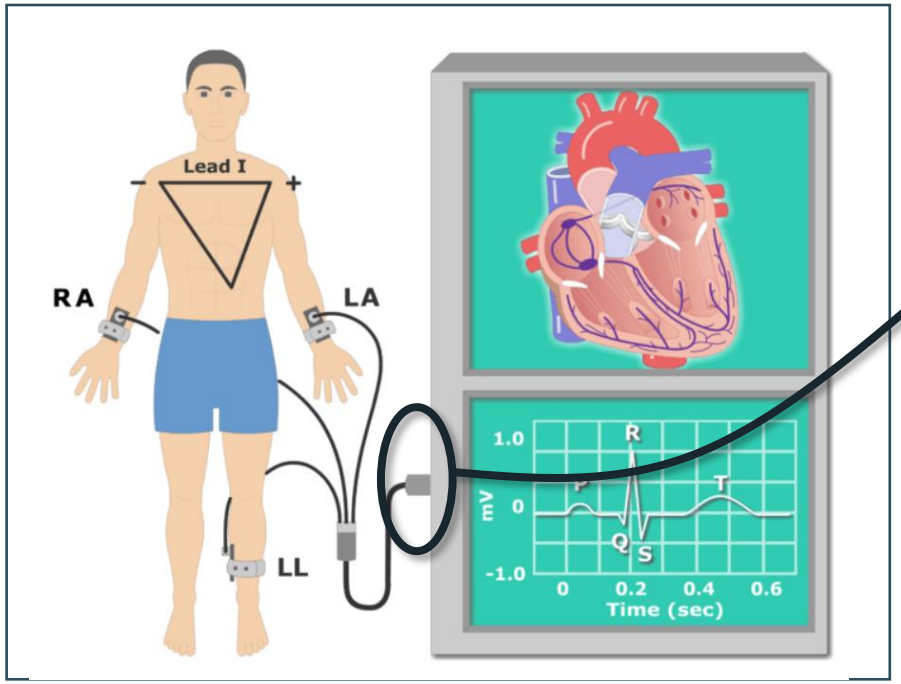
Teaching Assistants

- Exercise Sessions
- 8 sessions + Presentation
- Design Project
- Evaluation (10/20 points)
  - Results (5/20) report
  - Insight (5/20) oral presentation

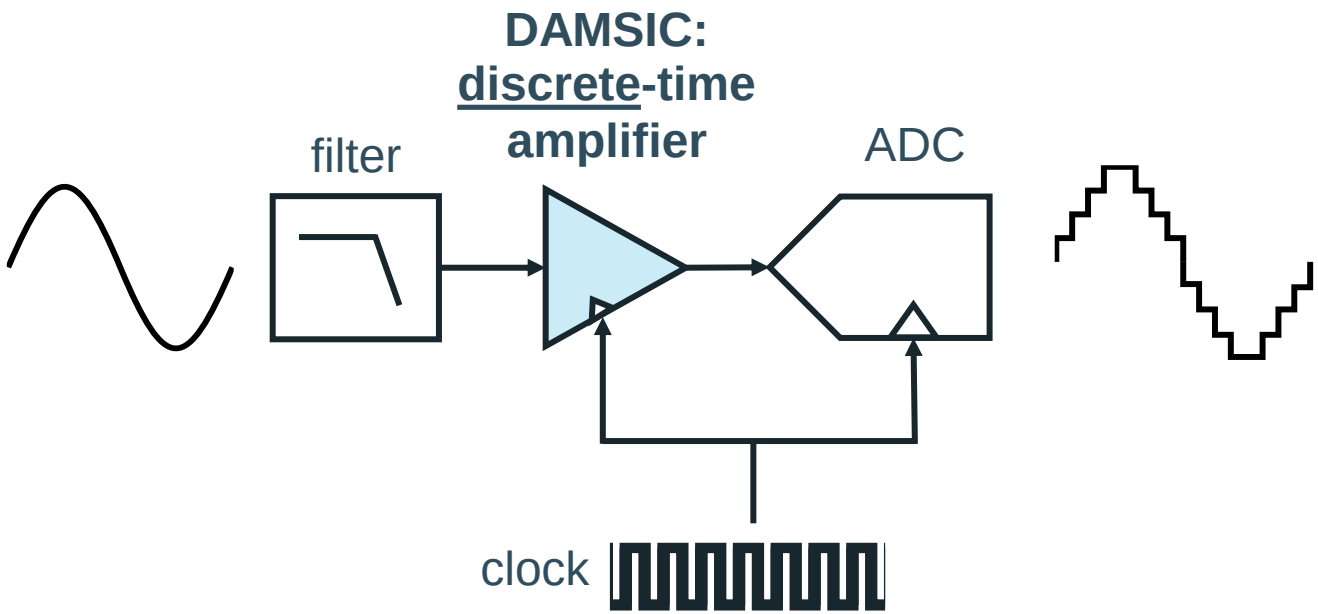
The DAMSIC project

What is it?

Your job: front-end of a high-performance sensor

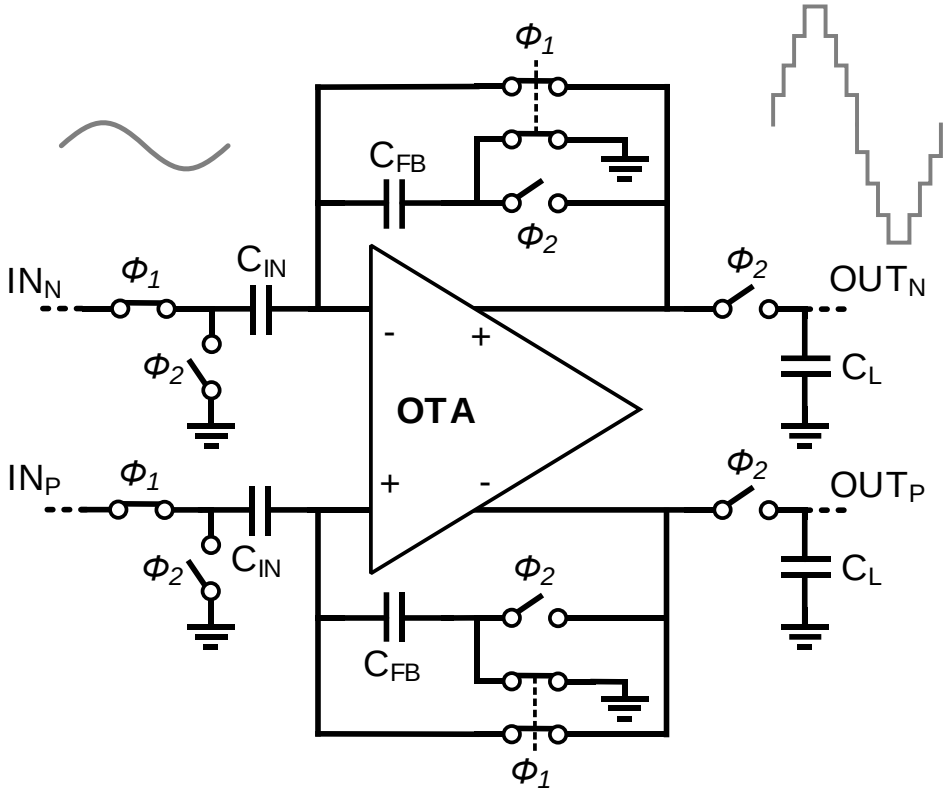


[https://www.getbodysmart.com/electrical-activity-heart/ekg/]



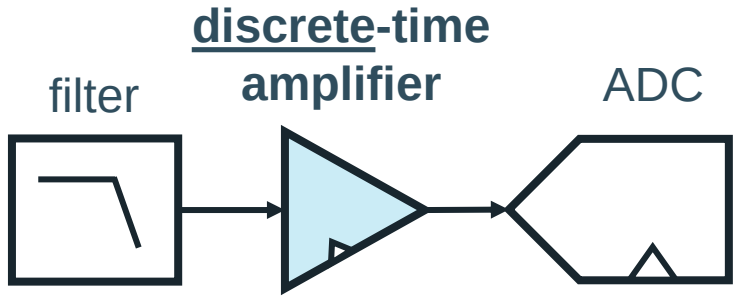
Design project goal

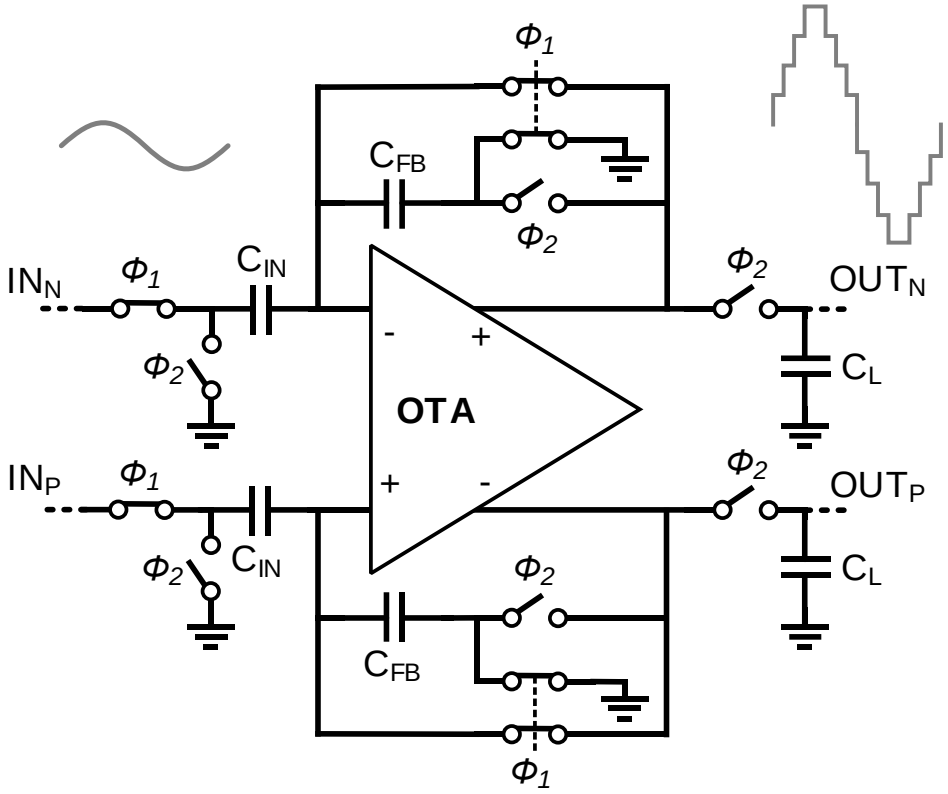
- First real design experience, follow-up to DIAC
  - Fundamental basics
  - Application specifications
  - **Switched-capacitor amplifier**
  - Deriving building block specifications
  - Design
  - Check application



Specifications

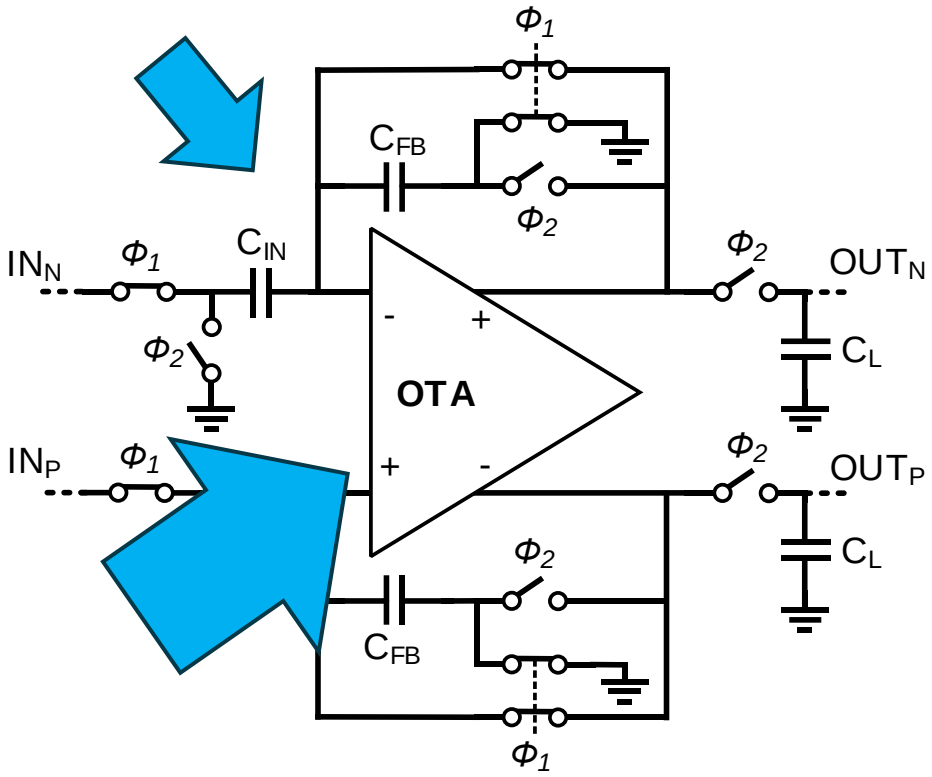
- Given to you, related to application
- Switched-capacitor amplifier
  - Gain
  - Sample phase
  - Amplification phase
  - Settling error
  - Stability





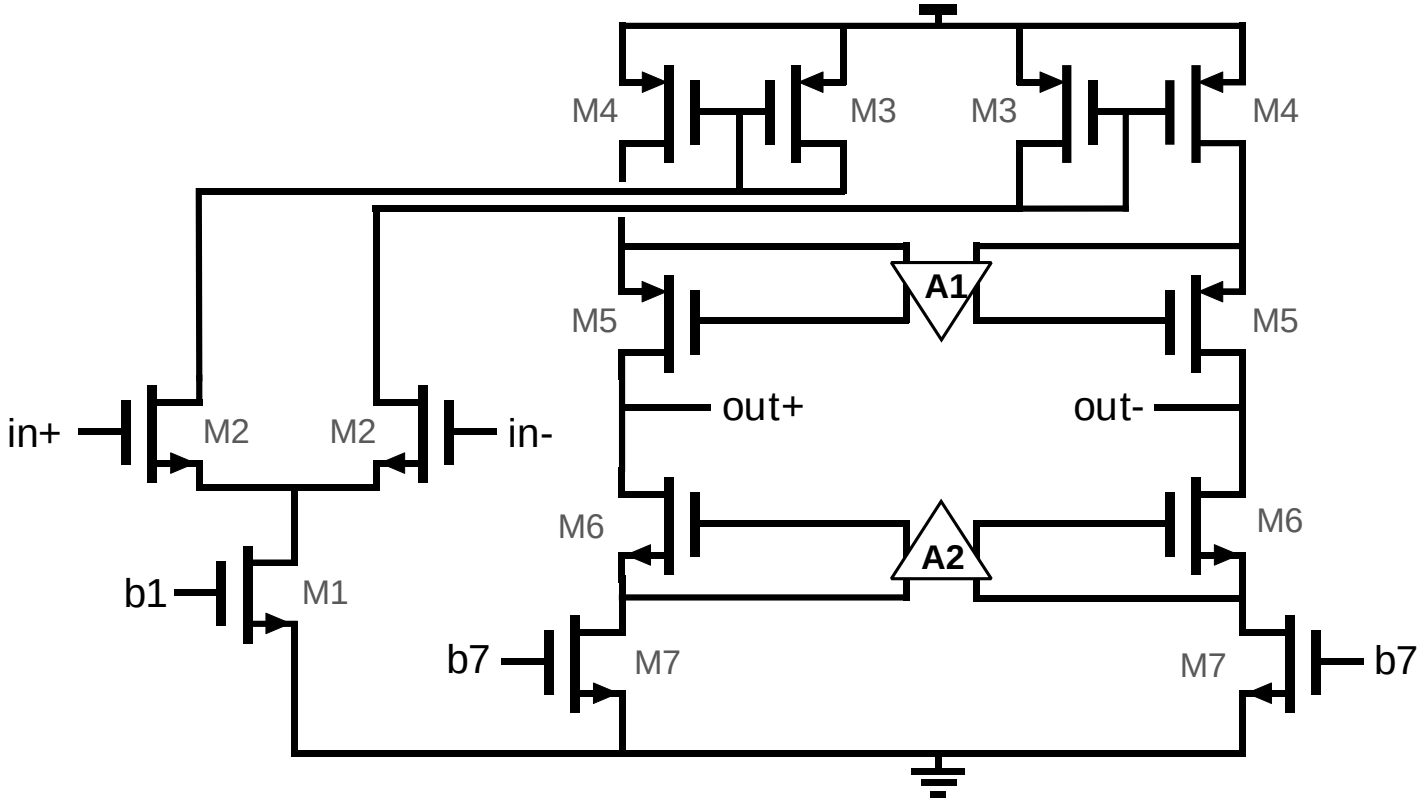
Building blocks' design

- Switches, clocks, capacitors
- **OTA → key block specfications**
  - Simulations at block-level
  - A_{DC}, GBW, BW, PM …



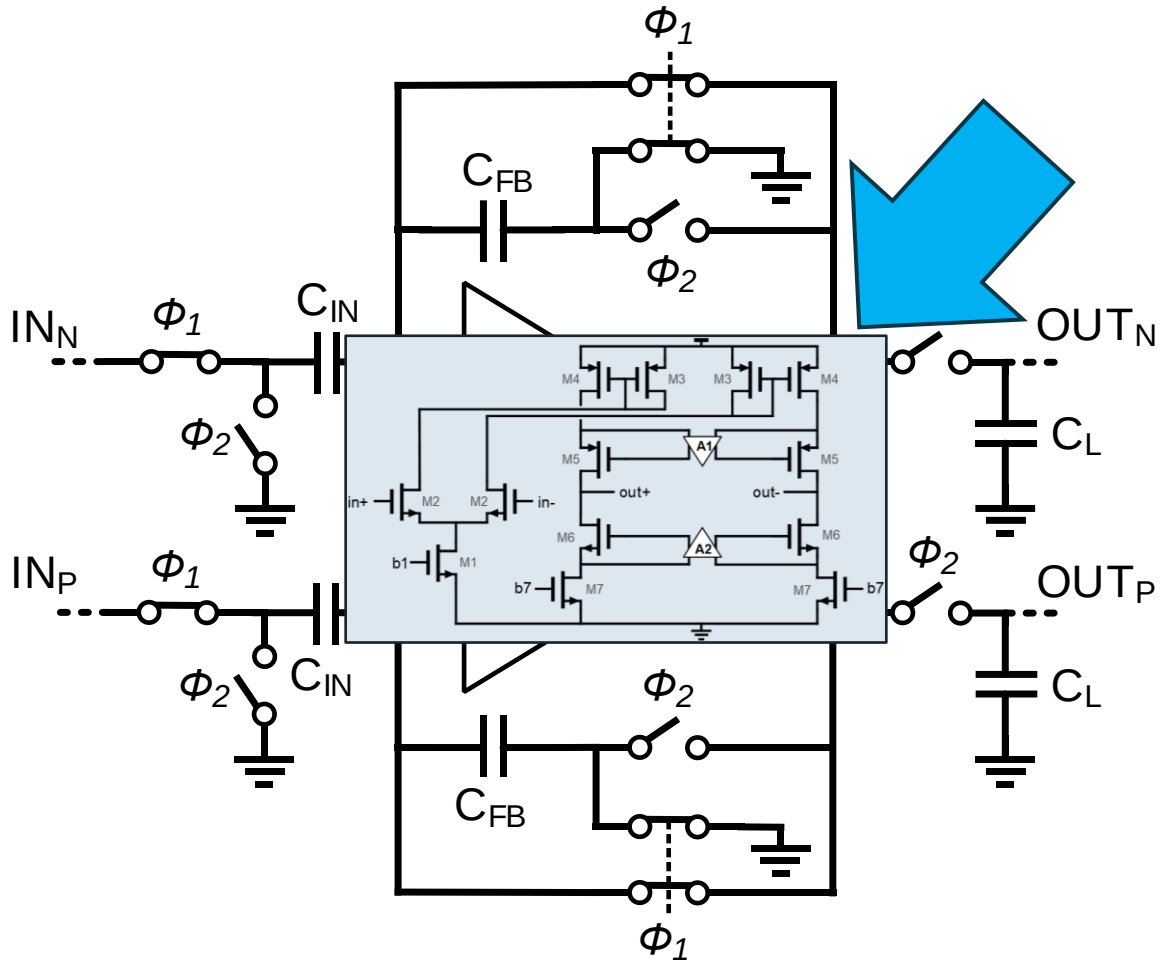
Transistor-level design

- The ‘real work’
- SNR, GBW, BW, PM, …
  - gm, r_{OUT}, I_{DS}, C_{PAR} etc. → W/L, DC-biasing, VTH etc.
- Three OTA designs
  - Two-stage (just in first weeks)
  - Symmetric (not for final)
  - Gain-boosted (final)



Finally: performance check

- Go back to high level and check the performance
- Specifications met? power cost? …
- Improvements?
- If time allows: extra design



Steps and timeline

Overall setup of the design sessions

- **4 steps** of design
  - Mini-lectures
  - Syllabus (booklet) + Toledo
- Assessed: report + presentation

Step 1 (Sessions 1 and 2)

- **Enroll on Toledo as a group of two**
- **Set-up workspace**
  - Toledo → [H05E4a] → Documents → Assignment
  - Configure Cadence Virtuoso with 45nm predictive PDK
- Mini lecture on *continuous time feedback*
- Mini lecture on *discrete-time and project simulations*

Step 1 (Sessions 1 and 2)

- **Refresh on feedback theory**
  - Follow mini-lecture
  - Experiment with two-stage OTA, exercises given in syllabus
- **Specs calculation (discrete-time)**
  - Application specs → OTA specs
  - Each group has their own specs (see Toledo)
  - Hand calculations
  - Check with ideal OTA

Step 2 (Session 3)

- Finalize block specifications
- **Run simulation of full system** with “ideal OTA” (given)
- Mini-lecture on *circuit design method: gm/I_D*

Step 3 (Sessions 4 and 5)

- **Design folded cascode OTA**
- Important: how to design the OTA
  - How to do it in advanced PDKs?
  - What are the limitations of the current topology?
    - We do not expect you to meet all specifications at this stage
    - BUT we want you to try so that you know what are the limits of this topology and this technology

Step 3 (Sessions 4 and 5)

- Intermediate deliverable by 10/03 (after Session 4)
  - Toledo → Deliverables
    - Mostly schematics and plots
    - Template is available
  - Not graded but highly recommended
    - TA feedback in Session 5

Step 4 (Sessions 6, 7 and 8)

- **Design the folded cascode OTA with gain-boosting**
- Mini-lecture on gain-boosting
- Intermediate deliverable by 24/03 (after Session 6)
  - Feedback on design in Session 7

Report

- Toledo → Deliverables
- Merge the three templates (Part I, II & III)
  - You may adapt the contents for the final deliverable if you made some changes from what have been submitted before
- Due 2nd of May
- Graded 5 out of 20 points for DAMSIC

Presentation

- 5’ Presentation + 10’ Q&A @ 9th of May 2025, Friday (in B02.50)
  - Other details or changes in details will be posted in Toledo
- Show your design process, not a summary of achieved results
  - To know **how you designed** your circuit, why did you make **your design decisions**
- **Both members** should know what’s happening in their design
  - It is possible for members in the same group to have different grades
- Graded on 5 out of 20 points for DAMSIC

Schedule overview

Session	Day	Session Topic	Mini-lecture	Deliverable
1	14/02	Cont. time OTA in feedback	Intro + CT OTA	
2	21/02	Project specification + discrete time	DT OTA + simulations	
3	28/02	Full system + design	gm/I_D design	
4	07/03	Folded-cascode design		Before #5
5	11/03	Folded-cascode design		
6	21/03	Gain-boosted OTA design	Gain boosting	Before #7
7	25/03	Gain-boosted OTA design		
8	28/03	Gain-boosted OTA design		**Final by 02/05**
Exam	**09/05**	Presentation + Q&A, details will follow		

How to work, in practice

Sessions and discussions

- Follow the syllabus and Toledo material when uploaded
- Attending sessions is key for success → TAs & your peers
- At the start of each session, discussions or tips/tricks may be discussed based on your progress
- TA discussions with groups will happen in the sessions after you have submitted the reports

Contacting TAs

- Do **not** email TAs about questions regarding the project (e.g. simulation errors, clarifications, concepts)
- **Use the Discussion Forum on Toledo**
  - Often, you are not the only one with that question
  - Other students might have already solved your problem
  - Answer eachother in the forum

Cadence

- It is extremely expensive (industry-standard, monopoly)
  - ESAT doesn't have infinite licenses
    - There are >60 of you (as of writing)
  - Not everyone can use it simultaneously

- Close you schematics when not in use!
- Never open Virtuoso twice on the same account
  - Think about your fellow students and thesis students!

Cadence and simulations

- Tutorials, schematic views, maestro views, and other block are already provided to you
- TAs have spent time to prepare this, so please look into this
  - Based on experience, answers to some of the students' simulation questions are already in the documents we have uploaded

Summary

Summary

- You goal: design OTAs for a switched-capacitor amplifier
- A timeline was provided: make sure you don’t get too far behind
- Intermediate reports will not be graded but recommended, you will be compiling them for your final report → presentation
- TAs can only be contacted via the sessions and Toledo forum

Questions? + short ~10 min. break ☺

- Form a group of 2 → enroll on Toledo (“Groups”)
- Download the project syllabus, first slides
- From syllabus: follow instructions to get DAMSIC Cadence library started

- After break, Prayag will cover some feedback design exercises (i.e. syllabus section 2)