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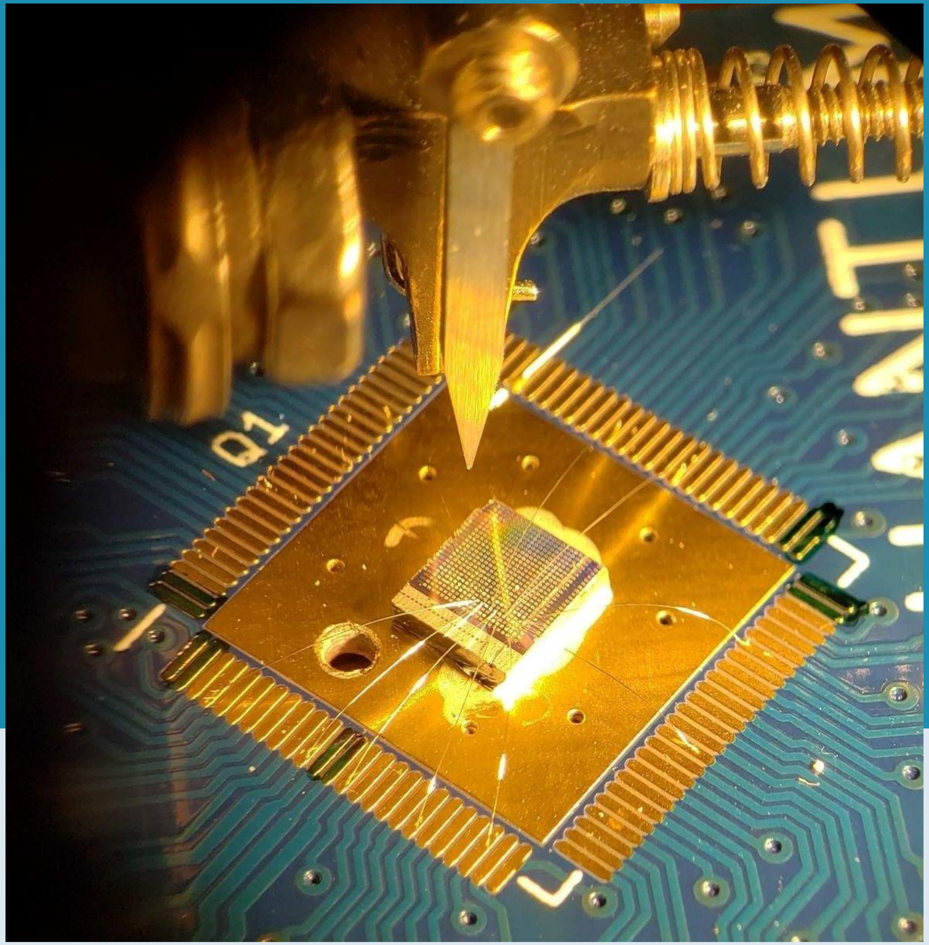
Design of Analog and Mixed-Signal Integrated Circuits B-KUL-H05E3A

Simulation Demo’s
STB, PSS+PNOISE, PAC



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Overview

- These slides show **how to setup simulations** for
  1. Stability ➔ STB simulation
  2. Noise ➔ PSS + PNOISE simulation
  3. Accuracy ➔ PAC simulation
- We also provide some **demo's** so you can try for yourself

- Note: we skip basic transient and AC simulations, these are **crucial** for stability and accuracy simulations though! See syllabus appendix, if needed

STABILITY LOOP GAIN SIMULATION SETUP AND DEMO

Stability simulation: what's needed?

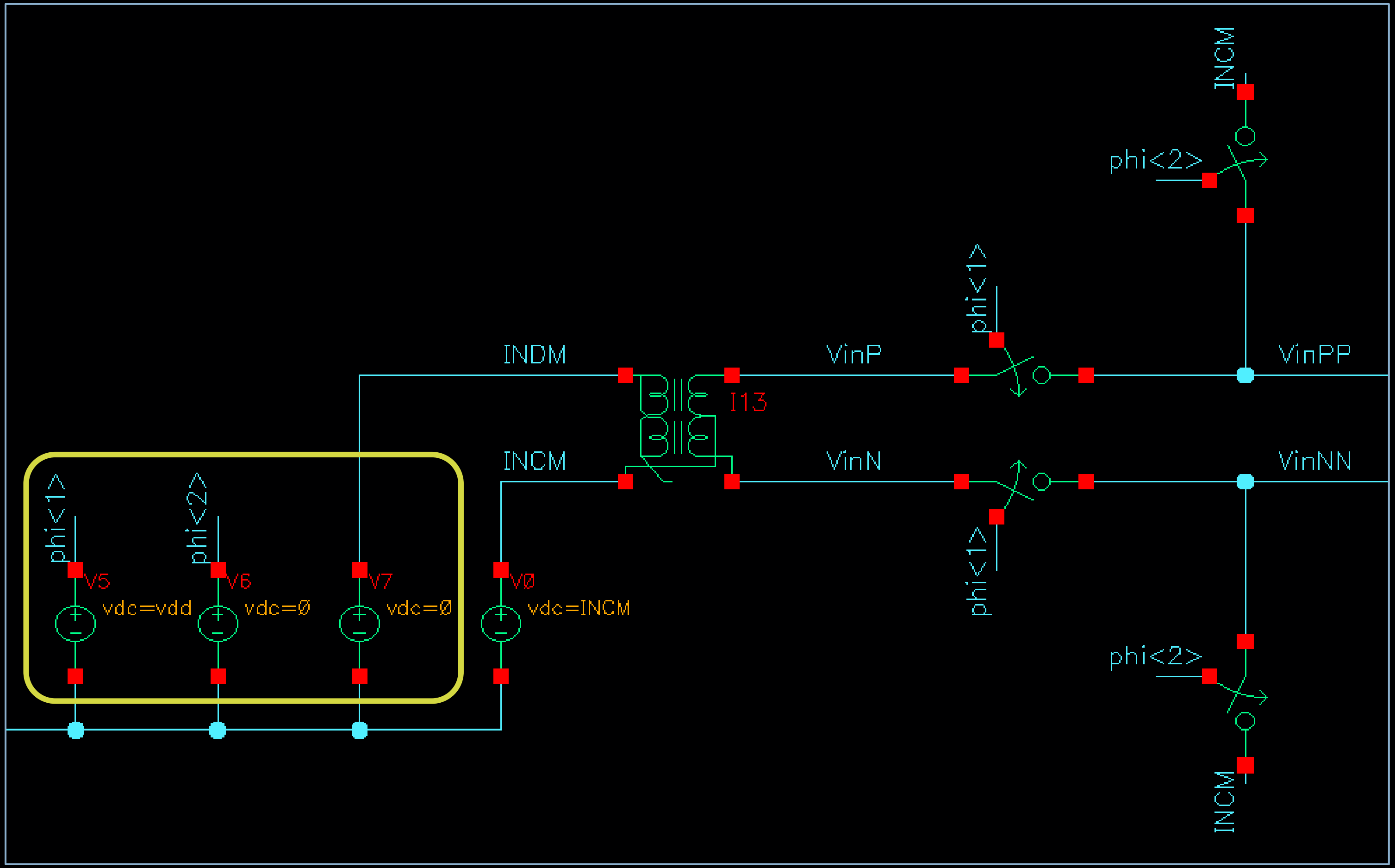
- An STB analysis assumes a single **operating point**
  - "Steady-state solution"

- So, you must force your switch-cap system in a single state first

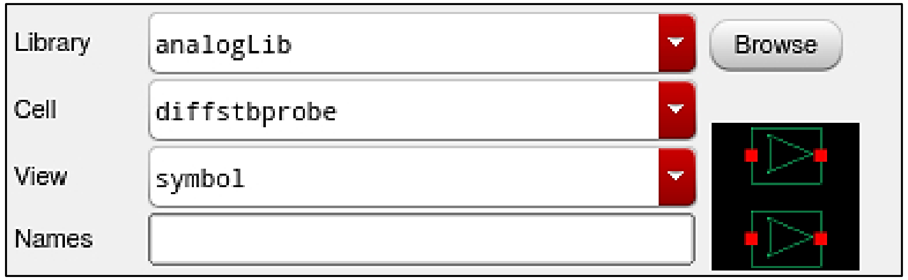
- In this system, you should force it into the **sample** phase
  - Hardest to get stable (unity feedback)
  - Also, the other phase doesn't bias the input of the OTA in steady-state..

Modifying the testbench for STB

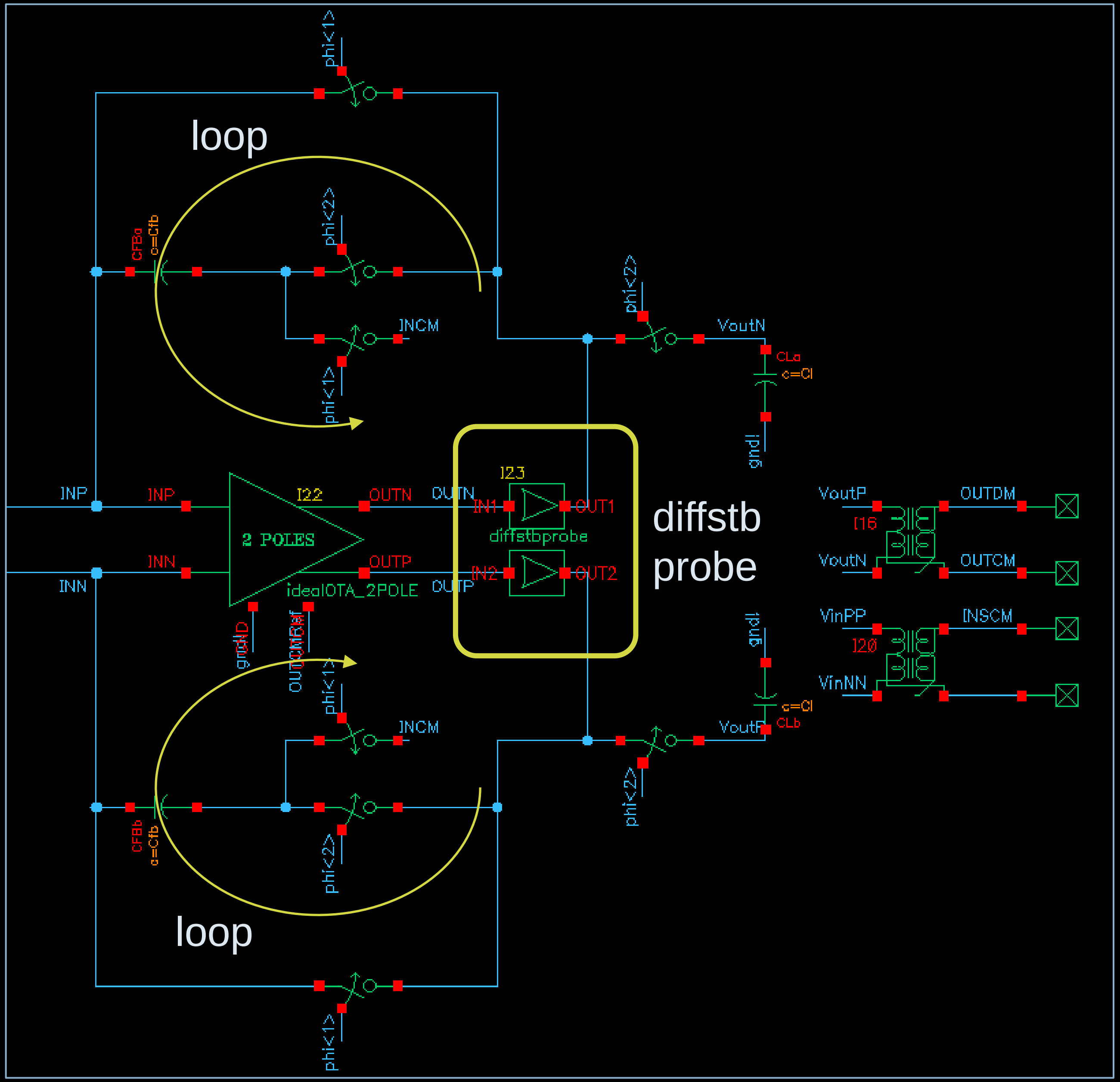
1. Copy the standard transient testbench
2. Modify to force the sampling phase
3. Make the differential input 0V too, since this is not an AC or transient simulation



diffstbprobe



- You also need to insert a “diffstbprobe”
  - Differential stability probe
- It must completely break your loop of interest
- In this example, we have an ideal 2-pole OTA which doesn’t have common-mode feedback. There’s only one differential feedback loop.

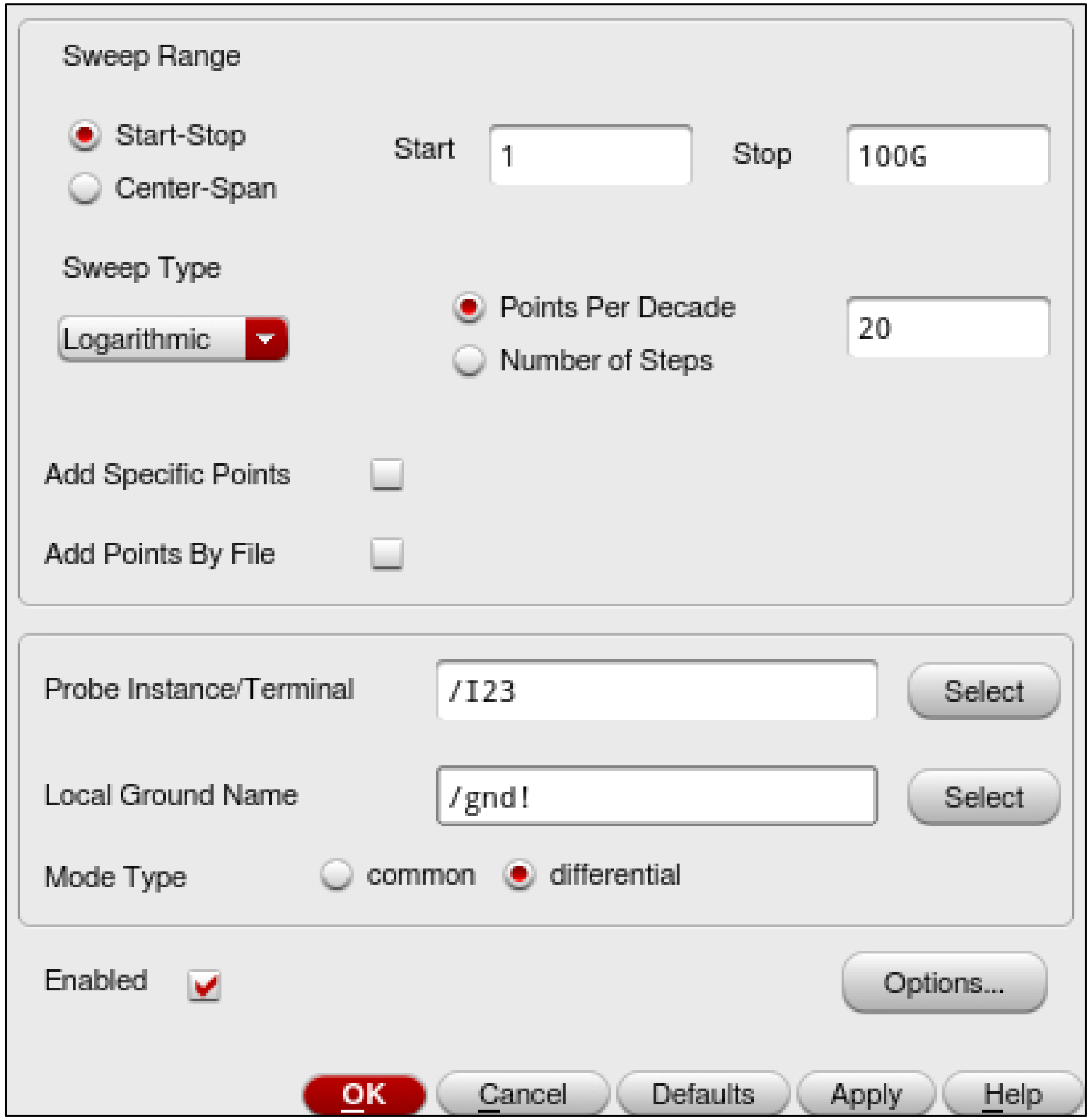


Modifying the testbench for STB

- Easiest location here: output of the OTA
- In the future you will have multiple feedback loops, resulting in multiple options

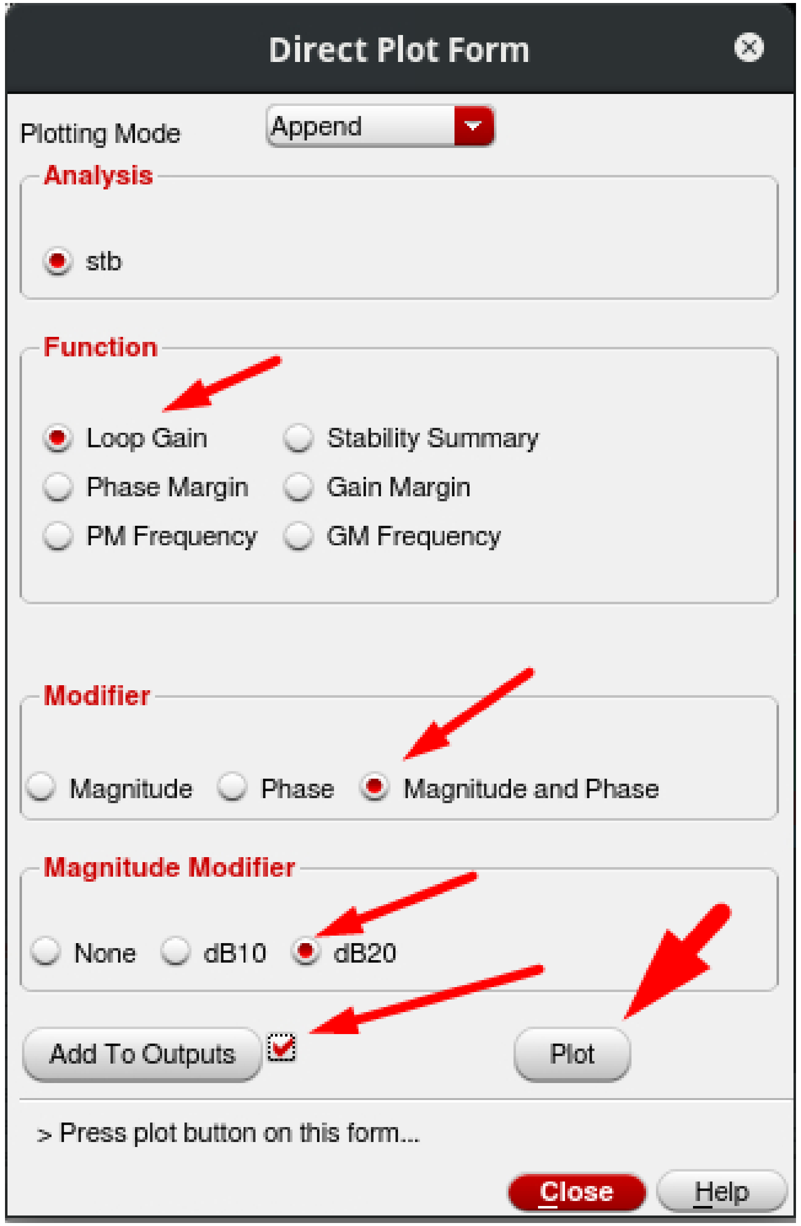
Simulation setup

1. Launch new) ADE Explorer view
2. Add analysis: choose “stb” and pick a frequency sweep (to get bode plot of loop gain)
3. “Probe Instance” = the diffstbprobe you inserted
4. Local Ground Name = /gnd!
5. Finish setting up design variables ➔ run!



Plotting STB's result

1. In ADE: Results > Direct Plot > Main Form ..
2. You can plot either Loop Gain bode plot, or just print the Stability Summary
3. Check "Add To Outputs" to push the expression to ADE, so you can re-use ☺
   - You could do the same for Phase Margin or Gain Margin options of the Direct Plot Form

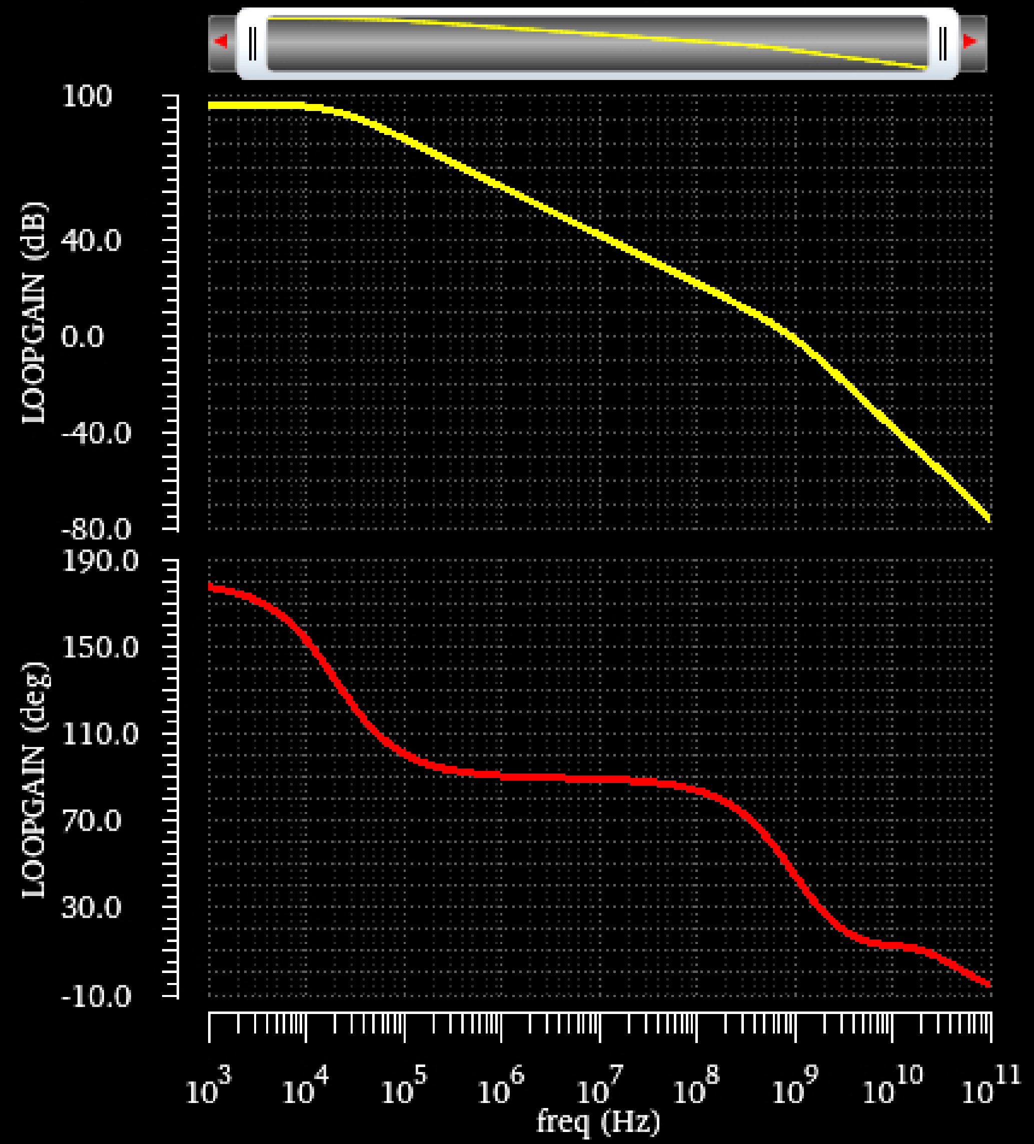


Demo 1: “demo_SCAMPLIFIER_STB_TB”

- We’ve modified the testbench schematic as described
- We’ve replaced the idealOTA by a 2-pole idealOTA
  - It has an extra gm-C stage, where gm = 1 and C = CP2 (variable)
  - So, an extra pole will be placed at roughly 1/(2π*CP2)
- The maestro view is already setup with design variables and a second pole that is close to the dominant unity-gain frequency
  - What is the phase margin?
  - Could you place the same OTA in a transient to see the predicted instability?

Demo 1 example

Cfb	0.2p
Cin	2p
Cl	2p
gm_OTA	25m
ro_OTA	2.5M
C_OTA	1p
F_POLE2	1G
CP2	1/(6.28*F_POLE2)
INCM	0.5
OUTCMRef	0.5
ron	5
vdd	1.1



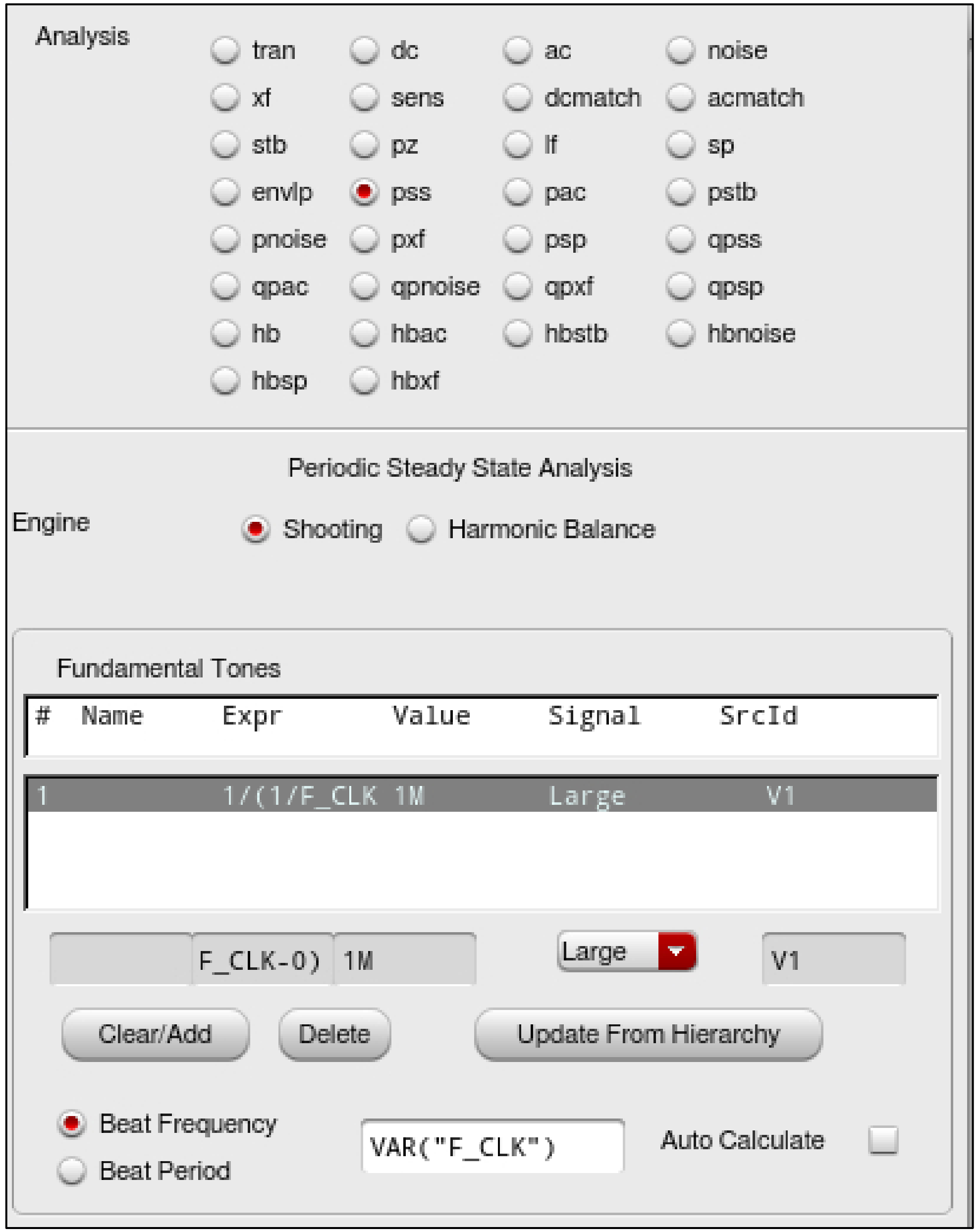
PSS + PNOISE
SIMULATION SETUP AND DEMO

PSS simulation and setup (1)

- Periodic steady state analysis
- It computes the **steady states vs. time** in your circuit within one period (normal AC sim = just one steady state)
- To keep simulation time low, we **disable the input sine wave** in the schematic ➔ the “period” will be limited by the clock
  - Trade-off for accuracy, generally OK for this kind of design in DAMSIC
  - You can set the input sine wave frequency to 0 Hz, Cadence treats it as DC source then

PSS setup (2)

1. Add PSS analysis
2. Shooting engine
3. Beat Frequency:
   - It's the period in which PSS perform analysis
   - Set equal to clock frequency variable
   - Or: Auto Calculate (will be same result)



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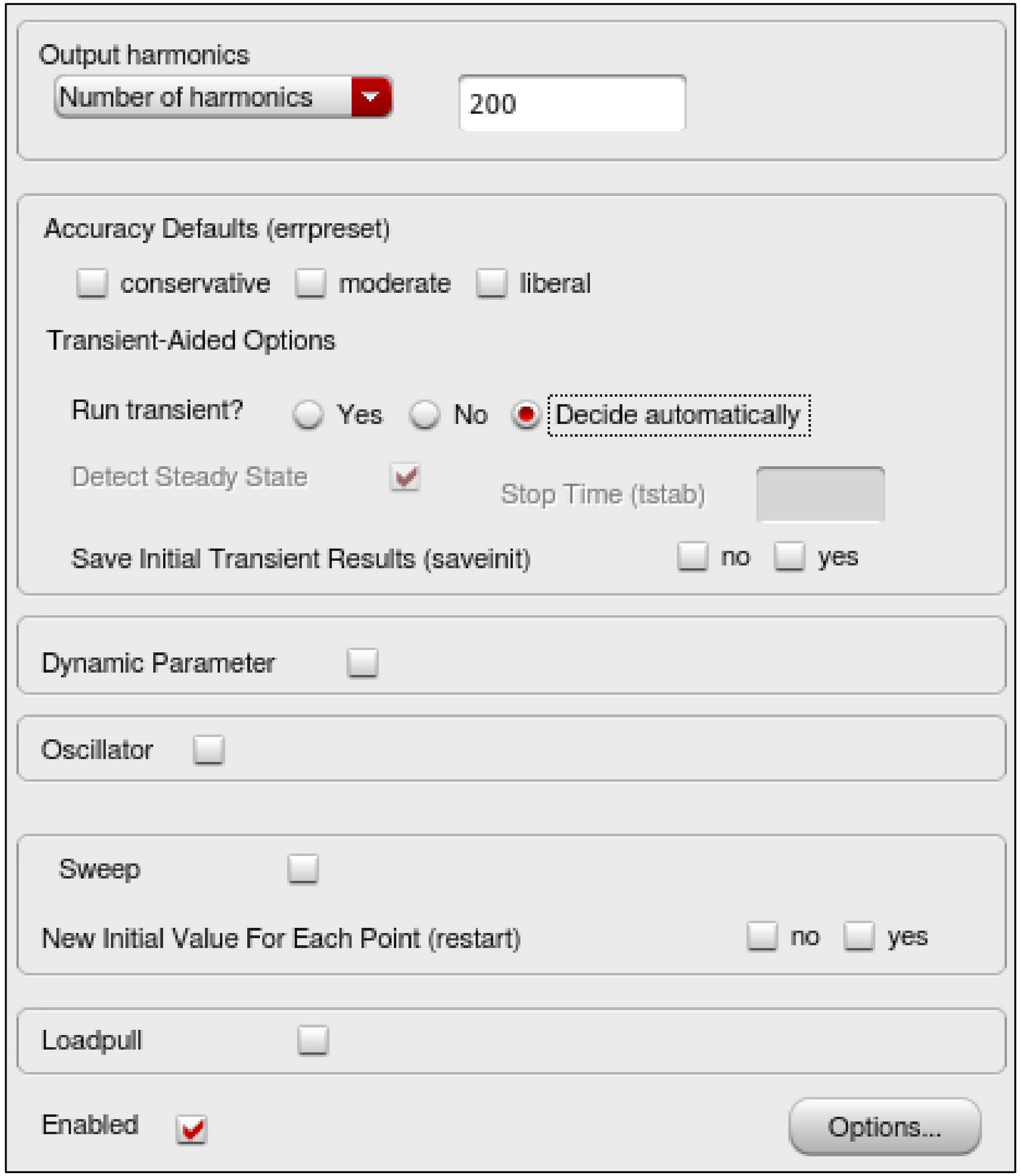
PSS setup (3)

1. Make number of harmonics into 100’s (trade-off with accuracy)
   - It sets the f_{MAX} considered by PSS
   - Above a certain amount, it will make no difference anymore (no extra noise)
   - Usually, 200 is good enough
2. Transient: decide automatically
   - Helps PSS to converge



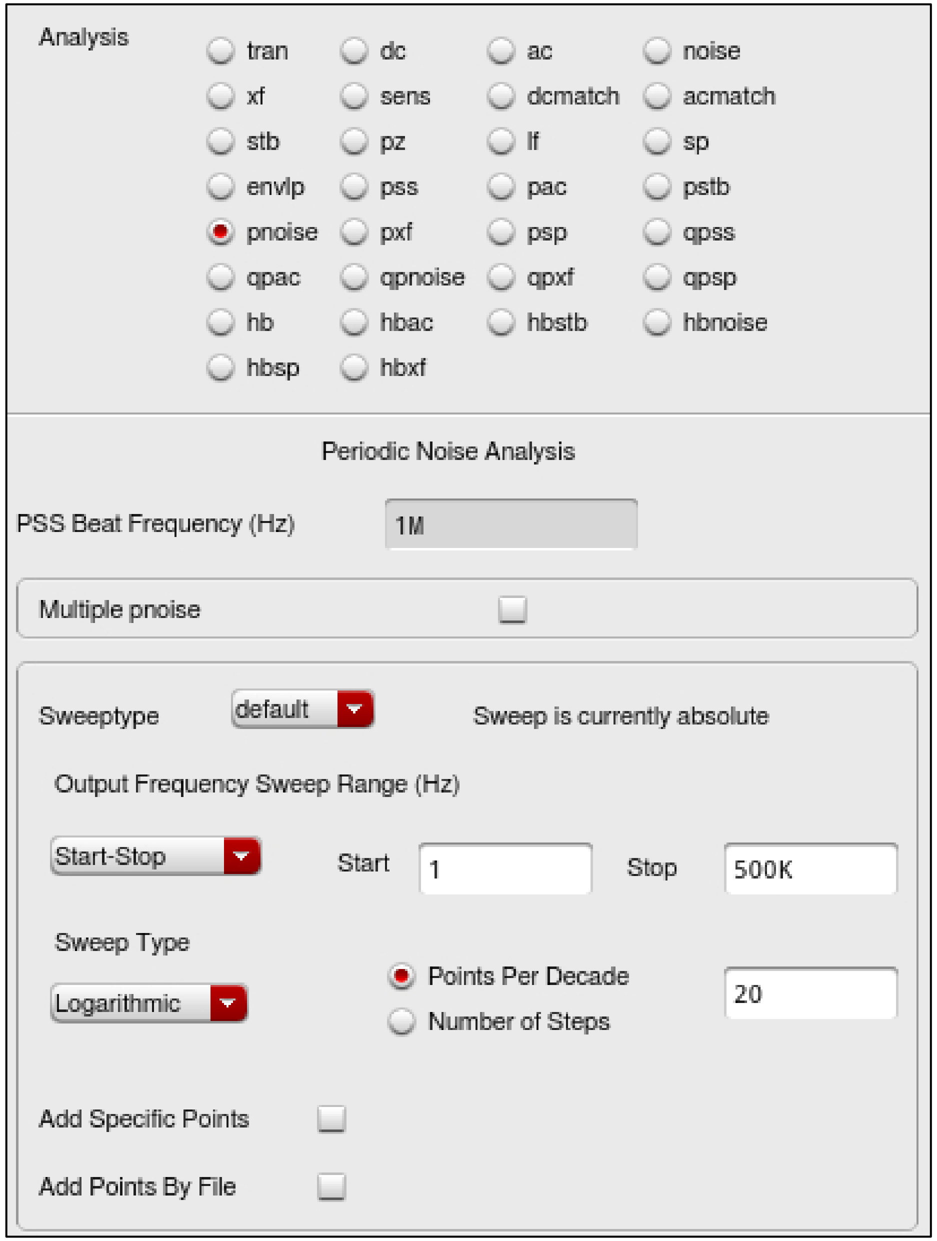
PNOISE simulation

- Periodic noise analysis
- It uses the steady-states computed by PSS to find either:
  - A time-average noise spectrum at the output, OR
  - Noise spectrum at the output at specific times
- We want the latter (i.e. after amplification phase)
- We integrate the noise spectrum to obtain the RMS noise voltage

PNOISE setup (1)

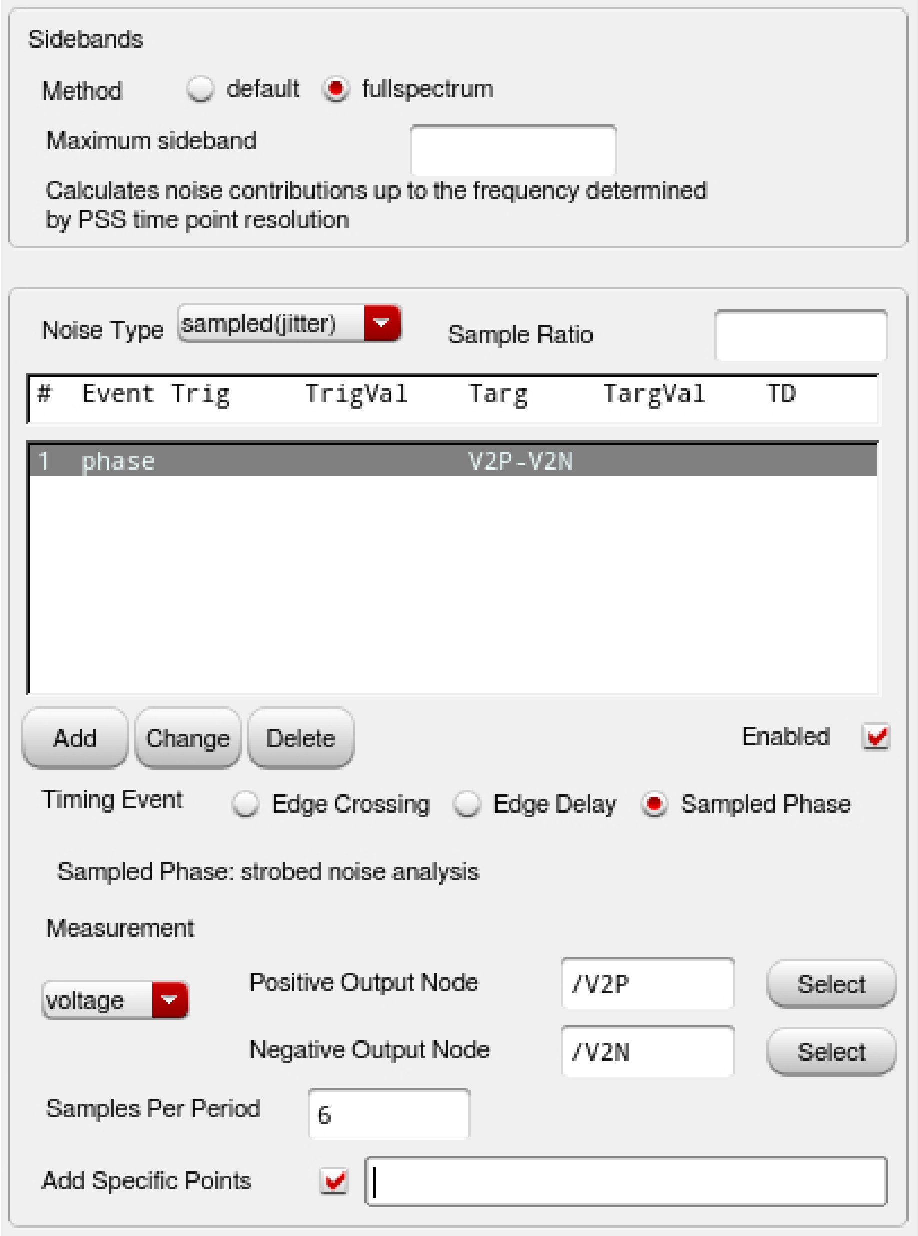
1. PSS Beat Frequency is obtained from PSS sim. setup of the same ADE test

2. Set frequency sweep range (for the noise PSD) **up to $f_S/2$**!
   - In this example, 500K = 1M/2
   - Tip: you could also write in the Stop field VAR(“F_CLK”)/2, if you have such a variable F_CLK



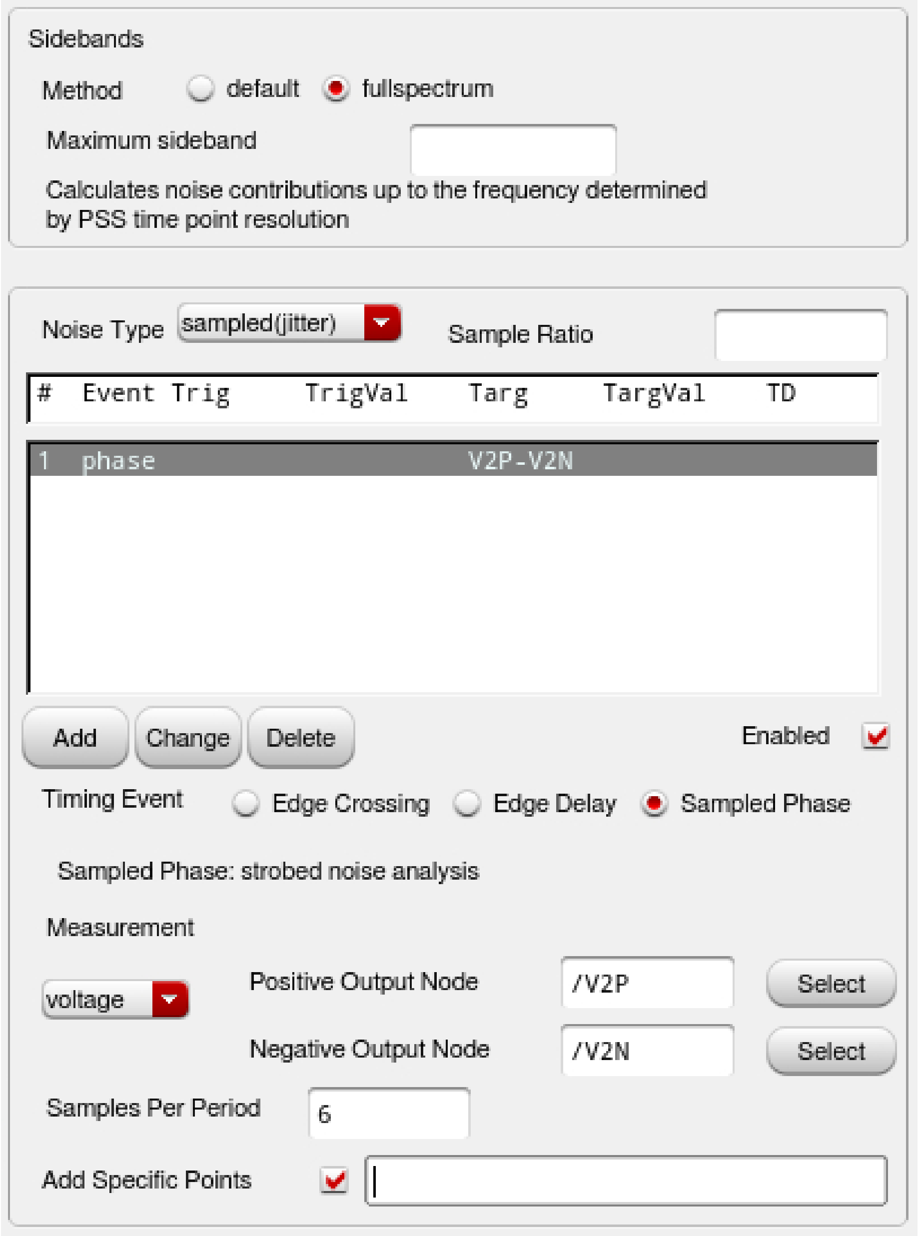
PNOISE setup (2)

1. Method = fullspectrum
   - To make sure you fold all the noise in
   - Keep maximum sidebands empty
2. Noise Type = sampled (jitter)
   - We need PSD at specific time!



PNOISE setup (3)

1. You will need to set sampling events:
   - Timing Event = Sampled Phase
   - Then select and positive and negative output node
   - Don't use a balun to measure differential noise (buggy)! Select the two diff. nodes of interest
   - Select no. samples per period and/or specific point in time (of the PSS result) where you want the PSD from (re-run later if the timing is off)
2. Then press "Add"! The event must be added to the list now
3. If you ever change the settings (e.g. samples per period), you **must** press "Change"!



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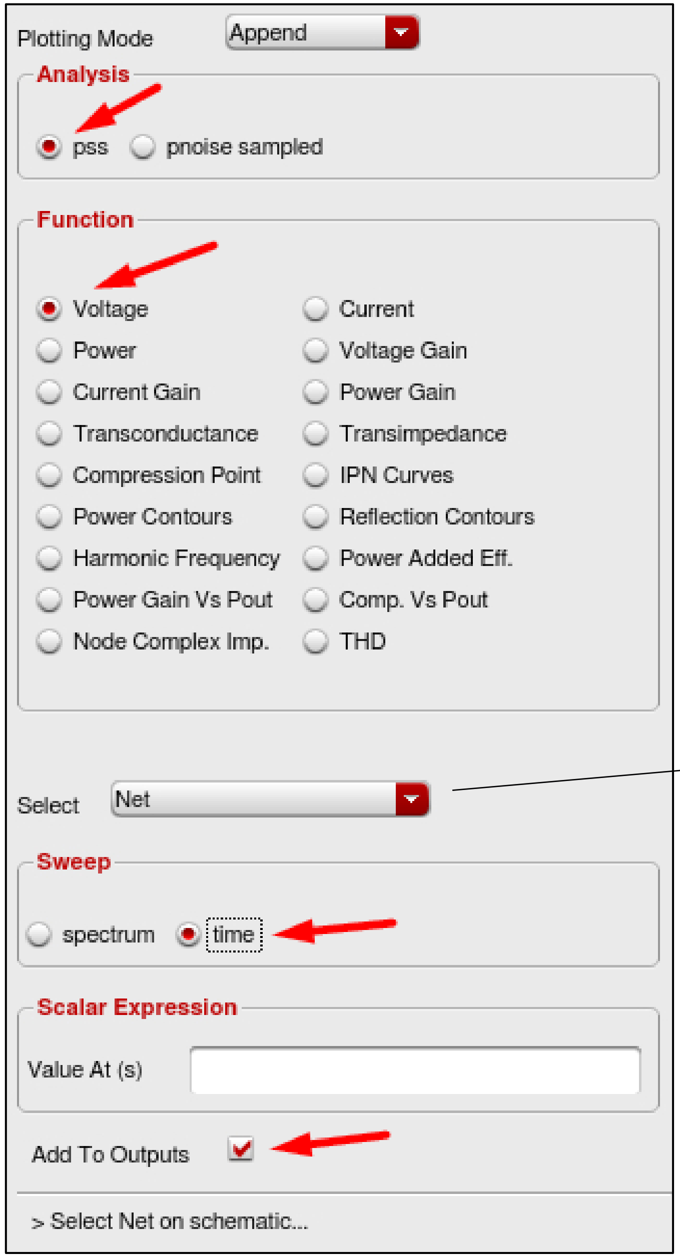
Plotting PSS results

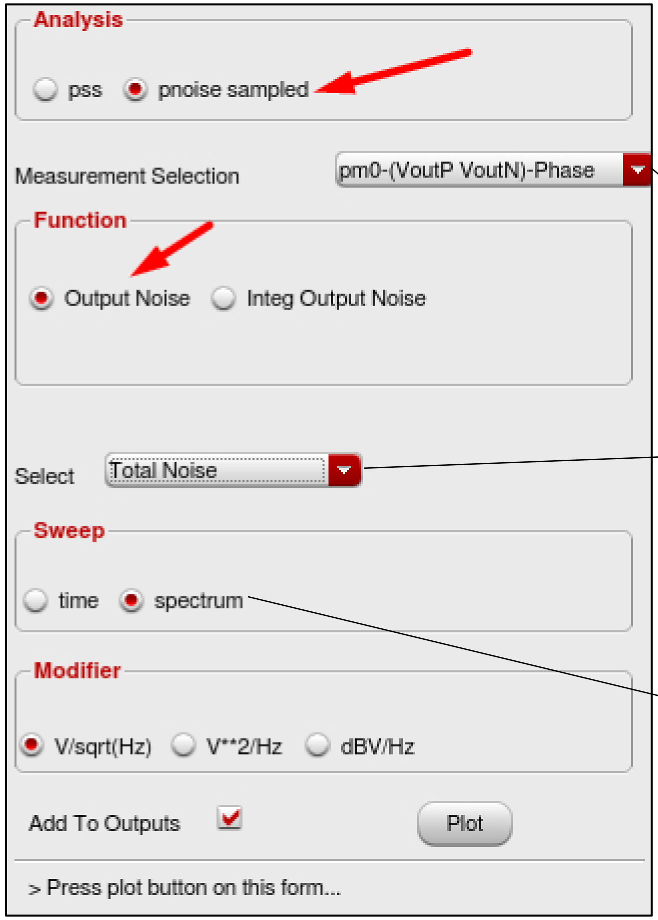
- As usual, in ADE use Results > Direct Plot > Main Form ..
- PSS form: plotting a voltage vs. time (in a single period) is usually what you do
- Check “Add To Outputs” to add the expression to ADE for future simulations ☺



Can also select a differential net if you want!

Plotting PNOISE results

Noise Spectrum

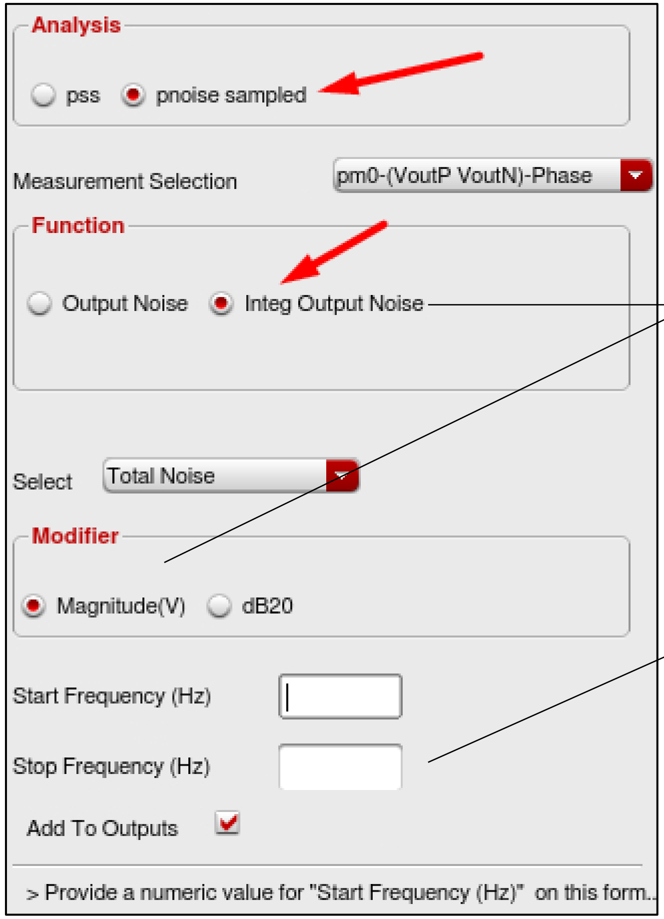


You set this up in PNOISE earlier

Total noise, or “noise per instance”, useful for design

Sweep spectrum, you’ll get the PSDs at different time moments

Integrated Noise

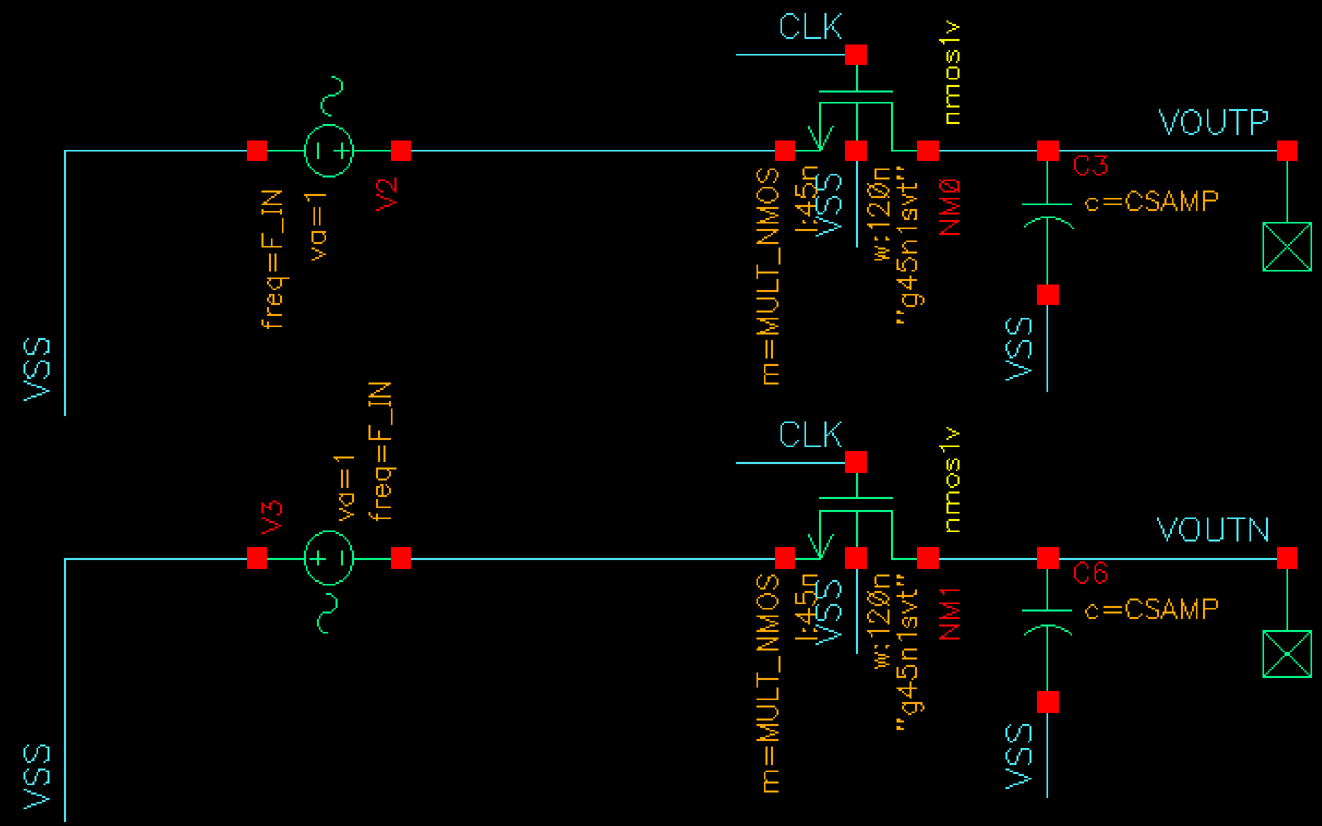


To get RMS value

Up to **f_s/2**!

You’ll get RMS noise vs. time

Demo 2: “demo_TH_NOISE_TB”

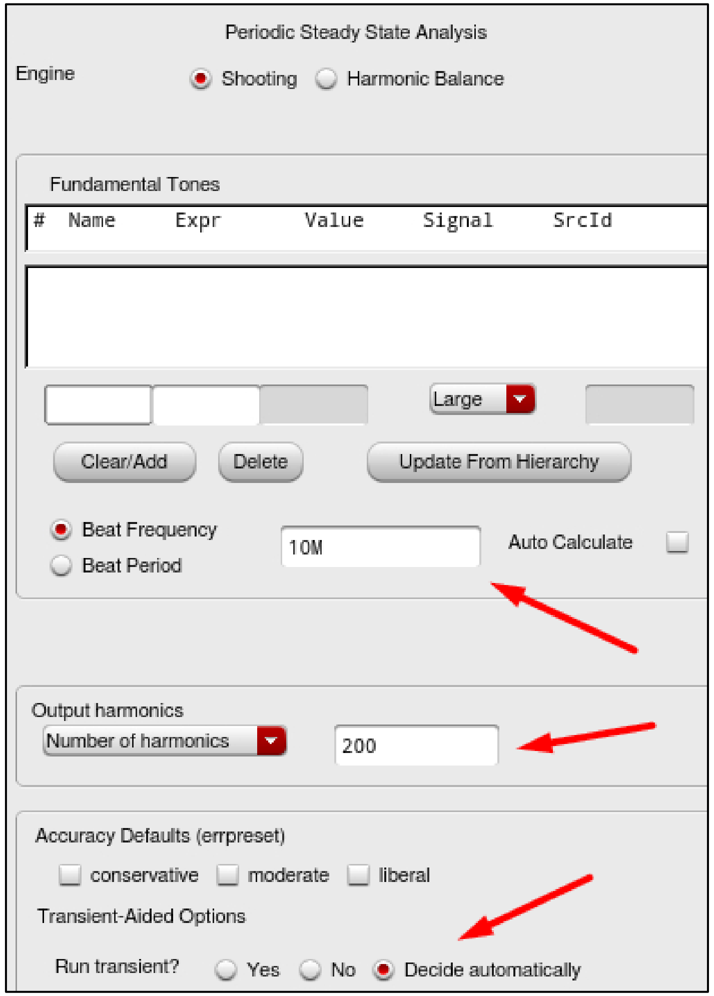


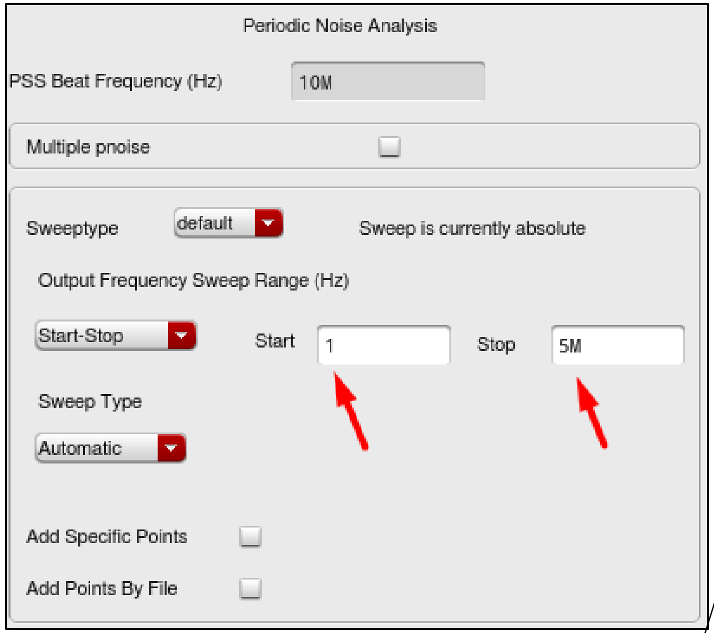
- Differential T/H with transistors ➔
- Total sampled differential noise power should be **2kT/C**

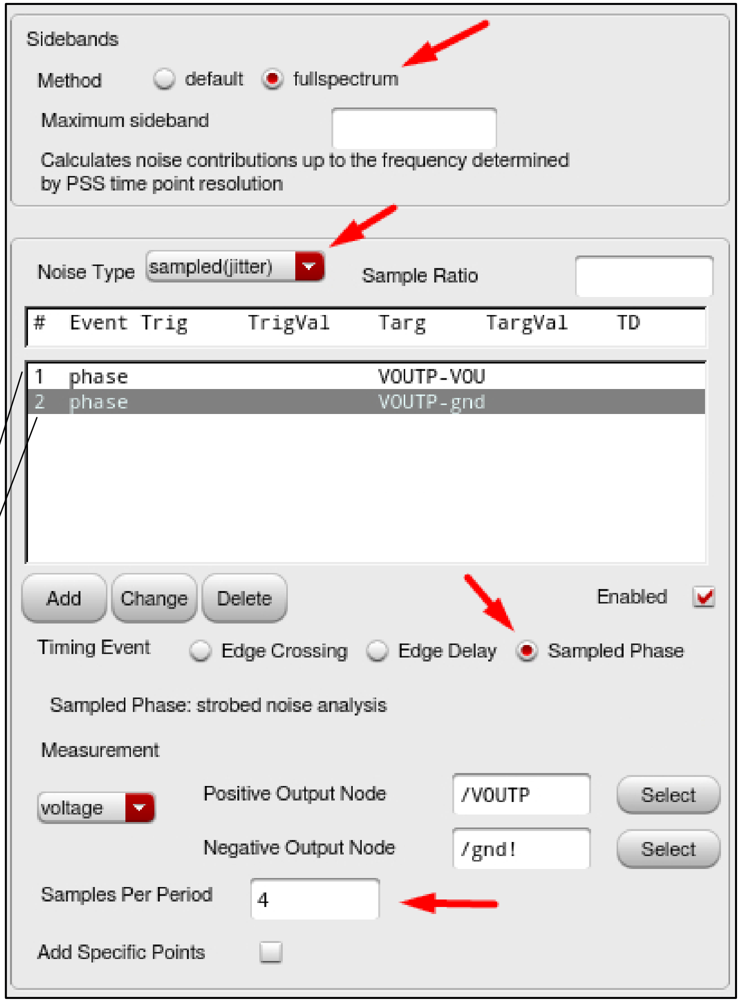
Demo 2: Setup

- We've set the sampling cap to 1 pF on each side
  - NMOS multiplier = 1, f_{CLK} = 10 MHz ⇔ shouldn't matter much
  - Expected single-ended RMS noise voltage is sqrt(kT/C) = **64 uV_{RMS}**
  - Expected differential RMS noise voltage is sqrt(2kT/C) = **90.5 uV_{RMS}**
- PSS, PNOISE are setup properly
- Setup and results are on next slides

Demo 2: Setup



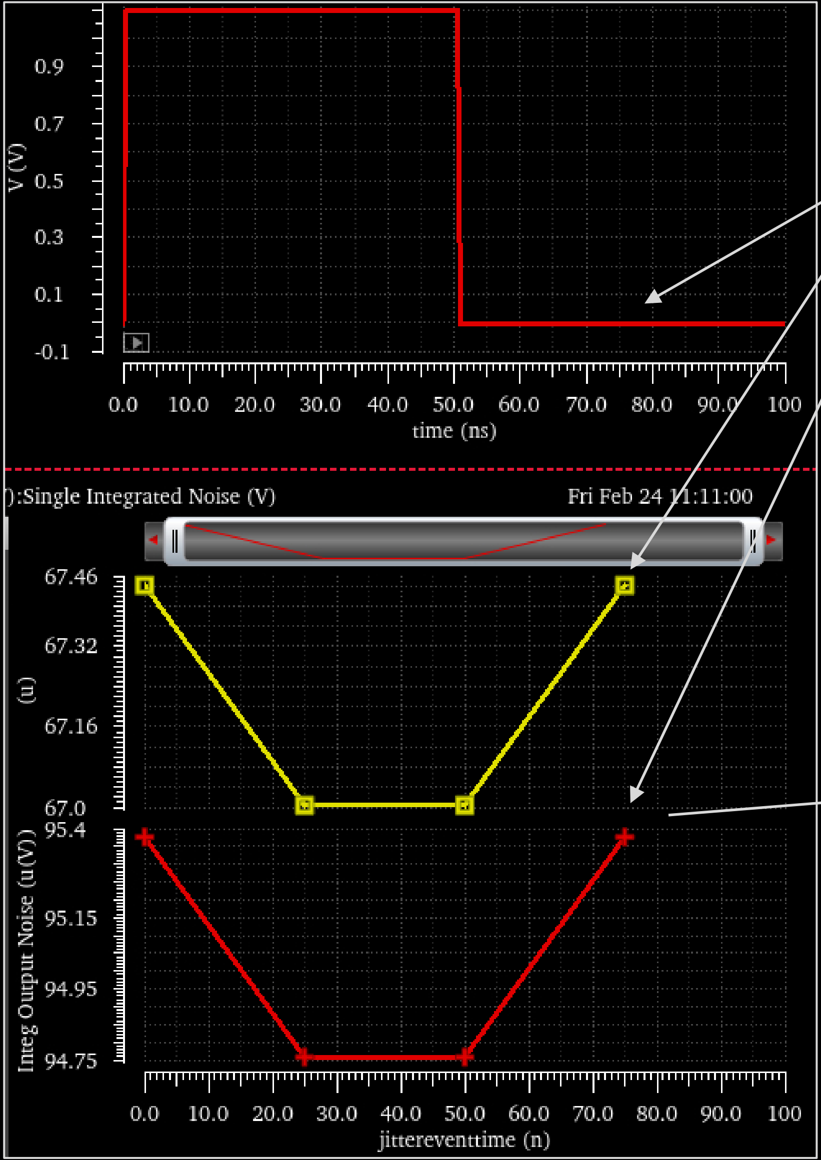




Differential and single-ended measurements

Demo 2: Results

Close enough! kT/C ignores 1/f ☺
And normally you'd overdesign

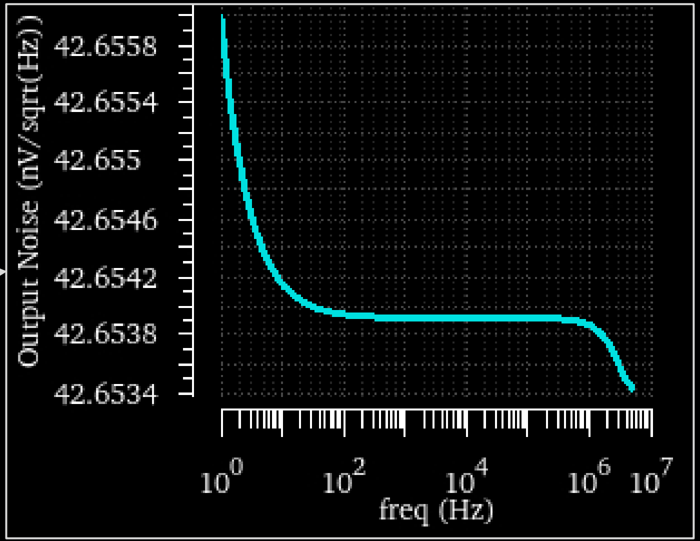


Check when clock = low

Single-ended:
~67.5 uV$_{RMS}$

Differential:
~95.4 uV$_{RMS}$

Noise Spectrum



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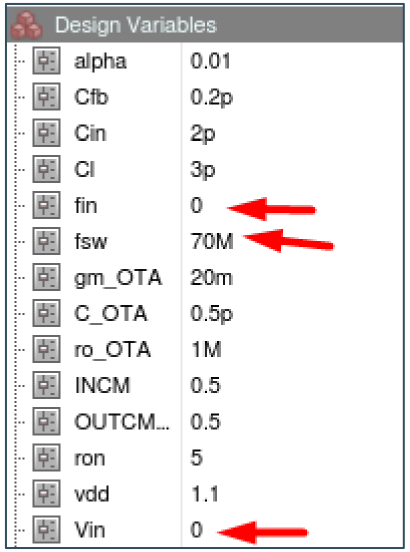
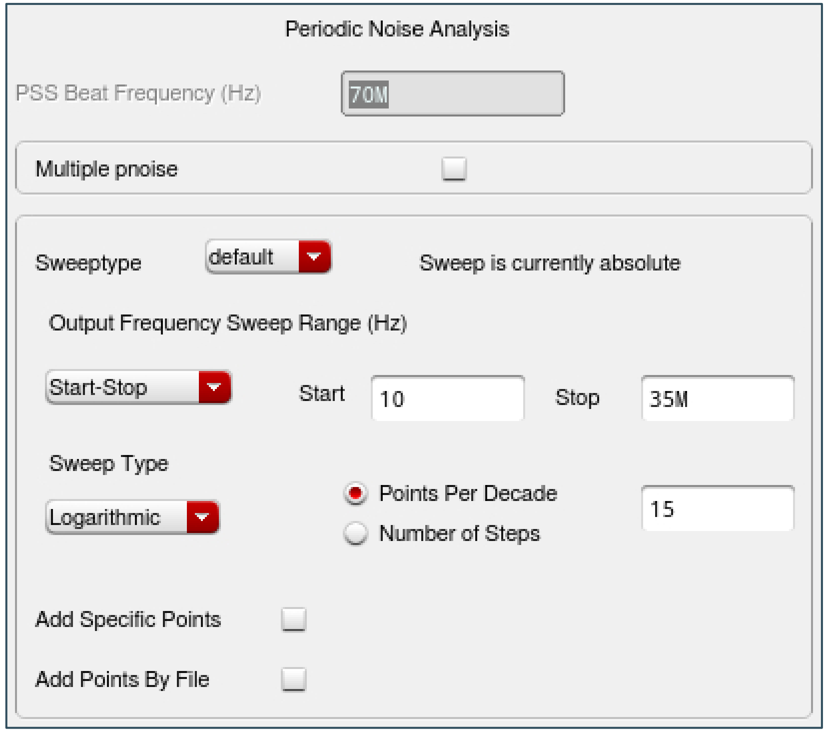
Demo 3: "demo_SCAmplifier_PNOISE_TB"

- To showcase how you would simulate noise in your DAMSIC project. Setup is very similar to demo 2!
- Important notes (see ADE):
  - Made fin = 0, Vin = 0 (via design variables)
  - Output baluns are disable in the schematic (else PNOISE becomes buggy)
  - Switching frequency is 70 MHz, so PNOISE and integral up to 35 MHz

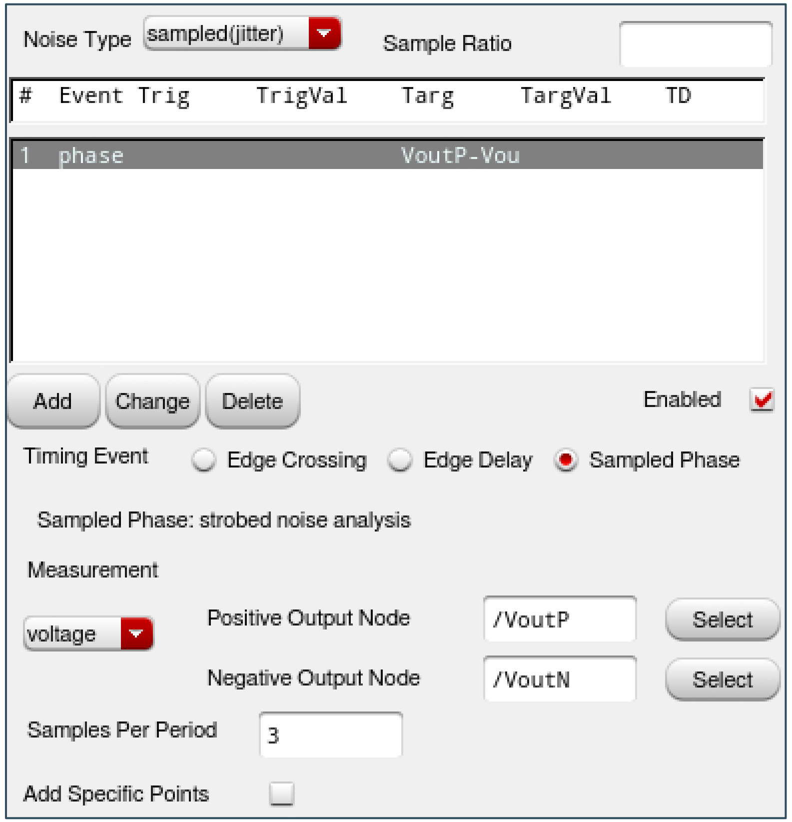
Demo 3: setup



Design Variables
alpha 0.01
Cfb 0.2p
Cin 2p
Cl 3p
fin 0
fsw 70M
gm_OTA 20m
C_OTA 0.5p
ro_OTA 1M
INCM 0.5
OUTCM... 0.5
ron 5
vdd 1.1
Vin 0

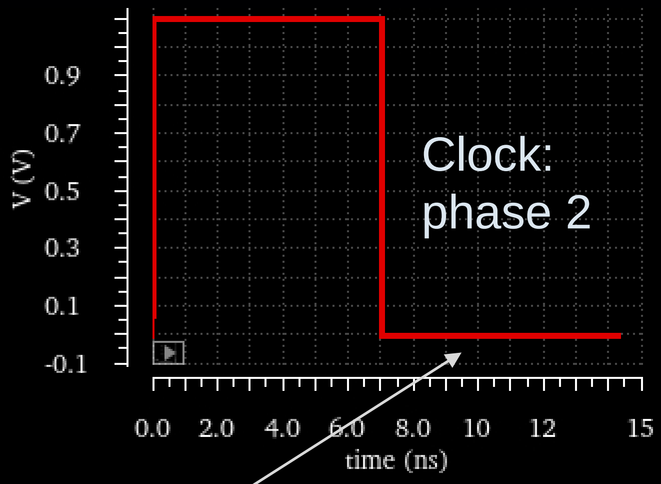


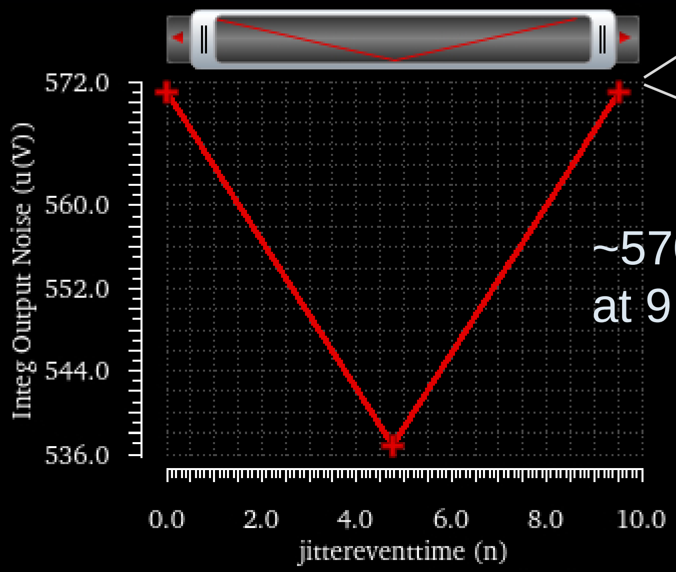
Periodic Noise Analysis
PSS Beat Frequency (Hz) 70M
Multiple pnoise
Sweeptype default
Sweep is currently absolute
Output Frequency Sweep Range (Hz)
Start-Stop
Start 10
Stop 35M
Sweep Type
Logarithmic
Points Per Decade
Number of Steps
15
Add Specific Points
Add Points By File



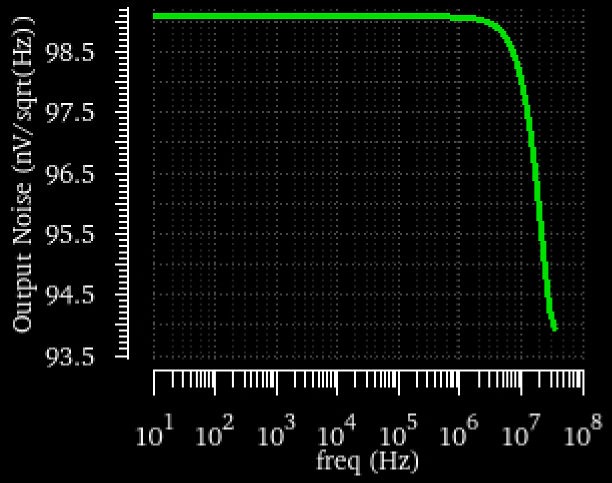
Noise Type sampled(jitter)
Sample Ratio
Event Trig TrigVal Targ TargVal TD
1 phase VoutP-Vou
Add
Change
Delete
Enabled
Timing Event
Edge Crossing
Edge Delay
Sampled Phase
Sampled Phase: strobed noise analysis
Measurement
voltage
Positive Output Node /VoutP Select
Negative Output Node /VoutN Select
Samples Per Period 3
Add Specific Points

Demo 3: results





~570 uV_{RMS}
at 9.5 ns



PSD at
9.5 ns

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PSS + PAC
SIMULATION SETUP AND DEMO

Static settling error ⇔ PAC

- PAC = **periodic AC simulation**
- It's a way to find your switched-cap amplifier's AC response
- PAC uses PSS to see the average voltage gain at the output ☺
  - remember, normal AC sim. considers only one steady state
- ➔ you can check the DC-gain of the switched-cap. ⇔ **static settling error!**
  - **PAC = alternative to long-duration transient simulation**

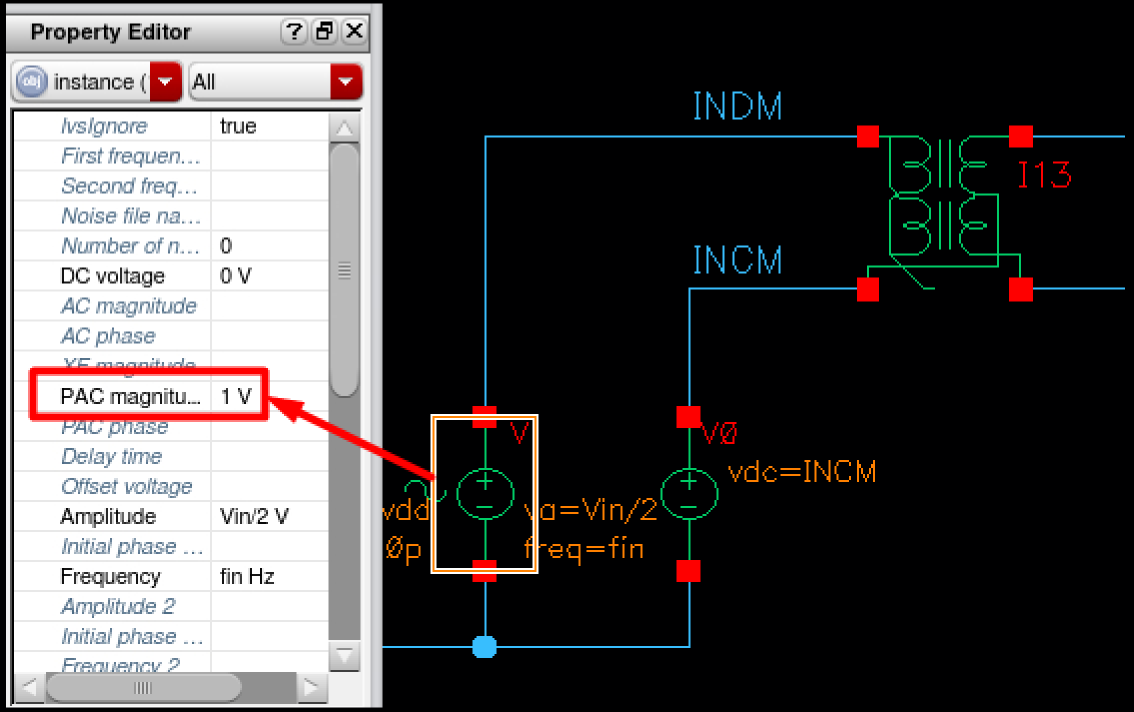
Demo 4: “demo_SCAmplifier_PAC_TB”

- Almost same setup as demo 3, now PSS + PAC

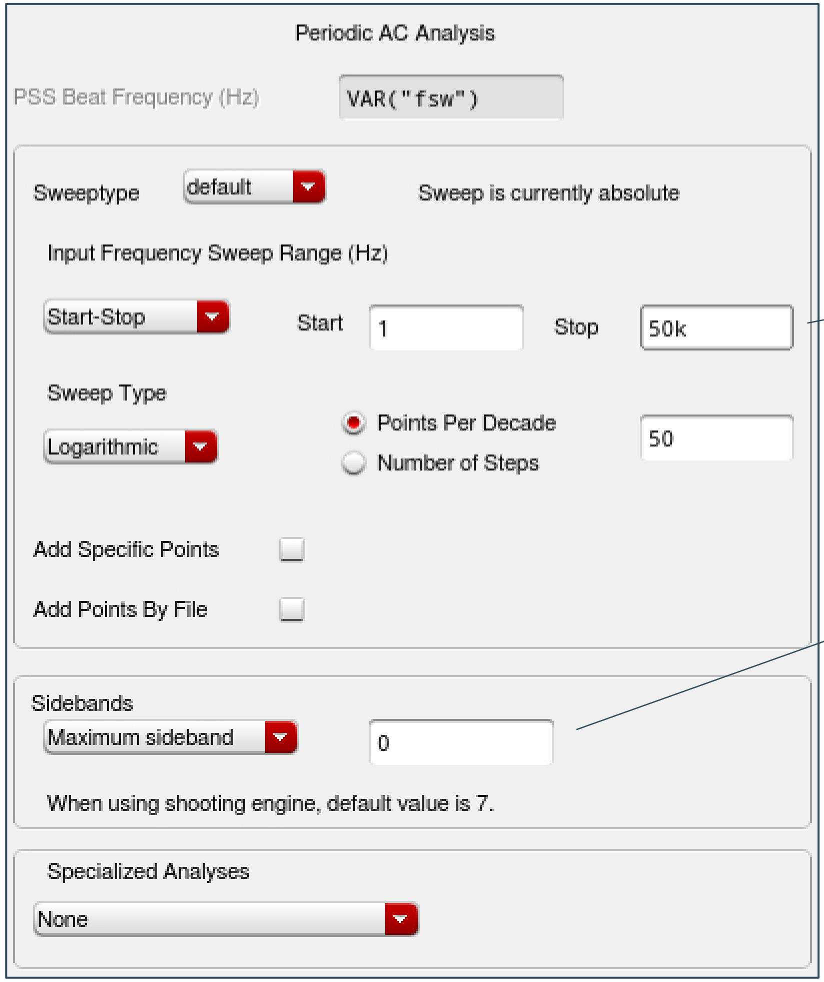
- Schematic:
  - Input source must have a **PACmagnitude** now (equal to 1)

- ADE:
  - **Lower switching frequency** to ~100k, you are interested in low-f effects
  - Enable PAC simulation (see setup on next slide) ➔ **sidebands = 0!**

Demo 4: schematic setup

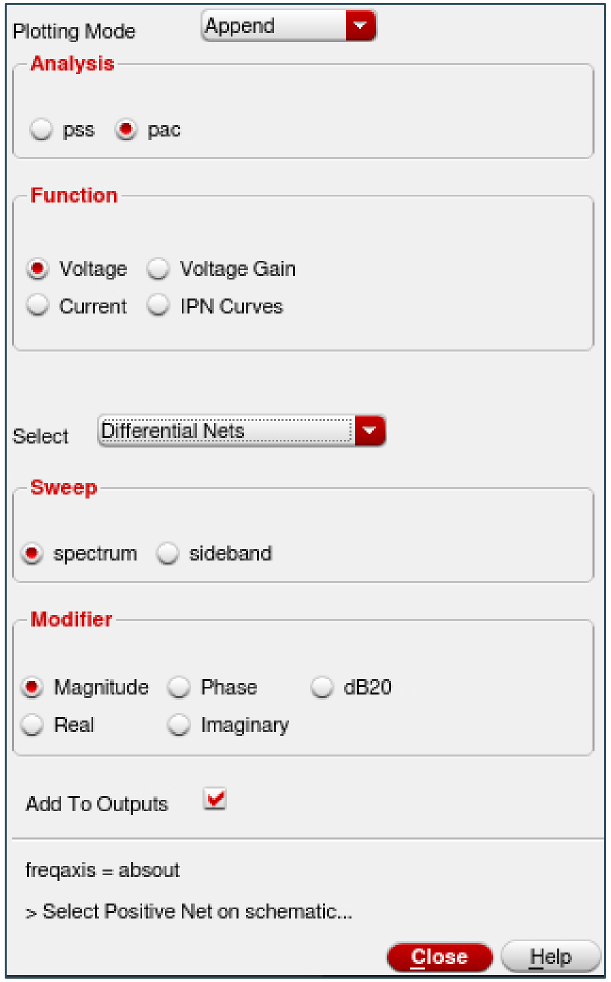


PAC setup + plotting (Direct Plot Form)



Again up to $f_S/2$

Must be 0!



Demo 4: results