Design of a Switched-Capacitor Amplifier

H05E4a DAMSIC Project 2025

Part II: Symmetrical OTA

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3 SYMMETRICAL OTA

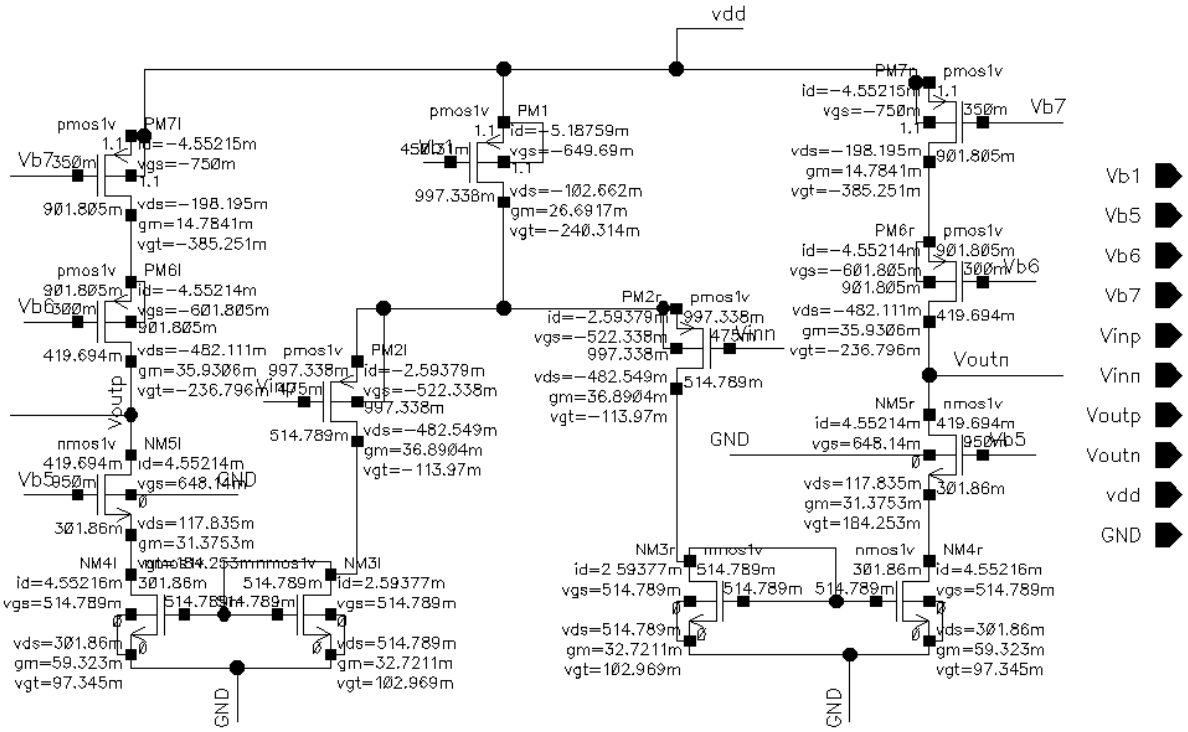
3.1 TABLE OF ACHIEVED RESULTS (SO FAR)

Enter your achieved results in the below table. You can leave some fields blank if you did not simulate (or design) for the specific parameter yet.

Parameter	**Unit**	**Achieved**
Input Swing	mV_{pp}	0.5~0.6
Output Swing	mV_{pp}	1012~1065
Total Integrated Output Noise	mV_{rms}	
SNR	dB	(*@ minimum Vin*)
C_L	pF	2.5
C_{FB}	pF	0.5
C_{IN}	pF	5
Open-Loop Gain	dB	33
Closed-Loop Gain	V/V	unstable
GBW (Sample Phase)	MHz	
Phase Margin (Sample Phase)	deg	
Dynamic Settling Error	%	(*settling error at the end of the amplification phase*)
Static Gain Error	%	
Power dissipation	mW	

3.2 SCHEMATIC DESIGN

1. Circuit schematic



2. Parameters of Transistor Dimensions and CMFB Block

CMFB Block Parameters		
A	**CMFBEst**	**R**
-1	**OUTCMRdEF**	**1kOhm**

Transistor Dimensions (W/L)							
	Pmos1	**Pmos2**	**Nmos3**	**Nmos4**	**Nmos5**	**Pmos6**	**Pmos7**
L (nm)	**225**	**225**	**450**	**450**	**450**	**450**	**450**
W (mm)	**0.36**	**0.36**	**0.36**	**0.72**	**0.36**	**0.36**	**0.21**
W / L	**1600**	**1600**	**800**	**1600**	**800**	**800**	**466.7**

3. **Transistor parameter and Branch Current**

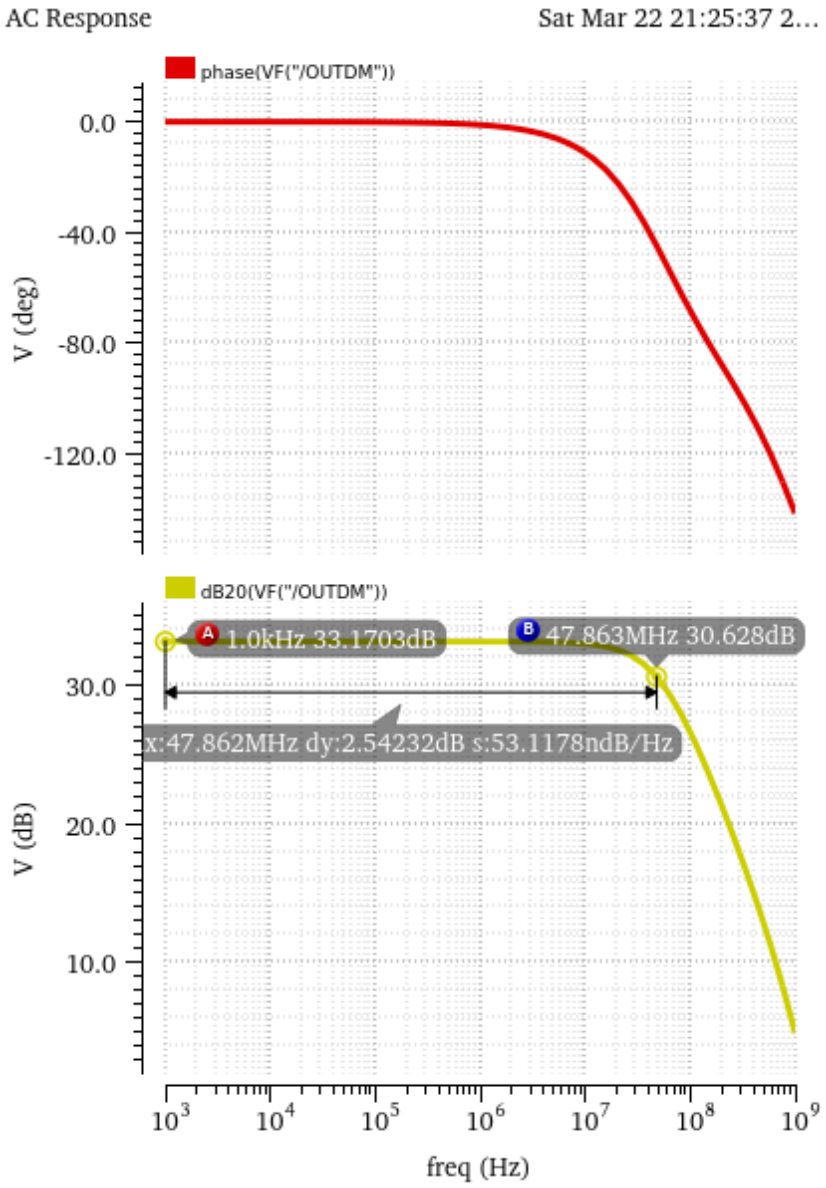
Transistor Parameters (gm, $V_{GT}=V_{GS}-V_{TH}$, V_{DS})							
	Pmos1	**Pmos2**	**Nmos3**	**Nmos4**	**Nmos5**	**Pmos6**	**Pmos7**
Gm (mS)	**26.7**	**36.9**	**32.7**	**59.3**	**31.4**	**35.9**	**14.8**
V_{GT} (mV)	**-240**	**-114**	**103**	**97.3**	**184**	**-237**	**-385**
V_{DS} (mV)	**-103**	**-483**	**515**	**302**	**118**	**-482**	**-198**

Branch Current	**Ids1**	**Ids2**	**Ids7**
I(mA)	**5.19**	**2.59**	**4.55**

3.3 SIMULATION RESULTS

In this subsection, insert the simulation details of your current symmetrical OTA design as requested below. **Please make sure that your plots are visible, and the axis labels and values are readable.**

1. Open-loop AC simulation: bode plot of OTA's gain



2. Closed-loop AC simulation: bode plot of differential loop gain in sampling phase

3. Closed-loop transient simulation: 2 consecutive cycles (f = f_S), input is DC within one cycle
   1st cycle: Vinp - Vinn = **minSwing/2**; 2nd cycle: Vinp - Vinn = **-maxSwing/2**
   Figure: a. Input waveform for differential mode (Vinp - Vinn)
   b. Output waveform for differential mode
   c. Output waveform for common mode
   d. Plot of the extracted settling error (% vs time) during the 2nd amplification phase

   Unstable
4. Closed-loop transient simulation: same as previous simulation, but lower f_S by 1000x.
5. Closed-loop PNOISE simulation: total differential output noise spectrum near end of sampling phase (in V/sqrt(Hz), from 1 Hz to f_S/2)