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The CMOS Gain-Boosting Technique

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Abstract. The gain-boosting technique improves accuracy of cascoded CMOS circuits without any speed penalty. This is achieved by increasing the effect of the cascode transistor by means of an additional gain-stage, thus increasing the output impedance of the subcircuit. Used in opamp design, this technique allows the combination of the high-frequency behavior of a single-stage opamp with the high DC-gain of a multistage design. Bode-plot measurements show a DC-gain of 90 dB and a unity-gain frequency of 116 MHz (16 pF load). Settling measurements with a feedback factor of 1/3 show a fast single-pole settling behavior corresponding with a closed-loop bandwidth of 18 MHz (35 pF load) and a settling accuracy better than 0.03 percent. A more general use of this technique is presented in the form of a transistor-like building block: the Super-MOST. This compound circuit behaves as a normal MOS-transistor but has an intrinsic gain *gm.ro* of more than 90 dB. The building block is self-biasing and therefore very easy to design with. An opamp consisting of only 8 Super-MOST's and 4 normal MOST's has been measured showing results equivalent to the design mentioned above.

1. Introduction

Speed and accuracy are two of the most important properties of analog circuits; optimizing circuits for both aspects leads to contradictory demands. In a wide variety of CMOS analog circuits such as switched-capacitor filters [1]–[3], algorithmic A/D converters [4], sigma-delta converters [5], sample-and-hold amplifiers and pipeline A/D converters [6], speed and accuracy are determined by the settling behavior of operational amplifiers. Fast-settling requires a high unity-gain frequency and a single-pole settling behavior of the opamp, whereas accurate settling requires a high DC-gain.

The realization of a CMOS operational amplifier that combines high DC-gain with high unity-gain frequency has been a difficult problem. The high-gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high unit-gain frequency requirement asks for a single-stage design with short-channel devices biased at high current levels.

Future processes with submicron channel length will enable us to realize higher unity-gain frequencies. However, the intrinsic MOS transistor gain *gm.ro* will then be lower [7], and the problem of achieving sufficient DC-gain becomes even more severe.

There have been several circuit approaches to circumvent this problem. Cascoding is a well-known means to enhance the DC-gain of an amplifier without degrading the high-frequency performance. The result is a DC-gain that is proportional to the square of the intrinsic MOS transistor gain *gm.ro*. In modern processes with short-channel devices and an effective gate-driving voltage of several hundreds of millivolts, the intrinsic MOS transistor gain *gm.ro* is about 20–25 dB, resulting in a DC-gain of the cascoded version of about 40–50 dB. This is however in many cases not sufficient [1], [8], [9].

Dynamic biasing of transconductance amplifiers [10]–[12], was one of the first approaches reported to combine high DC-gain with high settling speed. In this approach the bias current is decreased, either as a function of time during one clock period [10, 11] or as a function of the amplitude of the input signal [12], resulting in a higher DC-gain at the end of the settling period. This decreases the unity-gain frequency which makes the last part of the settling very slow.

In [13] a triple-cascode amplifier has been implemented where the gain is proportional to $(gm.ro)^3$. This approach has two significant disadvantages. First, every transistor added in the signal path introduces an extra pole in the transfer function. In order to obtain enough phase margin, the minimum load capacitance has to be increased, resulting in a lower unity-gain frequency. Secondly, each transistor reduces the output-swing by at least the effective gate-driving voltage.

In [8], positive feedback is used to enhance the gain of an amplifier. This approach however is limited by matching. A gain enhancement of about 16 dB is reported. Starting from an original gain of 50 dB, one could obtain 70 dB DC-gain. For high-Q, high-frequency switched capacitor filters, this is not sufficient. Even a moderate Q of 25 and a maximum deviation of 1 percent requires a minimum opamp gain of 74 dB [1, 8]. Therefore, we aim at a DC-gain of at least 80 dB combined with a unity-gain frequency of 100 MHz.

In [14], a regulated-cascode stage was reported that increases the DC-gain of a normal-cascode stage. In [15], the performance of this circuit with respect to output swing and output impedance was analyzed. The extension of this circuit into a general gain-boosting technique was presented in [16, 17], showing a complete opamp design with a measured DC-gain of 90 dB and a unity-gain frequency of 116 MHz. It was shown that this technique enhances the DC-gain of a cascoded amplifier several orders of magnitude *without* any penalty in speed or output swing.

This paper gives a complete overview of the gain-boosting technique and presents a general use of this technique in the form of a transistor-like building block: the Super-MOST.

In section 2 the principle of the gain-boosting technique is explained. Section 3 deals with the high-frequency behavior. Section 4 discusses the optimization toward fast settling behavior. In section 5, some remarks on output swing are made. In section 6, the circuit implementation of an opamp is presented; and in section 7 the measurement results of this opamp are shown. Then, in section 8, the Super-MOST is presented, along with measurement results of the device on its own as well as of an opamp built with this building block.

2. Gain-Boosting Principle

We start this section with the functioning of the simple cascode stage shown in figure 1. We show that the DC-gain can be expressed as the product of an *effective transconductance* $g_{m,eff}$ and the output-impedance. This explanation leads to the gain-boosting principle. The repetitive application of this principle leads to a decoupling of the DC-gain and the unity-gain frequency of an opamp.

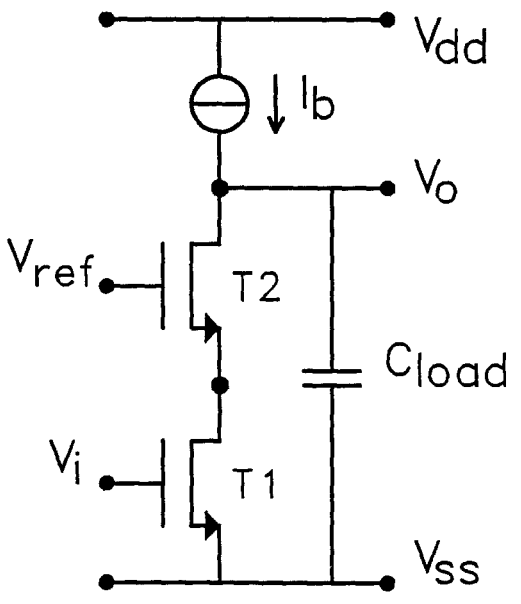

Fig. 1. Cascoded gain-stage.

2.1. Cascode Stage

The transfer function of the cascode stage can be found as follows. Suppose an ideal voltage source is connected to the output of the stage. If a voltage ΔV_i is applied to the input, a current ΔI_o will flow into the voltage source. For low frequencies:

$$\frac{\Delta I_o}{\Delta V_i} = g_{m1} \frac{(g_{m2}r_{o1} + r_{o1}/r_{o2})}{(g_{m2}r_{o1} + r_{o1}/r_{o2} + 1)} = g_{m,eff}. \quad (1)$$

This *effective transconductance* is almost equal to g_{m1}, the reduction is caused by the feedback via the drain of the input transistor. Removing the voltage source causes a change $\Delta V_o = \Delta I_o R_{out}$, where ΔI_o is calculated using (1) and R_{out} is the output resistance of the total circuit. The voltage-gain A_o is

$$A_o = g_{m,eff}R_{out} \quad (2)$$

The output impedance of the total circuit can easily be calculated to be

$$R_{out} = (g_{m2}r_{o2} + 1)r_{o1} + r_{o2} \quad (3)$$

which leads to the following expression for the DC-gain:

$$A_o = g_{m1}r_{o1}(g_{m2}r_{o2} + 1) \quad (4)$$

The behavior of the circuit, in the vicinity of the unity-gain frequency, is similar with the voltage source connected to the output. Now the load capacitor C_{load} forms the short-circuit to ground. At the unity-gain frequency we use the effective transconductance as given by (1), and this results in the following expression for the gain-bandwidth product (GBW):

$$\text{GBW} = g_{m,eff}/C_{load} \tag{5}$$

From equations (2) and (5) we may conclude that the only way to improve A_0 without reducing the GBW is to *increase the output impedance.* Note that this is the effect of the cascode transistor itself with respect to the noncascoded situation: the cascode transistor shields the drain of the input transistor from the effect of the signal swing at the output.

As we can see from (2), the DC-gain is proportional to the output impedance of the circuit. This implies that we may consider the gain of such a stage as the output-impedance normalized on $1/g_{m,eff}$. We will use this approach in section 4.

2.2. Gain-Boosting Principle

The technique presented here is based on increasing the cascoding effect of T2 by adding an additional gain-stage as shown in figure 2. This stage further reduces the feedback from the output to the drain of the input transistor. Thus, the output impedance of the circuit is further increased by the gain of the additional gain-stage A_{add}:

$$R_{out} = (g_{m2}r_{o2}(A_{add} + 1) + 1)r_{o1} + r_{o2} \tag{6}$$

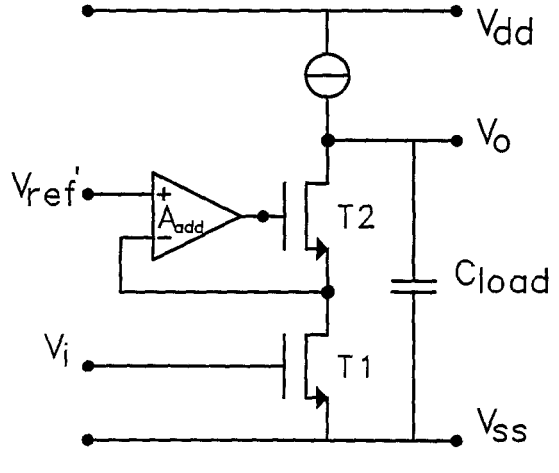

Fig. 2. Cascoded gain-stage with gain enhancement.

Moreover, the effective transconductance is slightly increased:

$$\frac{\Delta I_o}{\Delta V_i} = g_{m1}\frac{(g_{m2}r_{o1}(A_{add} + 1) + r_{o1}/r_{o2})}{(g_{m2}r_{o1}(A_{add} + 1) + r_{o1}/r_{o2} + 1)} = g_{m,eff} \tag{7}$$

Hence, the total DC-gain now becomes:

$$A_{o,tot} = g_{m1}r_{o1}(g_{m2}r_{o2}(A_{add} + 1) + 1) \tag{8}$$

Section 3 deals with the high-frequency behavior of this circuit and discusses what happens if the gain of the additional stage decreases as a function of frequency.

2.3. Repetitive Implementation of Gain Boosting

If the additional stage is implemented as a cascode stage, the gain-enhancement technique as described above can also be applied to this additional stage. In this way, a *repetitive* implementation of the gain-enhancement technique can be obtained as shown in figure 3. The limitation on the maximum voltage gain is then set by factors as leakage currents, weak avalanche, and thermal feedback. The implementation of the additional stage is discussed in section 6.

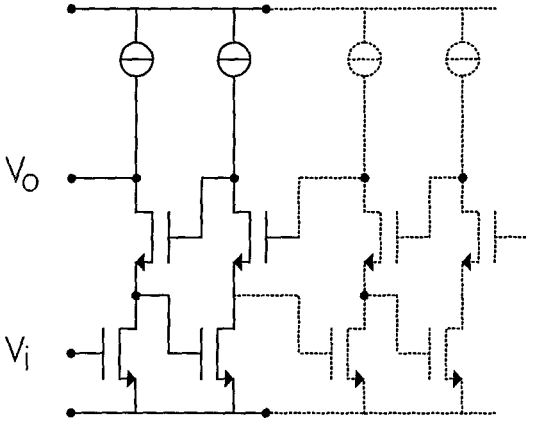

Fig. 3. Repetitive implementation of gain enhancement.

From the above, we may conclude that the repetitive usage of the gain-enhancement technique yields a *decoupling* of the opamp DC-gain and unity-gain frequency.

3. High-Frequency Behavior

In this section, we discuss the high-frequency behavior of the gain-enhanced cascode stage of figure 2. It is

shown that for a first-order roll-off, the additional stage need not be fast with respect to the unity-gain frequency of the overall design.

In figure 4, a gain Bode-plot is shown for the original cascoded gain-stage of figure 1 (A_{orig}), the additional gain-stage (A_{add}) and the improved cascoded gain-stage of figure 2 (A_{tot}). At DC, the gain enhancement A_{tot}/A_{orig} equals approximately $[1 + A_{add}(0)]$, according to equations (4) and (8). For $\omega > \omega_1$, the output impedance is mainly determined by C_{load}. In fact, we have to substitute $(R_{out}//C_{load})$ in equation (2) for R_{out}. This results in a first-order roll-off of $A_{tot}(\omega)$. Moreover, this implies that $A_{add}(\omega)$ may have a first-order roll-off for $\omega > \omega_2$ as long as $\omega_2 > \omega_1$. This is equivalent to the condition that the unity-gain frequency (ω_4) of the additional gain-stage has to be larger than the 3-dB bandwidth (ω_3) of the original stage, but it can be much lower than the unity-gain frequency (ω_5) of the original stage. The unity-gain frequencies of the improved gain-stage and the original gain-stage are the same.

From the above, to obtain a first-order roll-off of the total transfer function, the additional gain-stage does not have to be a fast stage. In fact, this stage can be a cascoded gain-stage as shown in figure 1, with smaller width and nonminimal length transistors biased at low current levels. Moreover, as the additional stage forms a closed loop with T2, stability problems may occur if this stage is too fast. There are two important poles in this loop. One is the dominant pole of the additional stage and the other is the pole at the source of T2. The latter is equal to the second pole, ω_6, of the main amplifier. For stability reasons, we set the unity-gain frequency of the additional stage lower than the second pole frequency of the main amplifier. A safe range for the location of the unity-gain frequency ω_4 of the additional stage is given by

$$\omega_3 < \omega_4 < \omega_6. \tag{9}$$

This can easily be implemented.

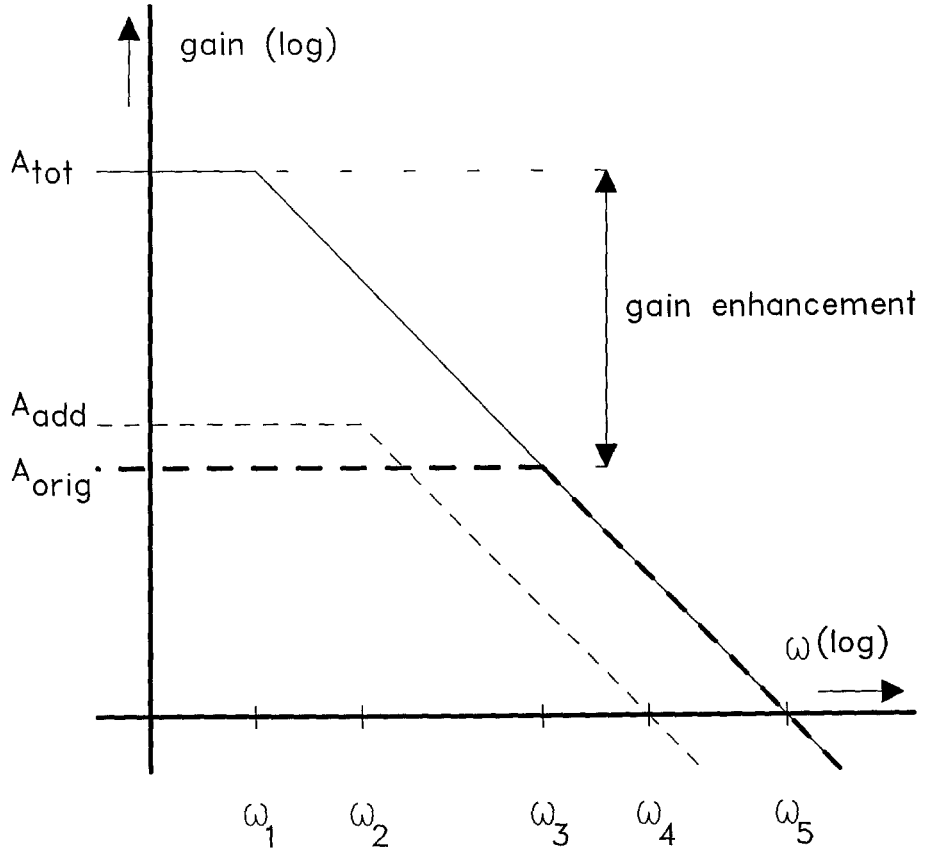

Fig. 4. Gain Bode-plots of the original cascoded gain-stage (A_{orig}), the additional gain-stage (A_{add}), and the improved cascoded gain-stage (A_{tot}).

4. Settling Behavior

In this section, the settling behavior of the gain-enhanced cascoded amplifier-stage is discussed. It is shown that a single-pole settling behavior demands a higher unity-gain frequency of the additional stage than a simple first-order roll-off in the frequency domain requires as discussed in the previous section. The reason for this is the presence of a closely spaced pole and zero (doublet). In section 4.1 the occurrence of a doublet in the gain-enhanced cascode amplifier-stage is discussed. Section 4.2 presents a graphical representation of the settling behavior of an opamp, and finally in section 4.3, the condition for one-pole settling is presented.

4.1. Doublet

From (6), the gain-enhancement technique increases the output impedance, Z_{out}, by a factor approximately equal to $(A_{add} + 1)$. The gain of the additional stage, A_{add}, decreases for frequencies above ω_2 (figure 4) with a slope of -20 dB/decade. For frequencies above ω_4, A_{add} is less than one, and the normal output impedance Z_{orig} of a cascode stage without gain-enhancement remains. This is shown in figure 5. Also shown is the impedance of the load capacitor Z_{load} and the parallel circuit which forms the total impedance, Z_{tot}, at the output node. A closer look at this plot reveals that a doublet is present in the plot of the total output impedance near ω_4.

Noncomplete doublet cancelation can seriously degrade the settling behavior of an opamp [18]. If a doublet is present in an opamp open-loop transfer function at ω_{pz} with a spacing of $\Delta\omega_{pz}$, the opamp is used in a feedback situation with feedback factor β, a slow-settling component is present with time constant $1/\omega_{pz}$. The relative magnitude (with respect to the total output signal) of the slow-settling component is given by [18]:

$$\frac{\Delta V_{out,slow}}{\Delta V_{out,total}} = \frac{\Delta\omega_{pz}}{\omega_{pz}} \cdot \frac{\omega_{pz}}{\beta\omega_{unity}} = \frac{\Delta\omega_{pz}}{\beta\omega_{unity}} \tag{10}$$

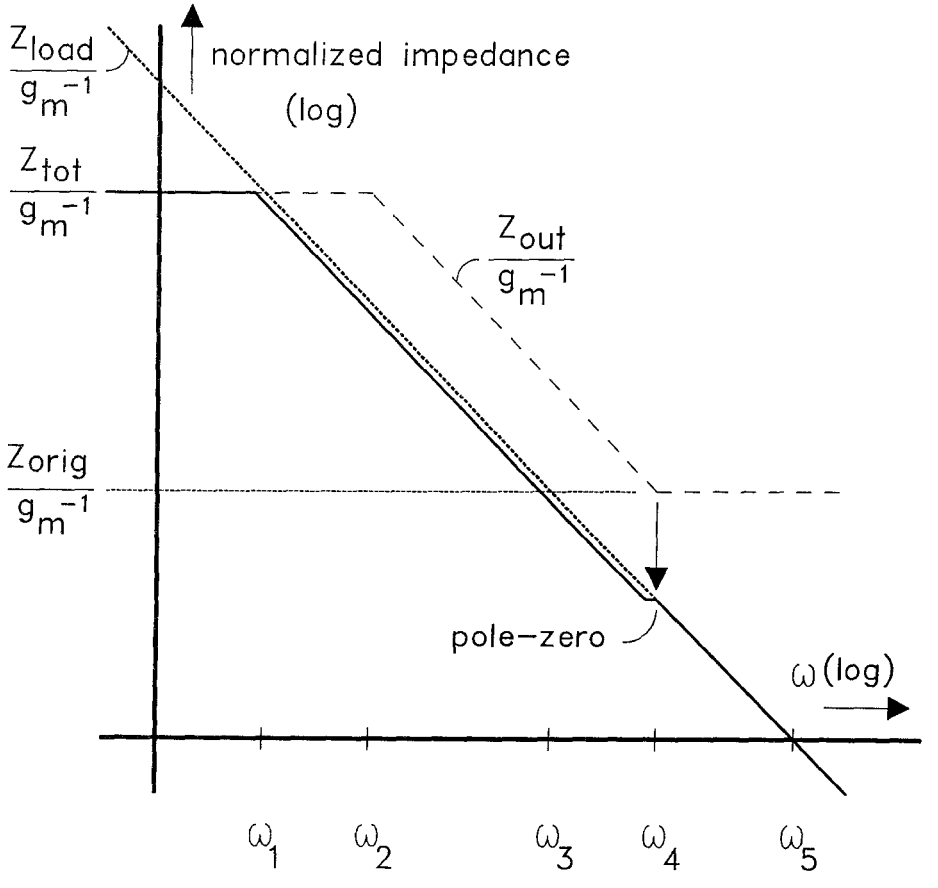

Fig. 5. The normalized output impedance as a function of frequency.

For a single-pole settling behavior, the relative magnitude of the slow-settling component, given in (10), has to be smaller than the ultimate settling accuracy $1/\beta A_{tot}(0)$. Note that for opamps with a very high DC-gain this requirement can be very difficult to realize.

4.2. Graphical Representation of Settling Behavior

The settling behavior of an opamp can be judged very well by plotting the relative settling error (the ratio of the signal at virtual ground of the opamp and the output-step) versus time, as shown in figure 6. Here an ideal single-pole settling behavior is shown as a straight line. In figure 6, the simulated result is shown of an opamp in unity-feedback with a unity-gain frequency of 25 MHz and a DC-gain of 100 dB. Curve A shows the result without the presence of a doublet: a straight line down to −100 dB with a steep slope corresponding to one small time constant. Curve B shows the result of an opamp with the same DC-gain and unity-gain frequency but now with a doublet of 500 KHz and 1 percent spacing. The slow-settling component causes a severe deviation from the straight line. According to (10), the slow-settling component has a relative magnitude of −74 dB in this situation, which is in close agreement with the result shown. The slope of this line is 50 times smaller than the slope of the fast-settling component. Curve C shows the result of a simulation with an opamp with again the same DC-gain and unity-gain frequency but now with a doublet at 2.5 MHz and a relative spacing of 10 percent. As seen from this figure, slow-settling components can easily be detected in this way. In section 7, where we show the measurement results, we use this representation to judge the settling behavior of our design.

4.3. Optimization of Settling Behavior

To determine the spacing in the doublet in the transfer function of the gain-enhanced cascode stage, consider again the impedance plot of figure 5. The total impedance at the output of the amplifier is the parallel connection of the load capacitance and the output impedance of the circuit. At ω_2, the output impedance of the circuit begins to decrase as a function of frequency due to the roll-off of the additional stage. This can be

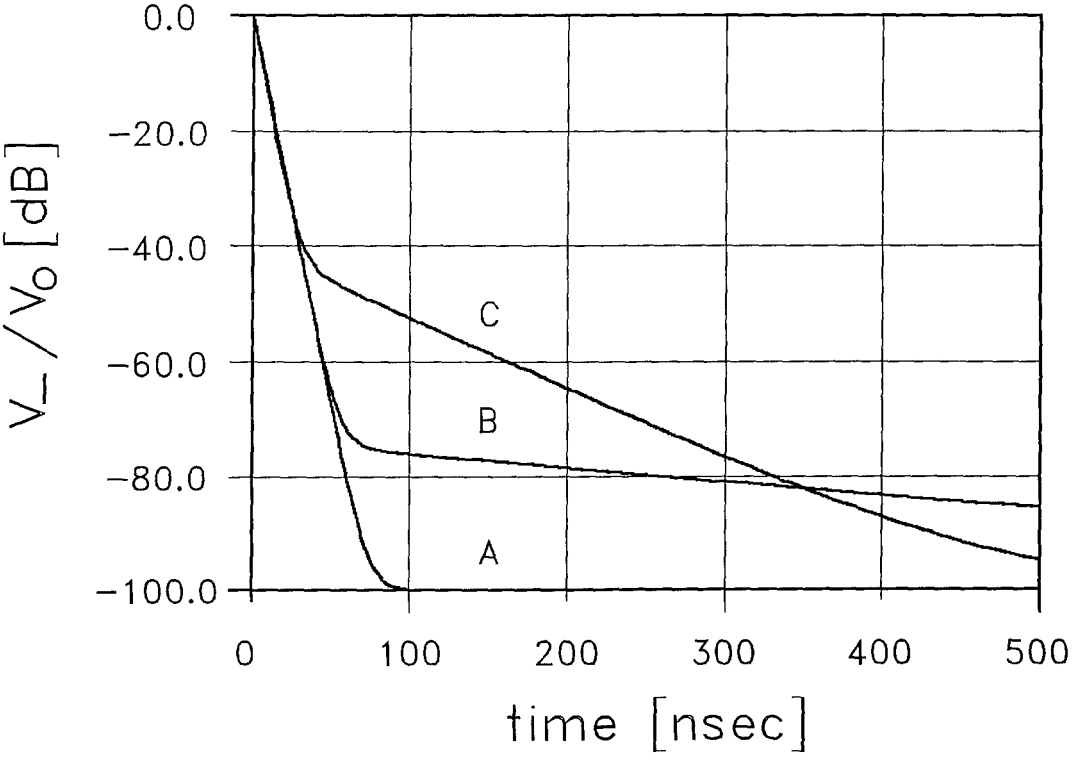

Fig. 6. Relative settling error as a function of time.

modeled as a small capacitor in parallel with the output resistor. The ratio between this small capacitor and the load capacitor is ω_1/ω_2 $(=\omega_3/\omega_4)$, as can be seen in figure 5. This small capacitor is simply parallel-connected to the (large) output capacitance and gives a small shift of the total impedance at the output. At ω_4 however, the effect of this small capacitor disappears due to the 1 in the $(A_{add} + 1)$ terms. At this frequency, a small shift in the total output impedance occurs, back to the original line (in figure 5) determined by the load capacitor only. It is also at this frequency where the doublet is located in the total transfer function. From the above we can conclude that the relative spacing of the doublet is approximately ω_3/ω_4. This results in a relative magnitude of the slow-settling component according to (10) of

$$\frac{\Delta V_{out,slow}}{\Delta V_{out.total}} = \frac{\omega_3}{\beta\omega_5} \tag{11}$$

which is equal to the inverse of the feedback factor β multiplied by the DC-gain of the original cascode stage without gain enhancement! Thus we may conclude that the pole-zero cancellation is not accurate enough. Our approach here is to make this "slow"-settling component fast enough. If the time constant of the doublet $1/\omega_{pz}$ is smaller than the main time constant $1/\beta\omega_{unity}$, the settling time will not be increased by the doublet. This situation is achieved when the unity gain frequency of the additional stage is higher than the -3 dB bandwidth of the closed-loop circuit. On the other hand, for reasons concerning stability, the unity-gain frequency must be lower than the second-pole frequency of the main amplifier as indicated by (9). This results in the "safe" area for the unity-gain frequency of the additional stage

$$\beta\omega_5 < \omega_4 < \omega_6 \tag{12}$$

as shown in figure 7. Note that this safe area is smaller than given by (9). A satisfactory implementation however is still *no problem*, even if $\beta = 1$, because the load capacitor of the additional stage, which determines ω_4, is much smaller than the load capacitor of the opamp, which determines ω_5.

5. Output Swing

The output swing is limited by the requirement that all transistors have to remain in the saturation region,

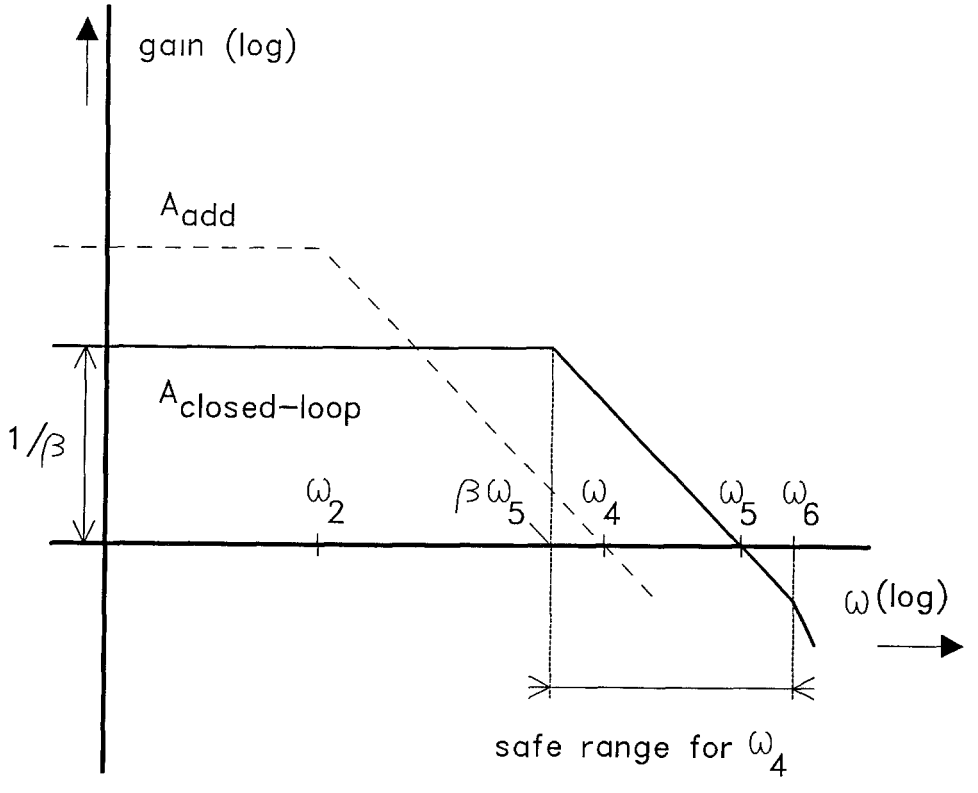

Fig. 7. The "safe" range for the unity-gain frequency of the additional stage.

otherwise a severe decrease in gain resulting in large distortion will occur. The edge of saturation of an MOS transistor occurs when the gate-drain voltage equals the threshold voltage at the drain [19]:

$$V_{D,min} = \frac{V_G - V_{to}}{1 + \alpha} \tag{13}$$

which is the effective gate-driving voltage divided by $(1 + \alpha)$ representing the body effect, where α is determined by processing [19]. Note that a large body-effect is advantageous there. In this design, an effective gate-driving voltage of 250 mV was chosen. With $\alpha = 0.3$, this results in a minimum drain-source voltage of 190 mV. Applying this result to the amplifier stage in figure 2 leads to a minimum output voltage of 380 mV and to a large-signal output swing of $V_{dd} - 2 * 380$ mV. With a 5.0 V supply, this results in a maximum output swing of 4.2 V. Note that a different criterion is used for the maximum swing and the output than in [15]. To be able to obtain this large output swing, the additional stage has to have an input common-mode range close to the supply voltage V_{ss}.

6. Opamp Circuit Implementation

In this section, the implementations of the main opamp and the additional gain-stages are discussed. The main stage is a folded-cascode amplifier [2]. The simplest implementation of the additional stage is one MOS-transistor [14, 15, 20]. We have chosen a cascode version because of its high gain and the possibility of repetitive usage of the gain-enhancement technique as discussed in section 2. The input-stage design of the additional amplifier is determined by the common-mode range requirement which is close to the V_{ss} as discussed before. As a consequence, a folded-cascode structure with PMOS input transistors is chosen for the additional amplifier in figure 2. To realize a very high output impedance, the current source in figure 2 is also realized as a cascoded structure with an additional gain stage. A fully differential version (figure 8) has been integrated in a 1.6-μm CMOS process. The two input transistors connected to V_{cm} have been added to control the common-mode bias voltage at the output. Using this scheme, the circuit can also be used as two single-ended opamps. The die photograph of figure 9 clearly shows that the additional stages are much smaller in chip area than the main opamp.

7. Opamp Measurement Results

As it is very difficult to measure differentially at high frequencies with sufficient accuracy, all measurements have been performed single-ended. The output node of the additional amplifier in figure 2 is connected to a bonding pad in order to be able to switch off the gain-enhancement technique. Results of gain measurements both with and without gain enhancement are shown in

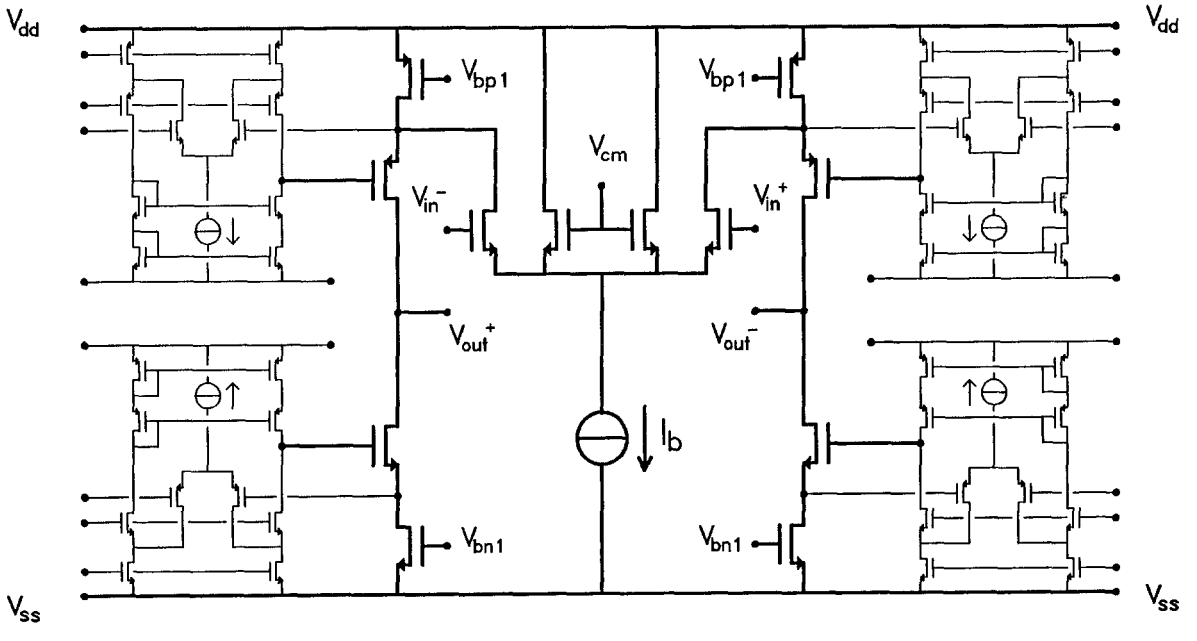

Fig. 8. Complete circuit diagram of the opamp.

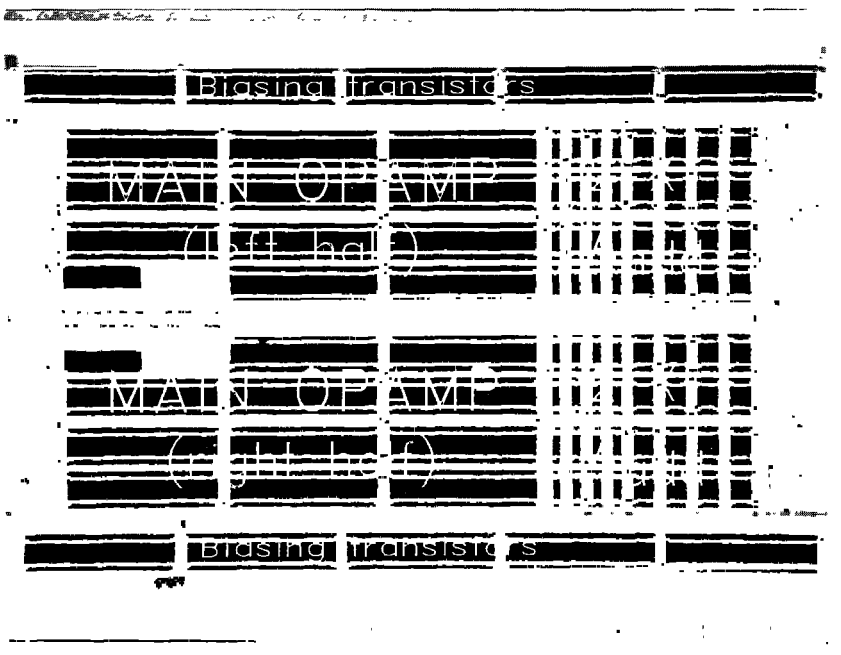

Fig. 9. Die photograph of the opamp.

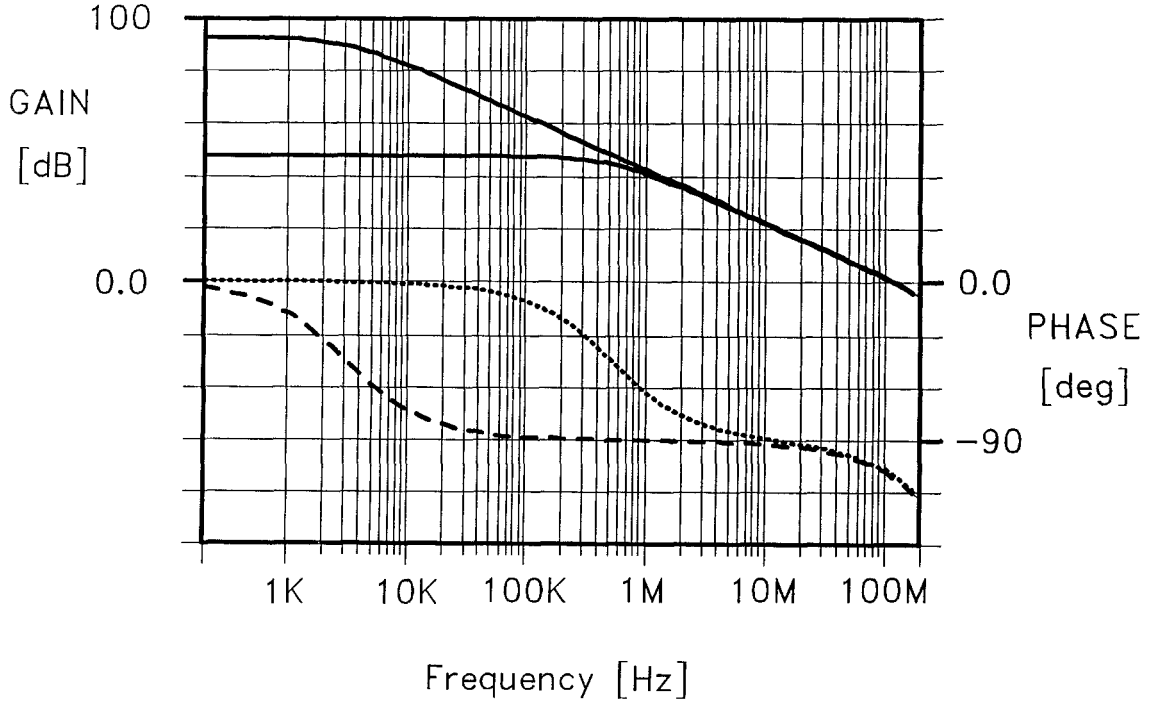

Fig. 10. Results of gain and phase measurements both with and without gain enhancement.

figure 10. A DC-gain enhancement of 45 dB was measured without affecting the gain or phase for higher frequencies, resulting in a total DC-gain of 90 dB combined with a unity-gain frequency of 116 MHz. This shows a good agreement with figure 4. Note that when measured differentially, both the DC-gain and the unity-gain

frequency are expected to be twice as high. The settling behavior is measured according to figure 11 by applying a step, ΔV_i, at the input. The resistors are needed for DC-biasing of the opamp and have no influence on the settling behavior. The error signal V_- at the opamp input, and the output signal V_0 are shown in figure 12. In figures 12a and 12b, ΔV_0 = 1V which is small enough to avoid slewing. With the gain enhancement switched off, an error signal of 4.75 mV is measured after settling (figure 12a). This corresponds to the measured DC-gain of 46 dB. Switching on the gain enhancement reduces the error signal to a value smaller than 0.1 mV (figure 12b), which corresponds to a DC-gain higher than 80 dB.

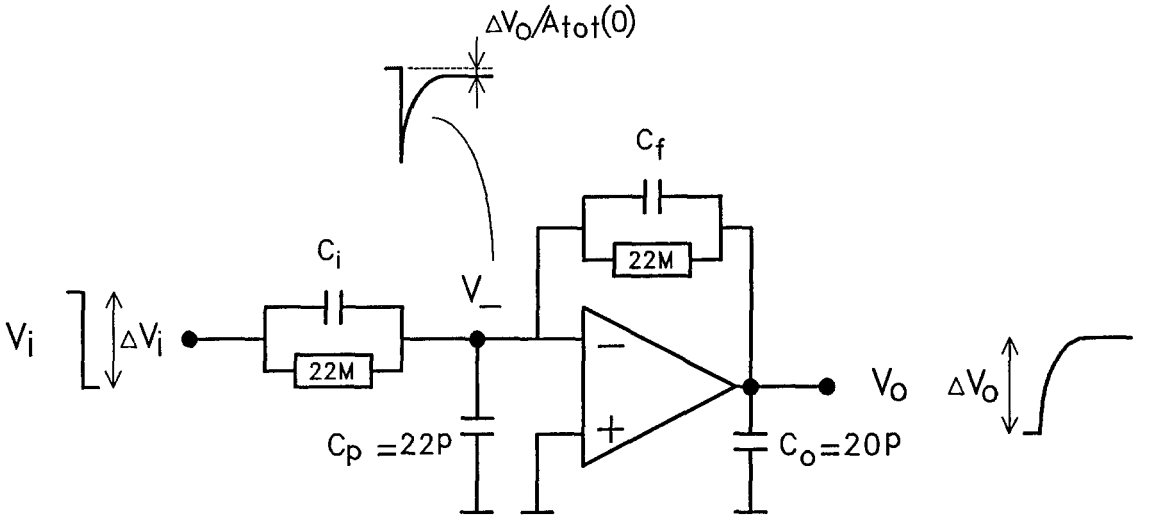

Fig. 11. Scheme for measuring settling behavior.

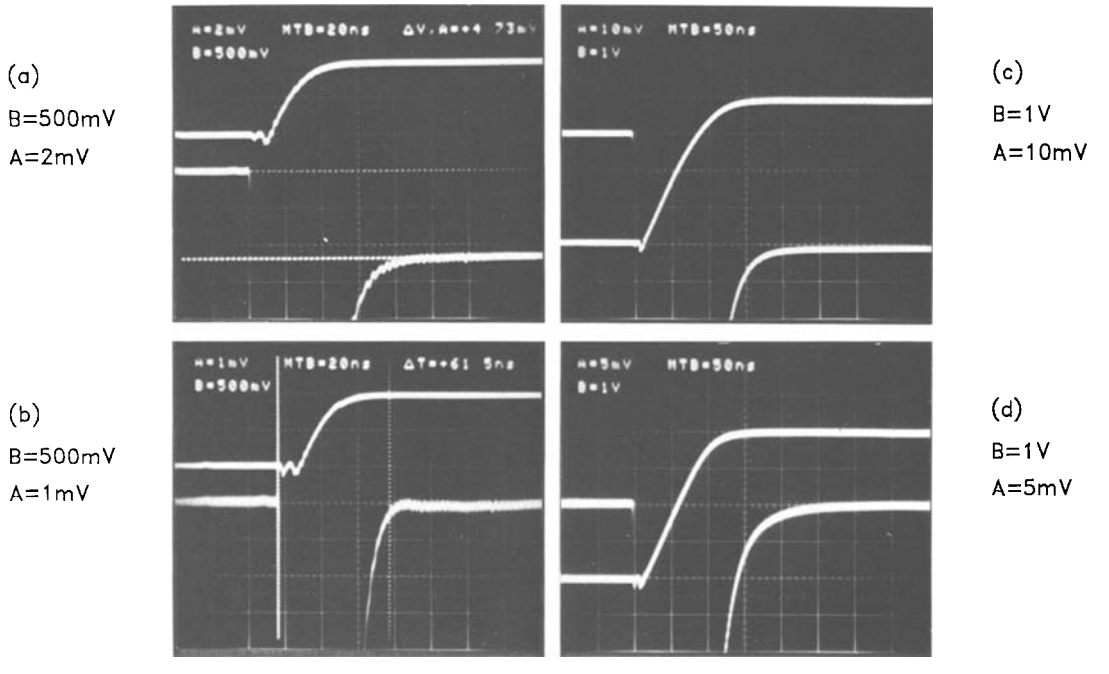

Fig. 12. Settling-measurement results. The output signal (upper trace) and the error signal at the opamp input (lower trace) with: (a) ΔV_0 = 1V and gain enhancement switched off, (b) ΔV_0 = 1V and gain enhancement switched on, (c) ΔV_0 = 4V and gain enhancement switched off, (d) ΔV_0 = 4V and gain enhancement switched on.

Settling speed can be calculated as follows. In figure 11 the feedback factor β is given by

$$\beta = \frac{C_f}{C_i + C_p + C_f} \tag{14}$$

whereas the unity-gain frequency is given by

$$\omega_{unity} = g_m \frac{C_i + C_p + C_f}{C_o(C_i + C_p + C_f) + (C_i + C_p)C_f} \tag{15}$$

The theoretical settling-time constant, τ, can now be calculated:

$$\tau = \frac{C_p + C_i + C_o + (C_i + C_p) \cdot C_o/C_f}{g_m} \tag{16}$$

In figure 11, C_o = 20 pF and $C_p = C_i = C_f$ = 22 pF, which is relatively large due to probing. With g_m = 0.012 A/V, we find ω_{unity} = 54 MHz, β = 1/3 and τ = 8.8 ns. Settling to 0.1 percent takes 7τ = 62 ns and corresponds to a 1-mV error at the output. With a feedback factor β = 1/3, this corresponds to an error signal of V_- = 0.33 mV. From figure 12b the measured settling time for 0.1 percent accuracy is 61.5 ns, which is in agreement with the theory. In figure 13, the measured settling behavior is shown as a function of time as discussed earlier. During the entire settling process, each 10-dB increase in settling accuracy takes approximately 8 ns. This clearly shows that there are no slow settling components. In figures 12c and 12d, ΔV_o = 4V, C_i = 33 pF, and C_f = 15 pF, showing a normal slewing behavior and a large output swing. The main measured characteristics of the opamp are summarized in table 1.

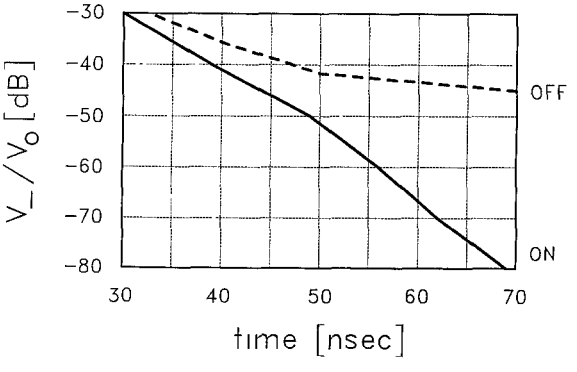

Fig 13. Measured relative-settling error as a function of time for both with and without gain enhancement.

8. The Super-MOST

A disadvantage of the above-shown implementation of the opamp is the complexity of the design and layout.

Table 1. Main characteristics of the opamp.

Gain enh.	on	off
DC gain	90 dB	46 dB
Unity-gain freq.	116 MHz	120 MHz
Load cap.	16 pF	16 pF
Phase margin	64 deg.	63 deg.
Power cons.	52 mW	45 mW
Output swing	4.2 V	4.2 V
Supply voltage	5.0 V	5.0 V

A disadvantage of cascoded amplifiers in general is the number of required biasing voltages resulting in long wires across the chip. These long wires consume a considerable amount of space and, what is worse, are susceptible to cross-talk and therefore instability. To circumvent this problem, the Super-MOST was developed.

8.1 Basic Idea and Circuit Description

The Super-MOST is a compound circuit that behaves like a cascoded MOS transistor and has, like a normal MOST, a source, a gate, and a drain terminal. The Super-MOST, however, has an extremely high output impedance due to implementation of the gain-boosting technique. Moreover, it does not require any biasing voltage or current other than one single power supply.

The circuit of an *N*-type Super-MOST is shown in figure 14a. The circuit consists of three parts:

1. Transistors N1 and N2 are the main transistor and its cascode transistor and form the core of the circuit. Their size determines the current-voltage relations and the high-frequency behavior of the "device."
2. Transistors N7, N8, P2, and P4 form the additional stage for the gain-boosting effect.
3. Transistors N3, P1, P3, N4, N5, and N6 are for biasing purposes and ensure that N2 is always biased in such a way that N1 is just 50–100 mV above the edge of saturation, independent of the applied gate voltage. This ensures a low saturation voltage of the Super-MOST.

The size of the transistors of the additional stage and of the biasing branch is as small as a few percent of the main transistors.

Figure 14b shows the symbols for the Super-MOST, S is the source terminal, G is the gate terminal, and D is the drain terminal. Furthermore, an extra low-impedance current-input terminal F is available which can be used for folded-cascode structures.

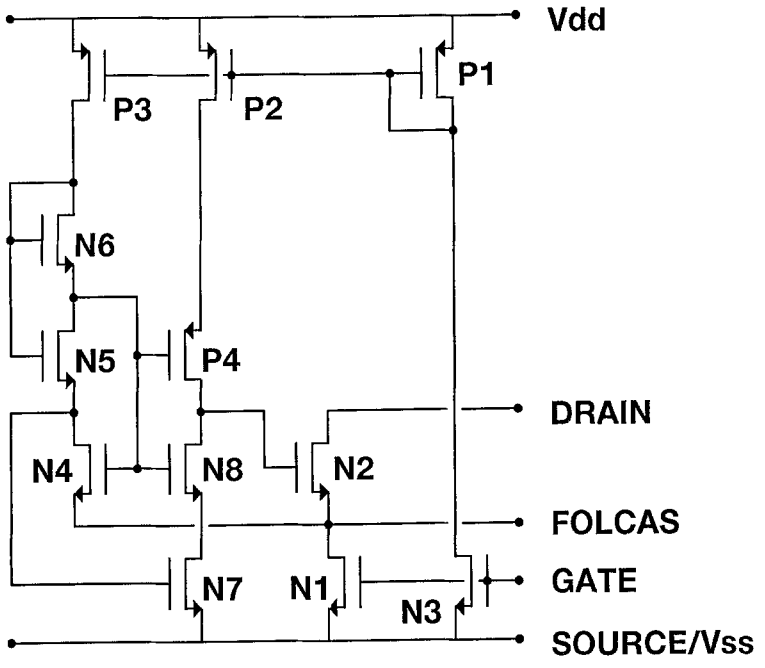

Fig. 14. a) *N*-type Super-MOST.

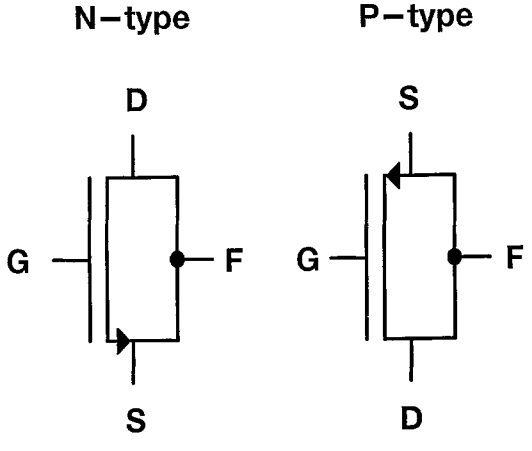

Fig. 14. b) Super-MOST symbols.

8.2. Measured "Device" Characteristics

Figure 15a shows the measured characteristics of a single *N*-type MOST and a Super-MOST for V_{gs} ranging from 0.7 V (a) to 1.0 V (g). The single MOST shows an early voltage of approximately 5 V whereas the Super-MOST has an early voltage several orders of magnitude higher. Note that the "device" is already saturated at a voltage only slightly above the saturation voltage of one single MOST, indicating a large possible output swing. In figure 15b, an enlargement of figure 15a is shown for V_{gs} = 0.95 V. From the I_{DS} curve, an early voltage of 1750 volts can be calculated which is an increase of 350 times compared to a single MOST.

8.3 Fundamental Limitation of the Gain-Boosting Technique

This measurement (figure 15b) also reveals the upper limit for the gain-boosting technique. The voltage V_F at the F terminal changes 0.8 mV as the drain voltage varies 5 V. This would imply an increase in early voltage and output impedance of 6250 times. The lower measured early voltage is due to a weak avalanche current which flows directly from drain to substrate and is therefore not influenced by the gain-boost technique. In fact, this weak avalanche current imposes an upper limit to the output impedance achievable with the gain-boosting technique.

8.4. Applications of the Super-MOST

The Super-MOST can be used as a normal MOS transistor. As an example, a current mirror has been realized as shown in figure 16a. Figure 16b shows the measured results for a *P*-type current mirror at several input currents and output voltages. The mirror accuracy is independent of output voltage and is only determined by matching.

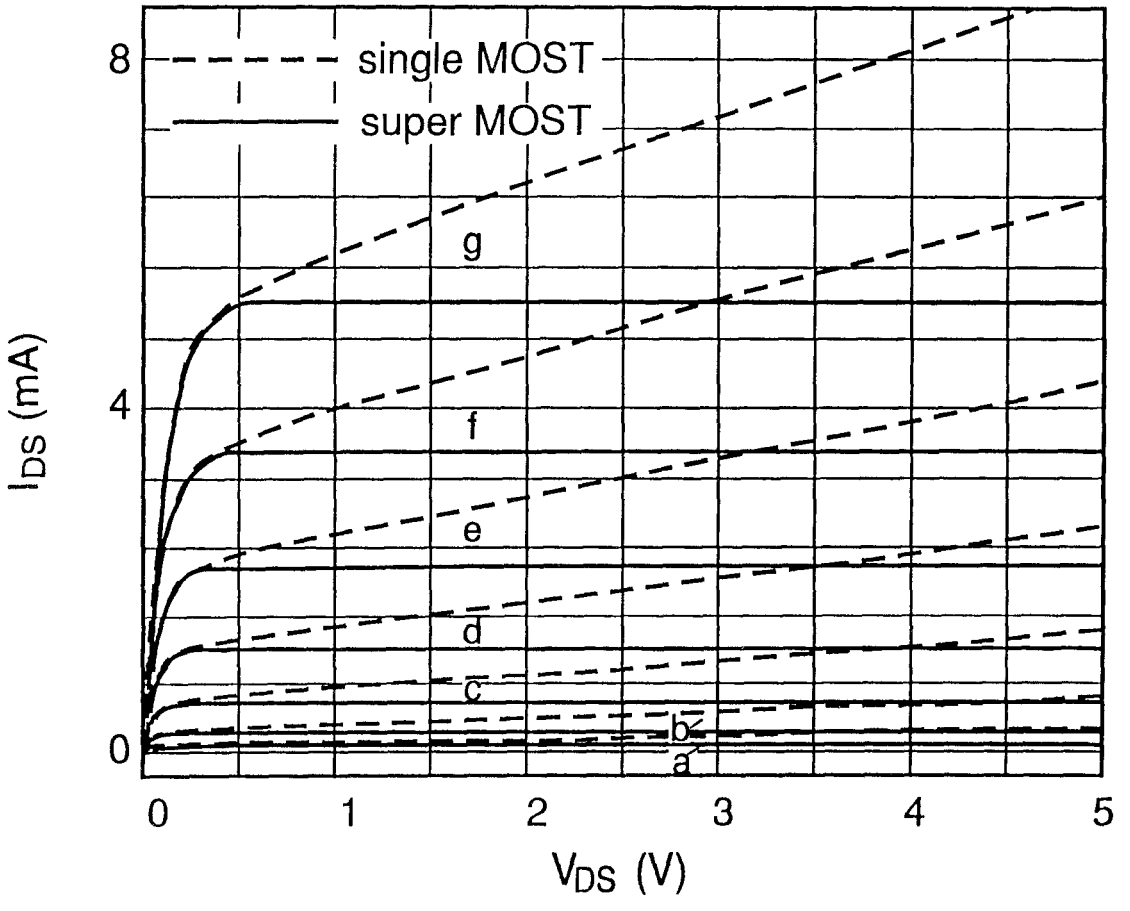

Fig. 15. a) Measured $I_{ds} - V_{ds}$ characteristics of single N-type MOST and Super-MOST for V_{gs} ranging from 0.7V (a) to 1.0V (g).

The F terminal of the Super-MOST provides a very low-ohmic current input which can be used for folded-cascode structures [2]. In figure 17 measurement results of a P-type Super-MOST show an input impedance lower than 1 ohm for low frequencies.

As an example, figure 18 shows a straightforward circuit topology of a folded-cascode opamp but now realized with Super-MOST's. Note that the tail current of the differential input-pair also consists of a Super-MOST. In this way the common-mode rejection ratio CMRR is increased several orders of magnitude for low frequencies. For the input-pair, normal transistors have been used. Measured results of this straightforward design are equivalent to the results shown in table 1.

Figure 19 shows the die photograph of the chip, containing 1 opamp, 1 N-type Super-MOST, and 2 P-type Super-MOST's. As can be seen, a Super-MOST consumes only 20 percent more chip area compared to a normal cascoded transistor. With a more careful layout this can be even further reduced. Because there is no need for extra biasing, the total opamp chip area is more than 25 percent smaller as compared to the design of figure 9.

8.5. Advantages of the Super-MOST

There are several advantages in using Super-MOST's as a building block in circuit design:

1. The design of high-quality opamps, OTAs, current sources, etc., can be split into two parts. First the design of the Super-MOSTs, in which the knowledge of proper biasing, gain-boosting, optimal settling, and stability is used. Much attention can be paid to an optimal layout also, as this subcircuit is going to be used in many designs at several points in the comprising circuit. Secondly, the design of the comprising circuit, which now becomes rather straightforward. In this higher-level design no knowledge of the gain-boosting principle or of optimal biasing of a cascode transistor is required. This eases the design of such circuits and shortens the design time considerably.

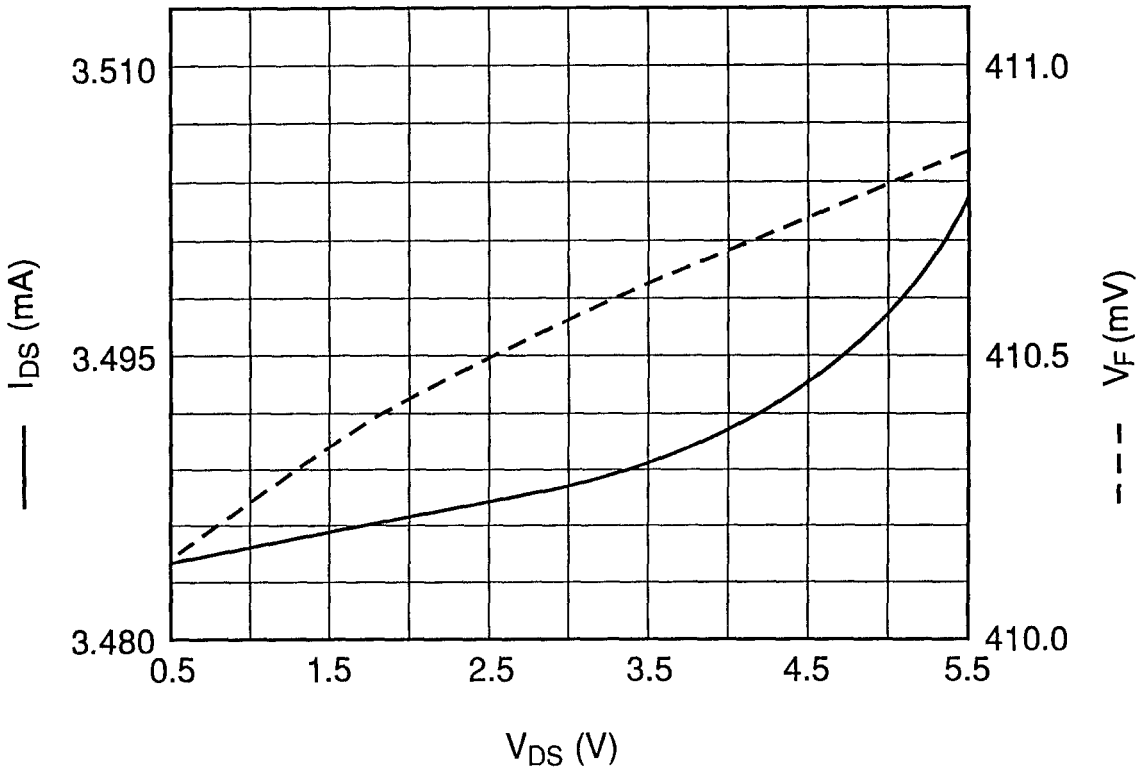

Fig. 15. b) Enlargement of curve f of figure 15a.

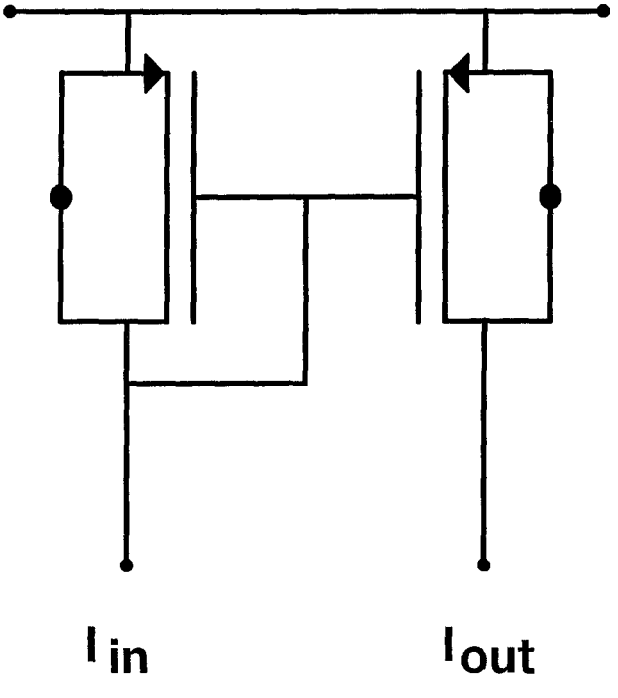

Fig. 16. a) Current mirror with Super-MOSTs.

2. The design of Super-MOSTs is very suitable for parameterized automatic generation.
3. As each Super-MOST is self-biasing, no long biasing wires are required on chip, leading to a design that is much less susceptible to cross-talk and therefore also for instability problems.
4. As wiring usually consumes a relatively large part of the chip area, the approach presented here consumes considerably less chip area.

Comparison of the die-photographs of figures 9 and 19 clearly shows the difference in design strategy with and without Super-MOSTs.

9. Conclusions

A technique is presented which decouples the DC-gain and unity-gain frequency of an opamp. A very high DC-gain can be achieved in combination with any unity-gain frequency achievable by a (folded-) cascode design.

With this technique, an opamp is realized in a standard 1.6-μm CMOS process, which has a DC-gain of 90 dB together with a unity-gain frequency of 116 MHz. The opamp shows one-pole roll-off and single-pole settling behavior.

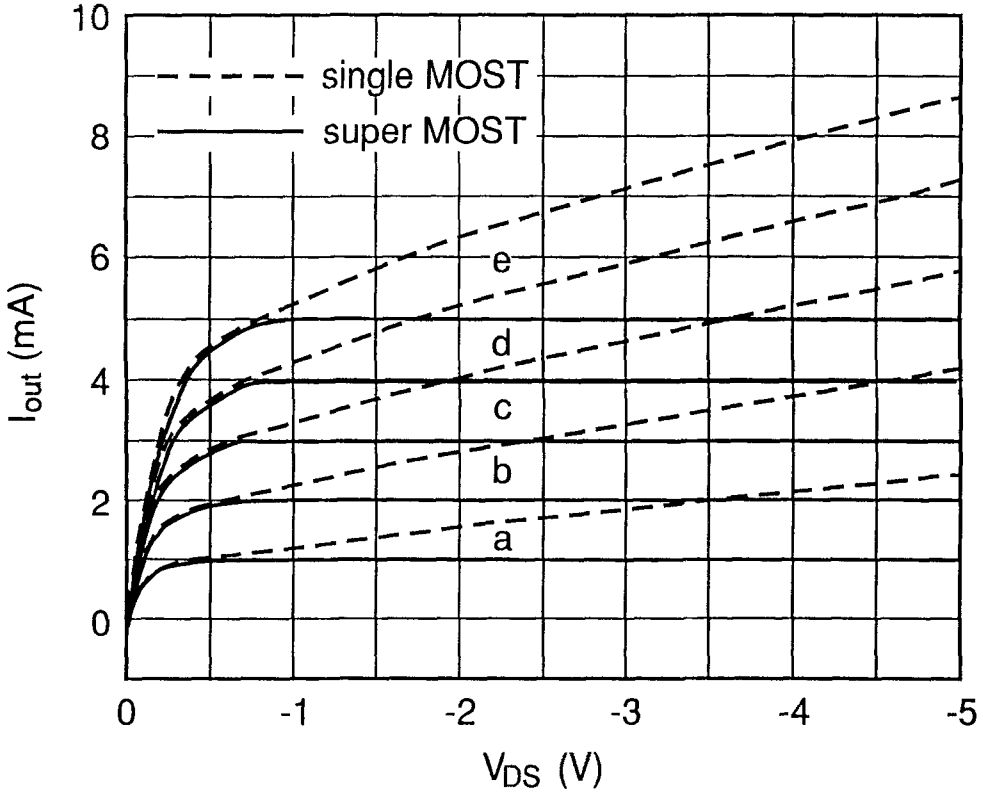

Fig. 16. b) Measured output current of a P-type current mirror with I_{in} ranging from 1.0 mA (a) to 5.0 mA (e).

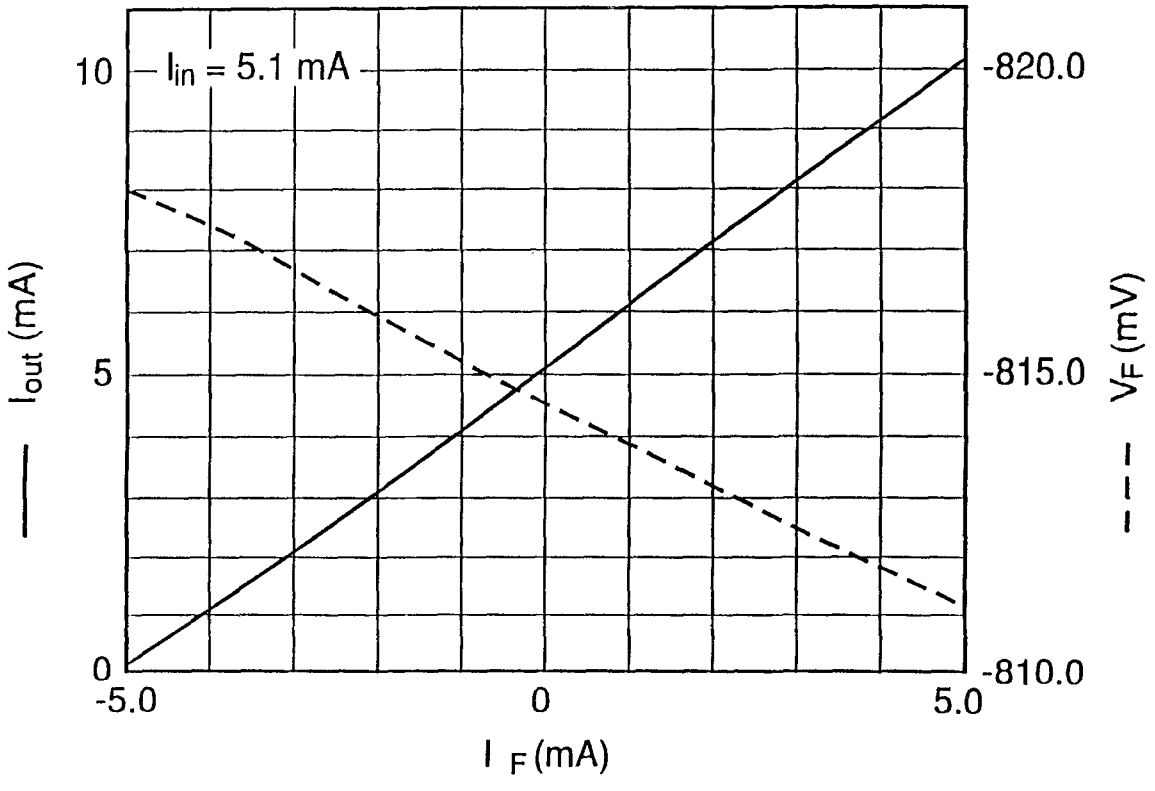

Fig. 17. Measured output current I_{out} and terminal voltage V_f as a function of I_f for a P-type Super-MOST.

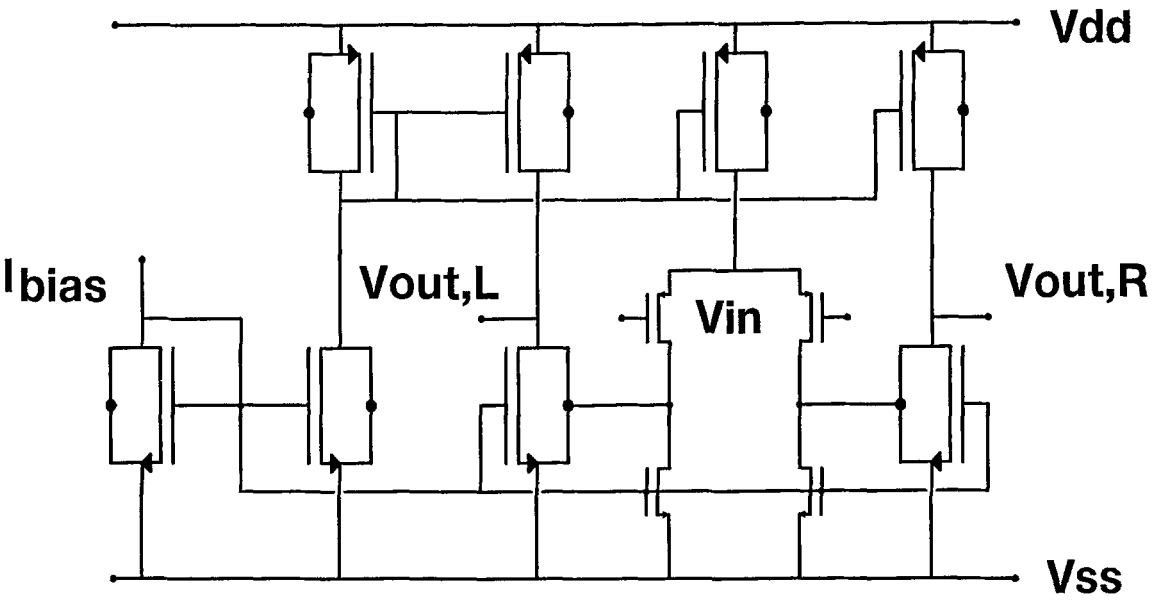

Fig. 18 Folded-cascode opamp realized with Super-MOSTs.

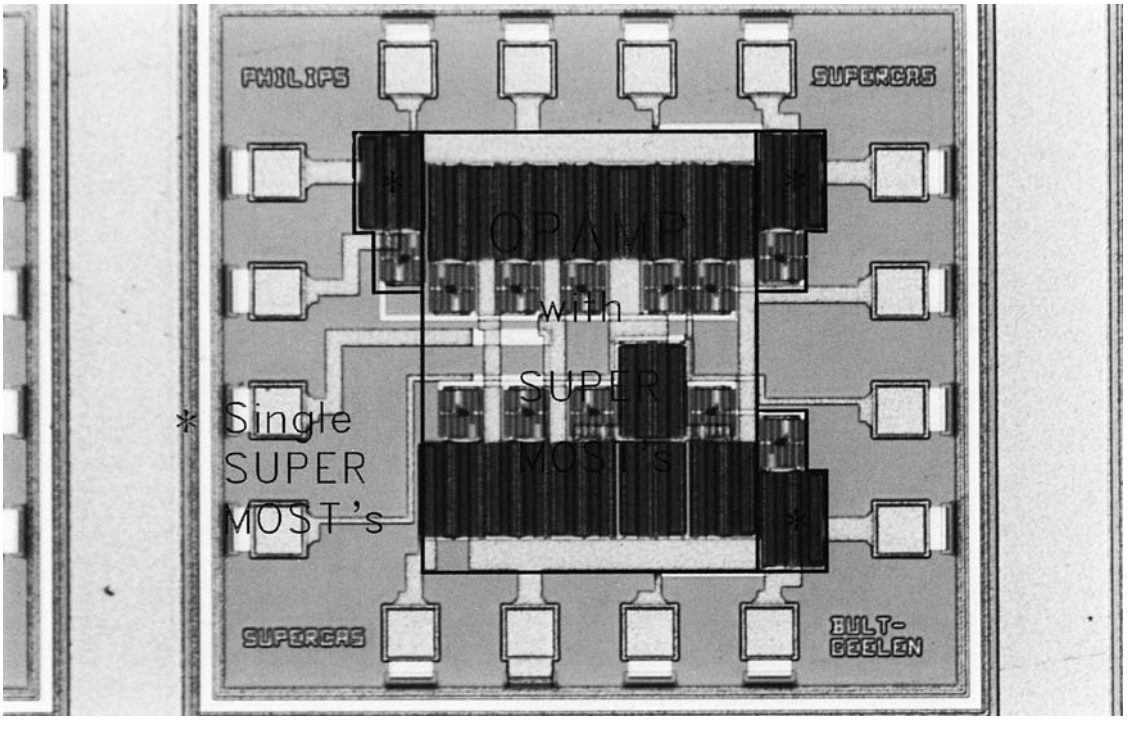

Fig. 19. Die photograph of Super-MOST opamp.

This technique does not cause any loss in output voltage swing. At a supply voltage of 5.0 V, an output swing of about 4.2 V is achieved without loss in DC-gain.

The advantages above are achieved with only an increase in chip area of 30 percent and an increase in power consumption of 15 percent.

The Super-MOST presented here considerably eases the design of high-gain amplifiers. As the building block is completely self-biasing, there are no long wires in the design, reducing cross-talk, instability, and chip area.

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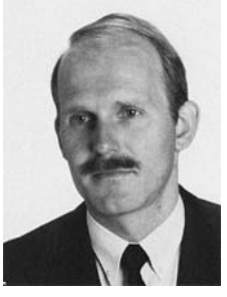

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