B-KUL-H05E3A Design Project

Switched-Capacitor Amplifier

Specification table

Group #	f_s [MHz]	SNR_{min} [dB]	ε_{gain} [%]	ε_{set} [%]	PM_{min} [°]	C_L [pF]	V_{in} [mV_{pp}]	A_{CL} [V/V]	Input pair
1	50	45	0.04	2	60	2	50~100	10	pMOS
2	50	45	0.05	2.2	60	2	50~100	10	nMOS
3	55	45	0.05	2.4	60	2	50~100	10	pMOS
4	55	45	0.06	2.6	60	2	50~100	10	nMOS
5	60	45	0.06	2.8	60	2	50~100	10	pMOS
6	60	45	0.07	3.0	60	2	50~100	10	nMOS
7	65	45	0.07	3.2	60	2	50~100	10	pMOS
8	65	45	0.04	5	60	2	50~100	10	nMOS
9	70	45	0.04	5.2	60	2	50~100	10	pMOS
10	70	45	0.05	5.4	60	2	50~100	10	nMOS
11	75	45	0.05	5.6	60	2	50~100	10	pMOS
12	75	45	0.06	5.8	60	2	50~100	10	nMOS
13	80	45	0.06	6.0	60	2	50~100	10	pMOS
14	80	45	0.07	6.2	60	2	50~100	10	nMOS
15	50	47	0.06	3	60	2.5	50~100	10	pMOS
16	50	47	0.07	3.2	60	2.5	50~100	10	nMOS
17	55	47	0.07	3.4	60	2.5	50~100	10	pMOS
18	55	47	0.08	3.6	60	2.5	50~100	10	nMOS
19	60	47	0.08	3.8	60	2.5	50~100	10	pMOS
20	60	47	0.09	4	60	2.5	50~100	10	nMOS
21	65	47	0.09	4.2	60	2.5	50~100	10	pMOS
22	65	47	0.06	5	60	2.5	50~100	10	nMOS
23	70	47	0.06	5.2	60	2.5	50~100	10	pMOS
24	70	47	0.07	5.4	60	2.5	50~100	10	nMOS
25	75	47	0.07	5.6	60	2.5	50~100	10	pMOS
26	75	47	0.08	5.8	60	2.5	50~100	10	nMOS
27	80	47	0.08	6.0	60	2.5	50~100	10	pMOS
28	80	47	0.09	6.2	60	2.5	50~100	10	nMOS
29	80	42	0.06	2.2	60	1.5	50~100	10	nMOS
30	50	42	0.06	2.4	60	1.5	50~100	10	pMOS
31	50	42	0.07	2.6	60	1.5	50~100	10	nMOS
32	55	42	0.06	2.8	60	1.5	50~100	10	pMOS
33	55	42	0.07	3.0	60	1.5	50~100	10	nMOS

f_s	Sampling frequency
SNR_{min}	Output signal to noise ratio @minimum input swing (i.e., $50mV_{pp}$)
ε_{gain}	Static gain error
ε_{set}	Dynamic settling error
PM_{min}	Minimum phase margin in worst case (i.e., unity-gain feedback)
C_L	Load capacitor
V_{in}	Peak-to-peak differential input swing (Note: amplitude is 25~50mV)
A_{CL}	Magnitude of closed-loop gain at low frequencies