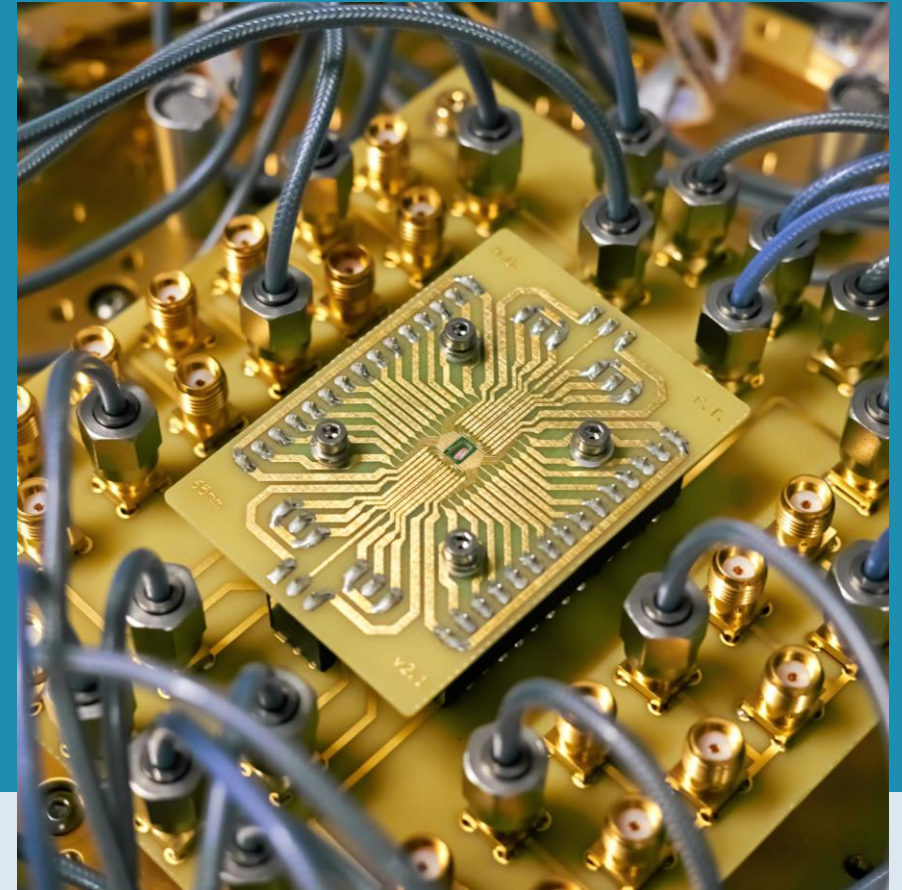


Design of Analog and Mixed-Signal Integrated Circuits B-KUL-H05E3A

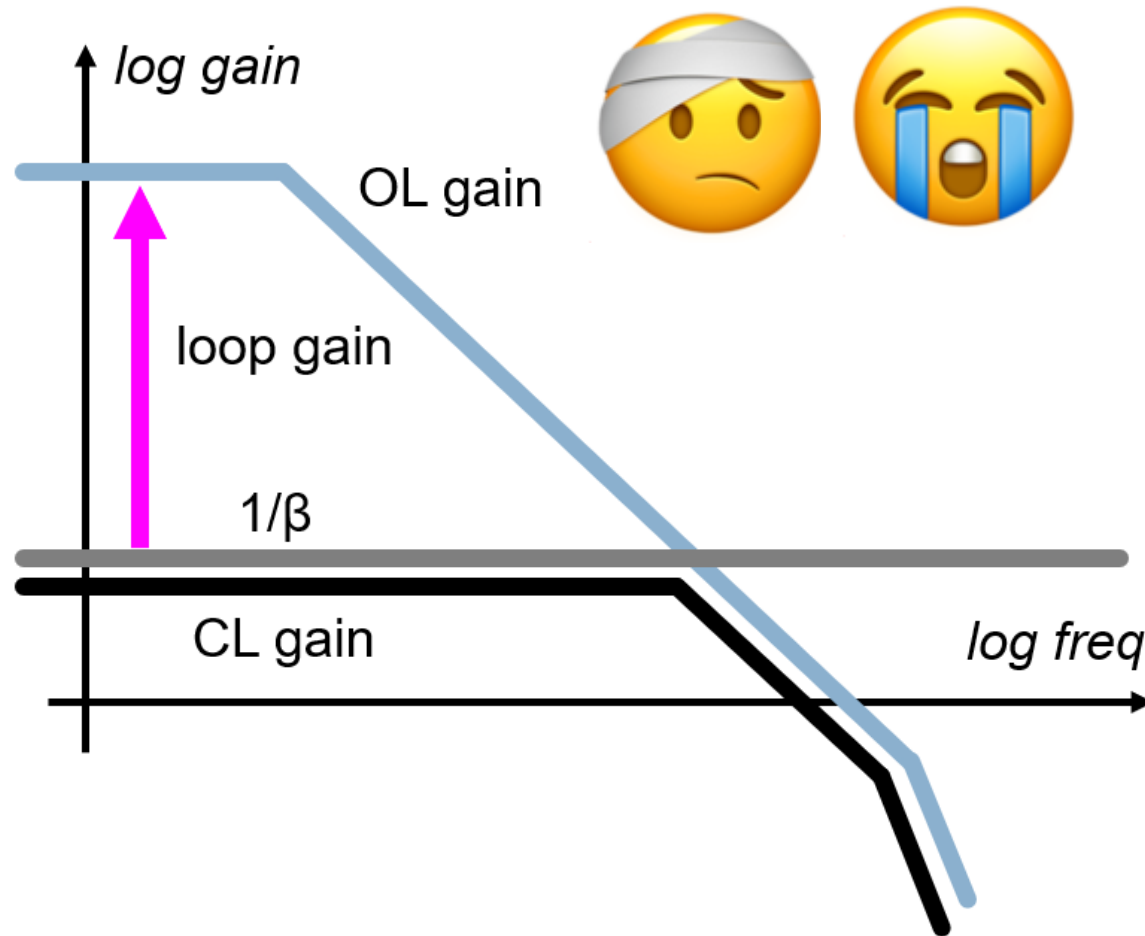
Gain-Boosting + Advice Session 6

Ir. Alberto Gatti, Jun Feng, Shuangmu Li, Prayag Wakale
Prof. Filip Tavernier and prof. Tim Piessens
Departement Elektrotechniek (ESAT)

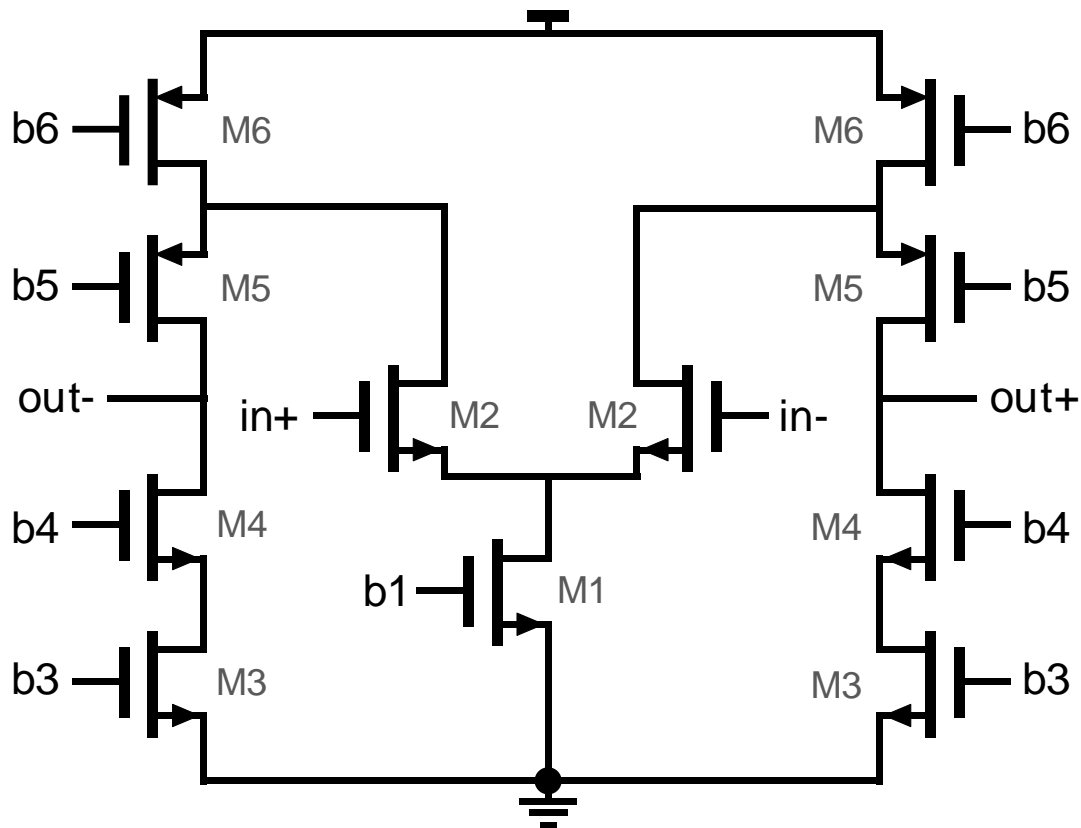


Gain Boosting

Struggling to get more gain?



Folded cascode? not much better



- ❗ Cascoding through current subtraction, not via mirroring
- ❗ But, gain again mainly set by two transistors (M2, M5) and output impedance of M4, M3

A technique to consider...

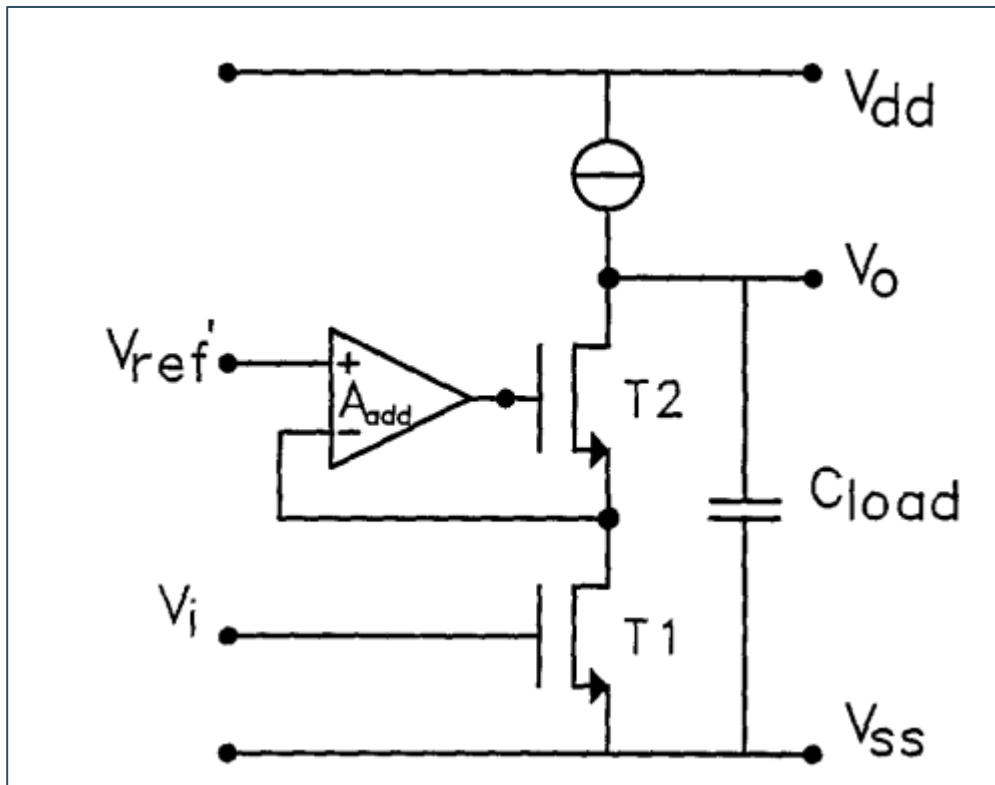
The CMOS Gain-Boosting Technique

KLAAS BULT AND GOVERT J.G.M. GEELEN

Philips Research Laboratories, Eindhoven, The Netherlands

Received January 9, 1991; Revised April 5, 1991.

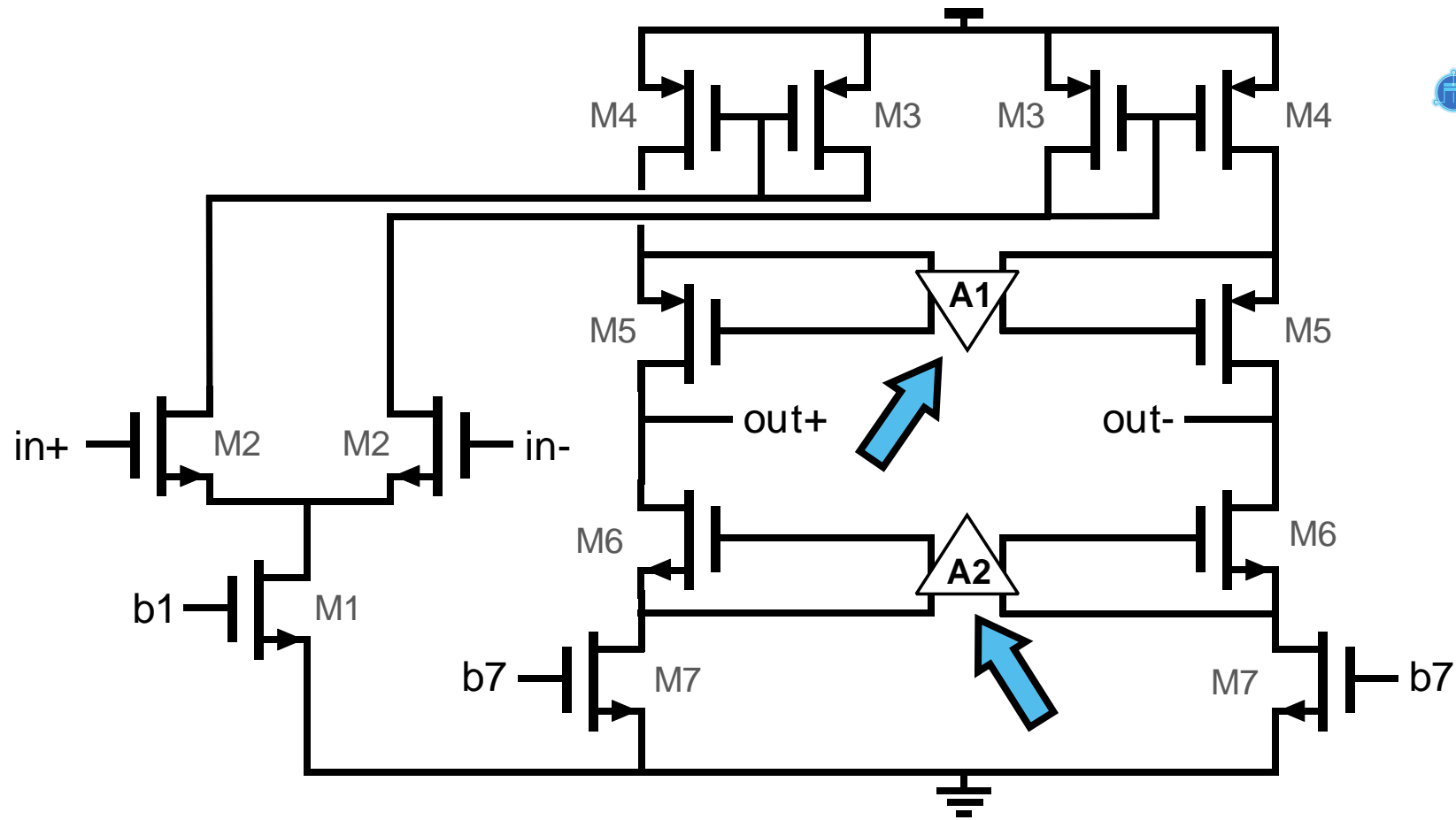
Gain-boosting



- **Additional gain A_{add}**
- In some books “regulated cascode”

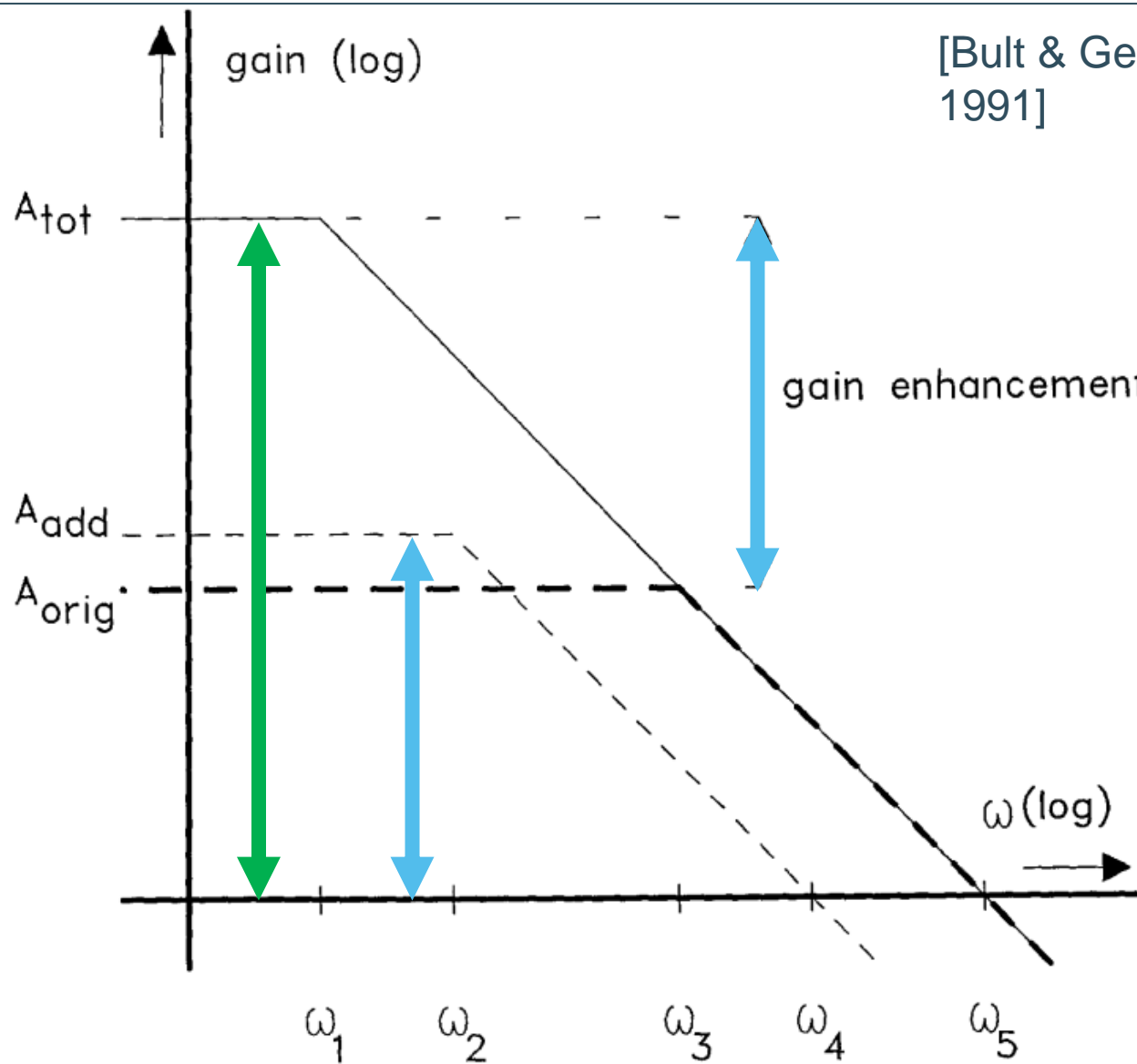
[Bult & Geelen, 1991]

Gain-boosting in DAMSIC



On both high and low sides!

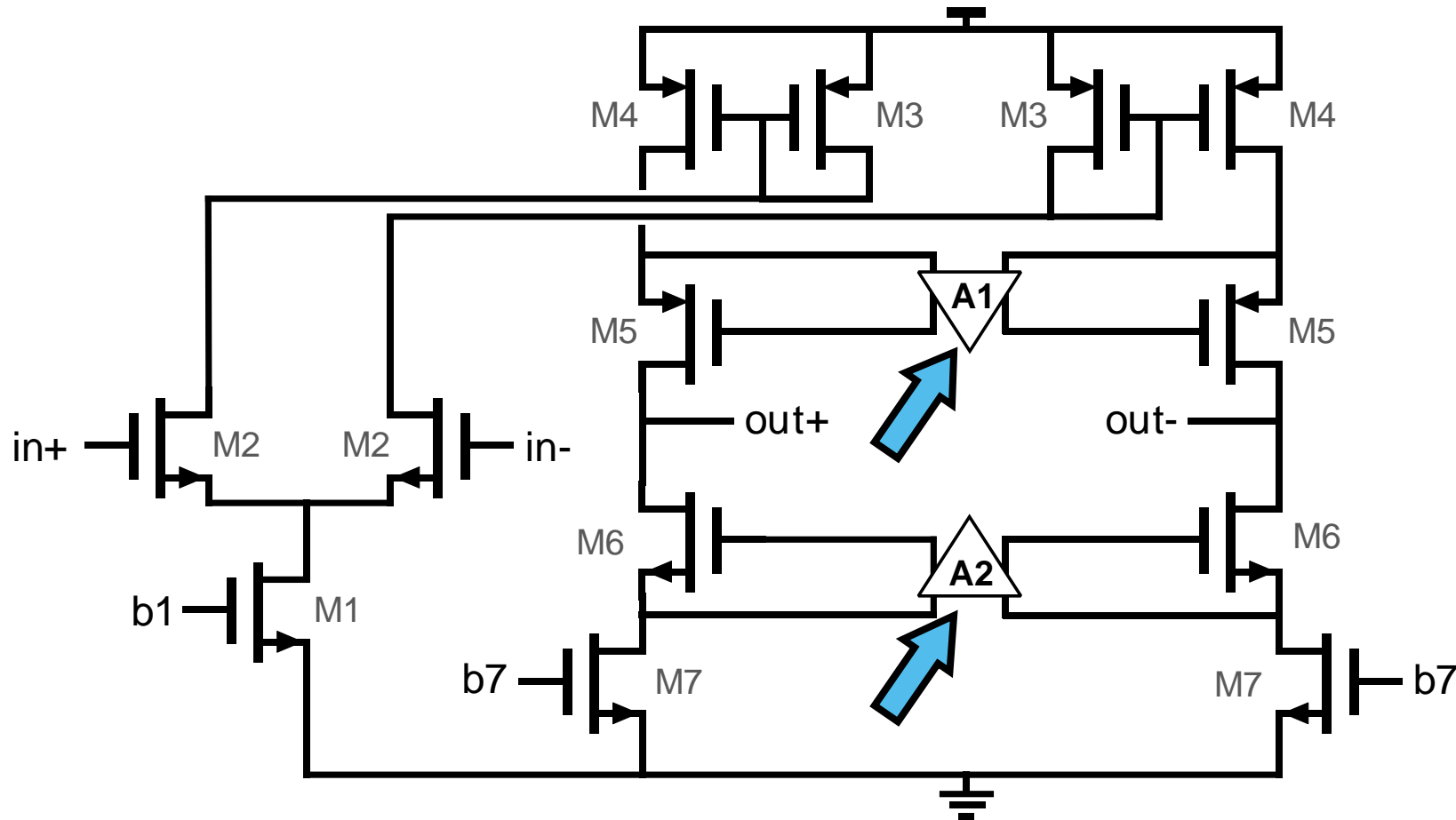
[Bult & Geelen, 1991]



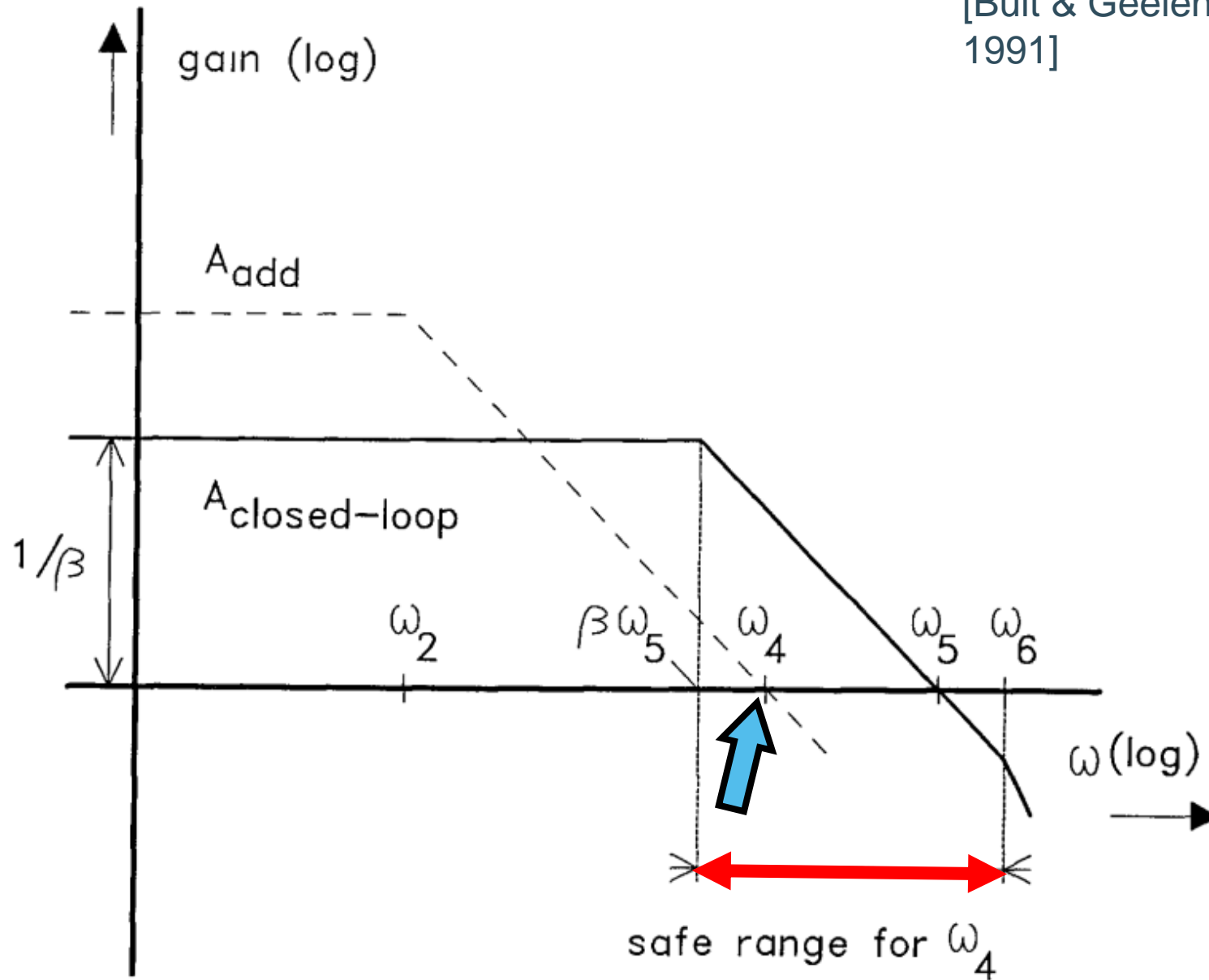
In **your case**:

- $A_{\text{orig}} = (g_m r_o)^2$
- A_{add} depends on the gain boosting OTA
- “How fast does A_{add} need to be...?”

Good question!



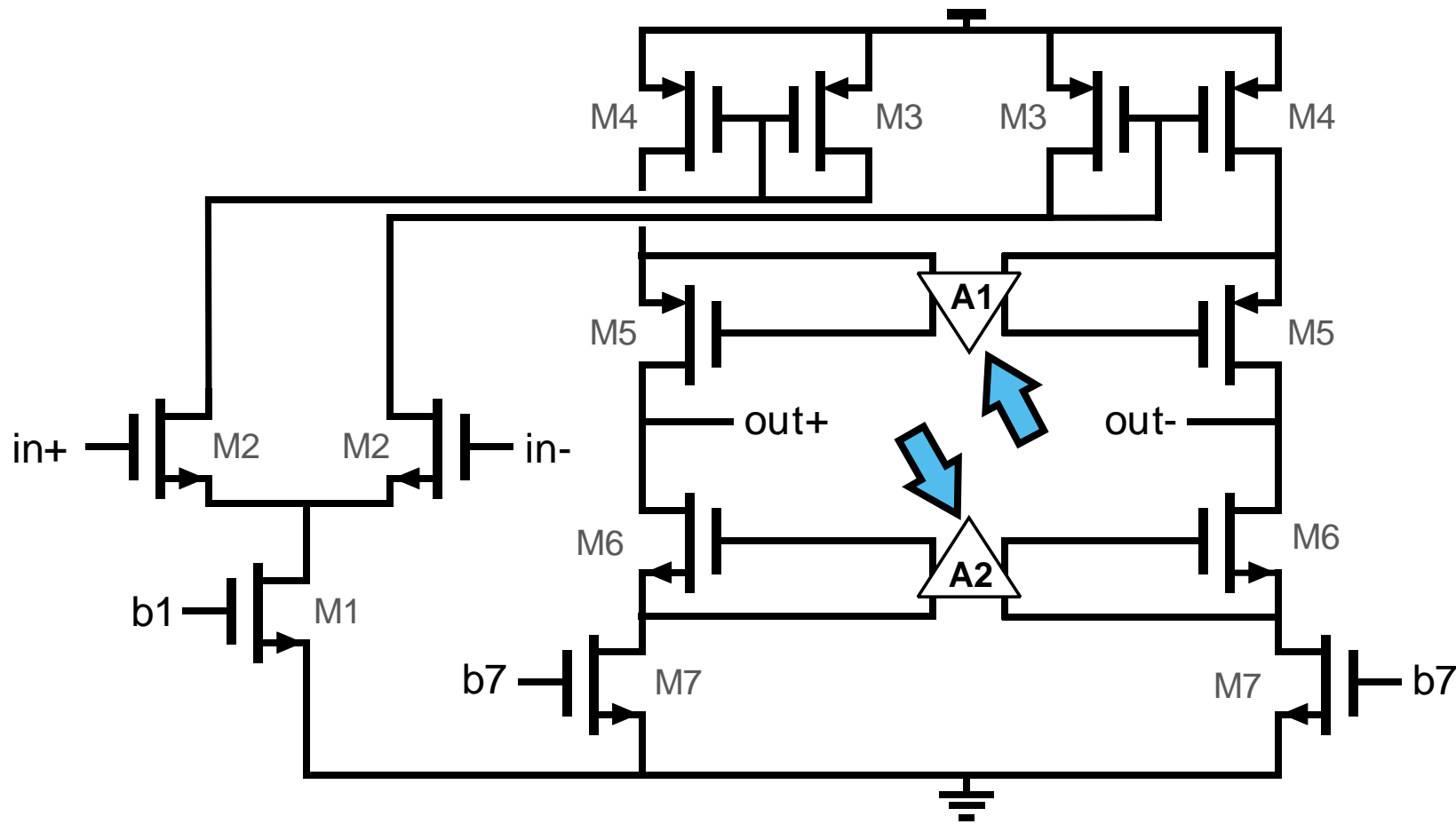
- Too slow:
 - **Settling issues**
- Too fast:
 - **Stability issues!**
- Main difference?
 - Small load...



Bult to the rescue, again

- Within safe range, near the GBW of the original design
- Start with the **same speed...!**

In practice? Recall that the load is small!

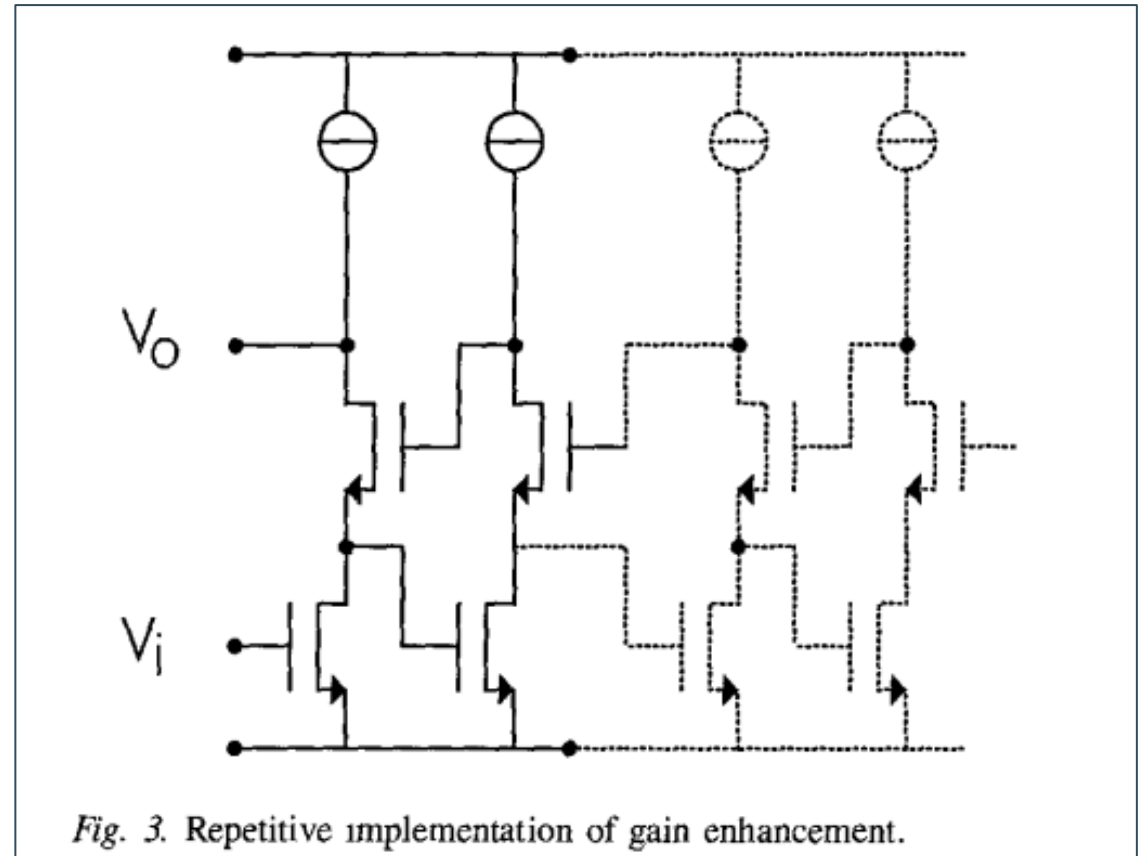


- Just insert an additional **capacitor** that dominates the loop. Your OTA is small 😊
- STB analysis is your friend!

Why is this such a popular technique?

- 🔌 Infinite gain @ max. speed
- 🔌 Good use of supply!

[Bult & Geelen,
1991]



Suggested design method



Use the **idealOTA** to verify/understand gain-boosting

- Main difference is lack of CMFB..!
- Especially learn to check stability!



Draw up specs for the boosting OTA

- Main difference = size, output CM... + add another CMFB loop!

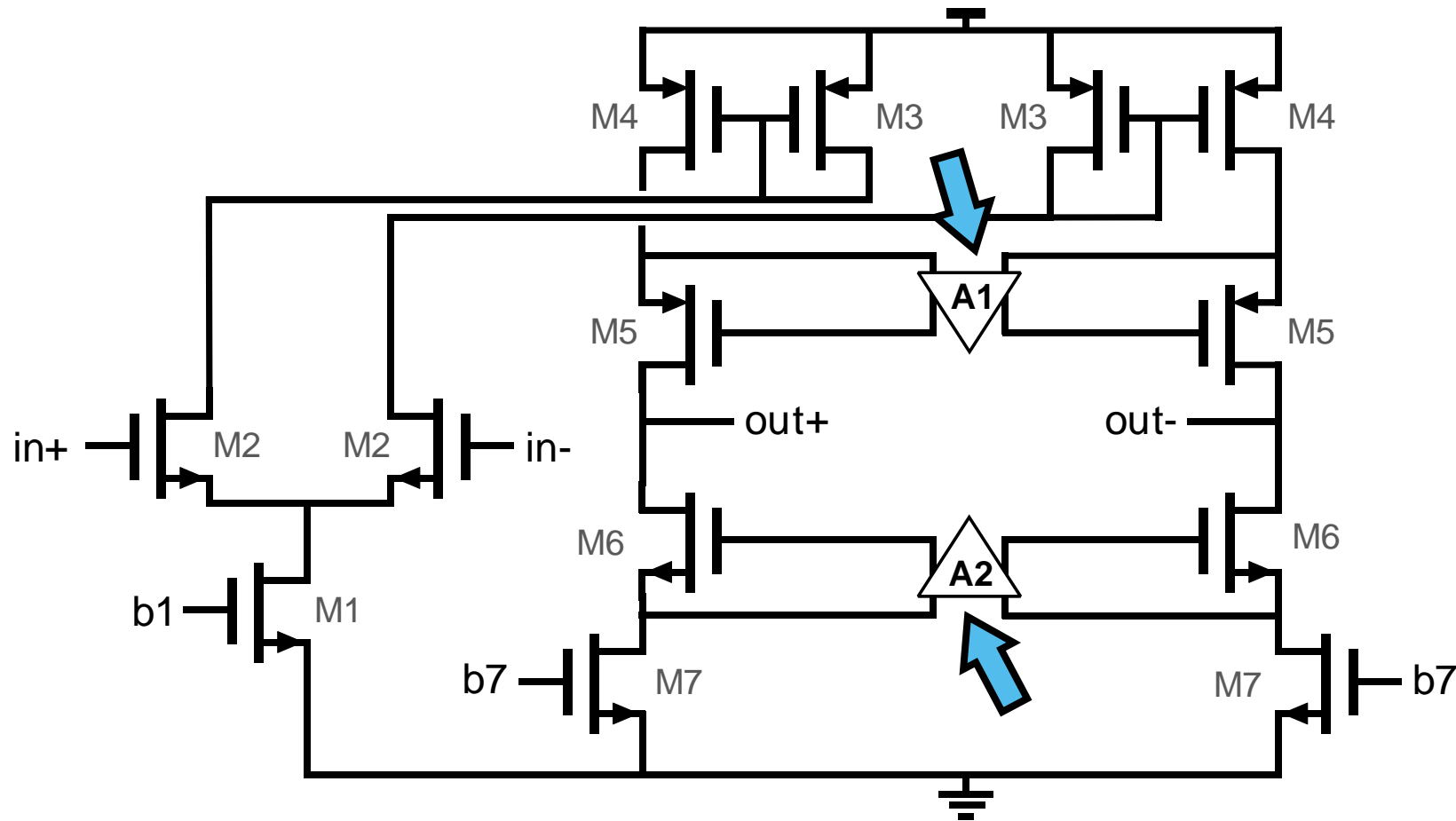


Design boosting OTA – what can you do with a folded-cascode?

- Check DC operating point and stability! Probably need to retune C_{ADD}



Rescale for noise if needed



If time is tight:

A1 can be the same as A2...

→ **Use DC sources to shift operating points**

Feel free to do even better!

References

- 🔗 Paper by Bult and Geelen → see Toledo
 - Should be enough
- 🔗 Razavi's CMOS design book has a short subsection on it
 - But no deep explanation of the settling / stability issues
- 🔗 Some videos on Youtube, but above should be sufficient!

Next Weeks & Final Assessment

Remaining design sessions 6, 7, 8

- 🔧 For you to work on gain boosting with folded cascode
 - No more extra material
- 🔧 Intermediate report 2: symmetric OTA by next Monday noon
 - Feedback next week Tuesday morning
- 🔧 Session 8: extra 30 mins to compensate for P&D

After that: prepare for final assessment



Final Report: May 2nd at noon

- Merge 3 reports, key part is gain-boosted OTA design
- **Everyone** submits one on their own (for admin reasons)



Oral Presentations: May 9th

- Slides: **upload in advance by 7th of May**
- 5 min presentation + 10 min Q&A (longer for trio)
- Detailed info + schedule will follow on Toledo

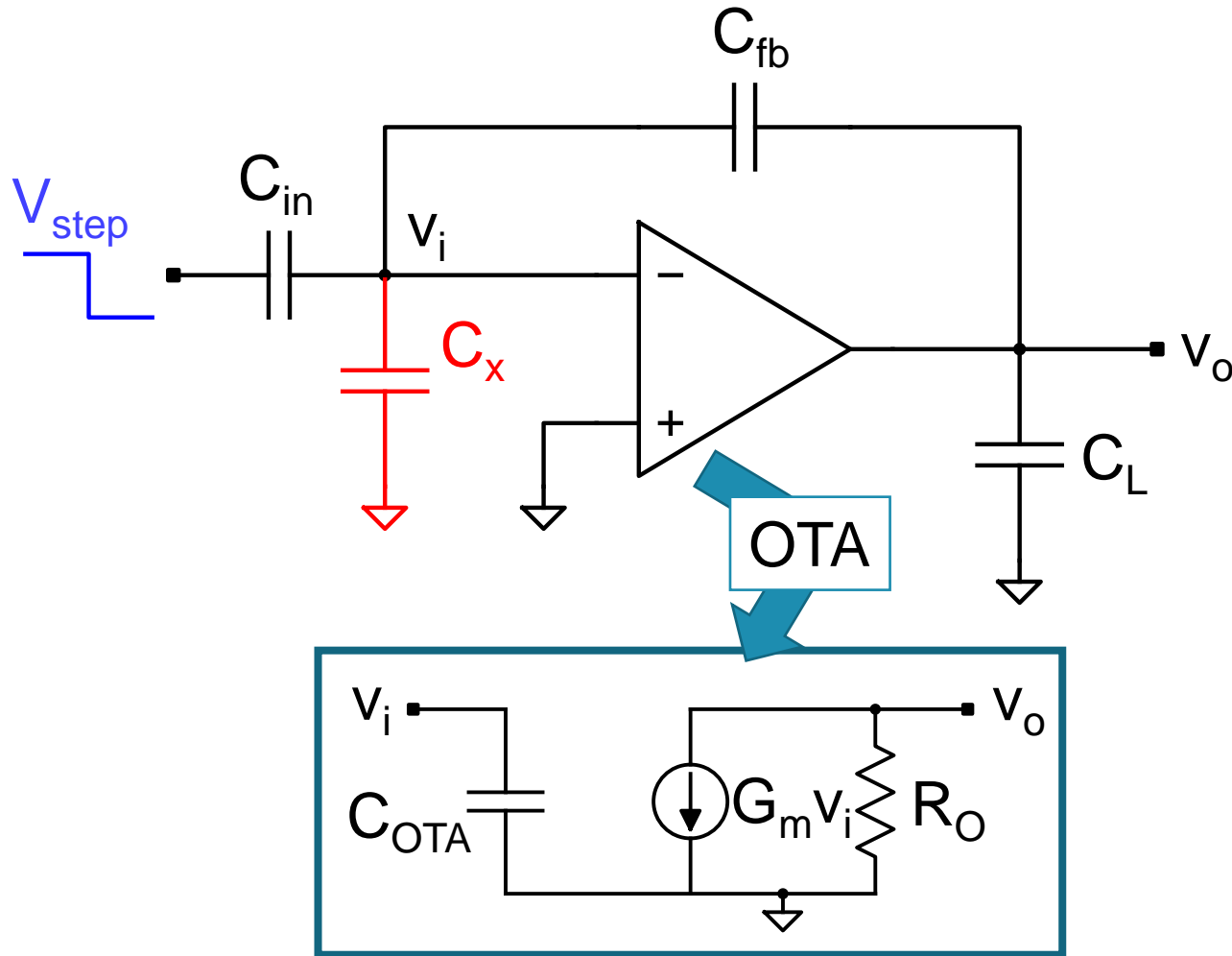
Thanks, questions?

Bonus Material

“Why don’t the posted targets work from the get-go?”

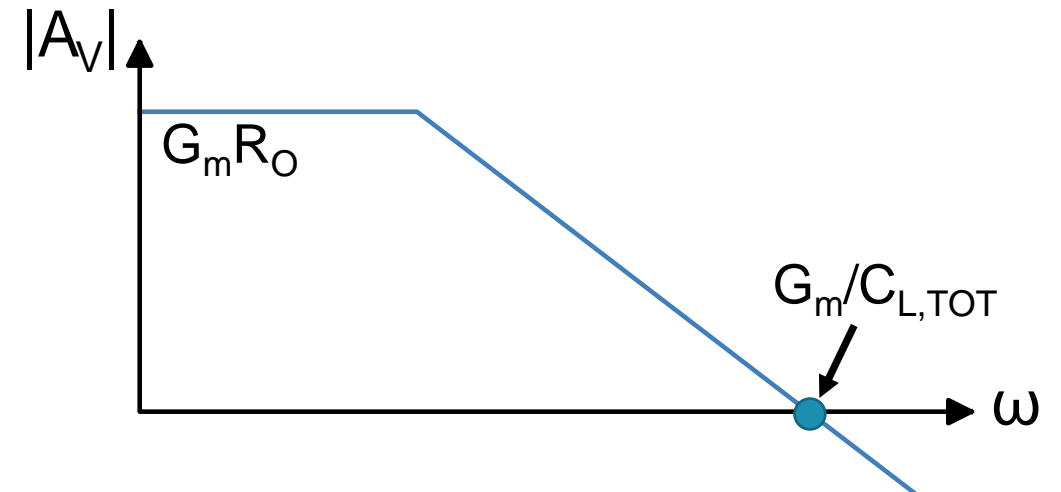
One aspect: parasitics at OTA input

Analysis of transient response in phase ϕ_2

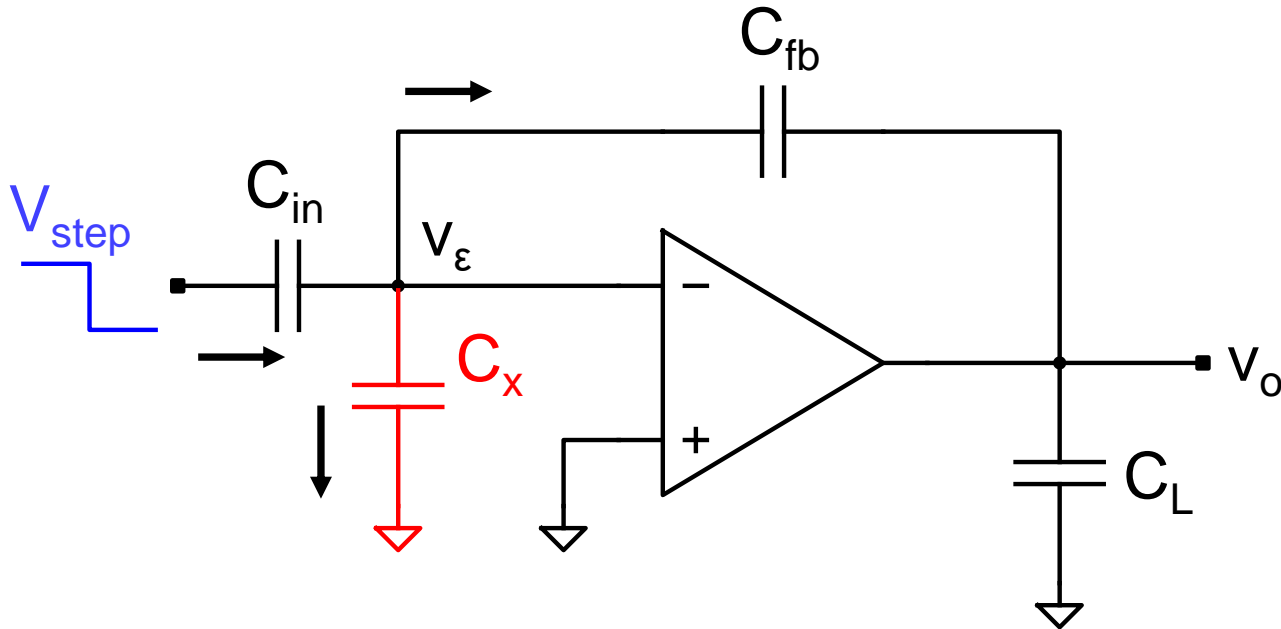


V_{step} = voltage on C_{in} at the end of the sampling phase

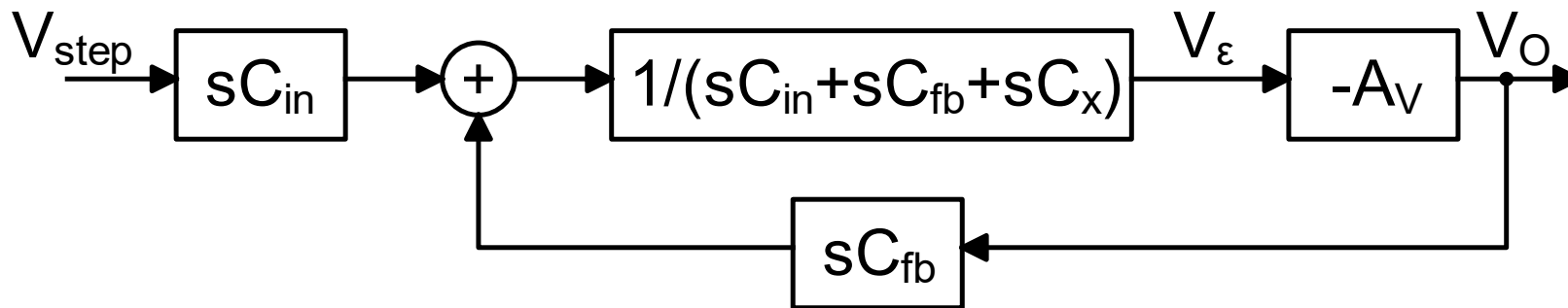
$$\frac{V_O(s)}{V_I(s)} = -A_V = -\frac{G_m R_O}{1 + s R_O C_{L,TOT}}$$



Effective circuit

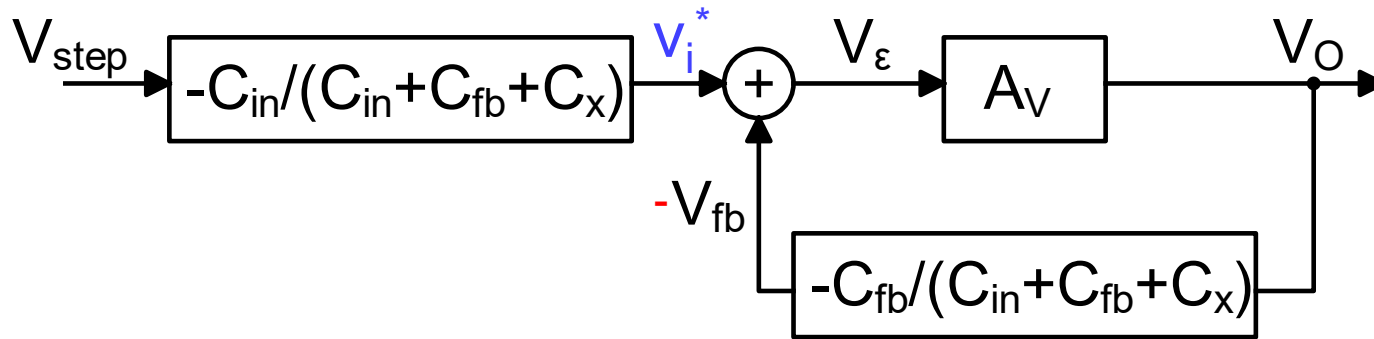


- Finite gain OTA $\rightarrow V_{\epsilon} \neq 0$
- $sC_{in}(V_{step} - V_{\epsilon}) = sC_x V_{\epsilon} + sC_{fb}(V_{\epsilon} - V_O)$
- $$V_{\epsilon} = \frac{sC_{in}V_{step} + sC_{fb}V_O}{s(C_{in} + C_x + C_{fb})}$$
- The feedback signal is a current!



**Shunt/shunt
feedback!**

A few tricks on the block diagram...



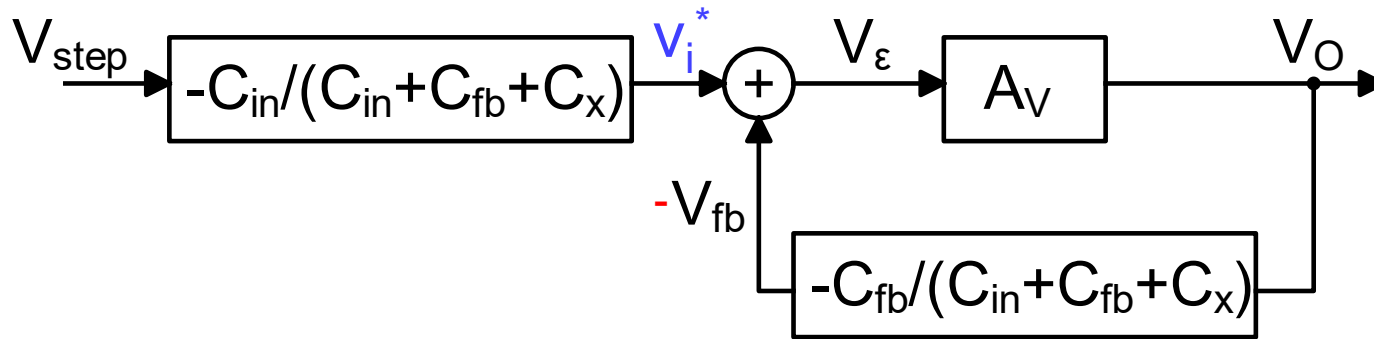
v_i^* is just a rescaled version of the input

$$\beta = \frac{V_{fb}}{V_O} = \frac{C_{fb}}{C_{in} + C_{fb} + C_x}$$

$$-\frac{C_{in}}{C_{in} + C_{fb} + C_x} = -\frac{C_{in}}{C_{fb}} \beta$$

$$\frac{V_O}{V_{step}} = -\frac{C_{in}}{C_{fb}} \beta \frac{A_V}{1 + \beta A_V} = \underbrace{-\frac{C_{in}}{C_{fb}}}_{\text{Ideal gain}} \cdot \underbrace{\frac{G_m R_O \beta}{1 + G_m R_O \beta}}_{\text{Gain error}} \cdot \underbrace{\frac{1}{1 + s \frac{C_{L,TOT}}{\beta G_m}}}_{\text{Settling error}}$$

To the time domain



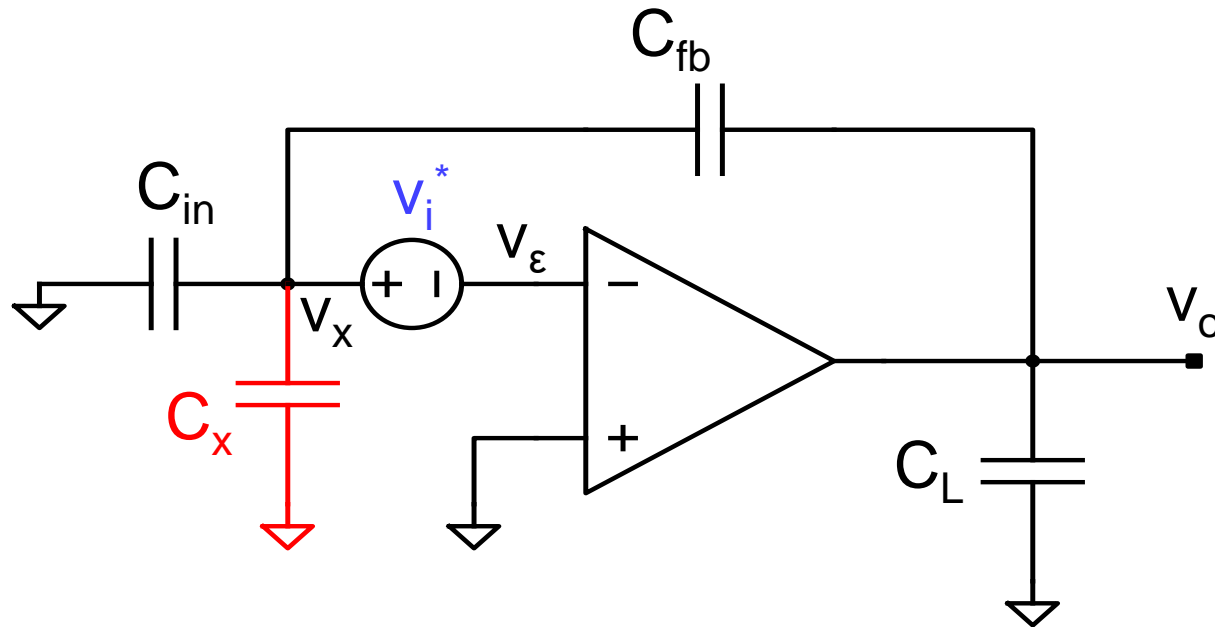
v_i^* is just a rescaled version of the input

$$\beta = \frac{V_{fb}}{V_O} = \frac{C_{fb}}{C_{in} + C_{fb} + C_x}$$

$$\text{⚙️ } v_O(t) = -\frac{C_{in}}{C_{fb}} V_{step} \cdot \frac{G_m R_O \beta}{1 + G_m R_O \beta} \cdot (1 - e^{-t/\tau})$$

$$\tau = \frac{1}{\omega_u} = \frac{1}{\frac{\beta G_m}{C_{L,TOT}}}$$

Feedback and load



$$C_{L,TOT} = C_L + \frac{C_{fb}(C_{in} + C_x)}{C_{fb} + C_{in} + C_x} = C_L + C_{fb}(1 - \beta)$$

$$\beta = \frac{C_{fb}}{C_{in} + C_{fb} + C_x}$$

$$\frac{V_O}{V_I^*} = \frac{A_V}{1 + \beta A_V} \approx \frac{1}{\beta} \frac{1}{1 + \frac{sC_{L,TOT}}{\beta G_m}}$$

