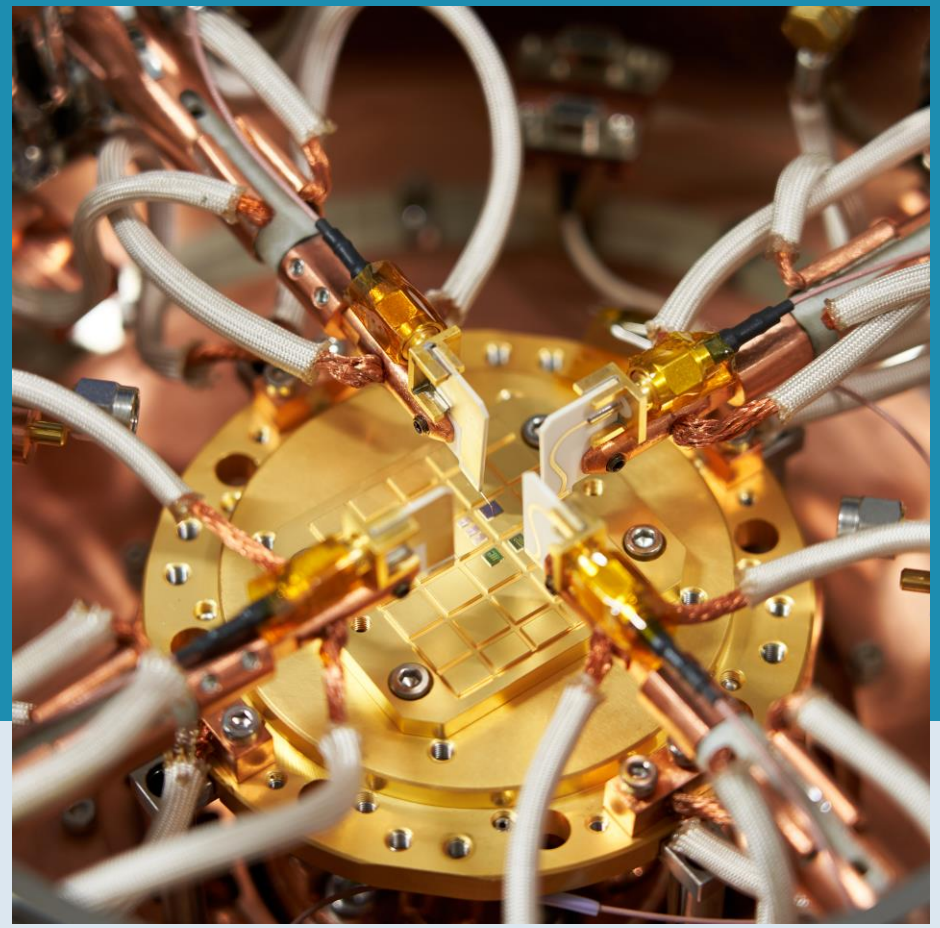
KU LEUVEN

Design of Analog and Mixed-Signal Integrated Circuits B-KUL-H05E3A

The g_m/I_D methodology



Alberto Gatti, Jun Feng, Shuangmu Li, Prayag J. Wakale, Ir.
Filip Tavernier, Tim Piessens, Prof. Dr. Ir.
Department of Electrical Engineering (ESAT)

Outline

- Motivation
  - Scaling in CMOS
  - Limitations of the Square Law model
- The g_m/I_D design approach
  - Basics
  - Extracting model data
- A design example
  - The IGS

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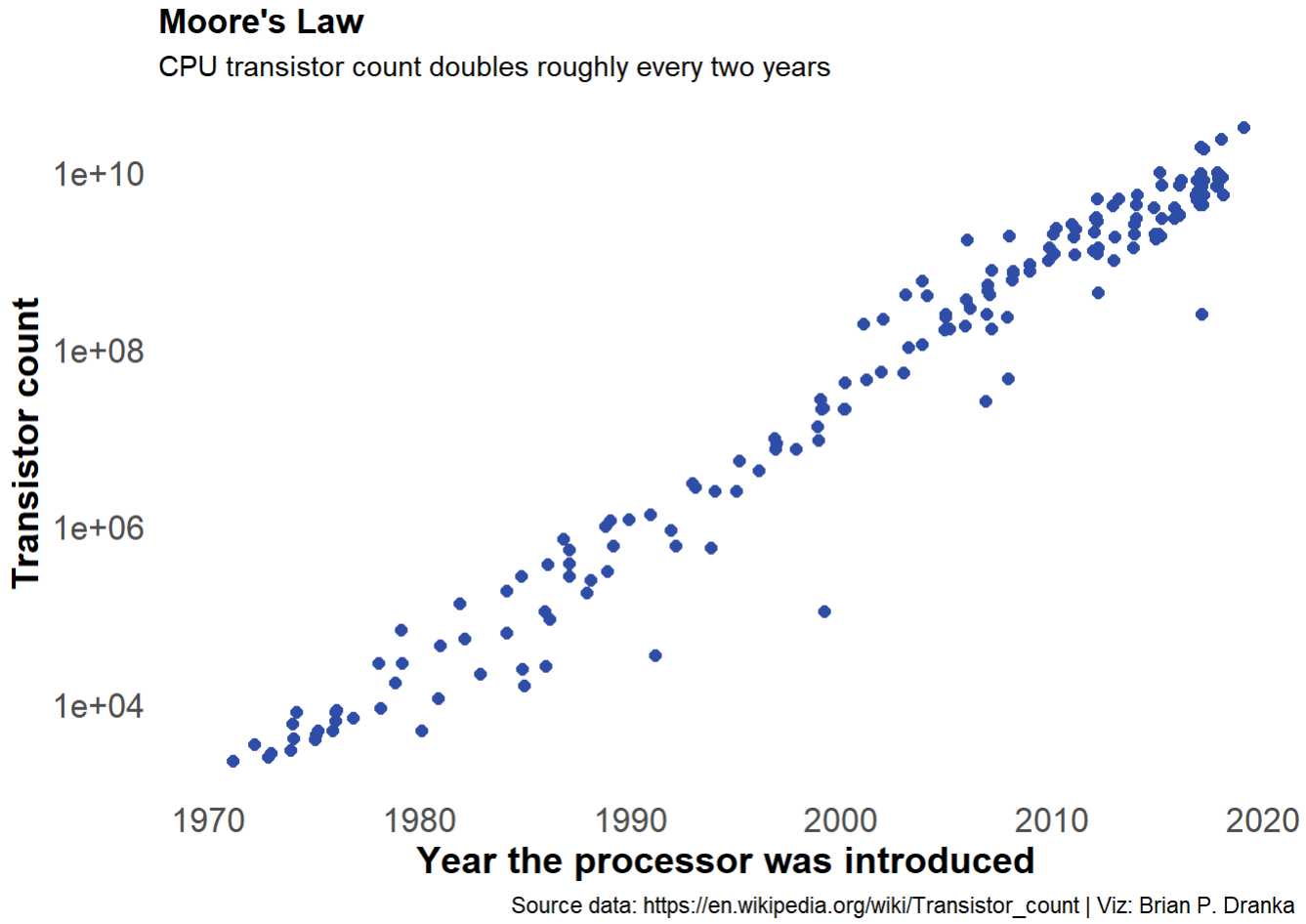
Why the scaling?

- Silicon area (transistor density)
- Speed (smaller parasitic caps)
- Power: $P_d \sim CV_{DD}^2 \cdot f$
- Analog is <u>always</u> essential…
  - Clock generation
  - Supply regulation
  - Sensor interfacing
- …but becomes challenging
  - Less intrinsic gain
  - Low V_{DD} → harder to reach high SNR
  - Worse 1/f noise



P. R. Kinget, "Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them," *2015 IEEE Custom Integrated Circuits Conference (CICC)*

Consequences of the scaling

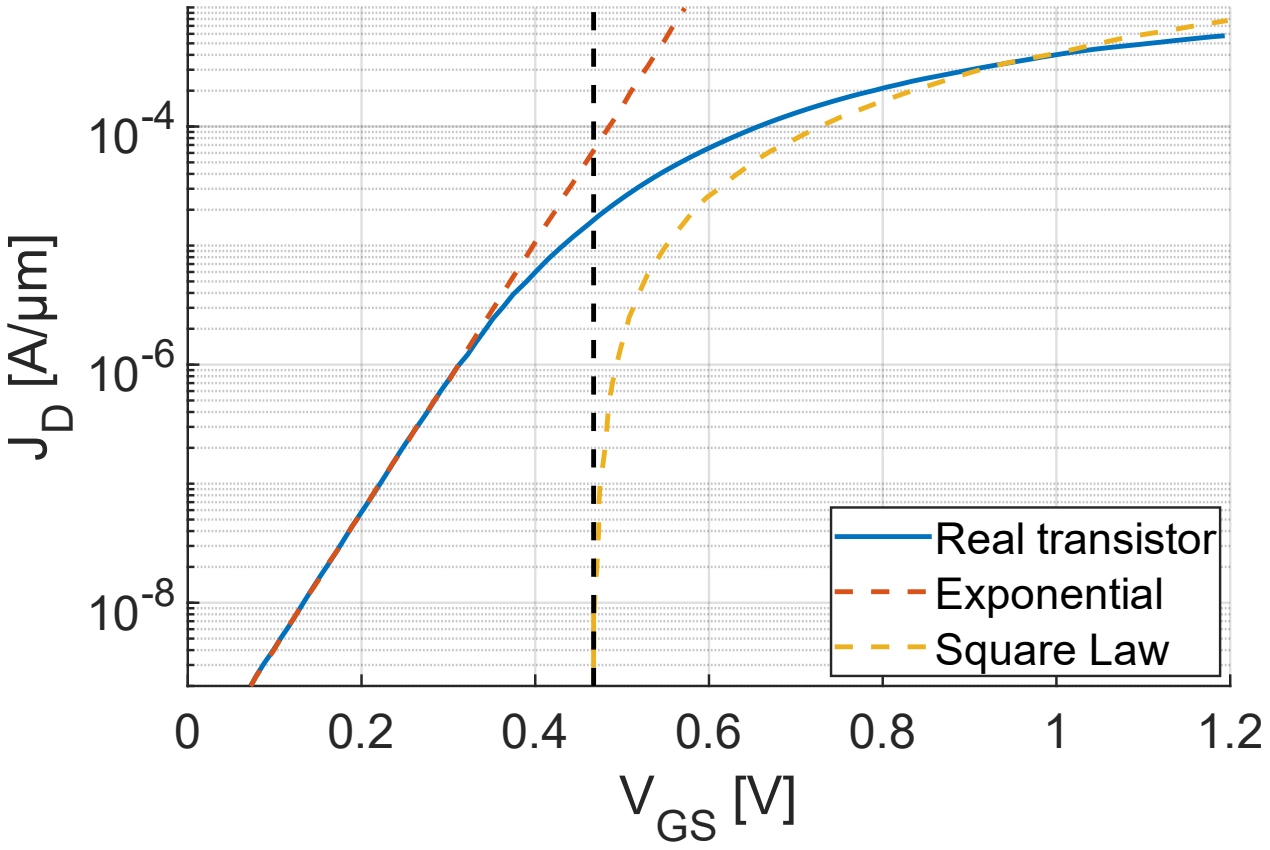
- Square Law model for a MOSFET in saturation:

$$I_D \approx \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2$$

No longer suitable for design with nanoscale technologies!

- Parameters like V_{th} and μ now depend on size, voltage, or both
  - Deviation from the square law equations!
- Unfortunately, no simple equations available anymore
  - Hand calculations no longer possible/accurate for design

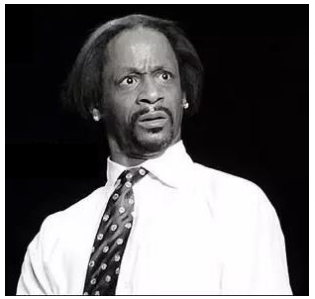
Square Law vs Modern CMOS



Current density of a minimum-length N-channel device in **65 nm** CMOS technology versus V_{GS}. The black vertical line marks the device threshold voltage.

Formulation of V_{th} in a modern model

$$V_{th} = VTH0 + \left(K_{1ox}\sqrt{\Phi_s - V_{bseff}} - K1\sqrt{\Phi_s}\right)\sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox}V_{bseff} + K_{1ox}\left(\sqrt{1 + \frac{LPE0}{L_{eff}}}\right)\sqrt{\Phi_s}$$



$$+ \left(K3 + K3B \cdot V_{bseff}\right)\frac{TOXE}{W'_{eff} + W0}\Phi_s - 0.5\left[\frac{DVT0W}{\cosh\left(DVT1W\frac{L_{eff}W'_{eff}}{l_{tw}}\right) - 1} + \frac{DVT0}{\cosh\left(DVT1W\frac{L_{eff}}{l_t}\right) - 1}\right](V_{bi} - \Phi_s)$$

$$- \frac{0.5}{\cosh\left(DSUB\frac{L_{eff}}{l_{t0}}\right) - 1}\left(ETA0 + ETAB \cdot V_{bseff}\right)V_{ds} - nv_t \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0(1 + e^{-DVTP1 \cdot V_{DS}})}\right)$$

- The equation for the current factor $\beta = \mu C_{ox}\frac{W}{L}$ is only "slightly less complicated"...
- A modern model has normally <u>over 200 parameters</u>

What to do now?

- **Option A**: become a S.P.I.C.E. Monkey!
  - Iterative, brainless tuning of design parameters
  - Loss of insight into circuit operation
  - Very time-inefficient
  - Mostly ending with sub-optimal results
- **Option B**: find a new link between high-level and transistor-level design
- Some particularly clever designers went through option B for you…
  - g_m/I_D methodology (Silveira, Flandre and Jespers)
  - Inversion Coefficient (IC) methodology (Enz, Krummenacher, and Vittoz)
  - Several other short-channel methodologies

See also: W. Sansen, “Minimum Power in Analog Amplifying Blocks: Presenting a Design Procedure,” IEEE Solid-State Circuits Mag., vol. 7, no. 4, pp. 83–89, 2015.

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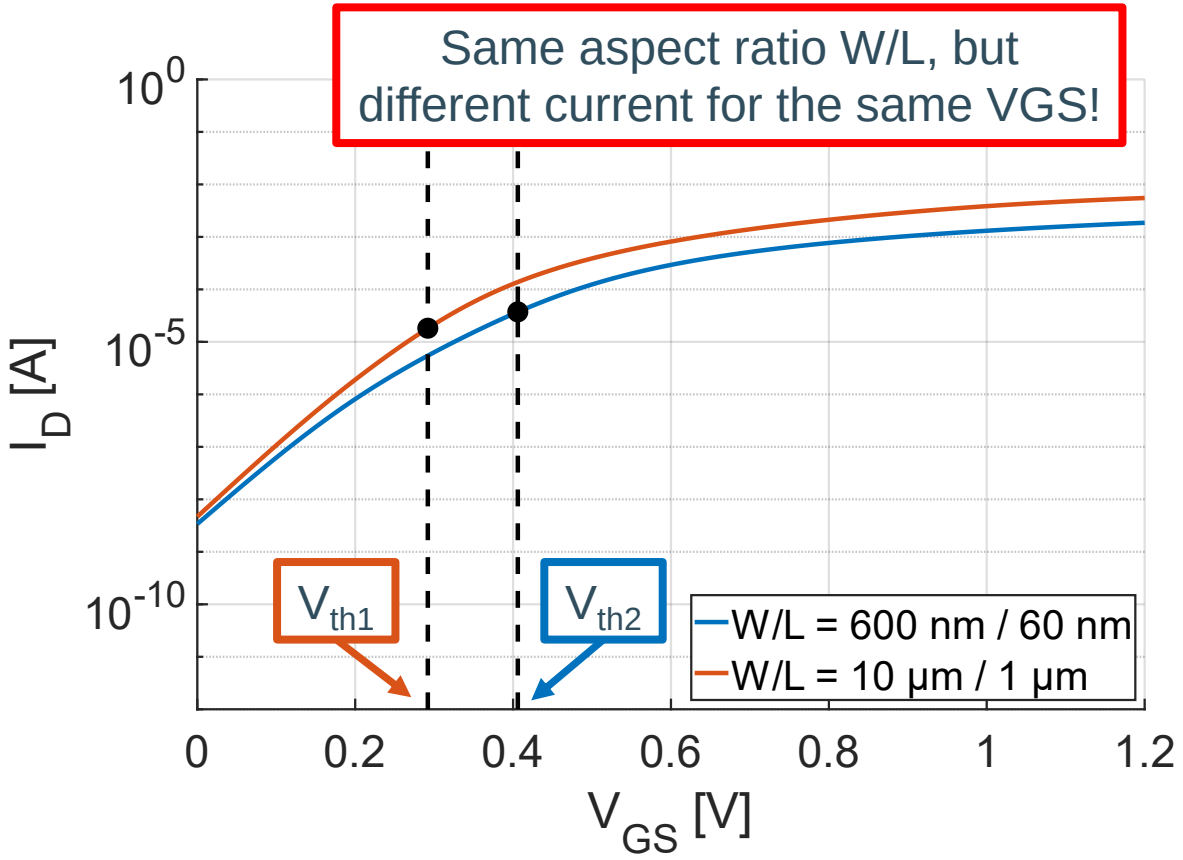
The inversion level

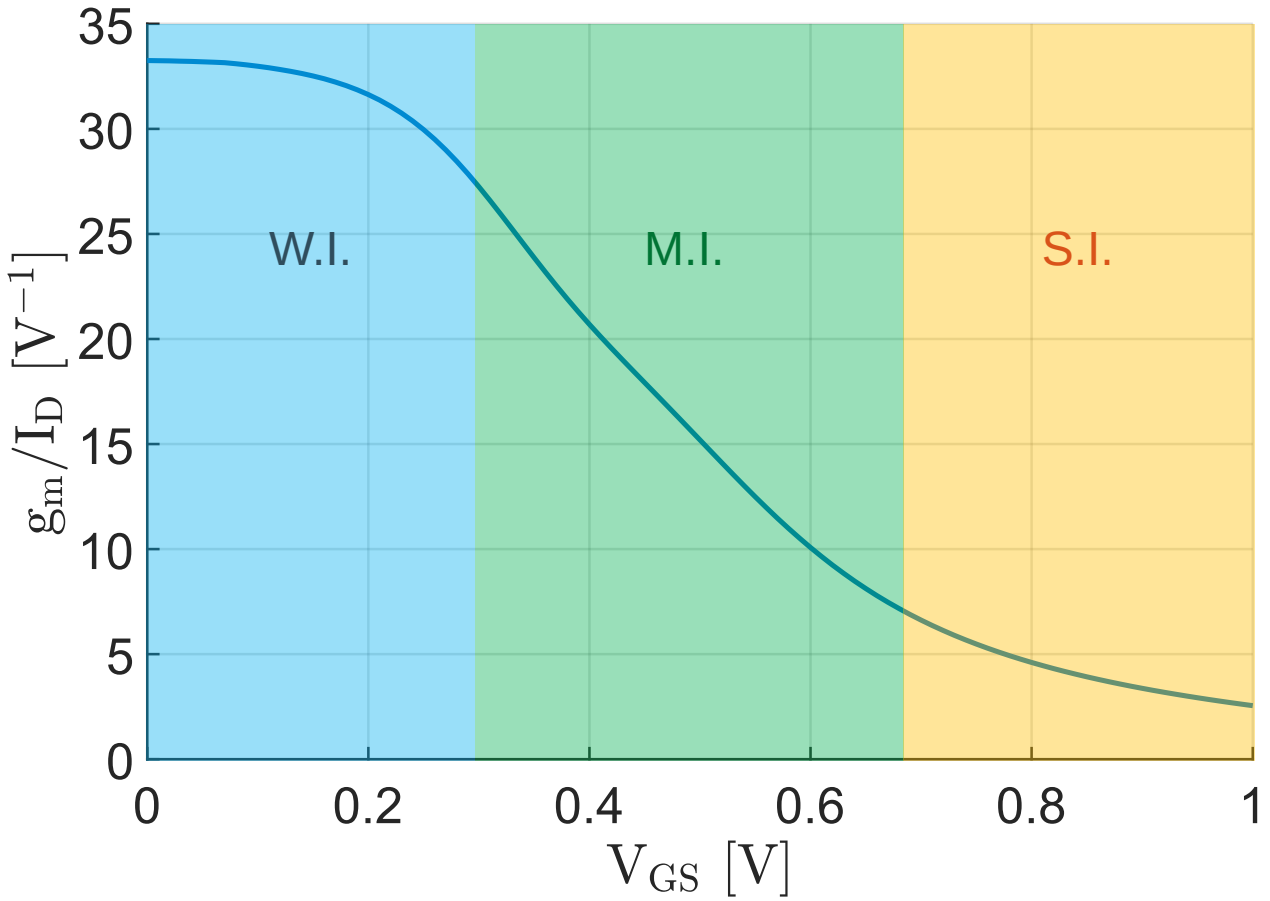
- $V_{OV} = V_{GS} - V_{th}$ no longer useful
  - V_{th} is not constant!
  - Also, no unique definition of V_{th}…
- Transistor behavior depends on the **inversion level**
  - Density of carriers in the channel
    - (Inversion layer)
- Two transistors with the same V_{GS} may have different inversion levels
  - Because their V_{th} may be different!



Example data for a real **65 nm** CMOS technology.

The transconductance efficiency g_m/I_D

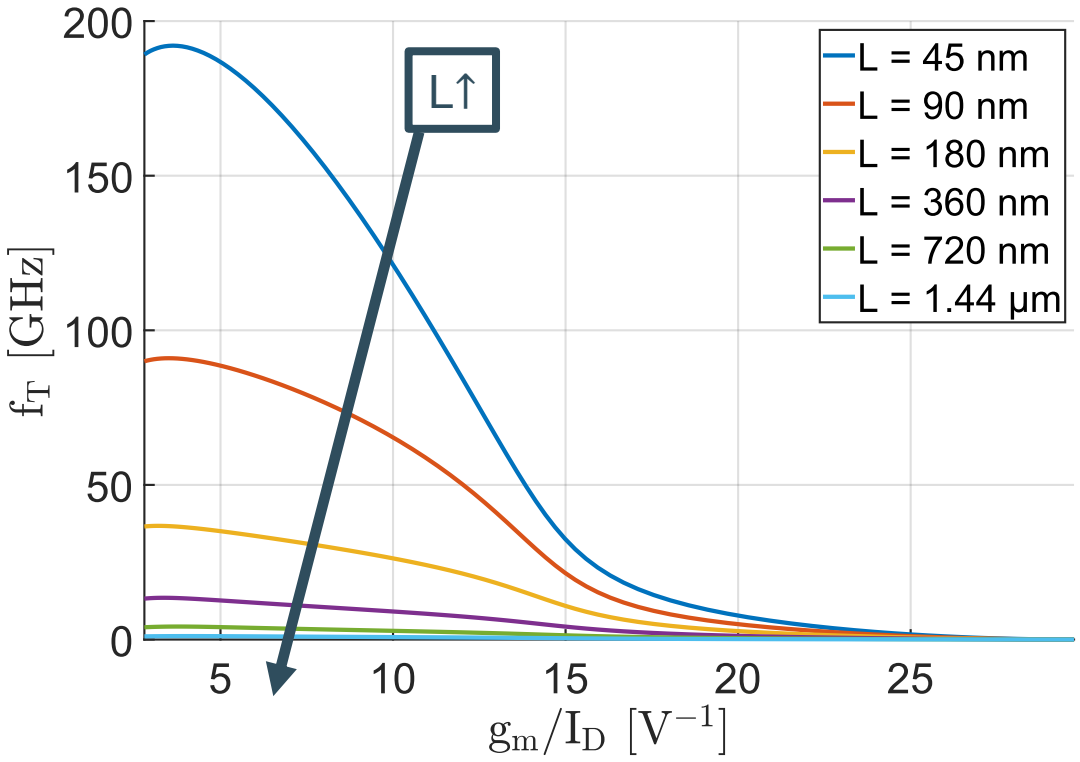
- $\frac{g_m}{I_D} = \frac{1}{nU_T}\frac{1}{q_i+1}\ [V^{-1}]$
  - $n =$ subthreshold factor
  - $U_T =$ thermal voltage (kT/q)
  - $q_i =$ normalized mobile charge density
- $\rho = \frac{g_m/I_D}{max(g_m/I_D)}$
- **Proxy for the inversion level**
  - Weak inversion ~ [$\rho < 0.8$]
  - Moderate inversion ~ [$0.8 < \rho < 0.2$]
  - Strong inversion ~ [$\rho > 0.2$]
- Amount of g_m for a given I_D

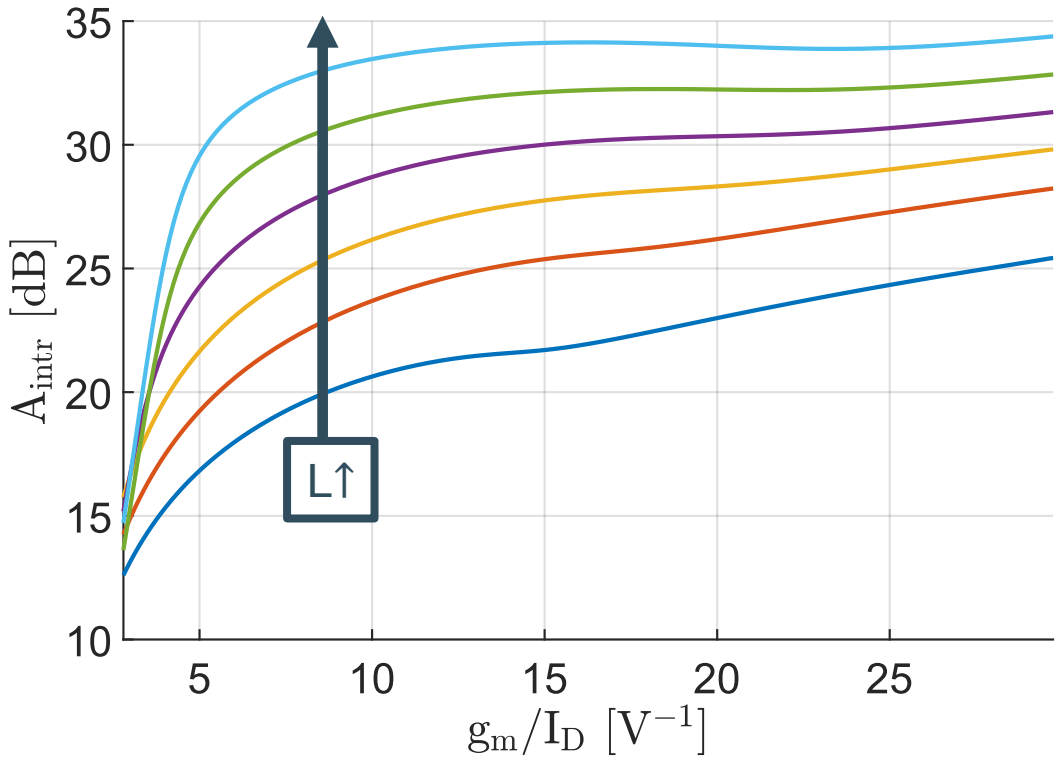


Example data for an N-channel device with **L = 180 nm** in the **45 nm GPDK**.

C. C. Enz and E. A. Vittoz, "Charge-based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design", John Wiley & Sons, 2006.

Transit Frequency and Intrinsic Gain





Transit Frequency f_T (left) and low-frequency intrinsic gain A_{intr} (right) versus g_m/I_D for several values of the channel length L. Curves for an N-channel device in the **45 nm GPDK**. **W = 40 µm, V_{DS} = 500 mV**.

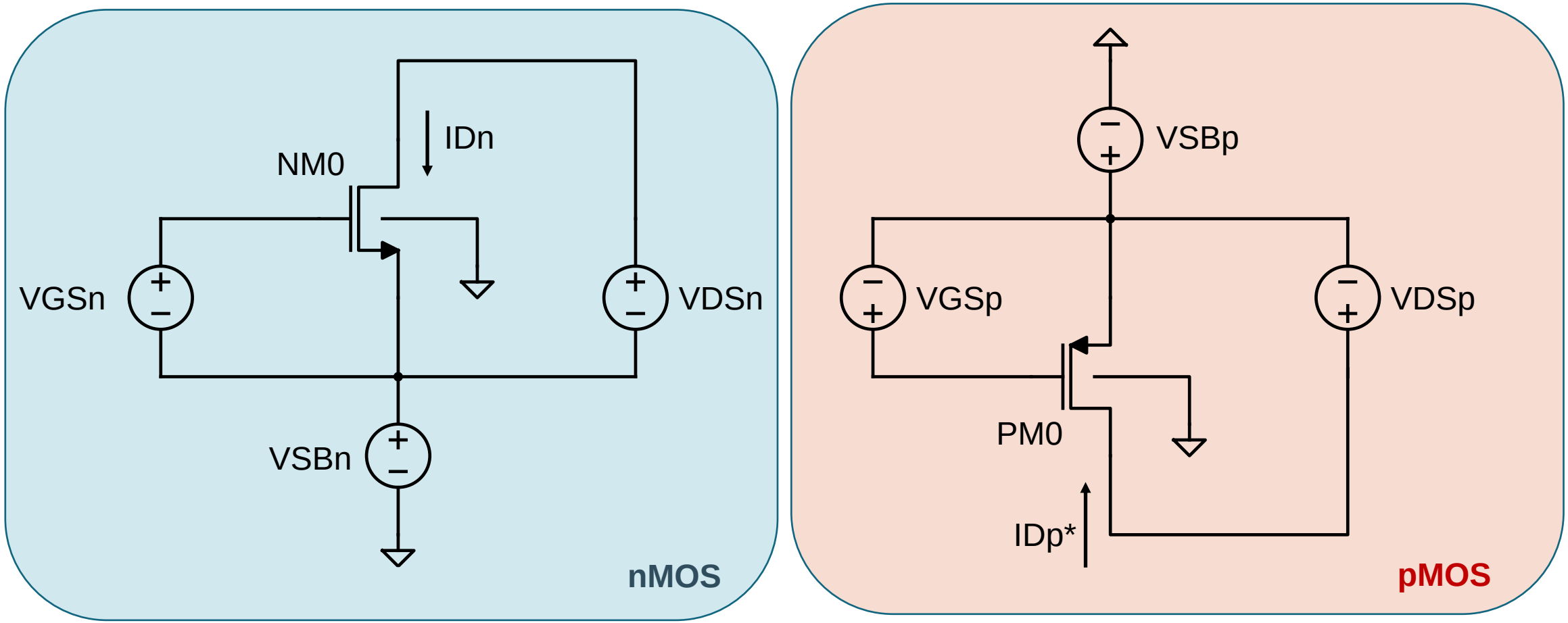
The Drain Saturation Voltage

- The drain saturation voltage V_{Dsat} can be expressed as:

$$V_{Dsat} = \frac{2}{g_m/I_D}$$

- In weak inversion, $V_{Dsat} \rightarrow 2nU_T$
- In strong inversion, $V_{Dsat} \approx V_{GS} - V_{th}$
  - No longer true in deep strong inversion because of mobility degradation

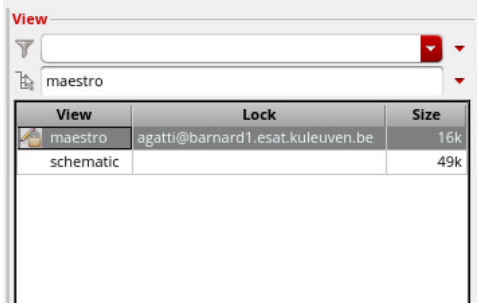
The g_m/I_D Testbench

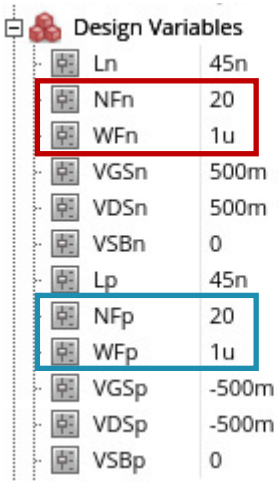


*currents in Spectre are defined as flowing into the nodes; therefore, IDp is negative

Use of the g_m/I_D Testbench

- Cellname: *gmoverid_plots*
  - Already in the library we provided!
- Open the *maestro* view in ADE Explorer
- pMOS voltages are <u>negative</u>
  - Remember to use <u>a negative step</u> in sweeps
- Channel width $W = NF \cdot WF$
  - $W =$ device width (design)
  - $NF =$ number of fingers
  - $WF =$ finger width
- A finger width of **0.5…2 µm** is a good compromise (for this node)*
  - In real circuits, NF and WF are chosen to optimize layout too



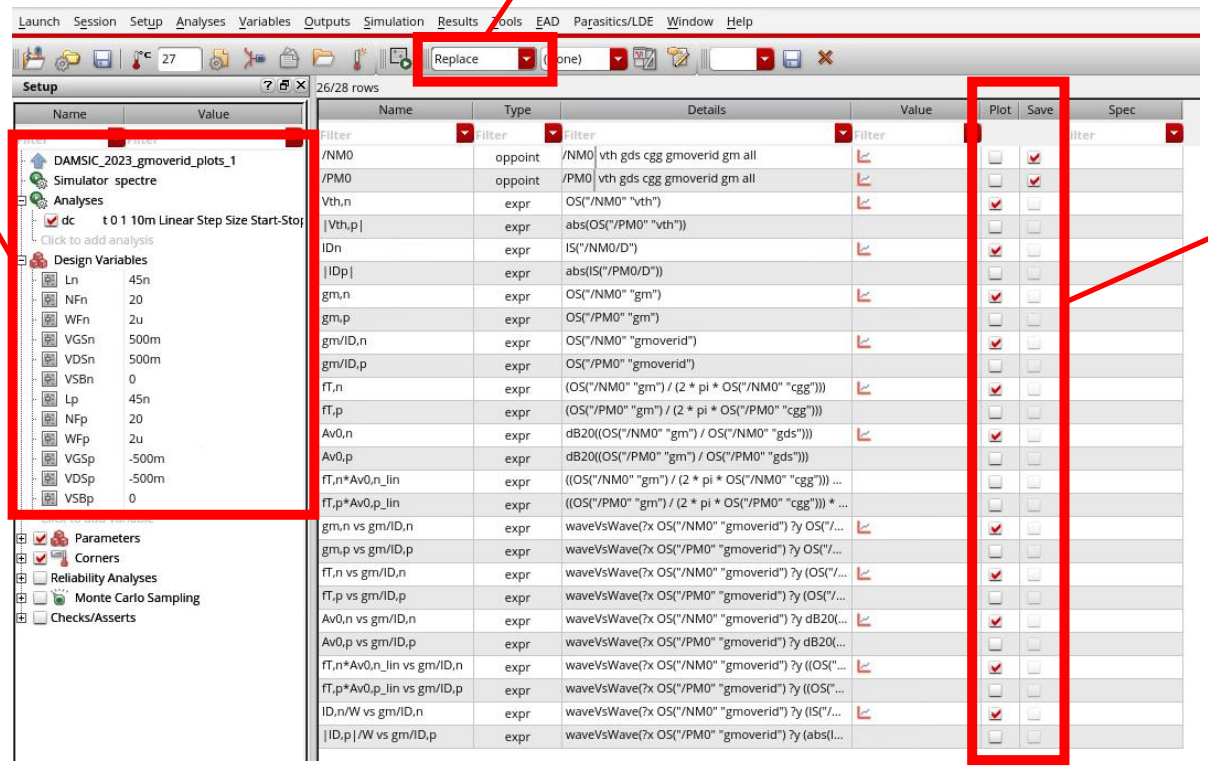


*W. Steyaert and P. Reynaert, “Layout optimizations for THz integrated circuit design in bulk nanometer CMOS,” in 2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Oct. 2017, pp. 1–4.

Use of the g_m/I_D Testbench

Select plot mode (Append, Replace, …)

Change the DC sweep and/or execute parametric simulations



Plot only what you need

(nMOS or pMOS, specific expressions, etc.)

General hint: if you need/want to plot more signals/expressions, use the Calculator (*Tools –> Calculator*) and the built-in Expression Builder of ADE Explorer/Assembler

Design tips (1)

- g_m/I_D is weakly dependent on W and V_{DS}
- I_D/W is weakly dependent on W* and V_{DS}
- However, for the same value of g_m/I_D but different values of W and/or V_{DS}, the value of other analog FoMs (g_m, f_T, …) can change!
  - Try to see how/if the plots change by varying W, L, V_{DS} and V_{BS}
- It's a good idea to double-check with the help of the g_m/I_D testbench
  - with W closer to the "final" size and the V_{DS} you expect in your circuit
- **Never forget to check that the devices are in saturation!**
  - By default, the g_m/I_D testbench sets $V_{DSn} = V_{DD}/2$ and $V_{DSp} = -V_{DD}/2$
    - This enforces saturation up to $\sim g_m/I_D = 4$ and it's a good starting point for design

*this seems counter-intuitive, but a small channel width has an impact on the device behavior, so the I_D/W plot will deviate for very small values of W. Try and see!

Design tips (2)

- Try to plot A_{intr} sweeping the channel length L
  - V_{GS} can be fixed to 500-600 mV for this purpose, or parametrized
  - After a certain value of L, increasing it further will have a diminishing return
- Have a look at the $A_{intr} \cdot fT$ plot(s)
  - Useful when you need a fair compromise between gain and speed
- Try replacing the devices with LVT/HVT ones
  - For the testbench to work, they must use the same names NM0/PM0
- Add your own expressions/plots!

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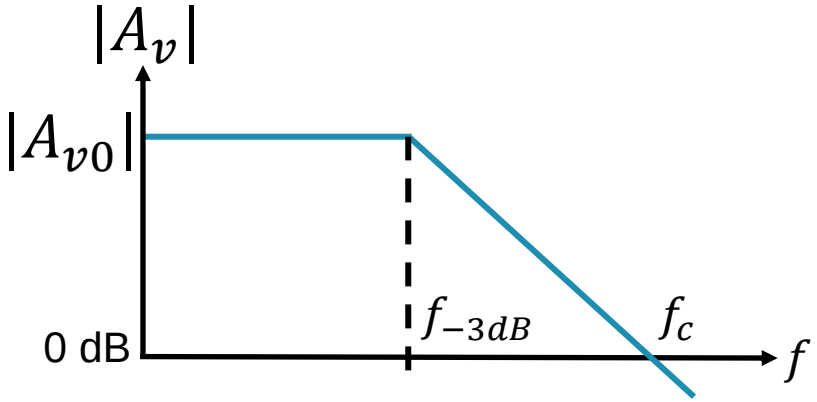
A generic sizing flow

NOT a magical recipe for design!

1. Determine g_m (from design specifications)
2. Pick L:
   - Short channel → high speed, small area;
   - Long channel → high intrinsic gain, improved matching…
3. Pick g_m/ID:
   - Large g_m / ID → low power, large signal swing (low V_{Dsat});
   - Small g_m / ID → high speed, small area.
4. Determine I_D (using g_m and g_m/I_D)
5. Determine W (using the I_D/W plot)

Design example: Intrinsic Gain Stage

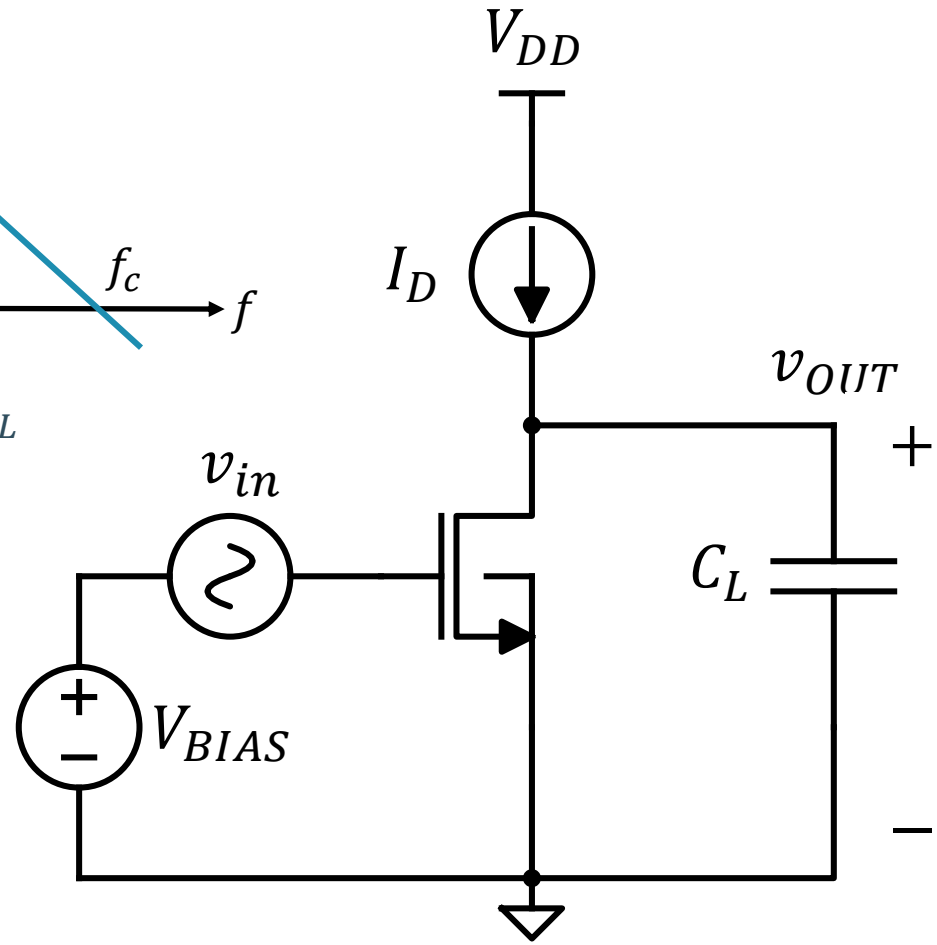
- Ideal version of a CS stage
- Specifications:
  - f_C * = 1 GHz with C_L = 1 pF
  - V_{DS} = 500 mV, V_{SB} = 0 V
  - $L = L_{min}$
  - $g_m/I_D = 10$



- We neglect junction capacitances and assume $C_{db} \ll C_L$
- Under these assumptions, the frequency response is well-approximated by the expression:

$$A_V(j\omega) = \frac{v_{OUT}}{v_{IN}} \cong \frac{A_{v0}}{1 + j\frac{\omega}{\omega_{-3dB}}}$$

  - $A_{v0} = -A_{intr} = -g_m/g_{ds}$
  - $\omega_{-3dB} = \frac{g_{ds}}{C_L} \rightarrow f_{-3dB} = \frac{g_{ds}}{2\pi C_L}$



*the crossing frequency f_C (also known as the unity-gain frequency f_u, in short UGF) is the frequency at which the Bode plot of the gain magnitude of an amplifier stage intersects the axis for y = 0 dB (unity gain)

Design example: Intrinsic Gain Stage (2)

- We know (GBW…) that $f_c = \frac{g_m}{2\pi C_L}$
  - Therefore $g_m = 2\pi f_c C_L \cong 6.28$ mS
- Specs are asking for minimum length, so $L = L_{min} = 45$ nm
- Since g_m/I_D is set to 10, we have $I_D = \frac{g_m}{g_m/I_D} = 628$ µA
  - Note that g_m/I_D = 10 → V_{Dsat} = 200 mV
  - If the output voltage goes below -300 mV from the quiescent V_{DS}, the device will leave saturation
- To calculate the value of W, we will use the I_D/W vs g_m/I_D plot
  - Already included in the g_m/I_D testbench

Design example: Intrinsic Gain Stage (3)

- From the plot, we get:

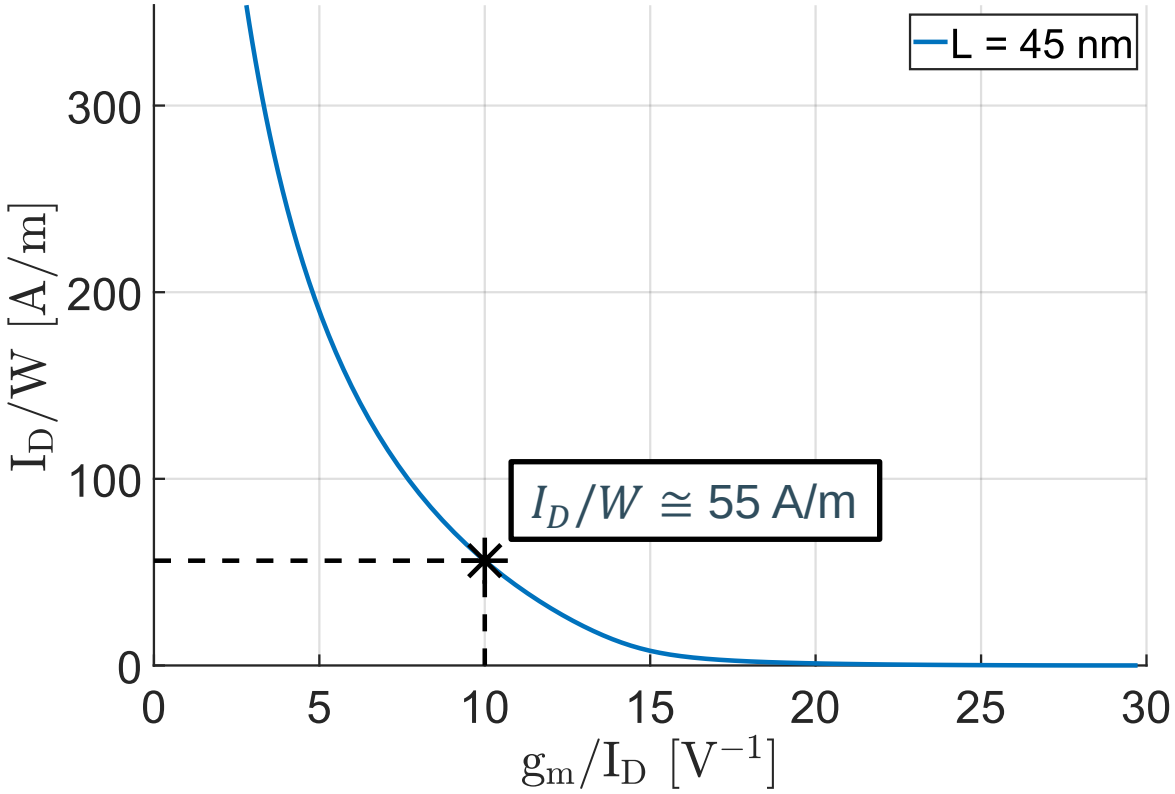
$$I_D/W \cong 55 \text{ A/m}$$

- We can finally compute:

$$W = \frac{I_D}{I_D/W} \cong 11.5 \text{ µm}$$

  - NF = 10 and WF = 1.15 µm will be fine

- We finally have our sizing:
  - W = 10*1.15 µm
  - L = 45 nm
  - I_D = 628 µA

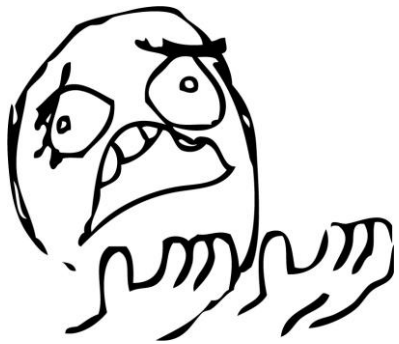


NOTE: it is a good idea to round down I_D/W and round up W

Verification of the IGS sizing

- To check the results, a testbench is available
  - Cell *IGS_Testbench* in the DAMSIC library
  - You can repeat the same exercise with the pMOS version

- Let's put in the numbers…
- …and we fail to reach the specs.
- Why?



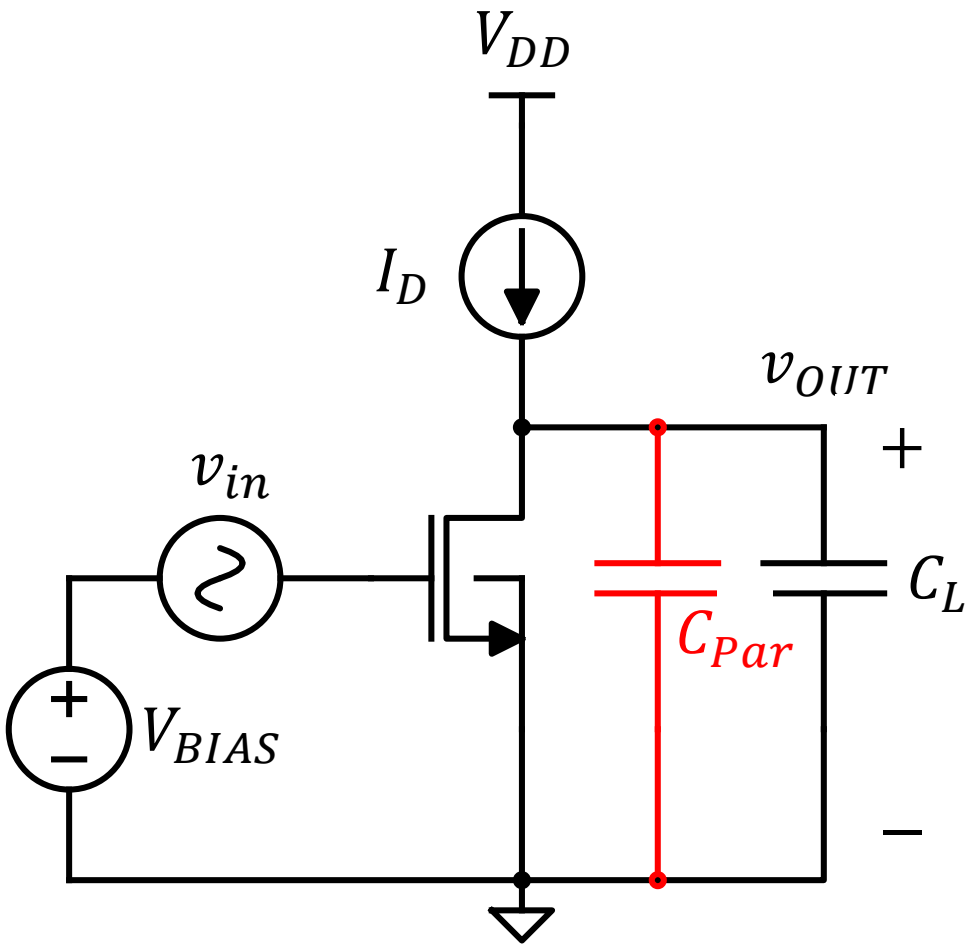
Name	Type	Details	Value	Plot	Save	Spec
/NM0	oppoint	/NM0 all		☐	☑	
/PM0	oppoint	/PM0 all		☐	☑	
gm,n	expr	OP("/NM0" "gm")	6.3m	☑	☐	> 6.28m
gm,p	expr	OP("/PM0" "gm")		☐	☐	> 6.28m
gm/ID,n	expr	OP("/NM0" "gmoverid")	10.03	☑	☐	
gm/ID,p	expr	OP("/PM0" "gmoverid")		☐	☐	
VGSn	expr	VDC("/Vinn")	668.3m	☑	☐	
VGSp	expr	(VDC("/Vinp") - VDC("/vdd!"))		☐	☐	
VDSn	expr	VDC("/Voutn")	500m	☑	☐	> (2 / calcVal("gm/ID,n"))
VDSp	expr	(VDC("/Voutp") - VDC("/vdd!"))		☐	☐	< (-1 * (2 / calcVal("gm/ID,p")))
|Av|,n	expr	dB20(mag(VF("/Voutn")))		☑	☐	
UGFn	expr	cross(dB20(mag(VF("/Voutn"))) 0)	993.3M	☑	☐	> 1G
Av0,n	expr	value(dB20(mag(VF("/Voutn"))) 1)	20.85	☑	☐	> 0
Av0,p	expr	value(dB20(mag(VF("/Voutp"))) 1)		☐	☐	> 0

Inclusion of the parasitic capacitance

- We neglected the parasitic capacitance at the output node
- We can compute C_{Par} from the UGF value:

$$f_c = \frac{g_m}{2\pi(C_L+C_{Par})} \rightarrow C_{Par} \cong 9.5 \text{ fF}$$

- We repeat the design procedure replacing C_L with $C_{TOT} = C_L + C_{Par}$
  - If the transistor size change considerably, we may need multiple iterations



Verification of the IGS resize

- New values:
  - W = 10*1.15 µm
  - L = 45 nm
  - I_D = 634 µA
- Now we have reached the specs!
- We just needed a bit more current
  - Pretty obvious, right?

Name	Type	Details	Value	Plot	Save	Spec
/NM0	oppoint	/NM0 all		☐	☑	
/PM0	oppoint	/PM0 all		☐	☑	
gm,n	expr	OP("/NM0" "gm")	6.344m	☑	☐	> 6.28m
gm,p	expr	OP("/PM0" "gm")		☐	☐	> 6.28m
gm/ID,n	expr	OP("/NM0" "gmoverid")	9.99	☑	☐	
gm/ID,p	expr	OP("/PM0" "gmoverid")		☐	☐	
VGSn	expr	VDC("/Vinn")	669.4m	☑	☐	
VGSp	expr	(VDC("/Vinp") - VDC("/vdd!"))		☐	☐	
VDSn	expr	VDC("/Voutn")	500m	☑	☐	> (2 / calcVal("gm/ID,n"))
VDSp	expr	(VDC("/Voutp") - VDC("/vdd!"))		☐	☐	< (-1 * (2 / calcVal("gm/ID,p")))
|Av|,n	expr	dB20(mag(VF("/Voutn")))		☑	☐	
|Av|,p	expr	dB20(mag(VF("/Voutp")))		☐	☐	
UGFn	expr	cross(dB20(mag(VF("/Voutn"))) 0)	1G	☑	☐	> 1G
UGFp	expr	cross(dB20(mag(VF("/Voutp"))) 0)		☐	☐	> 1G
Av0,n	expr	value(dB20(mag(VF("/Voutn"))) 1)	20.83	☑	☐	> 0
Av0,p	expr	value(dB20(mag(VF("/Voutp"))) 1)		☐	☐	> 0

Design tips (3)

- The maximum frequency of interest (f_c in the previous example) sets a limit on the choice of L
  - As a conservative rule of thumb*, circuits operate predictably only **up to $f_T/10$**
- Be smart when you choose g_m/I_D
  - Remember that $V_{Dsat} = 2/\left(\frac{g_m}{I_D}\right) \rightarrow$ places a limit on signal swing
  - For example, requiring V_{Dsat} = 150 mV means g_m/I_D = 13.33 V^{-1}
- **Models are not perfect**
  - This is essentially why a phase margin of a few degrees is not enough to ensure stability....
  - Always keep some margin on the specifications you want to achieve
  - Mismatch/PVT simulations are only as good as the silicon-proven reliability of the process
  - Foundries periodically update PDKs with improvements to the models and to the process, even after years
- Don't go crazy over differences of ± 1 dB in open-loop gain or ± 1 mV in bias voltages…
  - … the circuit will never behave so precisely anyway, in reality
  - High accuracy is achieved with feedback loops and/or other techniques (trimming, calibration, …)

*T.H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd ed. Cambridge University Press, 2004.

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Today’s Session

- Work on system level understanding, use ideal OTA
  - If you are fast, go on with transiter level design
- Check out the report template
- Seminar at 11, we stop at ~10:50