Design of a Switched-Capacitor Amplifier

H05E4a DAMSIC Project 2024

Part III: Gain-boosted OTA

Students: <Name1>, <Name2>

Group ID:

# Gain-boosted OTA

## Table of Achieved Results

Enter your achieved results in the below table.

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Unit** | **Achieved** |
| Input Swing | mVpp |  |
| Output Swing | mVpp |  |
| Total Integrated Output Noise | mVrms |  |
| SNR | dB |  |
|  |  |  |
| CL | pF | (*enter the specified value*) |
| CFB | pF |  |
| CIN | pF |  |
|  |  |  |
| Open-Loop Gain | dB | (*standalone OTA DC gain*) |
| Closed-Loop Gain | V/V |  |
| GBW (Sample Phase) | MHz |  |
| Phase Margin (Sample Phase) | deg |  |
|  |  |  |
| Dynamic Settling Error | % | (*settling error at the end of the amplification phase*) |
| Static Gain Error | % |  |
| Power dissipation | mW |  |

## Schematic Design

In this subsection, insert the schematic details of your final gain-boosted OTA design as requested below.

1. Figure: circuit schematics of the main amplifier + gain-boosting implementation. **Please make sure that it is readable even if the reader does not zoom in to your images.**
2. Figure or table: transistor dimensions for all involved OTAs, parameters of the CMFB blocks. **If you are making a table, please make sure that the name of the transistors are consistent with the figure you will attach in this subsection.**
3. Figure or table: voltages (VG, VD, VGT, VDS) and branch currents for all involved OTAs. **If you are making a table, please make sure that the name of the transistors are consistent with the figure you will attach in this subsection.**

You may remove these instructions.

## Simulation Results

In this subsection, insert the simulation results of your final gain-boosted OTA design as requested below. **Please make sure that your plots are visible, and the axis labels and values are readable.**

1. Open-loop AC simulation: bode plot of OTA’s gain
2. Closed-loop AC simulation: bode plot of differential **loop gain** of main feedback loop in sampling phase
3. Closed-loop AC simulation: bode plot of differential **loop gain** of gain boosting loop
4. Closed-loop AC simulation: bode plot of differential **loop gain** in main CMFB loop
5. Closed-loop transient simulation: 2 consecutive cycles (f = fS), input is DC within one cycle

1st cycle: Vinp - Vinn = **minSwing/2**; 2nd cycle: Vinp - Vinn = **-maxSwing/2**

*Figure:* a. Input waveform for differential mode (Vinp - Vinn)

b. Output waveform for differential mode

c. Output waveform for common mode

d. Plot of the extracted settling error (% vs time) during the2nd amplification phase

1. Closed-loop transient simulation: same as previous simulation, but lower fS by 1000x.
2. Closed-loop PNOISE simulation: total differential output noise spectrum near end of sampling phase (in V/sqrt(Hz), from 1 Hz to fS/2). To make sure we understand you, also include:

* The integrated noise vs. time
* The clock pulse voltage vs. time
* For more than 3 time points (change Samples per Period in PNOISE setup, make sure to press “change” to save the setting)

You may remove these instructions.

# Summary and Additional Remarks

Please summarize your achieved results: you don’t need to list all performance numbers. Emphasize to what extent each of your designs was able to conquer/reach/pass/fail the given target, and why.

You may also point out “special” things that you achieved.

Be concise and make sure the summary reads well, e.g., use multiple paragraphs if necessary. There is no necessity to completely fill this box. At the same time, you can extend this box if more space is needed.

You may remove these instructions.

# Other Results

In this section, if you wish, you may expand on extra/creative design work. E.g., biasing, CMFB implementation, other topologies… etc.

Though, please keep it concise and present it in more detail during your presentation.

You can also choose to remove this section.