Design of a Switched-Capacitor Amplifier

H05E4a DAMSIC Project 2025

Part II: Symmetrical OTA

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Group ID:

# Symmetrical OTA

## Table of Achieved Results (So Far)

Enter your achieved results in the below table. You can leave some fields blank if you did not simulate (or design) for the specific parameter yet.

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Unit** | **Achieved** |
| Input Swing | mVpp |  |
| Output Swing | mVpp |  |
| Total Integrated Output Noise | mVrms |  |
| SNR | dB | (*@ minimum Vin*) |
|  |  |  |
| CL | pF | (*enter the specified value*) |
| CFB | pF |  |
| CIN | pF |  |
|  |  |  |
| Open-Loop Gain | dB | (*standalone OTA DC gain*) |
| Closed-Loop Gain | V/V |  |
| GBW (Sample Phase) | MHz |  |
| Phase Margin (Sample Phase) | deg |  |
|  |  |  |
| Dynamic Settling Error | % | (*settling error at the end of the amplification phase*) |
| Static Gain Error | % |  |
| Power dissipation | mW |  |

## Schematic Design

In this subsection, insert the schematic details of your current symmetrical OTA design as requested below.

1. Figure: circuit schematics. **Please make sure that it is readable even if the reader does not zoom in to your images.**
2. Figure or table: transistor dimensions (W/L), parameters of the CMFB block. **If you are making a table, please make sure that the name of the transistors are consistent with the figure you will attach in this subsection.**
3. Figure or table: transistor parameters (gm, VGT, VDS) and branch currents. **If you are making a table, please make sure that the name of the transistors are consistent with the figure you will attach in this subsection.**

You may remove these instructions

## Simulation Results

In this subsection, insert the simulation details of your current symmetrical OTA design as requested below. **Please make sure that your plots are visible, and the axis labels and values are readable.**

1. Open-loop AC simulation: bode plot of OTA’s gain
2. Closed-loop AC simulation: bode plot of differential loop gain in sampling phase
3. Closed-loop transient simulation: 2 consecutive cycles (f = fS), input is DC within one cycle

1st cycle: Vinp - Vinn = **minSwing/2**; 2nd cycle: Vinp - Vinn = **-maxSwing/2**

*Figure:* a. Input waveform for differential mode (Vinp - Vinn)

b. Output waveform for differential mode

c. Output waveform for common mode

d. Plot of the extracted settling error (% vs time) during the2nd amplification phase

1. Closed-loop transient simulation: same as previous simulation, but lower fS by 1000x.
2. Closed-loop PNOISE simulation: total differential output noise spectrum near end of sampling phase (in V/sqrt(Hz), from 1 Hz to fS/2)